Matthew Hui

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Education

Cornell University Ithaca, NY

B.S. in Electrical & Computer Engineering *Aug. 2021 – May 2025 (Expected)*

GPA: 3.85, Dean's List (All Semesters)

Relevant Coursework: Complex ASIC Design, Computer Architecture, Digital Logic & Computer Organization, Digital VLSI Design, Analog IC Design, Advanced Analog IC Design, Digital Signal Processing

Experience

Digital ASIC Design Intern Jun. 2024 – Aug. 2024

Keysight Technologies *Colorado Springs, CO*

- Designed and implemented a data demuxing block integrated with custom FIFO-based memory controllers in Verilog to support data transitioning from single to 16-stream processing on a next-gen DSP ASIC
- Verified functionality with SystemVerilog test benches and Python golden models to ensure sufficient coverage
- Optimized block area and slack using Cadence Genus for synthesis and power, area, and timing analysis reports

Electrical Design Engineering Intern May. 2023 – Aug. 2023

Sensata Technologies *Attleboro, MA*

- Developed micro-fused strain gauge (MSG) simulation software in Delphi to expand ASIC-level testing
- Implemented an alternative characterization process to reduce data collection times by 95%
- Automated custom ASIC calibration processes with up to 98% accuracy using SENT to memory protocols

Teaching Assistant - Object Oriented Programming Aug. 2022 - Dec. 2024

Cornell University *Ithaca, NY*

- Led weekly discussion sections for 45 students covering data structures, recursion and Java concepts
- Host individual office hours for 50+ students to provide focused assistance on assignments and quizzes
- Design and grade 140+ assignments to provide constructive feedback on class material comprehension

Software Development Subteam Lead Aug. 2021 - Present

Cornell University *Ithaca, NY*

- Led a team of 6 software developers, utilizing Jira sprints to delegate and organize tasks in 2 week intervals
- Developed a mobile app using React Native to promote carbon offsetting initiatives for Sustainable Tompkins
- Contributed to full-stack development, implementing backend data processing working in a cross-functional team

Projects

MiniGPU | *Verilog, Python, iverilog, cocotb* Dec. 2024 - Jan. 2025

- Designed a simplified SIMT architecture for a GPU streaming multiprocessor with a custom 12-set ISA
- Developed custom Verilog modules for the fetcher, scheduler, decoder, ALU, LSU, and memory controller
- Leveraged Cocotb to implement coroutine-based monitors for simulating instruction and data memory accesses
- Created top-level simulations of vector addition and matrix multiplication kernels using the custom 12-set ISA

Multi-core System Processor | *Verilog, Python, Verilator, C* Sep. 2024 – Dec. 2024

- Designed a multi-core system integrating four custom RISC-V processors and eight designed caches in Verilog
- Utilized a simple 4 node torus-interconnect network model to integrate memory and processor message requests
- Leveraged Python (PyMTL3) for unit testing and cross-compiled C to RISC-V to evaluate cycle time
- Improved multi-threaded program cycle time performance by 65% compared to a single-core system

SRAM with Radar Code Generator | *Cadence Virtuoso Suite* Apr. 2024 – May. 2024

- Collaborated with a team of 3 to design and implement an 8x8 SRAM and a hamming radar-code generator
- Utilized Virutoso Schematic Editor to design 6T SRAM cells, bitline precharge, sense amplifier, and 3:8 decoder
- Designed optimized layouts using Layout XL, minimizing propagation delay and achieving an area of $0.0028\,\mathrm{mm}^2$

Specialized Skills

Languages: Verilog, SystemVerilog, Python, Cadence Virtuoso Suite, Java, C, C++, Javascript
Honors: Eagle Scout (2020)