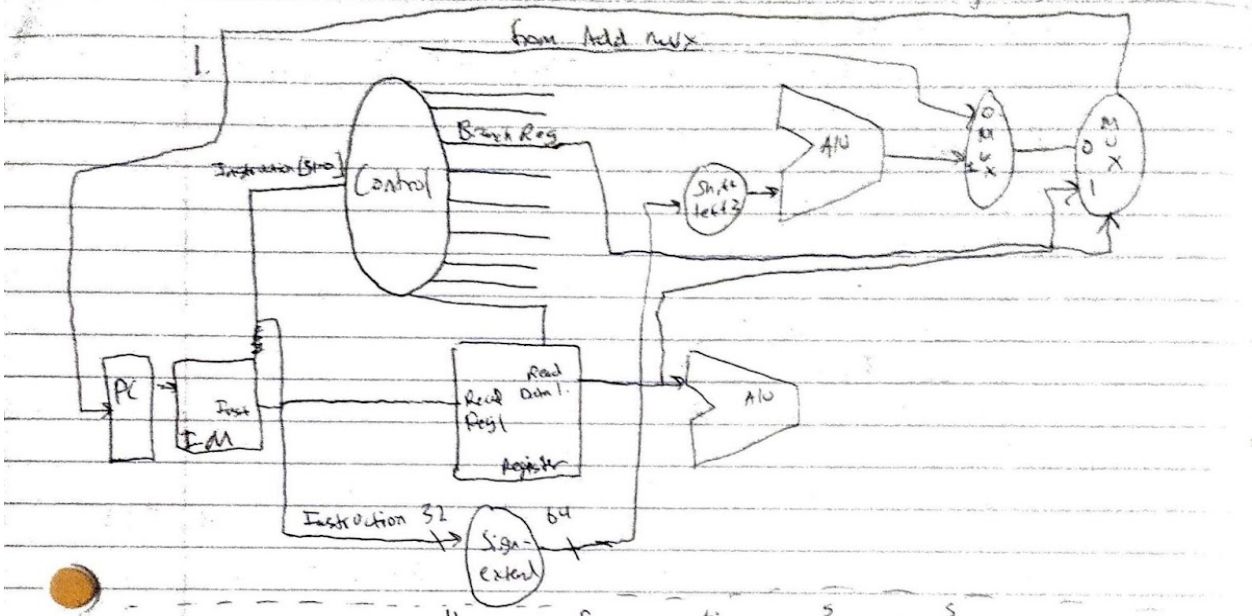
Mark Mitri 3/25/22
ECE 201 Project 3

1.



R-type: Opcode [31:21] 11 | Rm [20:16] 5 | shamt [15:10] 6 | Rn [9:5] 5 | Rd [4:0] 5

2.

Address = PC	Data
0x80 0000	0xD360 0C2A

Instruction address = PC + 4 = 0x80 0004

Instruction = ~~0x8b~~ = ~~1101 0011 0110 0000 0000 1100 0010 1010~~

OP Rm rt rd shamt Rn

= 1101 0011 0110 0000 0000 1100 0010 1010

OP Rm shamt Rn Rd

LSL

Opcode input = 1101 0011 011 = 0x69B = [OP]

Control signal = ALUOp = 1, Reg2Loc = 0

Read register 1 = ~~0x5~~ [Rn] = 00001 = 0x1

Write Register = 01010 = 0xA = [Rd]

Reg write = 1 = 0x1

Read data 1 = X1 = 0x5 [from Read reg1]

ALUOp = ~~0~~ 0x2

ALUctl = 1001 = 0x9

ALU = Shift 0x5 by 3 &

= 0101 << 3 = ~~1010~~ 0010 1000 = 0x28

Zero = 0 = 0x0

& MemToReg = 0x0

Write Data = 0x28

[X10] = 0x28

Address=PC	Data
0x800004	0x8B0A 000A

PC+4 = 0x800008

Instruction Address = 0x80 0004

Instruction = ~~0x8B0A 000A~~ 1000 1011 0000 1010 0000 0000 0000 0000 1010 2

OP RM Shamt Rn Rd

Opcode input = 1000 1011 000 = OP = 0x485 = ADD

Reg2Loc = 0x0

Read Reg 1 = 0x0 = Rn

~~Read Reg 2~~ ~~Write Reg~~ = 0xA = Rd = Read Reg 2

Reg Write = 0x1

Read Data 1 = [X0] = 0x1000 0000

Read Data 2 = [X10] = 0x28

ALUOP = ~~0x10~~ 0x2

ALUctl = 0010 = 0x2

ALU = ADD = X0 & X10

= 0x1000 0000 + 0x28

= 0x100 0028

Zero = 0x0

MemToReg = 0x0

Write Data = 0x100 0028

[X10] = 0x100 0028

Address = PC	Data
0x80 0008	0xF8400149

PC+4 = 0x80 000C

Instruction Address = 0x80 0008

Instruction = 1111 1000 0100 0000 0000 1001 0100 1001

1986 address 0 Rn Rt

~~Opcode input~~

1986_{ten} = LDUR Read Reg 1 = 01010 = 0xA = Rn

ALUsrc = 0x1 MemtoReg = 0x1, MemRead = 0x1, RegWrite = 0x1

Read Data 1 = [x10] = 0x1000 0028

Extended data = 0x0000 0000 0000 0000

ALU = add = 0x0000 0000 0000 0000

+ 0x10000028

0x1000 0028

Write Reg = 0x9 = Rt

~~Reg~~ Data address = 0x1000 0028

~~Use~~ WriteReg = Load memory data = 0x9 = Rt

~~Branch~~ PC ~~+4~~ = 0x80 000C
next

Address = PC	Data
0x80 0004	0xF840 814B

PC+4 = 0x80 0010

Instruction Address = 0x80 0010

Instruction = 1111 1000 0100 0000 1000 0001 0110 1011

1986 address 0 Rn Rt

1986_{ten} = LDUR Read Reg 1 = 01010 = 0xA = Rn

ALUsrc = 0x1, MEMtoReg = 0x1, MemRead, 0x1, RegWrite=0x1

Read Data 1 = [x10] = 0x1000 0028

Extended data = 0x0000 0000 0000 1000

0x0000,0000,0000,1000

ALU = add = 0x 0000 0000 0000 0008

+ 0x1000 0028

0x 1000 0030

Write Reg = 0x9 = Rt (x11) = 0x2222 CCCC

Data address = 0x1000 0030

Write Data = ~~Branch~~ load memory data = 0x9 = Rt

PC next = 0x80 0010

Address = PC	Data
0x80 0010	0xF800 014B

PC+4 = 0x80 0014

Instruction Address = 0x80 0010

Instruction = 1111 1000 0000 0000 0000 0001 0100 1011

1984 | address | 0 | Rm | Rt

1984 ten = STUR Read Reg1 = Rn = 01010 = 0xB

Reg2Loc = 0x1, ALUSrc = 0x1, MemWrite = 0x1

Read Data 1 = 0x1000 ~~0038~~ 0028

~~Extended~~ Data = 0x0000 0000 0000 0000

Read Data 2 = 0x1010 = Write data = 0x2222 CCCC

~~PC+4~~ = ALU = add = 0x1000 0028

0x 0000 0000 0000 0000

0x1000 0028

PC next = 0x80 0014

Address = PC	Data
0x80 0014	0xF800 4149

PC+4 = 0x80 0018

Instruction Address = 0x80 0014

Instruction = ~~0x4000~~ 0x 1111 1000 0000 0000 1000 0001 0010 1001

1984 | address | 0 | Rm | Rt

1984 ten = STUR Read Reg1 = Rn = 01010 = 0xB = Rn

Reg2Loc = 0x1, ALUSrc = 0x1, MemWrite = 0x1

Read Data 1 = 0x1000 0028

Extended Data = 0x0000 0000 0000 0000

Read Data 2 = 0x11 = Write Data = 0x2222 CCCC

ALU = add =

0x0000 0008 0000 1000

+ 0x1000 0020

0x1000 1028

PC_{next} = 0x80 0018

Address = PC	Data
0x80 0018	0xD600 03C0

Instruction Address = 0x80 0018

Instruction = 1101 0110 0000 0000 0000 0011 1100 0000

op | address | Rn | Rd

Opcode = 0x6B0 = Branch

Branch Reg = 0x1

Read Reg 1 = Rn = 11110 = 0x1E

Write Reg = Rd = 000000 = 0x0

Read Data 1 = [x30] = 0x40 101C

Extended data = 0x0000 00

0x 0000 0008 0040 101C

PC = 0x0000 0008 0040 101C

This is my project 3. I needed to include these words to upload to turnitin. THis has nothing to do with my project 3.