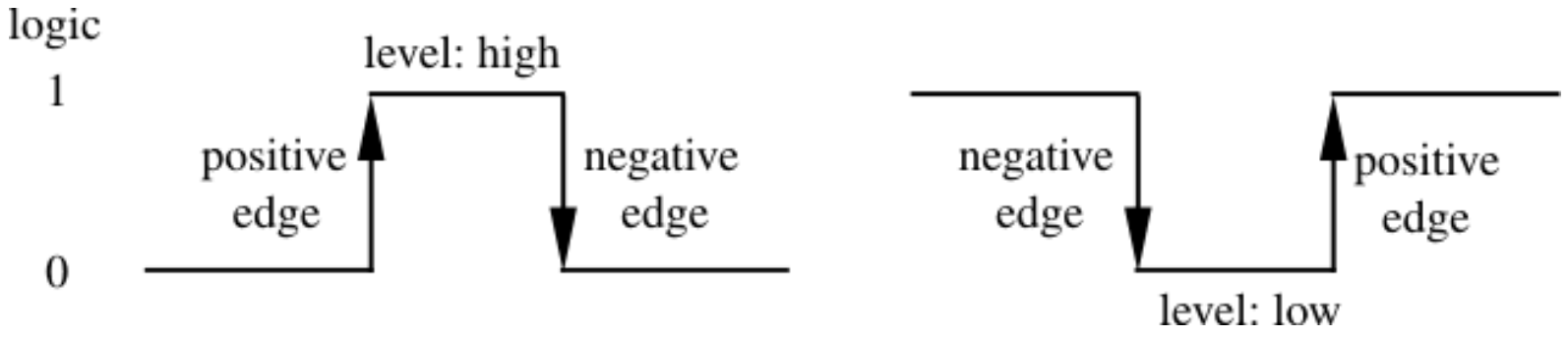
MEMS1082

Chapter 6 Digital Circuit 6-4

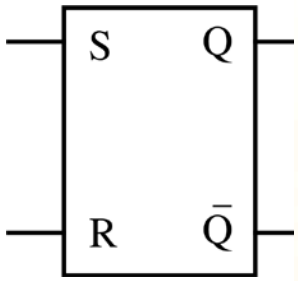
Sequential Logic

- Sequential logic devices usually respond to inputs when a separate trigger signal transitions from one level to another.
- The trigger signal is referred to as the **Clock (CK)** signal.



Flip-Flops

- Flip-flops is called a bi-stable device, since it has only two possible stable output states: 1 (high) and 0 (low).
- It has the capability of remaining in a particular state until input signal cause it to change.
  - **S** is the **SET** input, **R** is **RESET** input
  - Q and $\overline{Q}$ are the **complementary** outputs

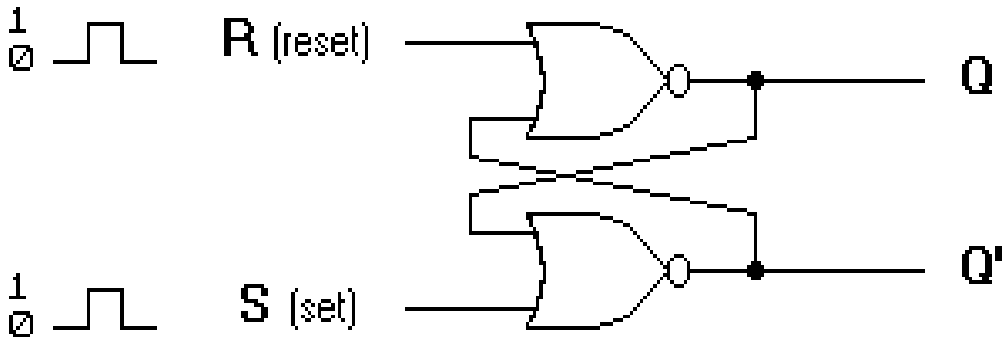


1. As long as the inputs S and R are both 0, the outputs of the flip-flop remain unchanged.
2. When S is 1 and R is 0, the flip-flop is *set* to $Q = 1$ and $\overline{Q} = 0$.
3. When S is 0 and R is 1, the flip-flop is *reset* to $Q = 0$ and $\overline{Q} = 1$.
4. It is "not allowed" (NA) to place a 1 on S and R simultaneously since the output will be unpredictable.

Flip-Flops

- A flip-flop circuit can be constructed from two NAND gates or two NOR gates.
- Flip-flop has two outputs, Q and $\overline{Q}$, and two inputs, *set* and *reset*. This type of flip-flop is referred to as an ***SR flip-flop*** or ***SR latch***.

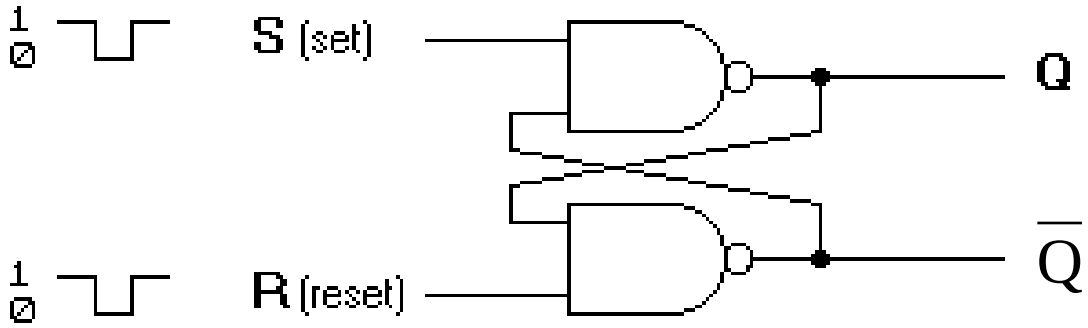
Basic flip-flop circuit with NOR gates



S R	Q Q'	
1 0	1 0	
0 0	1 0	(after S=1, R=0)
0 1	0 1	
0 0	0 1	(after S=0, R=1)
1 1	0 0	↖ NA

Flip-Flops

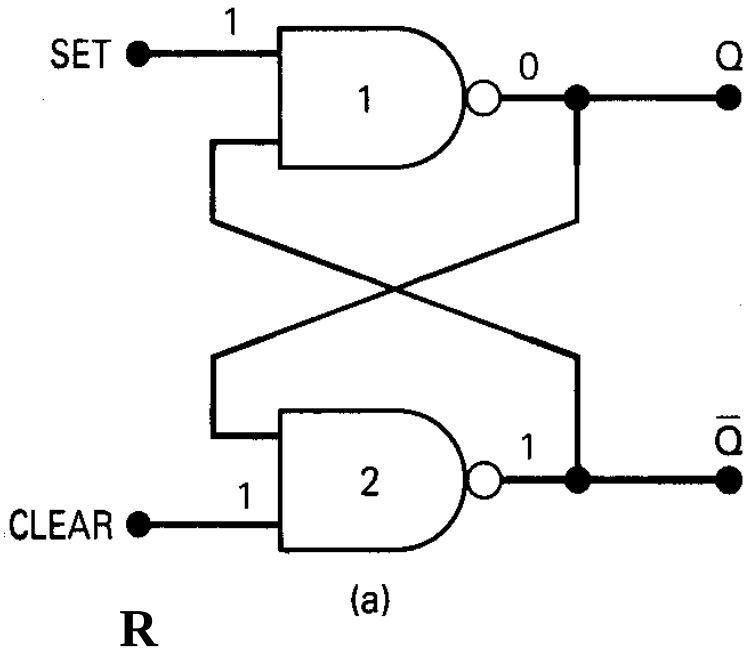
Basic flip-flop circuit with NAND gates (NAND latch)

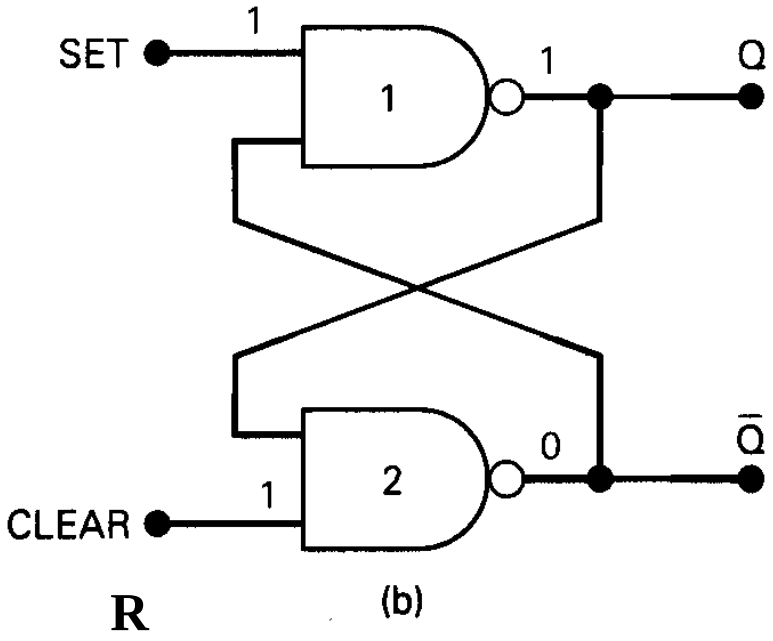


S	R	Q	$\overline{Q}$	
1	0	0	1	
1	1	0	1	(after S=1, R=0)
0	1	1	0	
1	1	1	0	(after S=0, R=1)
0	0	1	1	↖ NA

Basic flip-flop circuit with NAND gates

NAND latch has two possible resting states when SET = CLEAR = 1.



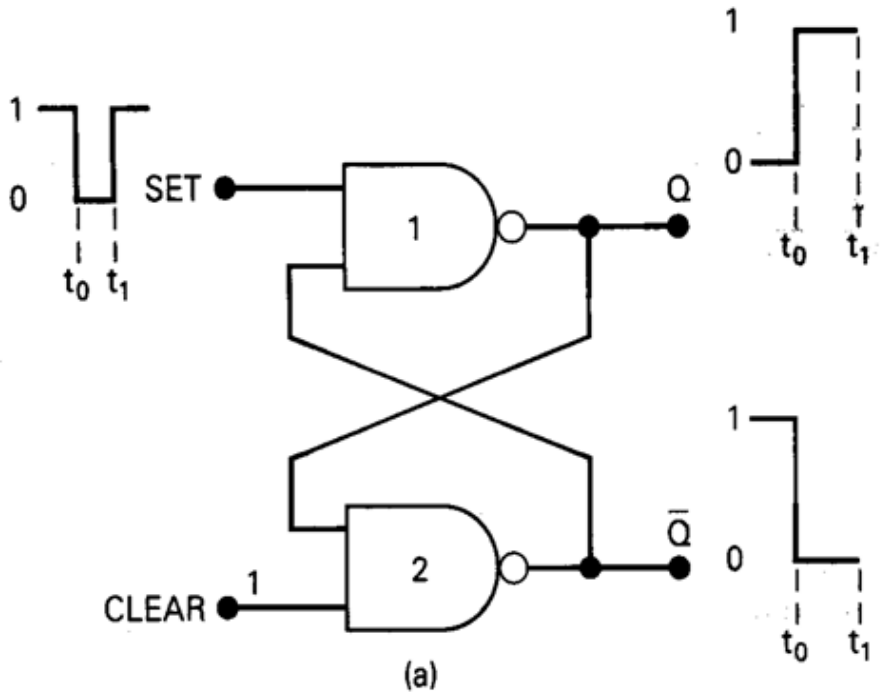


After S=1, R=0

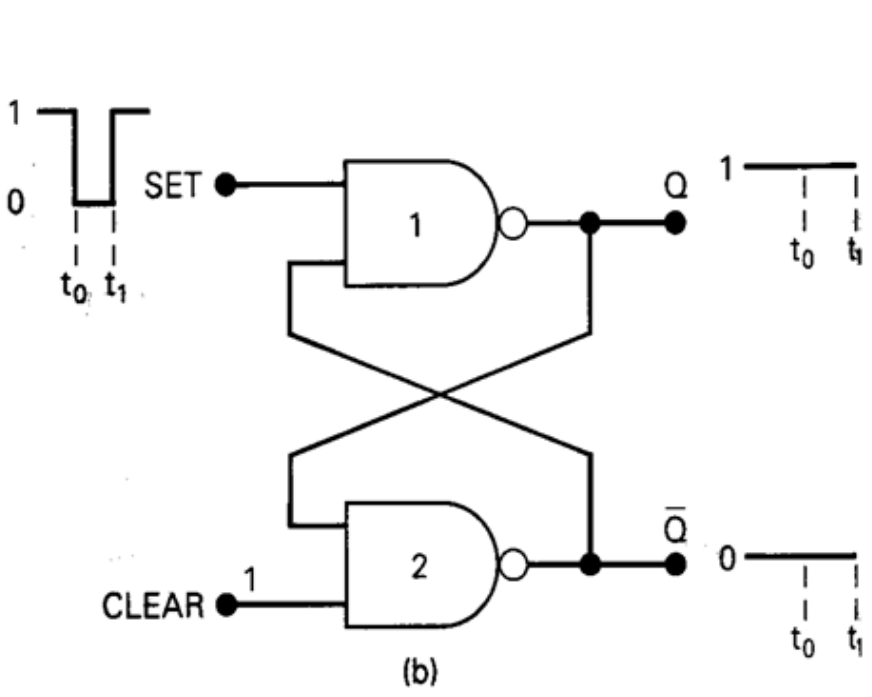
After S=0, R=1

Basic flip-flop circuit with NAND gates

Figure Pulsing the SET input to the 0 state will always produce the $Q = 1$, $\overline{Q} = 0$: output state (a) $Q = 0$ prior to SET pulse; (b) $Q = 1$ prior to SET pulse.



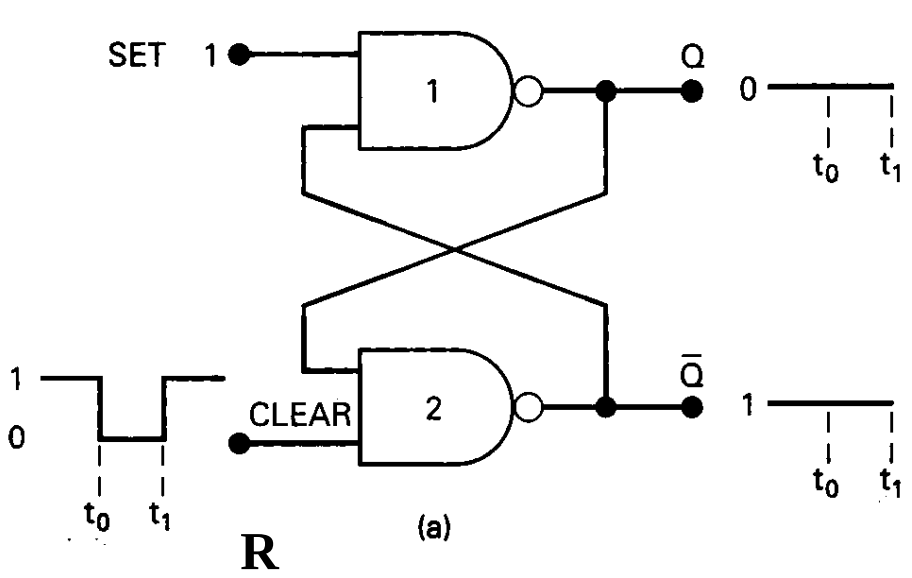
R

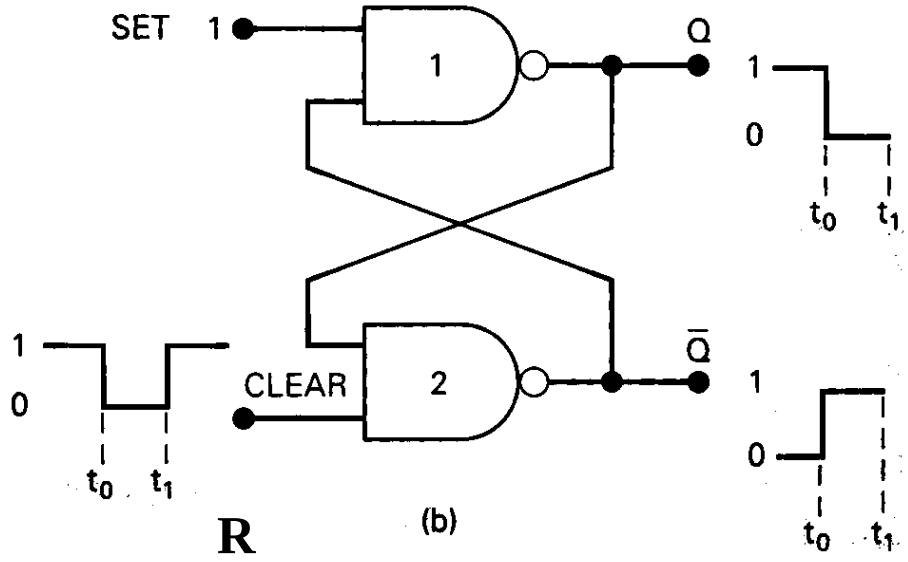


R

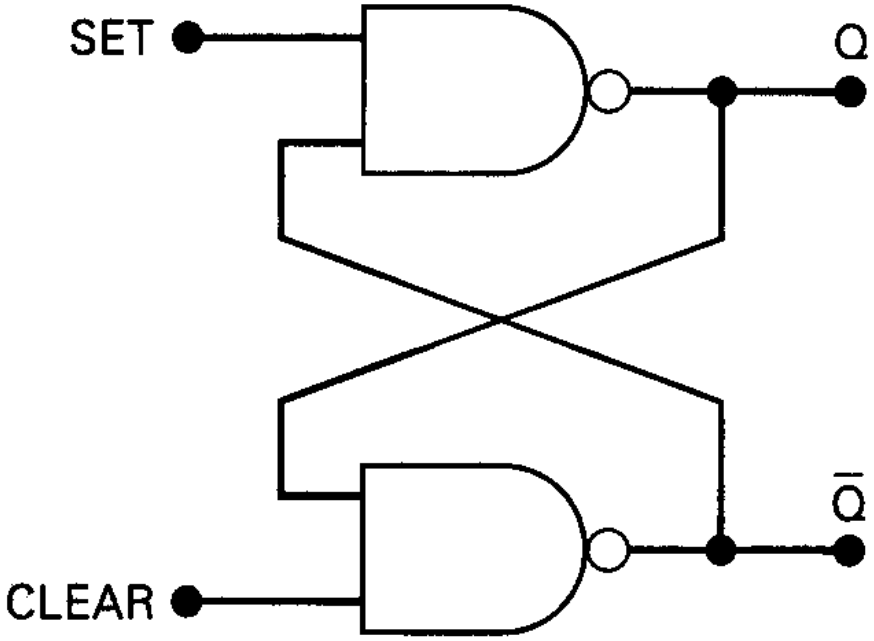
Basic flip-flop circuit with NAND gates

Figure Pulsing the CLEAR input to the LOW state will always produce $Q = 0$, $\overline{Q} = 1$:
(a) $Q = 0$ prior to CLEAR pulse; (b) $Q = 1$ prior to CLEAR pulse.





Basic flip-flop circuit with NAND gates



(a)

Set	Clear	Output
1	1	No change
0	1	Q = 1
1	0	Q = 0
0	0	Invalid*

*produces $Q = \bar{Q} = 1$

(b)

(a) NAND latch; (b) truth table.

Flip-Flops

- Truth Table for the RS Flip-flop

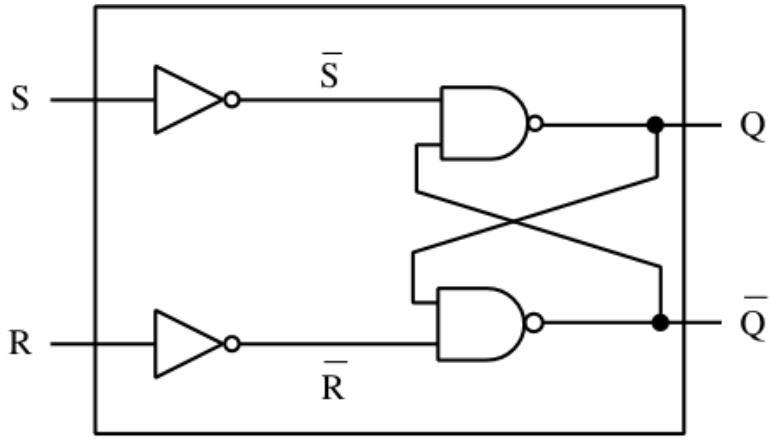
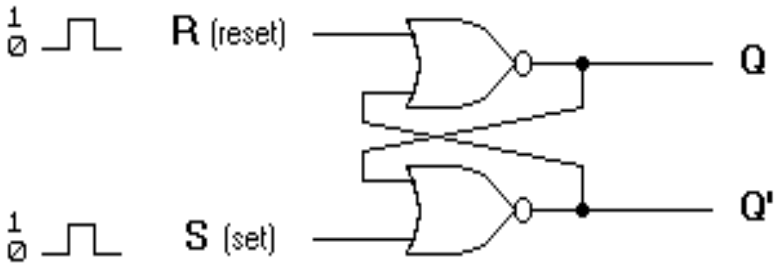


Table 6.4 Truth table for the RS flip-flop

Inputs		Outputs	
S	R	Q	$\overline{Q}$
0	0	Q_0	$\overline{Q_0}$
1	0	1	0
0	1	0	1
1	1	NA	

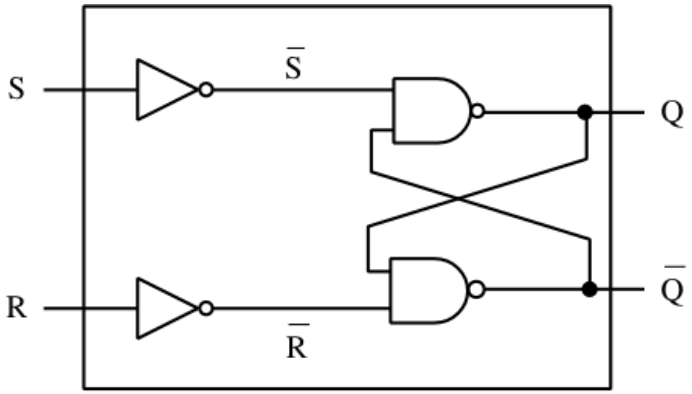
Compare with



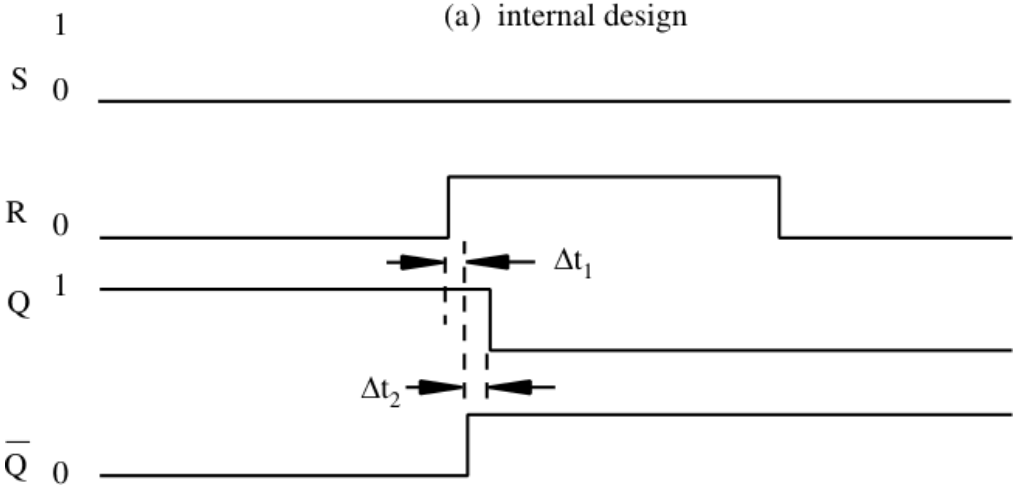
S R	Q Q'	
1 0	1 0	
0 0	1 0	(after S=1, R=0)
0 1	0 1	
0 0	0 1	(after S=0, R=1)
1 1	0 0	← NA

Flip-Flops

- RS flip-flop internal design and timing



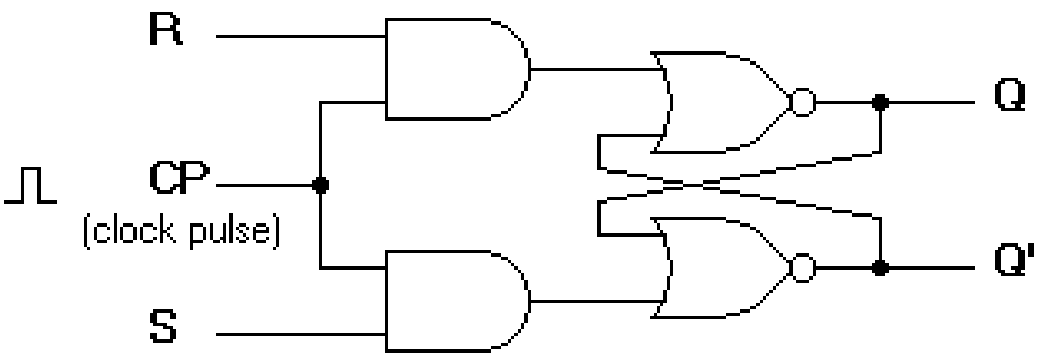
(a) internal design



(b) timing diagram

Triggering of Flip-Flops

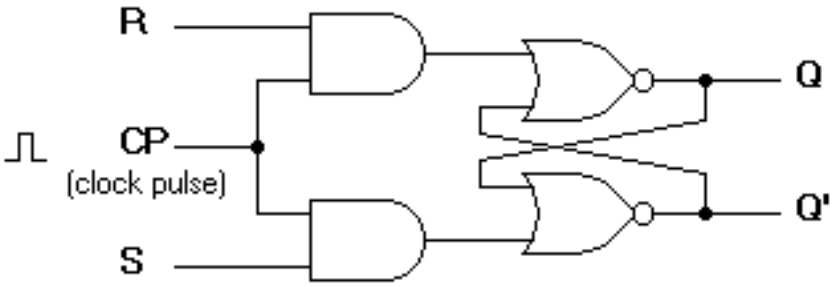
- The clocked SR flip-flop consists of a basic NOR flip-flop and two AND gates. The outputs of the two AND gates remain at 0 as long as the clock pulse (or CP) is 0, regardless of the S and R input values. When the clock pulse goes to 1 (positive-edge transition), information from the S and R inputs passes through to the basic flip-flop. With both S=1 and R=1, the occurrence of a clock pulse causes both outputs to momentarily go to 0. When the pulse is removed, the state of the flip-flop is indeterminate, i.e., either state may result, depending on whether the set or reset input of the flip-flop remains a 1 longer than the transition to 0 at the end of the pulse.

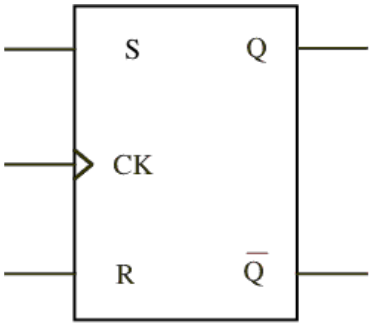


Q S R	Q(t+1)
0 0 0	0
0 0 1	0
0 1 0	1
0 1 1	indeterminate
1 0 0	1
1 0 1	0
1 1 0	1
1 1 1	indeterminate

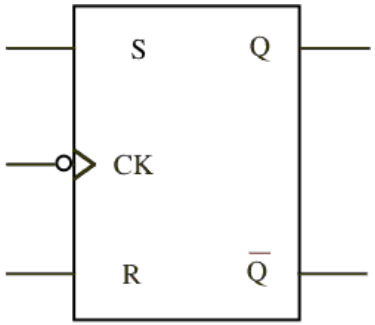
↑ CK

Edge-triggered RS flip-flops





(a) positive edge-triggered



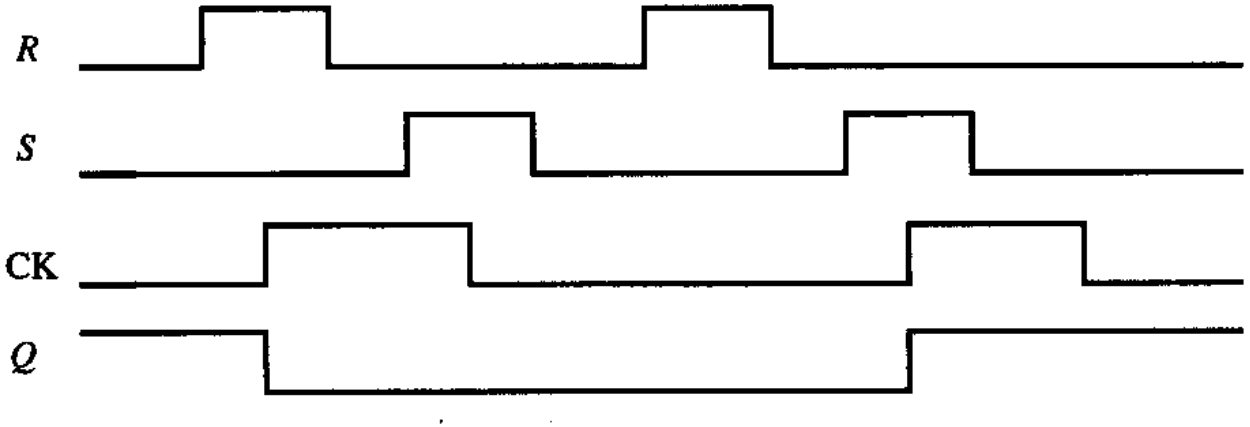
(b) negative edge-triggered

Table 6.5 Positive edge-triggered RS flip-flop truth table

S	*R*	CK	*Q*	$\overline{Q}$
0	0	↑	Q_0	$\overline{Q_0}$
1	0	↑	1	0
0	1	↑	0	1
1	1	↑	NA	
X	X	0, 1	Q_0	$\overline{Q_0}$

As long as no positive edge transition

Edge-triggered RS flip-flops

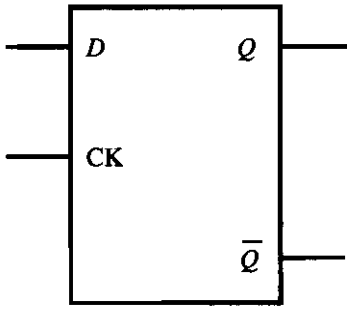


Positive edge-triggered RS flip-flop timing diagram.

1. If *S* and *R* are both 0 when the clock edge is encountered, the output state remains unchanged.
2. If *S* is 1 and *R* is 0 when the clock edge is encountered, the flip-flop output is **set** to 1. If the output is at 1 already, there is no change.
3. If *S* is 0 and *R* is 1 when the clock edge is encountered, the flip-flop output is **reset** to 0. If the output is at 0 already, there is no change.
4. *S* and *R* should never both be 1 when the clock edge is encountered.

Latch-not edge triggered device

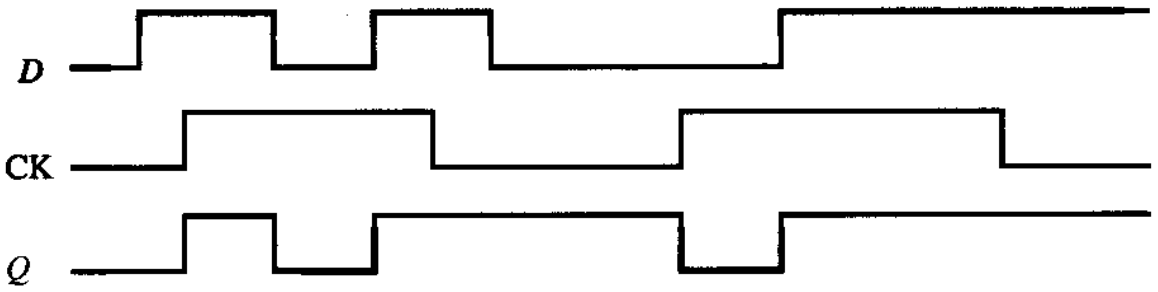
- Output Q tracks the input D as long as CK is high
  - Transparent when CK is high



Latch.

Table 6.6 Latch truth table

D	CK	*Q*	$\overline{Q}$
0	1	0	1
1	1	1	0
X	0	Q_0	$\overline{Q}_0$



Latch timing diagram.

Asynchronous inputs

- Preset and clear functions to override any inputs… called asynchronous inputs
- Present is to set the output Q to high (1), clear input is to set the output Q to low

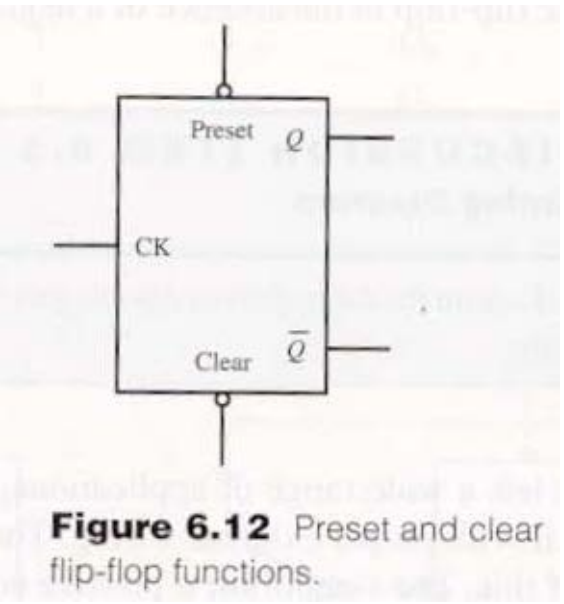
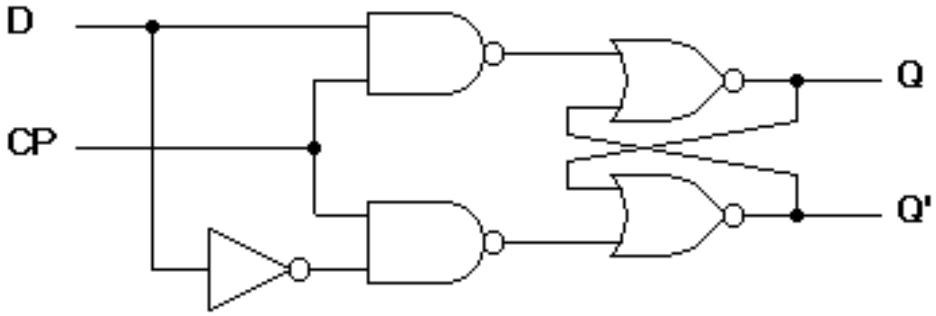
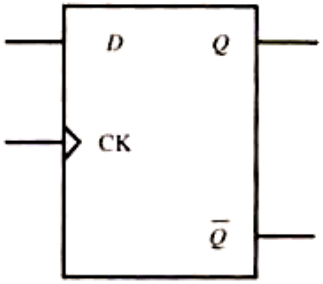


Figure 6.12 Preset and clear flip-flop functions.

D Flip-Flops

- The D flip-flop is a modification of the clocked SR flip-flop. The D input goes directly into the S input and the complement of the D input goes to the R input. The D input is sampled during the occurrence of a clock pulse. If it is 1, the flip-flop is switched to the set state (unless it was already set). If it is 0, the flip-flop switches to the clear state.





Positive edge-triggered D flip-flop.

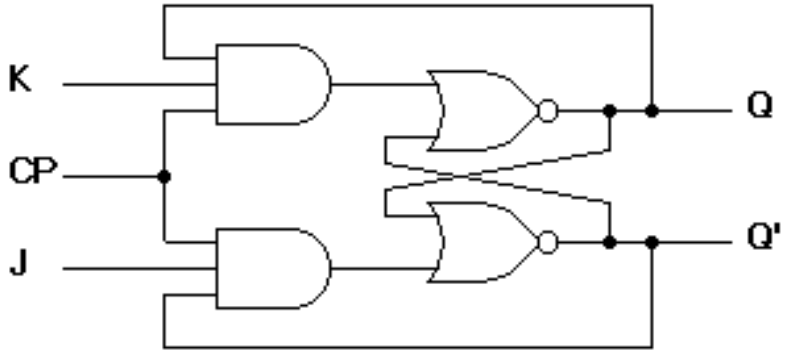
Table 6.7 Positive edge-triggered D flip-flop truth table

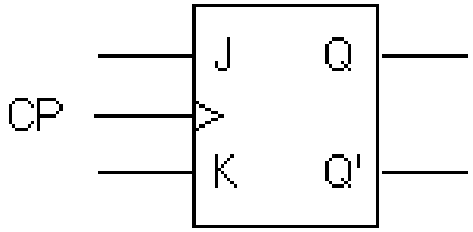
D	CK	*Q*	$\overline{Q}$
0	↑	0	1
1	↑	1	0
X	0	Q_0	$\overline{Q_0}$
X	1	Q_0	$\overline{Q_0}$

Q D	Q(t+1)
0 0	0
0 1	1
1 0	0
1 1	1

JK Flip-Flop

- A JK flip-flop is a refinement of the SR flip-flop in that the indeterminate state of the SR type is defined in the JK type. Inputs J and K behave like inputs S and R to set and clear the flip-flop .
- J is for set and the letter K is for clear.
- When logic 1 inputs are applied to both J and K simultaneously, the flip-flop switches to its complement state, i.e., if Q=1, it switches to Q=0 and vice versa.
- Output Q is ANDed with K and CP inputs so that the flip-flop is cleared during a clock pulse only if Q was previously 1. Similarly, output Q' is ANDed with J and CP inputs so that the flip-flop is set with a clock pulse only if Q' was previously 1.

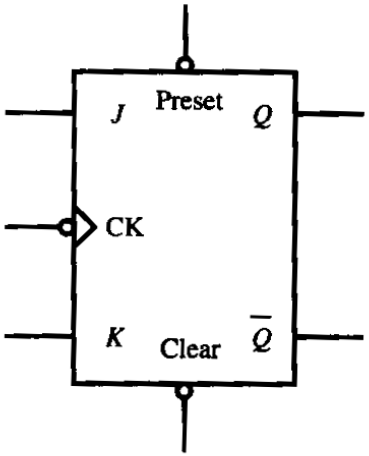




Transition table

Q J K	Q(t+1)
0 0 0	0
0 0 1	0
0 1 0	1
0 1 1	1
1 0 0	1
1 0 1	0
1 1 0	1
1 1 1	0

JK Flip-Flop



Negative edge-triggered JK flip-flop.

Table 6.8 Truth table for a negative edge-triggered JK flip-flop

$\overline{\text{Preset}}$	$\overline{\text{Clear}}$	CK	J	K	Q	$\overline{Q}$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0			NA		
1	1	↓	0	0	Q_0	$\overline{Q}_0$
1	1	↓	1	0	1	0
1	1	↓	0	1	0	1
1	1	↓	1	1	$\overline{Q}_0$	Q_0
1	1	0, 1	X	X	Q_0	$\overline{Q}_0$

JK Flip-Flop

Table 6.9 Positive edge-triggered T flip-flop truth table

T	$\overline{\text{Preset}}$	$\overline{\text{Clear}}$	Q	$\overline{Q}$
↑	1	1	$\overline{Q}_0$	Q_0
0	1	1	Q_0	$\overline{Q}_0$
1	1	1	Q_0	$\overline{Q}_0$
X	0	1	1	0
X	1	0	0	1

T (toggle) flip-flop
Toggle: the output changes to opposite state

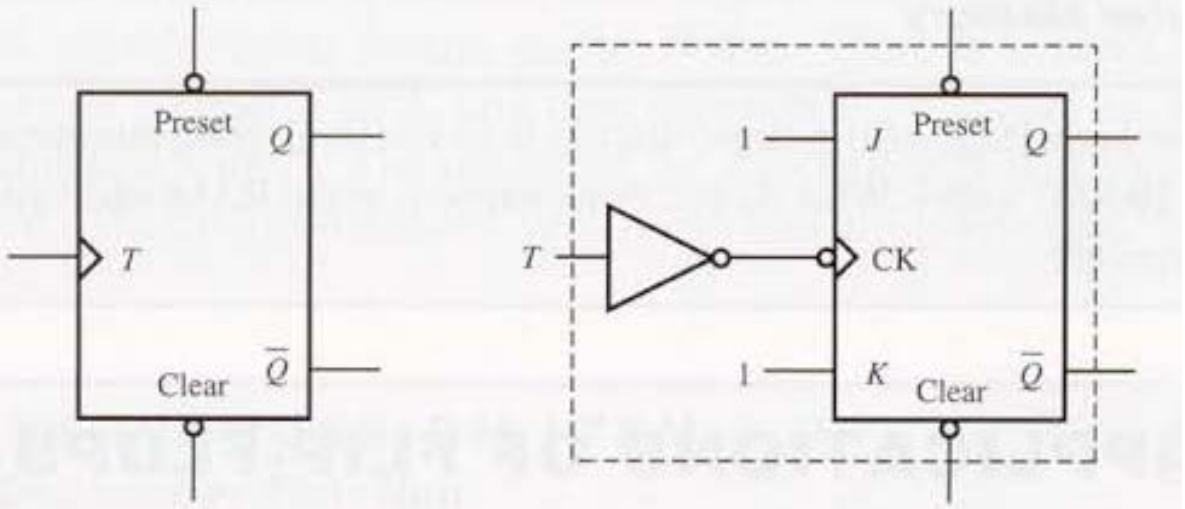
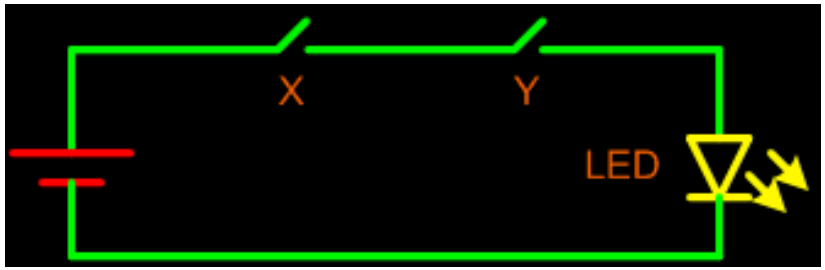


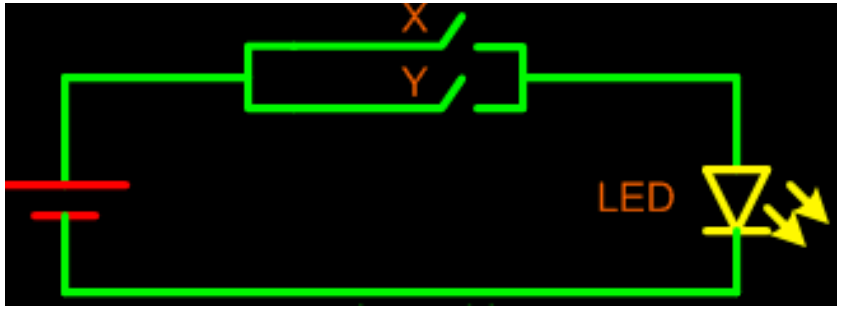
Figure 6.15 Positive edge-triggered T flip-flop.

Switch circuits

- Logic described previously can be implemented as an actual circuit. Switches are left open for logic 0 and closed for logic 1.
- Two variable AND circuit X·Y

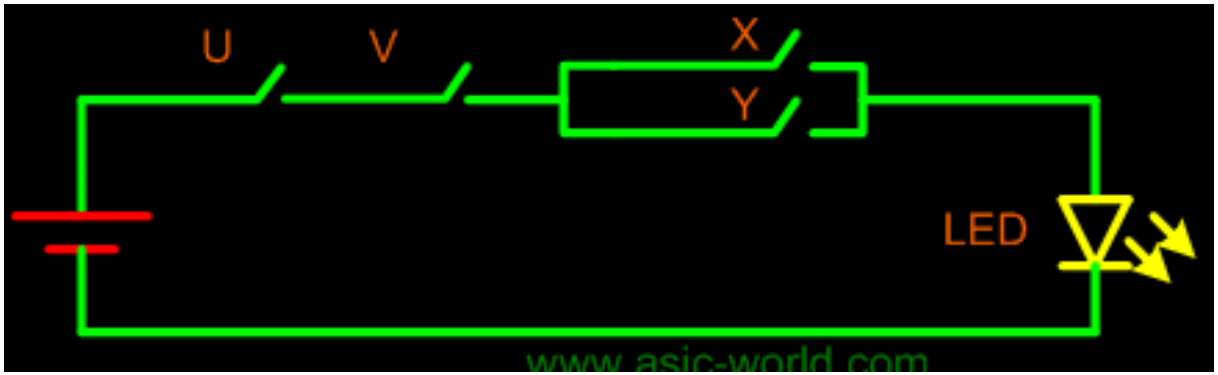


- Two variable OR circuit X + Y



Switch circuits

- Four variable circuit UV(X + Y)



AND Gate

AND gate AND logic

$C = A \cdot B$

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

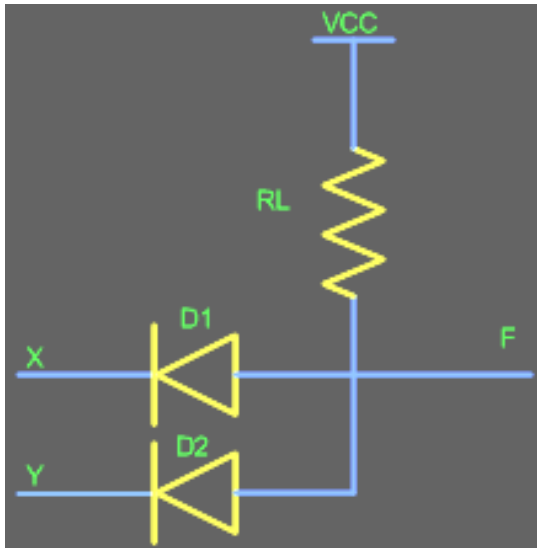
- Two input AND gate using "diode-resistor" logic is shown in figure below, where X, Y are inputs and F is the output.

If X = 0 and Y = 0, then both diodes D1 and D2 are forward biased and thus both diodes conduct and pull F low.

If X = 0 and Y = 1, D2 is reverse biased, thus does not conduct. But D1 is forward biased, thus conducts and thus pulls F low.

If X = 1 and Y = 0, D1 is reverse biased, thus does not conduct. But D2 is forward biased, thus conducts and thus pulls F low.

If X = 1 and Y = 1, then both diodes D1 and D2 are reverse biased and thus both the diodes are in cut-off and thus there is no drop in voltage at F. Thus F is HIGH.



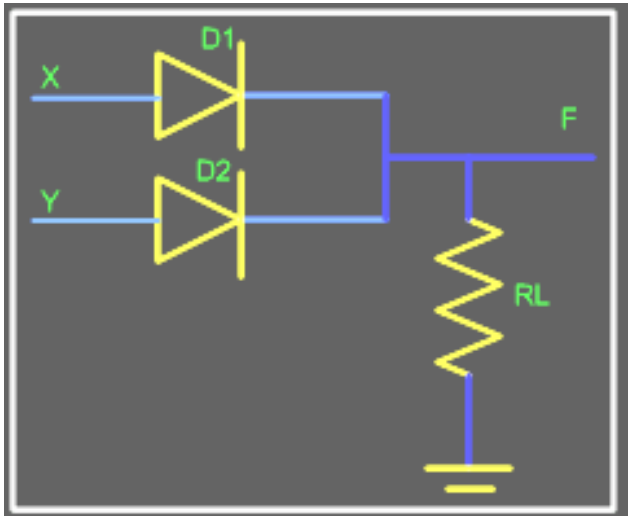
OR Gate

OR gate OR logic

$C = A + B$

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Two input OR gate using "diode-resistor" logic is shown in figure below, where X, Y are inputs and F is the output:



If X = 0 and Y = 0, then both diodes D1 and D2 are reverse biased and thus both the diodes are in cut-off and thus F is low.

If X = 0 and Y = 1, D1 is reverse biased, thus does not conduct. But D2 is forward biased, thus conducts and thus pulling F to HIGH.

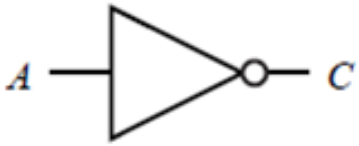
If X = 1 and Y = 0, D2 is reverse biased, thus does not conduct. But D1 is forward biased, thus conducts and thus pulling F to HIGH.

If X = 1 and Y = 1, then both diodes D1 and D2 are forward biased and thus both the diodes conduct and thus F is HIGH.

NOT Gate

Inverter (INV, NOT)

Invert signal (complement)



$C = \bar{A}$

A	C
0	1
1	0

NOT gate using "transistor-resistor" logic is shown in the figure below, where X is the input and F is the output.

When X = 1, The transistor input pin 1 is HIGH, this produces the forward bias across the emitter base junction and so the transistor conducts. As the collector current flows, the voltage drop across RL increases and hence F is LOW.

When X = 0, the transistor input pin 2 is LOW: this produces no bias voltage across the transistor base emitter junction. Thus Voltage at F is HIGH.