Fundamentals of Logic Design (EE316)
Fall 2014

Course:
EE316; Unique #s: 16700, 16705, 16710, 16715, 16720, 16725, 16730, 16735

Lecture:
MWF 12-1PM in RLM 4.102

Lab: In ECJ 1.222

Unique Number	Day	Time	TA
16700	F	10 – 11AM	
16705	Th	11AM - noon	
16710	F	11AM - noon	
16715	Th	1 – 2 PM	
16720	W	2 – 3 PM	
16725	T	2:30 – 3:30 PM	
16730	M	3 – 4 PM	
16735	T	4 – 5 PM	

Instructor:
Dr. Nina K. Telang
Office Hours: W: 1:30-3PM, F: 1:30-4PM in ACA 108
Email: telang@ece.utexas.edu

Teaching Assistants:
Biying Xu (being.xby@gmail.com)
Manoj Rao (manojhrao@utexas.edu)
Michael Mahoney (mwmahoney@utexas.edu)
Ken Tang (kenleetang@gmail.com)

Text:
Fundamentals of Logic Design, 7th Edition, by Charles Roth and Larry Kinney. The latest edition of the text is required. The book includes a CDROM with software that you will need to perform the labs.

Course Objectives:
The textbook for this course is organized by units. We will be covering all units except for Units 6 and 19. The important topics covered will be:

1. Binary Arithmetic and Boolean Algebra (Units 1-5)
2. Implementation of Logic Functions using NAND and NOR gates (Units 7-8)
3. Muxes, Decoders, and Programmable Logic Devices (Unit 9)
4. VHDL – Hardware Description Language (Unit 10)
5. Design of Sequential Logic Circuits: latches, flip-flops, clocks, using both state charts as well as VHDL (Units 11-18)
6. System Level Design with VHDL (Unit 20)

Prerequisites:
EE 306: Introduction to Computing OR CS 429: Computer Organization and Programming

Attendance:
You are **expected to attend** each and every lecture. We will be doing in-class exercises and pop-quizzes and you will be evaluated on your classroom participation.

Lecture Schedule:

Week	Unit	Topic
8/27 – 8/29	Units 1-2	Introduction, Number Systems and Conversion
9/2 - 9/5	Units 2-3	Boolean Algebra
9/8 – 9/12	Units 4-5	Applications of Boolean Algebra
9/15 – 9/19	Unit 7	Multi-level logic with NAND and NOR gates
9/22 – 9/26	Unit 8	Combinational Circuit Design and Simulation using gates
9/29 – 10/3	Unit 9	Multiplexers, Decoders, and Programmable Logic Devices
10/6 – 10/10	Unit 10	Introduction to VHDL
10/13 – 10/17	Unit 11	Latches and Flip-flops
10/20 – 10/24	Unit 12	Registers and Counters
10/27 – 10/31	Unit 13	Analysis of Clocked Sequential Circuits
11/3 – 11/7	Unit 14-15	State graphs and tables, state minimization
11/10 – 11/14	Unit 16	Sequential Circuit Design
11/17 – 11/21	Unit 17	VHDL for Sequential Logic
11/24 – 11/26	Unit 18	Circuits for Arithmetic Operations
12/1 – 12/5	Unit 20	VHDL for Digital System Design

Homework:
Homework problems will be assigned almost every week. You are expected to submit your homework at the beginning of class. No late submission will be graded.
Below is a **tentative** list of homework problems and due dates. Announcements will be made in class and on Canvas regarding changes. If no changes are announced, assume the list below.

HW1: 9/5	1.10(b), 1.11(a), 1.12(a), 1.18(a-b), 1.19(c), 1.20(a), 1.25, 1.39 [1.36 in 6th], 2.10(b), 2.11(a-c), 2.13(c), 2.15(a), 2.16(a), 2.18(b-d), 2.22(c)
HW2: 9/12	3.13(a), 3.15(b), 3.16(a), 3.19(a), 3.21(c), 3.33(a), 3.36, 4.16, 4.19(c), 4.20, 4.27(a-c), 4.40
HW3: 9/19	5.14(b-c), 5.15(b-c), 5.20(d), 5.22(b), 5.33, 5.35(a-c)
HW4: 9/26	7.20, 7.21(a-b), 7.25(a), 7.42 [7.39 in 6th], 7.45(a) [7.42(a) in 6th]
HW5: 10/1	8.6, 8.7, 8.10, 8.11, 9.14, 9.16, 9.19
Midterm Exam#1: 10/3 (Units 1-8)	
HW6: 10/17	9.31, 9.41, 10.10, 10.11, 10.14(a), 10.15, 11.13, 11.14, 11.18, 11.26
HW7: 10/24	12.21(a-c) [12.20(a-c) in 6th], 12.26 [12.25 in 6th], 12.36 [12.32 in 6th]

HW8: 11/3	13.7, 13.18 [13.21 in 6th], 14.12, 14.14, 14.36
Midterm Exam#2: 11/7 (Units 9-13)	
HW9: 11/17	15.12(a,c,d), 15.24, 15.37(a-b), 15.38(c), 16.21(a) [16.18(a) in 6th], 16.23(a-b) [16.20(a-b)], 16.33(a) [16.29(a) in 6th]
HW10: 12/1	17.18(a,c,d), 17.20(a-b), 17.24, 17.28(a)
HW11: do not submit	18.9, 18.12(a), 18.19(a), 18.28(a-b)

Lab Schedule:

You are expected to sign up for one of the lab sessions associated with the class. The labs will be conducted in ECJ 1.222. Lab weeks run from Tuesday to the following Monday, except for the last week which is a Monday to Friday week.

The software package that comes with the textbook includes *LogicAid*, *SimUaid*, and *DirectVHDL*. It is recommended that you install this software on your own personal computer. Lab assignments are due by the end of student's lab section. Submission of a hardcopy of lab assignment (coverpage, printout, etc.) will serve as a timestamp. After submitting a hardcopy, students still need to have the lab checked out by any TA. Checkouts will progress in the order submitted. If the wait is too long, students can come back and checkout anytime in the week after the lab is due. Labs turned in late receive 5% penalty per working day that it is late. Labs need to be checked out within a week after the due date, after which students will not receive any credit for the check-out portion of the lab (which is 50% of the lab grade). Early submission of labs receives 5% extra credit if submitted 2 working days early, and 2% extra credit for 1 working day early. Early submission is encouraged and can save time on the checkout process. Please put name and lab section on lab submissions.

Week	**Lab**	**Topic**	**Demo (by TA)**	**Due By**
Week 2	Lab 1	Unit 4 - Design a 4-input 1-output circuit and verify with SimUaid. (4.13 or 4.14)	9/2 – 9/8	9/9 – 9/15
Week 3	No lab	Problem solving session	9/9 – 9/15	N/A
Week 4	Lab 2	Unit 8 - Design logic for a 7 segment display using DesignAid and SimUaid. (8.A-8.S)	9/16 – 9/22	9/23-9/29
Week 5	Lab 3a	Unit 10 - Download your design from Lab 2 to the Xilinx board.	9/23-9/29	9/30-10/6
Week 6	Lab 3b	Unit 10 - Design an adder/decoder/mux/ROM in VHDL using DirectVHDL. (10.A-10.N)	9/30-10/6	10/14-10/20
Week 7	No new lab	Problem Review	10/7-10/13	N/A
Week 8	Lab 4	Unit 12 - Use SimUaid to design a circuit that counts in a specified sequence. (12.10.a-12.10.n)	10/14-10/20	10/21-10/27
Week 9	Lab 5a/b	5.a Unit 16 - Design a state machine; implement in output and next-state logic with inv, 2/3/4 ip NAND/NOR (16.1-16.14) 5.b Unit 16 - Write your design and testbench	10/21-10/27	5.a 11/4-11/10 5.b 11/4-11/10

		from 5.1 in VHDL and download to the Xilinx board.		
Week 10	No new lab	Problem Review	10/28-11/3	N/A
Week 11	Lab 6	Unit 17 - Simulate a sequential design in VHDL (17.A - 17.M)	11/4-11/10	11/18-11/24
Week 12	No new lab	TBD	11/11-11/17	N/A
Week 13	Lab 7	Unit 20 - Design a multiplier/divider with VHDL (20.A-20.W)	11/18-11/24	12/1-12/5
Week 15	Final Exam Review	TBD	12/1-12/5	N/A

Grading Policy:

Homework/Classwork (Note that classwork includes pop-quizzes and group exercises)	10%
Labs	30%
Exams (2)	30%
Final	30%

Class information on-line:
The on-line information for this course is available on the Canvas site: http://courses.utexas.edu. In order to use this site you need your EID. Some things that will be available on this site:

- All lecture slides
- Homework assignments for the semester.
- Lab documents.

Web-based, password-protected class sites are associated with all academic courses taught at The University. Syllabi, handouts, assignments and other resources are types of information that will be available within these sites. Site activities could include exchanging e-mail, engaging in class discussions and chats, and exchanging files. In addition, electronic class rosters will be a component of the sites. Students who do not want their names included in these electronic class rosters must restrict their directory information in the Office of the Registrar, Main Building, Room 1. For information on restricting directory information see:
http://www.utexas.edu/student/registrar/ferpa/ferpa.qs.faculty.htm

Getting help: If you have a question please ask! Do not wait till the last minute. **I am available to answer questions after class during my office hours**, or by email.

Drop Policy: The last day to drop this course without permission from the Dean is the 4th class day. After this day, drops are approved only in the case of health or personal problems.
An engineering student should make an appointment with his/her departmental advisor to discuss adding or dropping any course if the change will alter the classes that were originally approved by the departmental advisor. If the add or drop requires the approval of the Dean, then the student will need to schedule an appointment with an Academic Advisor in the Office of Student Affairs, ECJ 2.200 (471-4321) to discuss the request.

Additional information can be found at: http://www.engr.utexas.edu/current/policies/pol_add-drop-wdraw.cfm

Academic Dishonesty: Cheating will **not** be tolerated and will be dealt with according to the policy established by the office of the Dean of Students.

Students with disability: The University of Texas at Austin provides, upon request, appropriate academic adjustments for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, or the College of Engineering Director of Students with Disabilities at 471-4321.