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PHASE 2

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ECE 4120

SPRING 2023

1. Modified Block Diagram

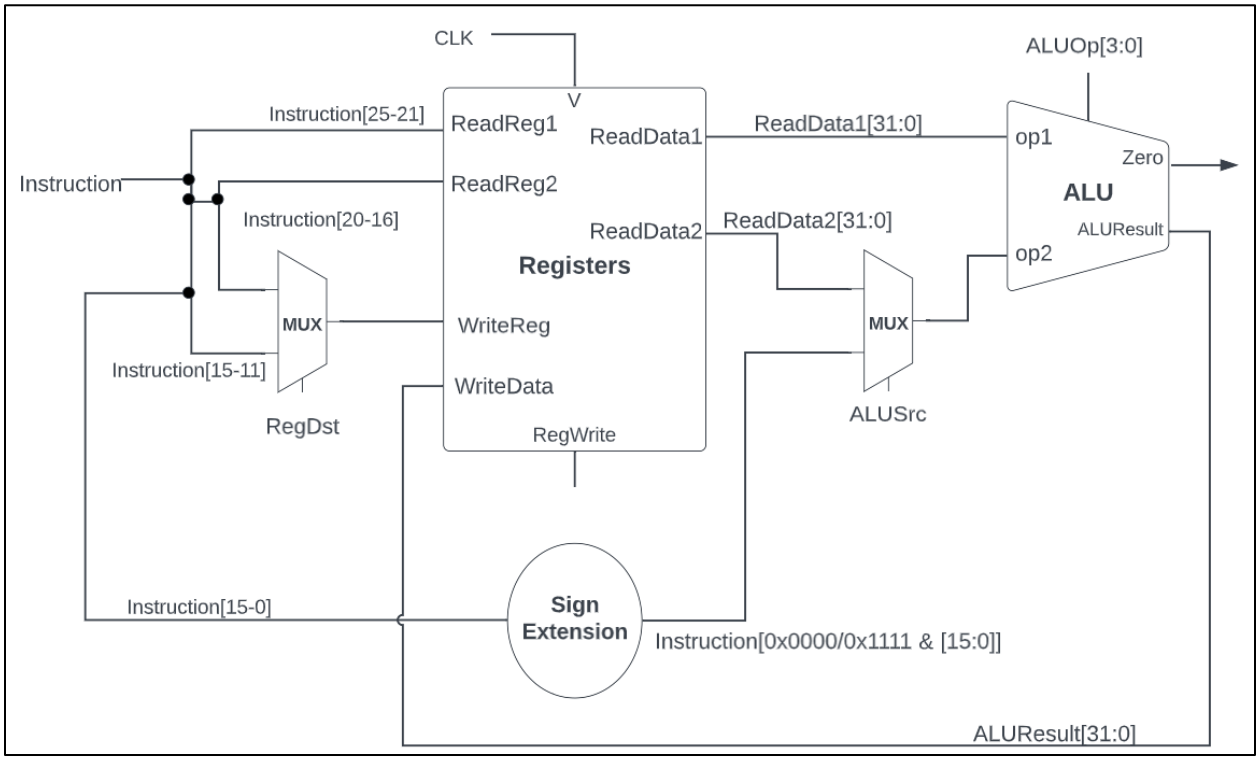

Figure 1: Block Diagram of Phase 2 Implementation

2. Objectives

The objective of Phase 2 is to fully implement the Decode Unit of the MIPS processor, as well as parts of the Execution Unit. The first large component of the Decode Unit is the Registers. This unit is responsible for storing the values of the 32 different registers the MIPS instruction set can manipulate and perform operations on. The next major component of Phase 2 is the Arithmetic Logic Unit (ALU). The ALU is responsible for performing mathematical and logical operations on selected registers when given an appropriate instruction from the Decode Unit. Finally, the Sign Extension Unit is implemented to transform the 16-bit immediate/address signal of the instruction fetched from memory to a 32-bit signal that can be fed into the ALU. Once all new components were created and tested, they were connected to the Phase 1 components to progress the completion of the MIPS processor.

3. Elaboration of VHDL Implementation

The Register Unit was broken into two sub-units: the Read Unit and the Write Unit. The first step was creating a 32-bit register component that would make up the 32 registers for the Register Unit. Next, a 32x1 multiplexer component was created to complete all necessary components for the Read Unit. Both the mux and the register were implemented using behavioral architecture for simplicity of code. The next component created was the 5x32 decoder to decipher which register was the be written to when the write enable was HIGH. With all of these components completed,

a higher-level Register Unit entity was created to port map all components through a structural architecture. The methodology of behavioral components port mapped to high level entities holds true for each major entity created in Phase 2 as it provides a simple and straight-forward approach to completing the design. The Sign Extension Unit was a single entity created using a behavioral architecture by concatenating the most significant bit of the input 16 times to itself to create a 32-bit output signal. The last major entity created was the ALU, which was also done using a behavioral architecture with a case statement that selects the appropriate operation based on the ALUOp input signal. The 2x1 multiplexers located before and after the Register Unit were created with a behavioral architecture using if-else statements. Finally, all components were port mapped in a top-level entity through a structural architecture to complete the entire Phase 2 circuit.

4. Flow Summary / RTL View / Technology Map

Flow Summary

<<Filter>>

Flow Status	Successful - Mon Mar 27 17:28:51 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	DU
Top-level Entity Name	Phase2
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	1,888 / 49,760 (4 %)
Total registers	1032
Total pins	115 / 360 (32 %)
Total virtual pins	0
Total memory bits	6,656 / 1,677,312 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

Figure 2: Flow Summary

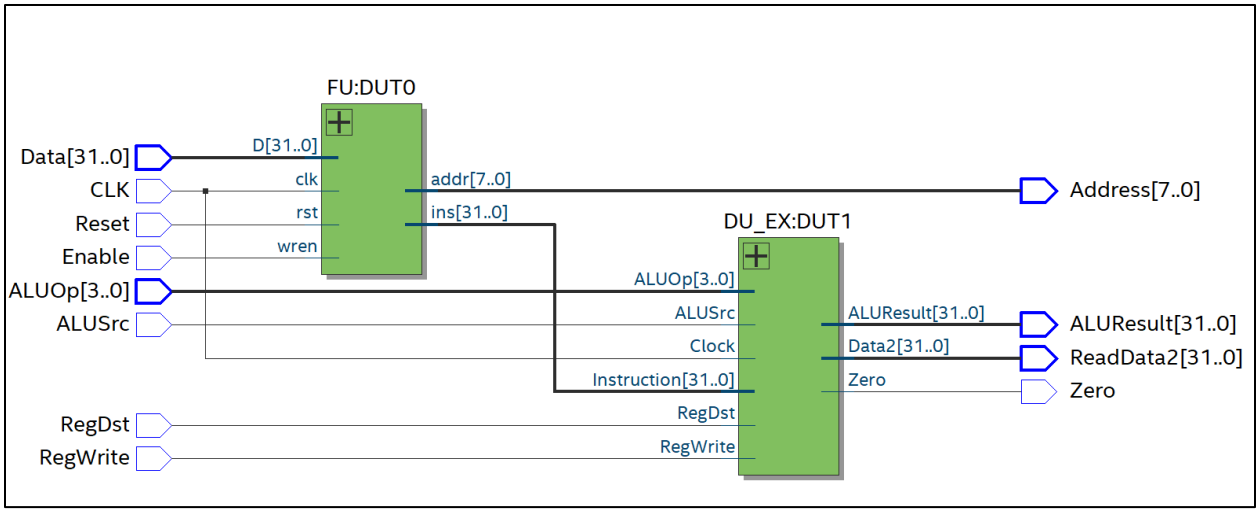

Figure 3: RTL View

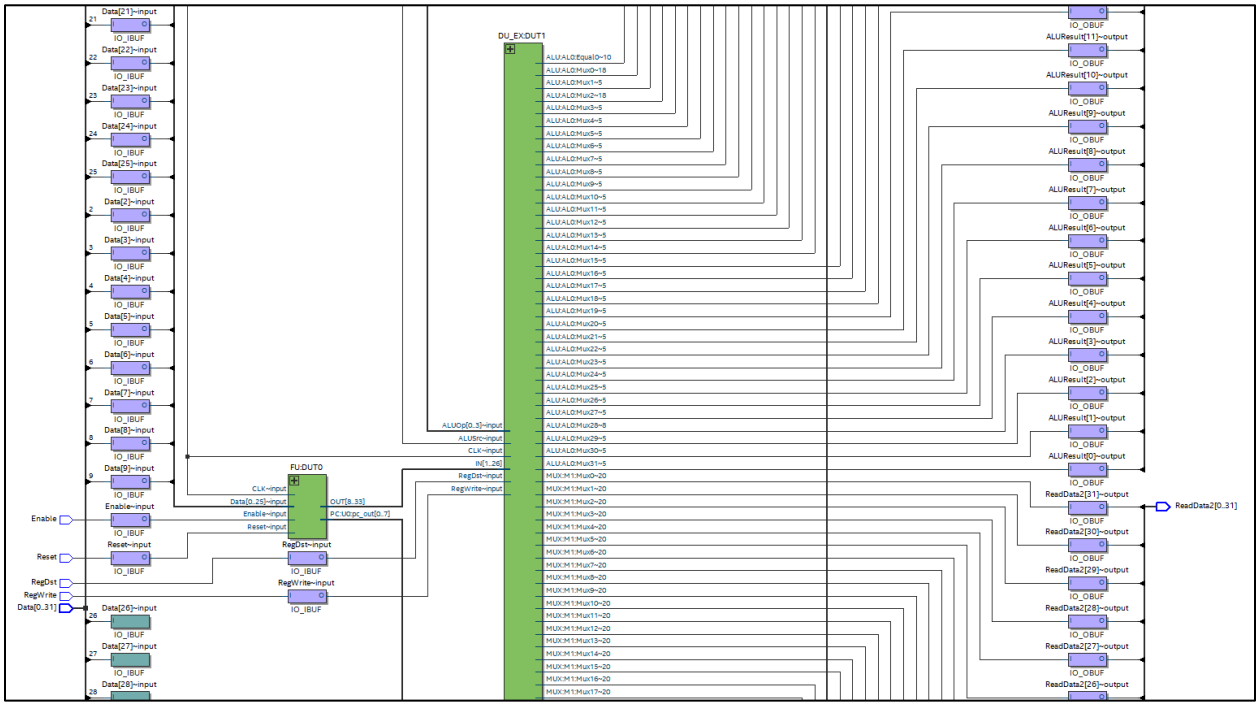

Figure 4: Technology Map View (Zoomed in)

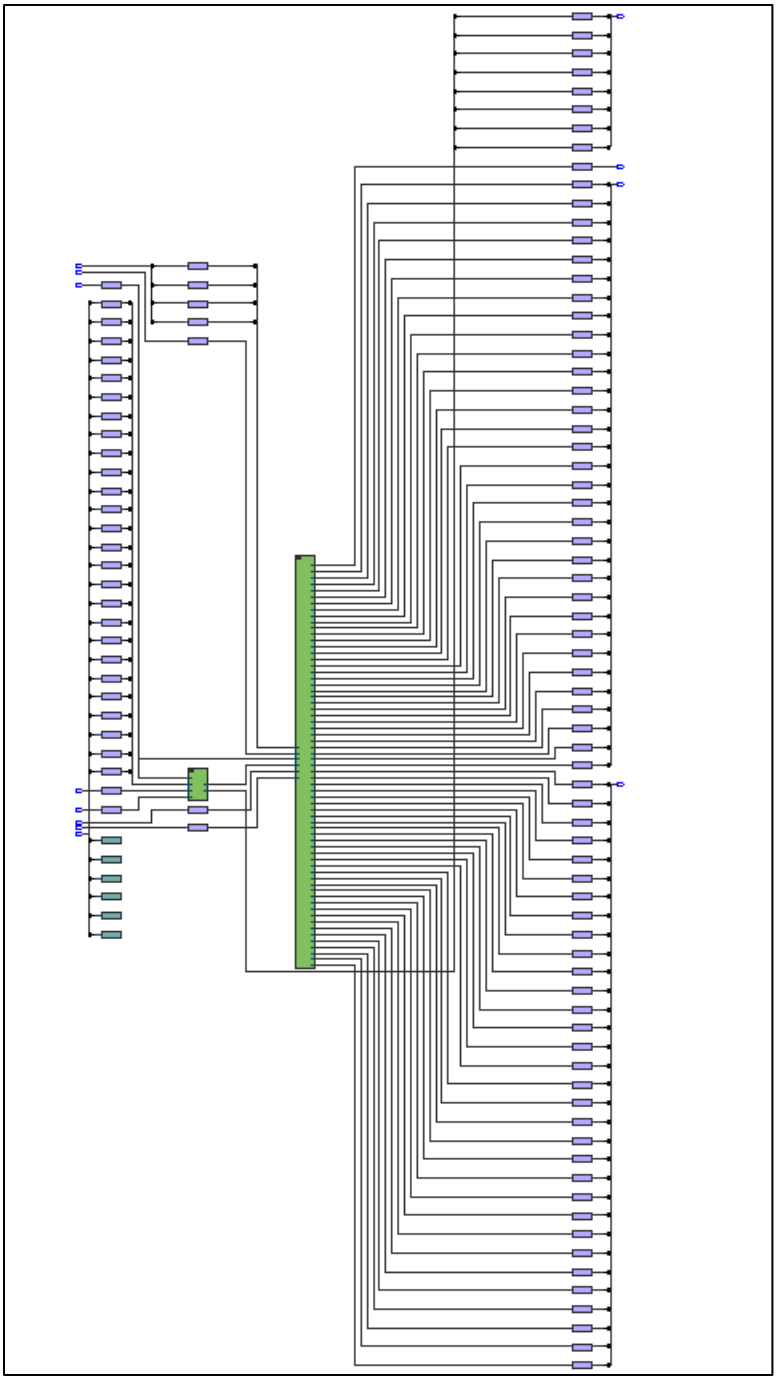

Figure 5: Technology Map View (Full View)

5. *Elaboration of Test Bench*

The test bench was created using an empty entity and a behavioral architecture that uses the top-level Phase 2 component. The Register Unit was loaded with the constant 0x0000000C (12 in decimal) for testing purposes in the reg32 entity so that each register holds the value 12. Instruction Memory was loaded the same as was done in Phase 1; inside of the behavioral architecture of the test bench after every 75 ns. Additionally, a clock signal with a 100 ns period was created to drive the system. The last step was to initialize the control signals to the muxes, ALU, and Register Unit. The Register Unit and mux signals were initialized in the signal definitions before the begin statement of the architecture. However, the ALUOp signal was changed every 100 ns to appropriately perform the operation on the instruction being input to the ALU from the Register Unit.

6. *Waveform Analysis*

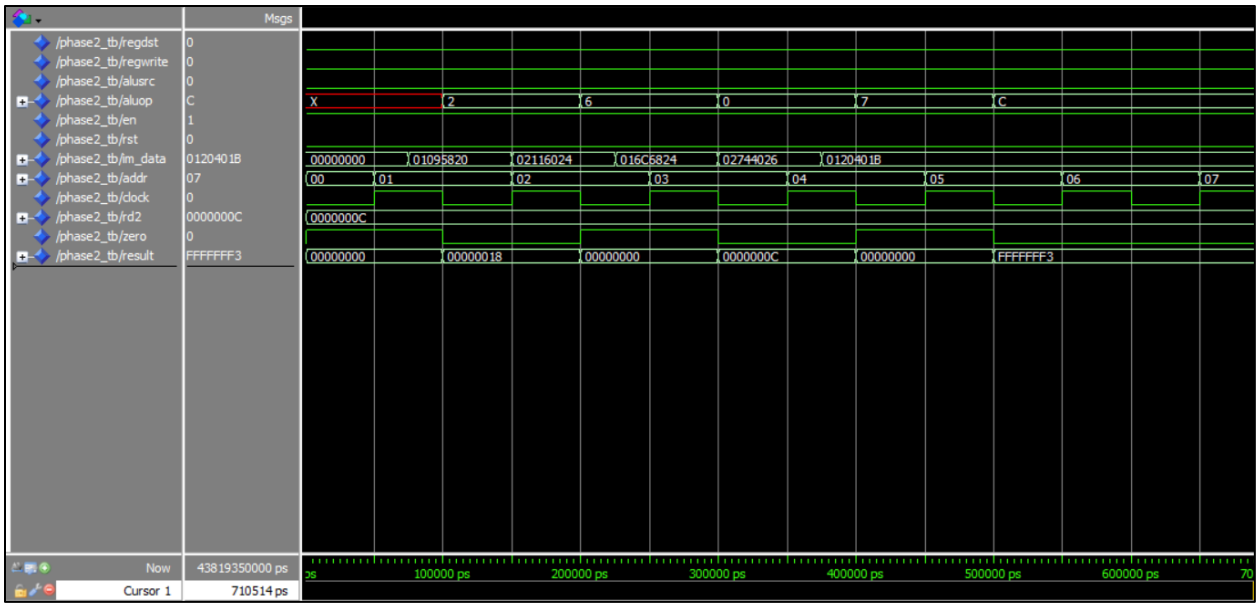

Figure 6: Phase 2 Waveform

The waveform shows each instruction input into the Registers Unit and the ALU Result, Zero Flag, and Read Data 2 outputs at each clock edge. As seen above, the Read Data 2 output is constantly 0x0000000C as it was initialized to this value for testing purposes. Additionally, the Zero Flag is only HIGH when the ALU Result is LOW, which displays proper functionality. Finally, the result changes based on the Instruction Data input. The loading is seen in the im_data signal and the addr signal which represent the Instruction to be executed and the Address of the PC counter respectively. This is the same method as used in Phase 1 of the project and based on the written results of the ALU Result, still works. The below table shows the different operations performed and their results as shown in the waveform.

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Table 1

Operation	Register Value(s)	ALU Result	Zero Flag
ADD	0x0000000C	0x00000018	0
SUB	0x0000000C	0x00000000	1
AND	0x0000000C	0x0000000C	0
XOR	0x0000000C	0x00000000	1
NOR	0x0000000C	0xFFFFFFF3	0

7. Timing Analyzer Results

a. **Fmax = 71.88 MHz**
b. **Setup Time = 0.013 ns**
    i. **Slack Time = 0.087 ns**
c. **Hold Time = 0.356 ns**
    i. **Slack Time = 0.356 ns**

Using a 14 ns clock frequency, the above setup and hold times are obtained using the Timing Analyzer in Quartus. Additionally, keeping the frequency of the clock below the 71.88 MHz maximum yields positive slack time for the setup time. The hold time is independent of the clock frequency but is still not violated with the addition of the Phase 2 hardware components. So, if the system is clocked at a rate of 71.88 MHz or less, then no hazards shall occur in the processor.

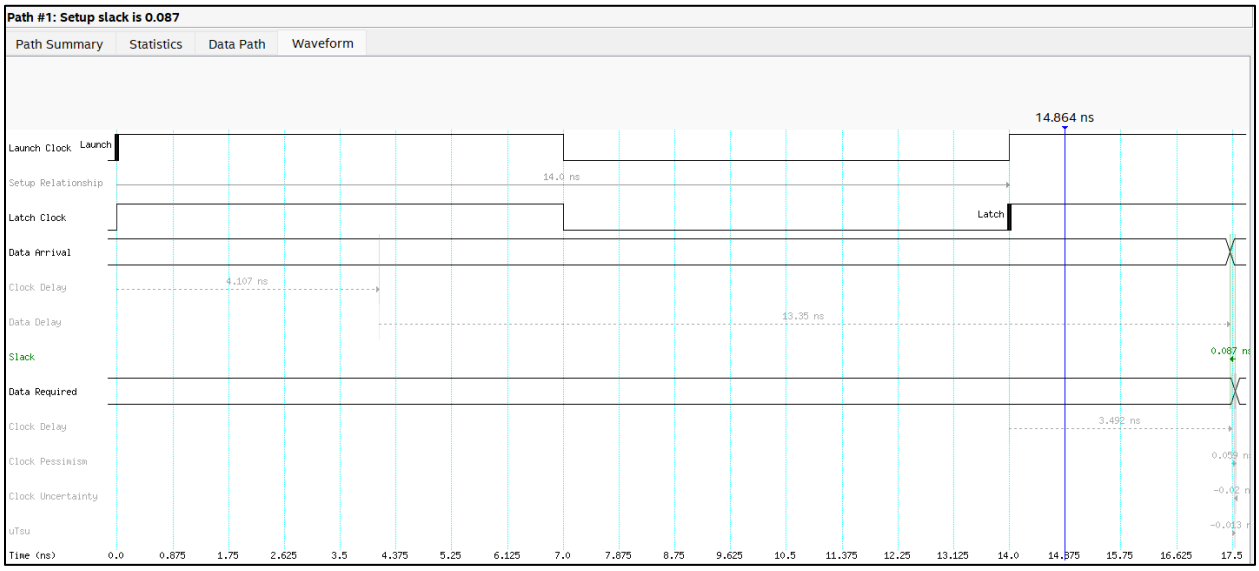

Figure 7: Setup Time Report Summary

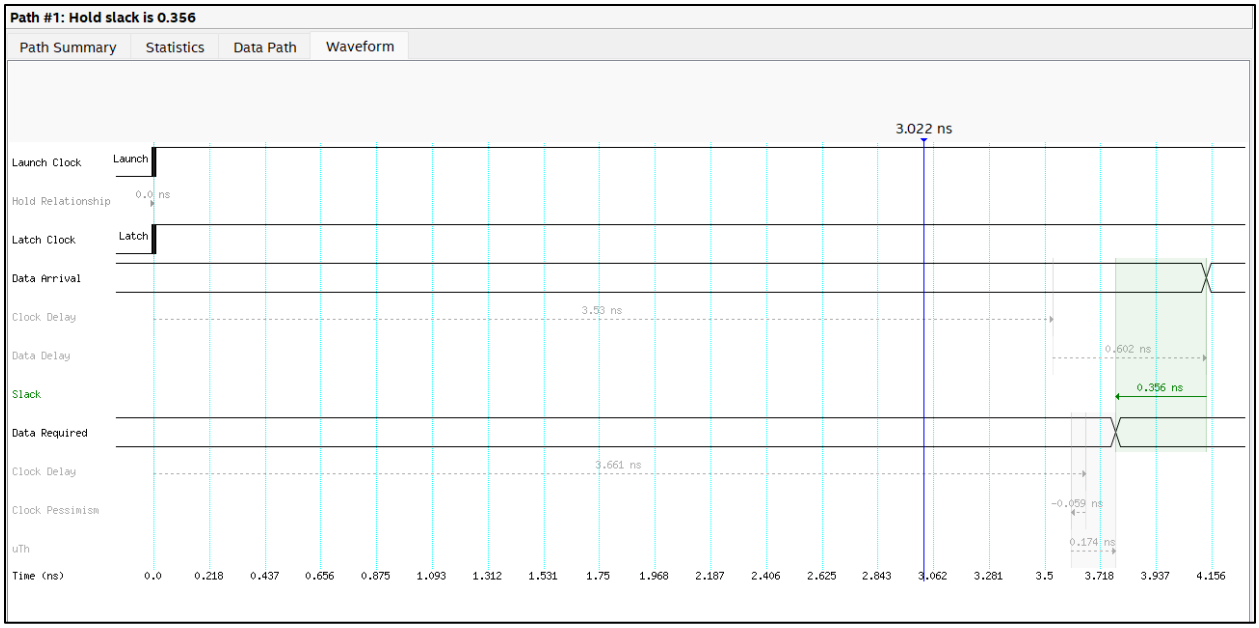

Figure 8: Hold Time Report Summary

8. Conclusions

Phase 2 of the MIPS processor project took ample amount of time to complete but added important functionality to the system. Overall, the results are promising and both Phase 1 and Phase 2 seem to be functioning together to produce correct results when tested. However, with the addition of the Phase 2 components, the maximum clock frequency of the system decreased by about 280 MHz going from ~350 MHz to ~70 MHz to avoid setup time violation. Additionally, no changes to hardware were required to maintain a valid hold time for the system as the additions of Phase 2 still yields positive slack time based on the results of the Timing Analyzer.