NAME:
NUMBER:
DATE: 24.01.2022

Q1:

Design a folded cascade OTA with pMOS transistors at the input and single ended output. The load of the OTA is 2pF. Ensure that the rising and falling Slew-rate are at least 50V/us, the GBW should be at least 50MHz and the low frequency gain should be at least 60dB. Draw the bode-plot of your designed OTA.

- Also calculate the non-dominant pole and pole-zero doublet
- Draw the bode-plot of your designed OTA.
- What is the phase margin of your OTA for unity feedback?

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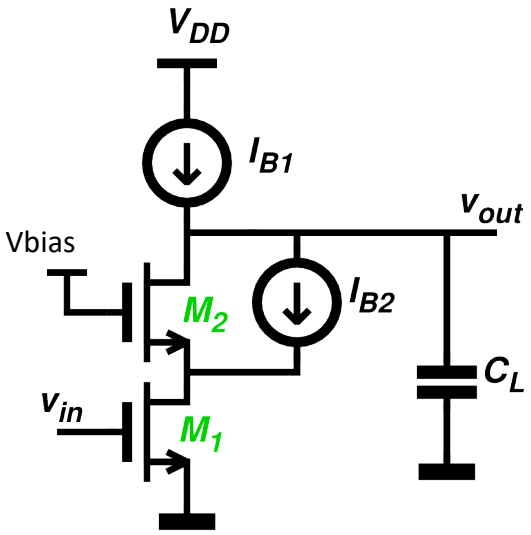
Q2:

For the circuit below: derive the expression for gain, bandwidth, GBW, SR and non-dominant pole.

Also calculate these values for:

VDD=3.3V, IB1=50uA, IB2=20uA, CL=1pF,

W1=3um, L1=1um, W2=3um, L2=1um



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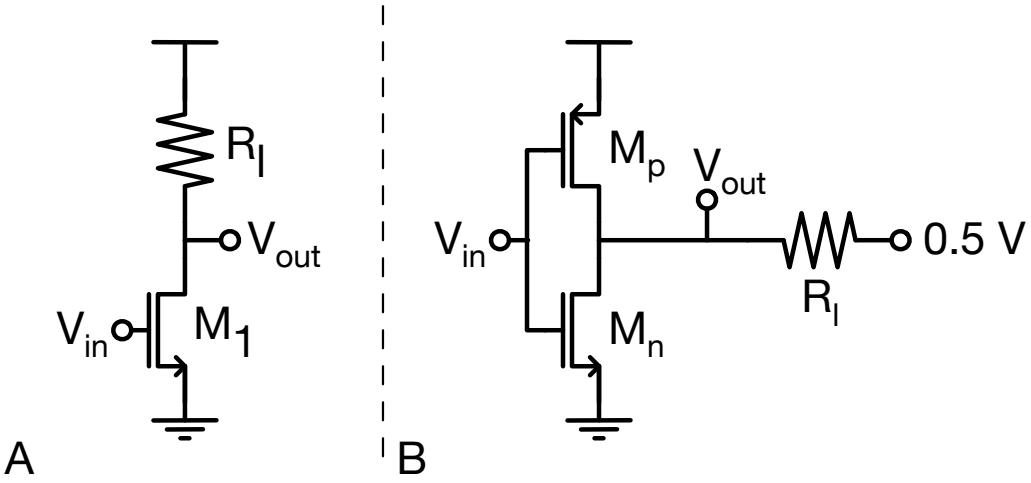
Q3

1. Amplifier A has a DC input and output voltage of 0.5 V. Derive its IM_2 for a sinusoidal input signal of 40 mV_{ptp} assuming a linear load resistor R_l.
2. Derive IM_2 of amplifier for the same conditions and the same input signal.
3. In reality, the Early voltage (V_E) is not infinity. Qualitatively discuss the effect of a realistic Early voltage on IM_2.



$$I_{DS,n} = K_n' \frac{W}{L}(V_{GS} - V_T)^2 \left(1 + \frac{V_{DS}}{V_E L}\right)$$

$$I_{SD,p} = K_p' \frac{W}{L}(V_{SG} - V_T)^2 \left(1 + \frac{V_{SD}}{V_E L}\right)$$

V_{DD}	1 V
T	300 K
L_{min}	65 nm
K_n'	440 µA/V^2
K_p'	140 µA/V^2
V_T	0.3 V
C_{ox}	12 fF/µm^2
V_E	∞ V/µm