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EXAM DIAC 20.01.2022

Q1:

Design a symmetrical OTA with **casocodes at the output**, PMOS transistors at the input and a single ended output. The load of the OTA is a capacitor of 1pF. Ensure that the rising and falling Slew-rate are at least 40V/us and the low frequency gain should be at least 60dB.

- Use a B-factor of 2
- What is the GBW that you obtain with the above specifications?
- Also calculate the non-dominant pole and pole-zero doublet
- Draw the bode-plot of your designed OTA.
- What is the phase margin of your OTA for unity feedback?

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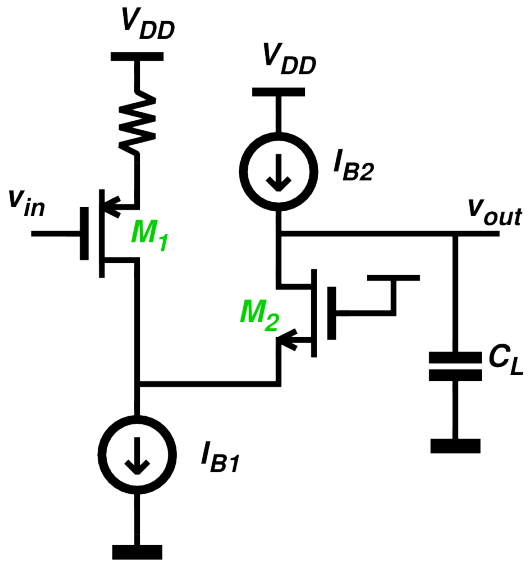
Q2:

For the circuit below: derive the expression for gain, bandwidth, GBW, SR and non-dominant pole.

Also calculate these values for: VDD=3.3V, IB1=50uA, IB2=10uA, CL=1pF,

W1=3um, L1=1um, W2=3um, L2=1um, the resistor at the source of M1 has a value of 10kΩ



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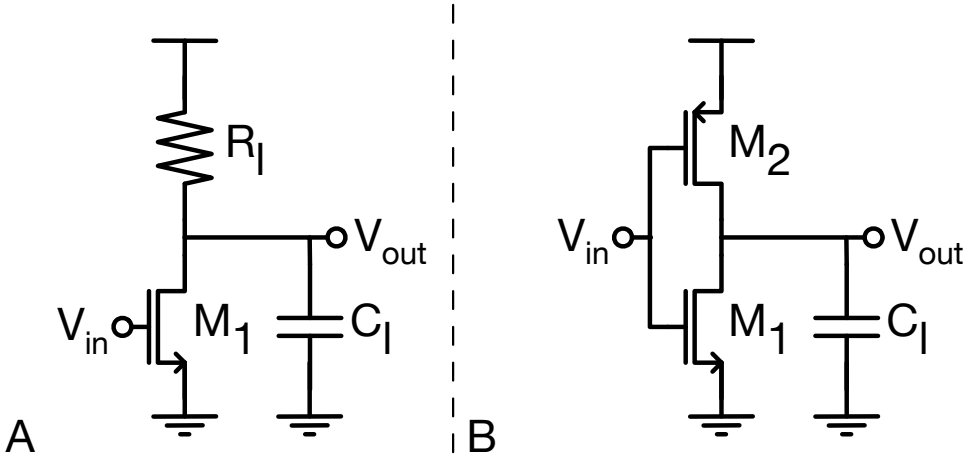
Q3

1. Amplifier A must have a DC input and output voltage of 0.5 V and a maximum input-referred thermal noise voltage of 5 nV/√Hz. Determine its minimum current consumption.
2. Determine the minimum current consumption of amplifier B for the same specifications as amplifier A. Explain the difference between both current consumptions.
3. Determine the transistor sizes in amplifier B for a noise corner frequency at 1 MHz.



$$I_{DS,n} = K_n' \frac{W}{L}(V_{GS} - V_T)^2 \left(1 + \frac{V_{DS}}{V_E L}\right)$$

$$I_{SD,p} = K_p' \frac{W}{L}(V_{SG} - V_T)^2 \left(1 + \frac{V_{SD}}{V_E L}\right)$$

V_{DD}	1 V
T	300 K
L_{min}	65 nm
K_n'	440 µA/V^2
K_p'	140 µA/V^2
V_T	0.3 V
C_{ox}	12 fF/µm^2
V_E	5 V/µm
$KF_{F,n}$	4 x 10^{-39} C^2/µm^2
$KF_{F,p}$	10^{-39} C^2/µm^2