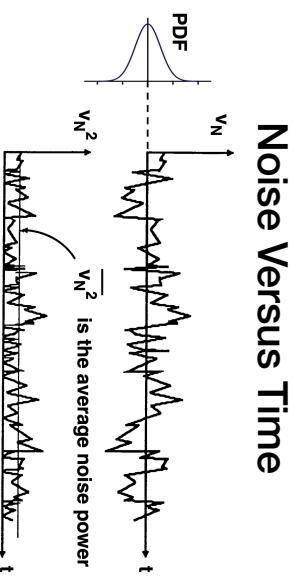


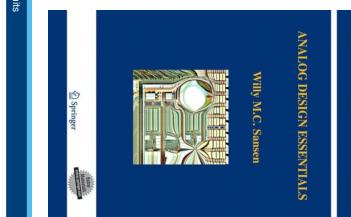
Noise in Elementary Transistor Circuits

prof. dr. ir. Filip Tavernier



Outline

- Definitions of noise
- Noise of an amplifier
- Noise of a follower
- Noise of a cascode
- Noise of a current mirror
- Noise of a differential pair
- Capacitive noise matching

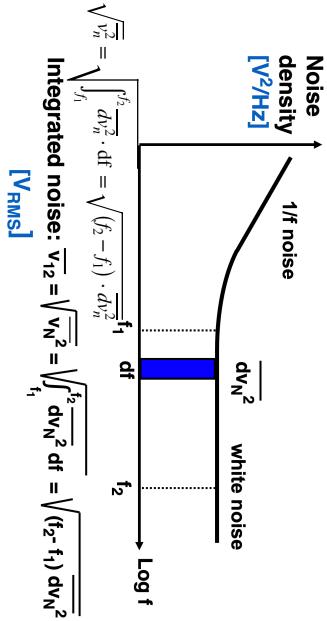


2

Ref: Van der Ziel (Prentice Hall 1954, Wiley 1986), Ott (Wiley 1988)
Noise in elementary transistor circuits

4

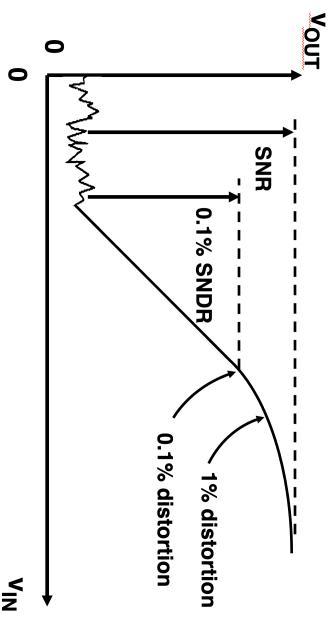
Noise Versus Frequency



Noise in elementary transistor circuits

5

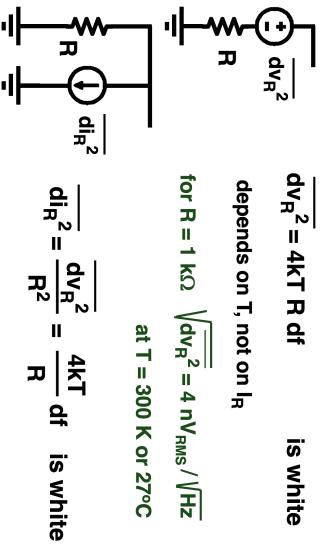
SNR and SNDR



Noise in elementary transistor circuits

2

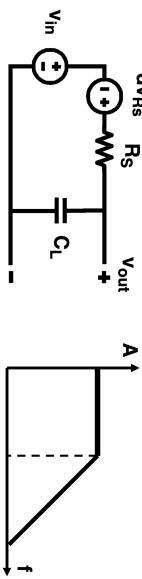
Resistor Thermal Noise



Noise in elementary transistor circuits

5

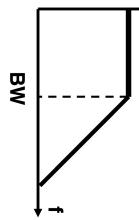
Integrated Noise of a Resistor



$$\overline{dv_{Rs}^2} = 4kT R_S df$$

$$\overline{v_{Rs}^2} = \int_0^\infty \frac{dv_{Rs}^2}{1 + (f/BW)^2}$$

$$BW = \frac{1}{2\pi R_S C_L}$$



Noise in elementary resistor circuits

$$K F_{Rsi} \approx 2 \cdot 10^{-21} \text{ Scm}^2$$

$$V_R + \frac{dv_{Ri}^2}{R} = V_R^2 \frac{K F_{Ri}}{A_R} \frac{df}{f}$$

$$K F_{Rpoly} \approx 10 K F_{Rsi}$$

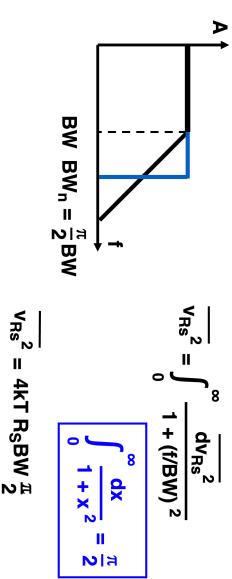
for $R = 1 \text{ k}\Omega$ with $20 \square$'s of $50 \Omega/\square$ and $1 \mu\text{m}$ wide and $V_R = 0.1 \text{ V}$

$$\sqrt{\overline{dv_{Ri}^2}} = 16 \text{ nV}_{\text{RMS}} / \sqrt{\text{Hz}} \text{ at } 1 \text{ Hz}$$

Ref. Vandamme, ESSDERC '04

10

Integrated Noise and Noise Bandwidth



$$\overline{v_{Rs}^2} = \int_0^\infty \frac{dv_{Rs}^2}{1 + (f/BW)^2}$$

$$BW = \frac{\pi}{2} BW_n$$

$$\overline{v_{Rs}^2} = 4kT R_S BW \frac{\pi}{2}$$

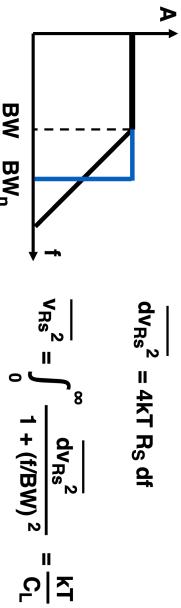
$$\overline{v_{Rs}^2} = \frac{kT}{C_L}$$

$$C_L = 1 \text{ pF} \quad v_{Rs} = 65 \text{ }\mu\text{V}_{\text{RMS}}$$

Noise in elementary resistor circuits

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Integrated Noise Versus Noise Density



$$\overline{dv_{Rs}^2} = 4kT R_S df$$

$$\overline{v_{Rs}^2} = \int_0^\infty \frac{dv_{Rs}^2}{1 + (f/BW)^2} = \frac{kT}{C_L}$$

Noise density [V^2/Hz] $\sim R_S$ (or $1/g_m$)

Integrated noise [V_{RMS}] $\sim 1/C_L$

Resistor 1/f Noise

$$K F_{Rsi} \approx 2 \cdot 10^{-21} \text{ Scm}^2$$

$$V_R + \frac{dv_{Ri}^2}{R} = V_R^2 \frac{K F_{Ri}}{A_R} \frac{df}{f}$$

$$K F_{Rpoly} \approx 10 K F_{Rsi}$$

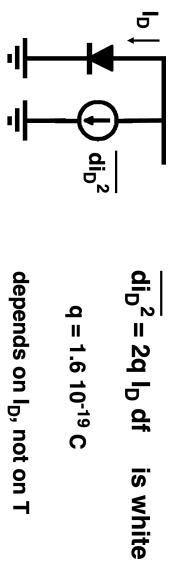
for $R = 1 \text{ k}\Omega$ with $20 \square$'s of $50 \Omega/\square$ and $1 \mu\text{m}$ wide and $V_R = 0.1 \text{ V}$

$$\sqrt{\overline{dv_{Ri}^2}} = 16 \text{ nV}_{\text{RMS}} / \sqrt{\text{Hz}} \text{ at } 1 \text{ Hz}$$

Ref. Vandamme, ESSDERC '04

10

Diode Shot Noise



$$\overline{di_D^2} = 2q I_D df \quad \text{is white}$$

$$q = 1.6 \cdot 10^{-19} \text{ C}$$

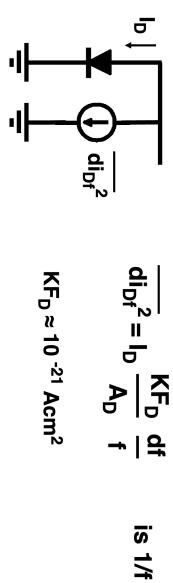
depends on I_D , not on T

$$\text{for } I_D = 50 \mu\text{A} \quad \sqrt{\overline{di_D^2}} = 4 \text{ pA}_{\text{RMS}} / \sqrt{\text{Hz}}$$

Noise in elementary transistor circuits

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Diode 1/f Noise



$$\overline{di_D^2} = I_D \frac{K F_D}{A_D} \frac{df}{f}$$

$$K F_D \approx 10^{-21} \text{ A cm}^2$$

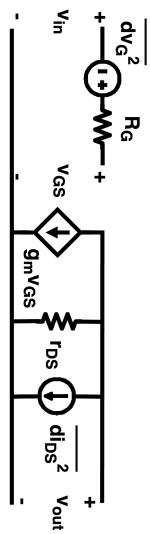
For a diode of $A_D = 5 \times 2 \mu\text{m} = 10 \mu\text{m}^2$ and $I_D = 0.1 \text{ mA}$

$$\sqrt{\overline{di_D^2}} = 1 \text{ nA}_{\text{RMS}} / \sqrt{\text{Hz}} \text{ at } 1 \text{ Hz}$$

Noise in elementary transistor circuits

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MOST Thermal Noise



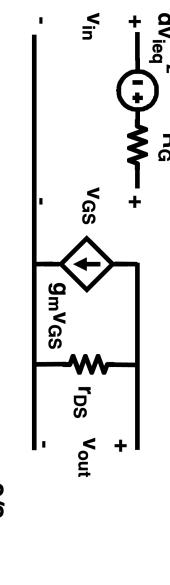
$$\overline{dV_G^2} = 4kT R_G df$$

$$\overline{dI_{DS}^2} = \frac{4kT}{R_{CH}} df = 4kT \frac{2}{3} g_m df$$

Ref. Van der Ziel, Prentice Hall 1954, Wiley 1986.

Noise in elementary transistor circuits. 13

MOST Equivalent Input Noise

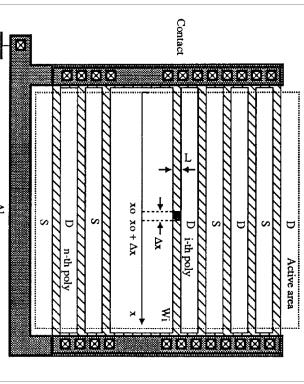


$$\overline{dV_{IEQ}^2} = 4kT (R_{eff}) df \quad R_{eff} = \frac{2/3}{g_m} + R_G$$

High Freq.: $\overline{dV_{IEQ}^2} = (C_{GS} \omega)^2 \overline{dV_{IEQ}^2}$ is correlated

Noise in elementary transistor circuits. 14

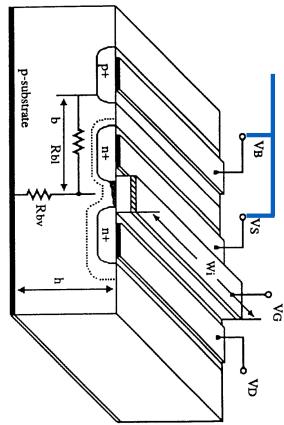
MOST Gate Resistance



Noise in elementary transistor circuits.

15

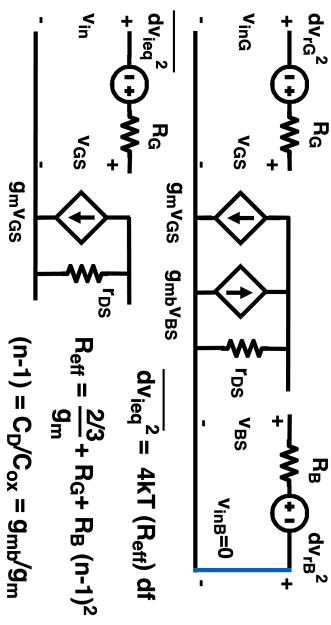
MOST Substrate Resistance



Ref. Chang, Kluwer 1991

Noise in elementary transistor circuits. 16

MOST Total Thermal Noise

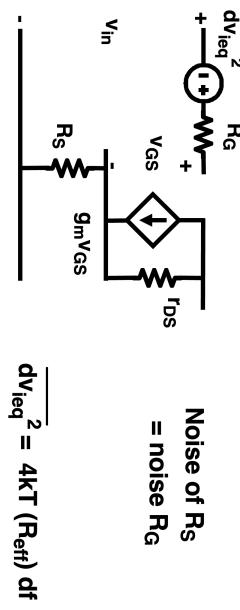


$$\overline{dV_{IEQ}^2} = 4kT (R_{eff}) df \quad R_{eff} = \frac{2/3}{g_m} + R_G + R_B (n-1)^2$$

Noise in elementary transistor circuits.

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MOST Source Resistance

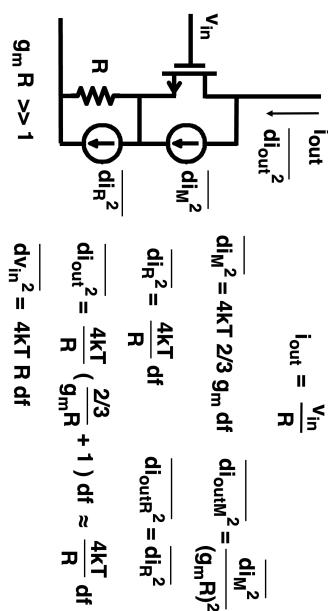


$$R_{eff} = \frac{2/3}{g_m} + R_G + R_S + R_B (n-1)^2$$

Noise in elementary transistor circuits.

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Noise by Source Resistance



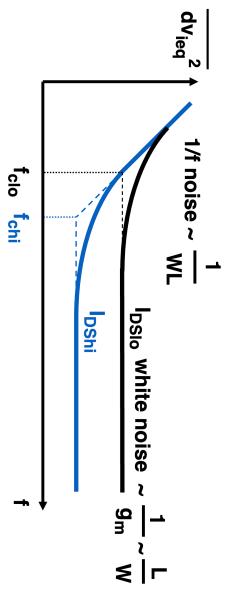
$$g_m R \gg 1$$

$$\overline{dV_{in}^2} = 4kT R df$$

Noise in elementary resistor circuits.

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MOST Noise Versus Frequency

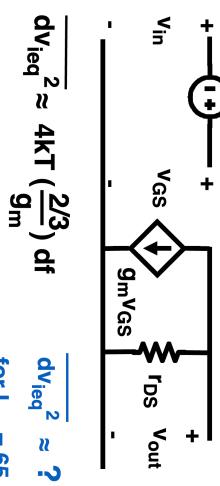


Corner frequency $\sim g_m$

Noise in elementary transistor circuits.

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Example: MOST Equivalent Input Noise



$$\overline{dv_{eq}^2} \approx 4kT (\frac{2}{3}) df$$

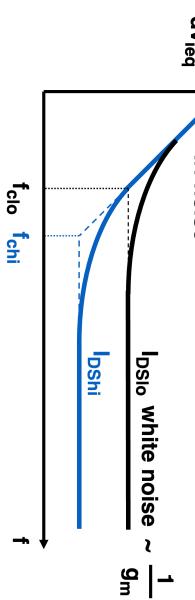
$$\overline{dv_{eq}^2} \approx ?$$

for $i_{ds} = 65 \mu A$

Noise in elementary transistor circuits.

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Example: MOST Noise Corner Frequency



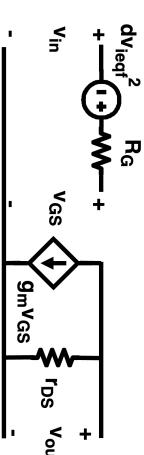
Ex. : f_c ? For $i_{ds} = 65 \mu A$;

$K_n' = 60 \mu A/V^2$ and $L = 1 \mu m$ (0.35 μm process)

Noise in elementary transistor circuits.

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MOST 1/f Noise



$$\overline{dv_{eqf}^2} = \frac{K F_F}{WL C_{ox}^2} \frac{df}{f}$$

pMOSFET $K F_F \approx 10^{-32} C^2/cm^2$

nMOST $K F_F \approx 4 \cdot 10^{-31} C^2/cm^2$

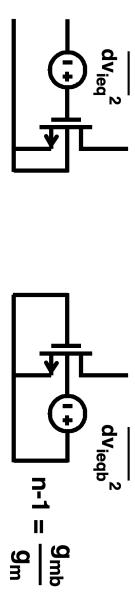
pJFET $K F_F \approx 10^{-33} C^2/cm^2$

$W & L$ in μm ; C_{ox} in F/cm^2

Noise in elementary transistor circuits.

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MOST Equivalent Noise at Bulk



$$\overline{dv_{eq}^2} = 4kT (\frac{2}{3}) df$$

n -MOST $K F_F \approx 4 \cdot 10^{-31} C^2/cm^2$

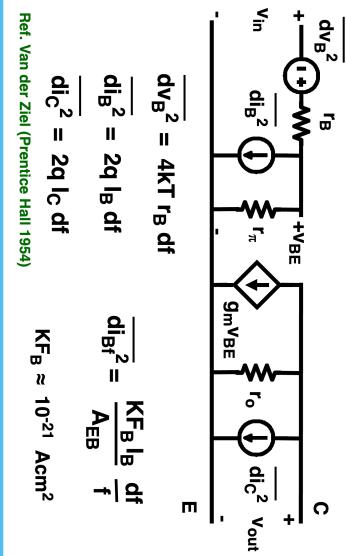
p -JFET $K F_F \approx 10^{-33} C^2/cm^2$

$W & L$ in μm ; C_{ox} in F/cm^2

Noise in elementary transistor circuits.

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BJT Noise



$$\overline{dV_B^2} = 4kT r_B df$$

$$\overline{dI_B^2} = 2q I_B df$$

$$\overline{dI_{Br}^2} = \frac{K F_B I_B}{A_{EB}} \frac{df}{f}$$

$$\overline{dI_C^2} = 2\alpha I_C df$$

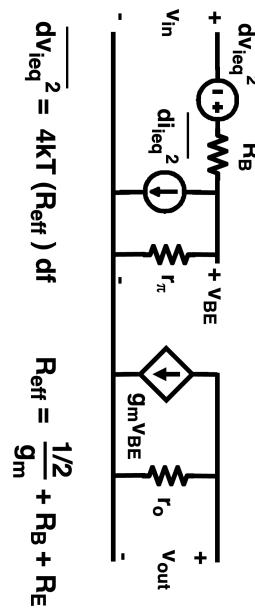
$$K F_B \approx 10^{-21} \text{ Acm}^2$$

Ref. Van der Ziel (Prentice Hall 1954)

Noise in elementary transistor circuits

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BJT Equivalent Input Noise



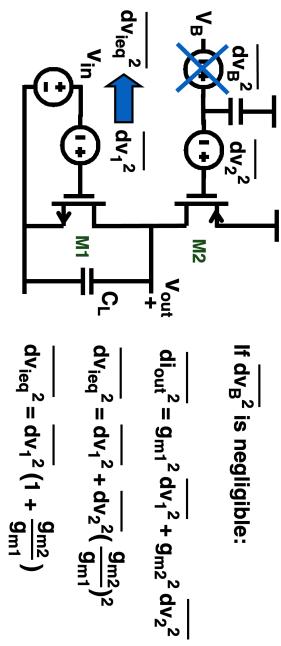
Noise in elementary transistor circuits

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Outline

- Definitions of noise
- Noise of an amplifier
- Noise of a follower
- Noise of a cascode
- Noise of a current mirror
- Noise of a differential pair
- Capacitive noise matching

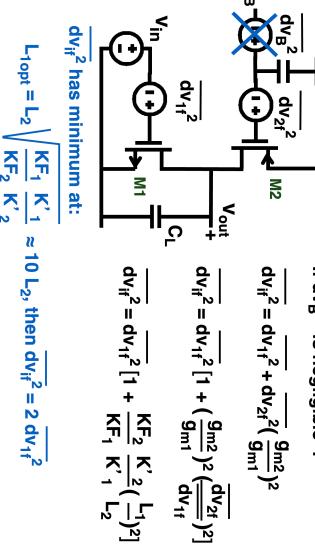
Amplifier Thermal Noise



Noise in elementary transistor circuits

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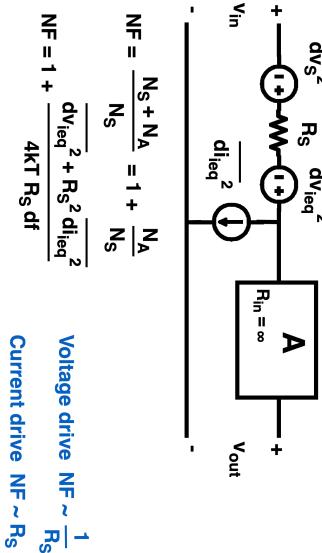
Amplifier 1/f Noise



Noise in elementary transistor circuits

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Amplifier Noise Figure



Noise in elementary transistor circuits

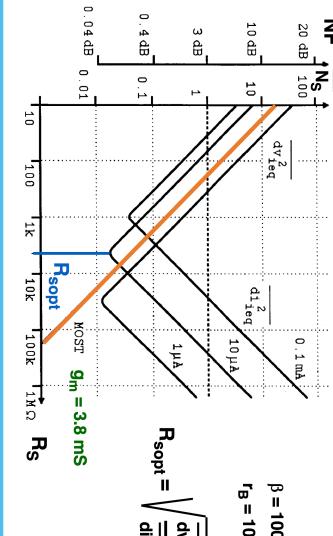
30

Noise in elementary transistor circuits

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Resistive Noise Matching

Outline



Noise in elementary transistor circuits

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Outline

- Definitions of noise
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Noise in elementary transistor circuits

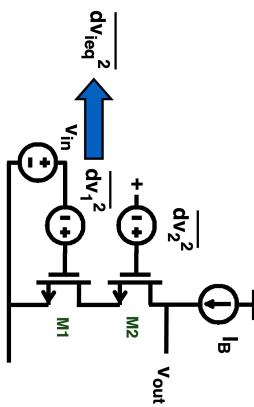
32

- Definitions of noise
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Noise in elementary transistor circuits

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Cascode Noise



$$\overline{dV_{i\text{eq}}^2} = \overline{dV_1^2} + \overline{dV_2^2} \cdot \frac{1}{(g_m r_{o1})^2} \approx \overline{dV_1^2}$$

Noise in elementary transistor circuits

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Cascode Input-Referred Noise



Noise in elementary transistor circuits

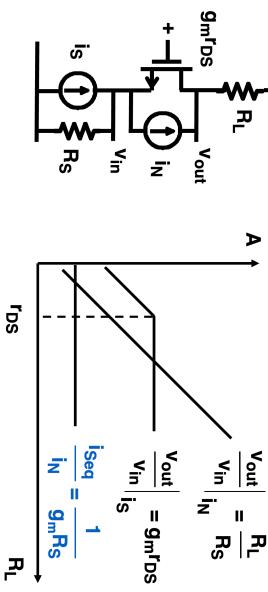
33

- Definitions of noise
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Noise in elementary transistor circuits

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Cascode Noise Transfer Functions

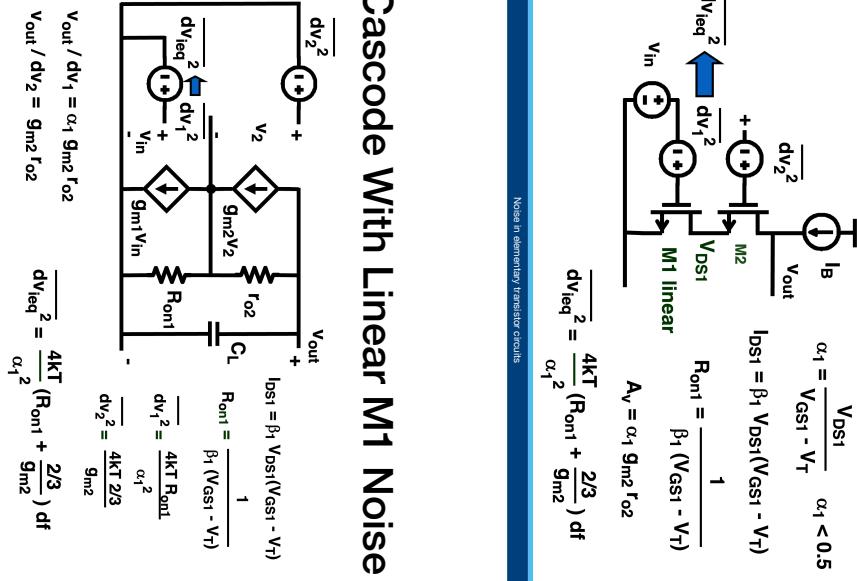


Cascode noise i_N is only negligible if R_S is large!!!

Noise in elementary transistor circuits

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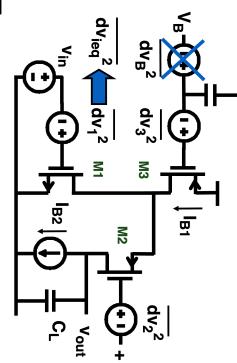
Cascode With Linear M1 Noise



Noise in elementary transistor circuits

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Folded Cascode Noise



Noise in elementary transistor circuits

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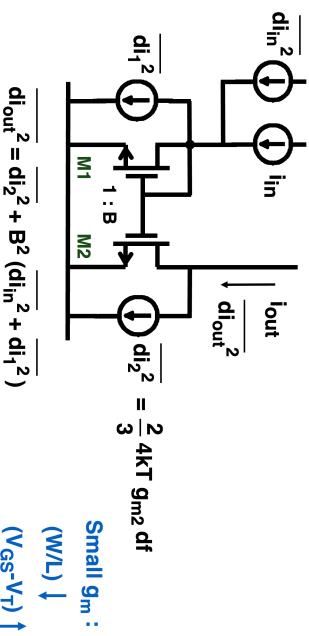
Outline

- Definitions of noise
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- Capacitive noise matching

Noise in elementary transistor circuits

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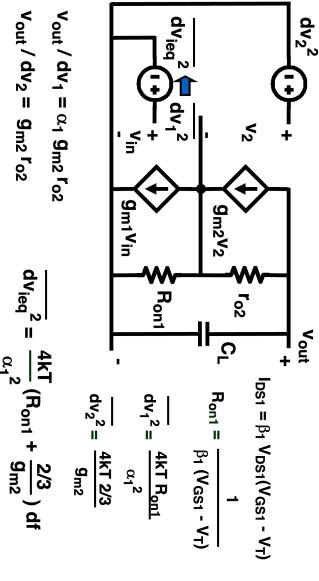
Current Mirror Noise



Noise in elementary transistor circuits

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Cascode With Linear M1 Noise



Noise in elementary transistor circuits

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Noise in elementary transistor circuits

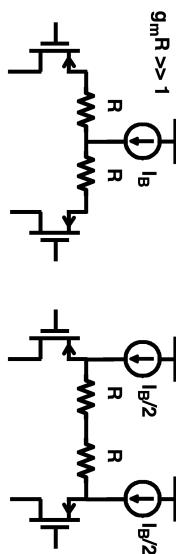
39

Differential Amplifier Noise

Outline

-

Source-Degenerated Differential Pair Noise



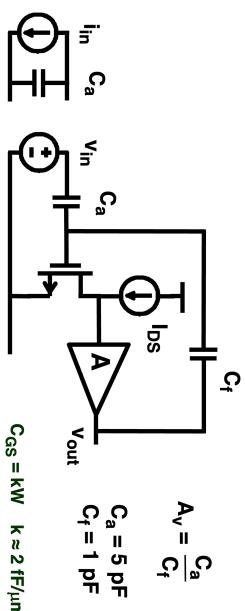
$\frac{dI_{out}^2}{R} = 2 \frac{\pi \lambda^2}{df}$	$\frac{dI_{out}^2}{R} = 2 \left(\frac{\pi \lambda^2}{df} + dI_B^2 \right)$
$dI_{in}^2 = 2 (4kT R df)$	$\frac{dI_B^2}{R} = 4kT R df / 3 g_{mB}$

Noise in elementary transistor circuits

The diagram shows a differential pair circuit. The top stage consists of two NMOS transistors, M1 and M2, with their drains connected to a common node. The source of M1 is connected to the drain of M3, and the source of M2 is connected to the drain of M4. The gate of M3 is connected to the negative input terminal V_{SS} , and the gate of M4 is connected to the positive input terminal V_{DD} . The drain of M3 is connected to the drain of M4. The drain of M1 is connected to the drain of M2. The drain of M1 is connected to the negative output terminal V_{SS} through a resistor R_L . The drain of M2 is connected to the positive output terminal V_{DD} through a resistor R_L . The gate of M3 is controlled by a current source $\frac{dI_1}{2}$ and a voltage-controlled current source $\frac{dI_1^2}{2}$. The gate of M4 is controlled by a current source $\frac{dI_2}{2}$ and a voltage-controlled current source $\frac{dI_2^2}{2}$. The drain of M1 is connected to the drain of M2 through a resistor R_L .

5

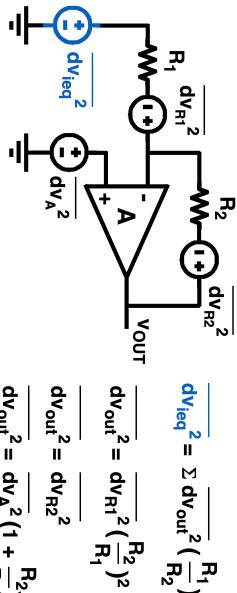
Amplifier With Capacitive Source



Noise in elementary transistor circuit

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Opamp With Feedback Noise

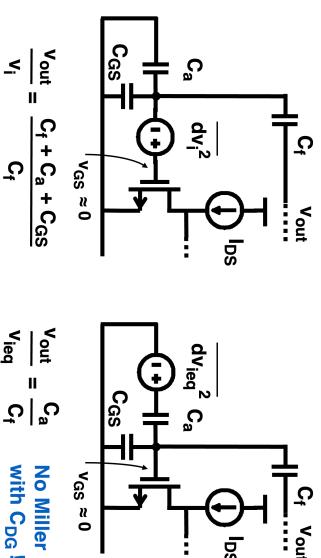


$$\overline{dv_{\text{req}}^2} = \overline{dv_{R1}^2} + \overline{dv_{R2}^2} \left(\frac{R_1}{R_2} \right)^2 + \overline{dv_A^2} \left(1 + \frac{R_1}{R_2} \right)^2 \approx \overline{dv_{R1}^2} + \overline{dv_A^2}$$

Noise in elementary transistor circuits

0

Calculating Equivalent Input Noise



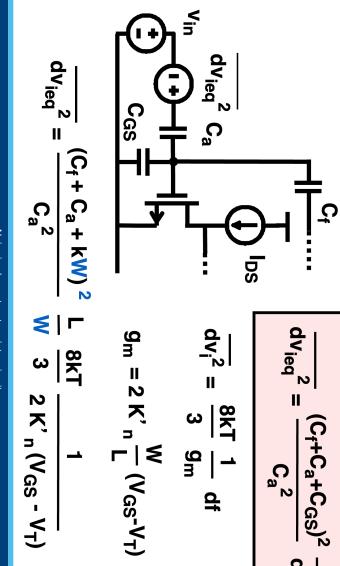
Noise in elementary transistor circuit

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Noise in elementary transistor circuits

1

Calculating Equivalent Input Noise

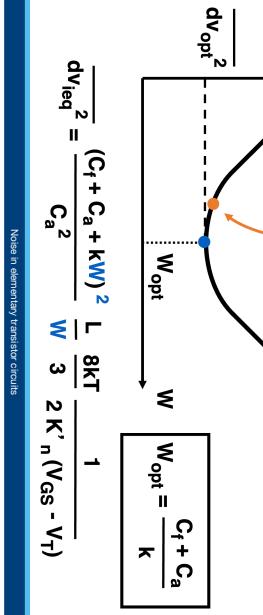


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Noise in elementary transistor circuits

Capacitive Noise Matching

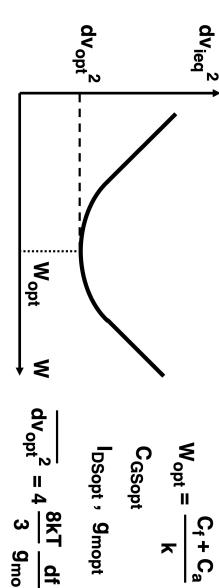
Operating point
Noise matching
where
 $C_{GS} = C_f + C_a$



Noise in elementary transistor circuits

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SNR With Capacitive Noise Matching



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Noise in elementary transistor circuits

Outline

- Definitions of noise
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Noise in elementary transistor circuits

KU LEUVEN

Distortion in elementary transistor circuits

prof. dr. ir. Filip Tavernier

Outline

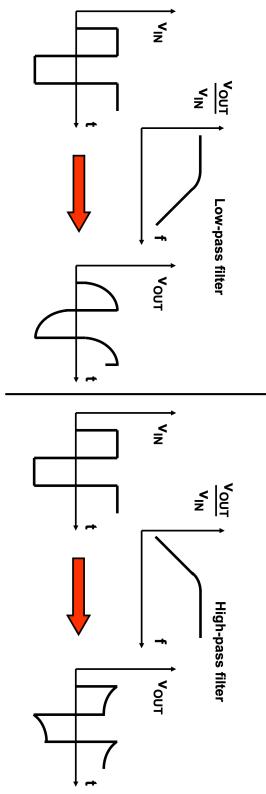
- Definitions and metrics of distortion

- Distortion in components
- Distortion reduction
- Distortion in OPAMPS
- Summary



What it is NOT

Distortion is NOT the result of linear filtering!



No new frequency components

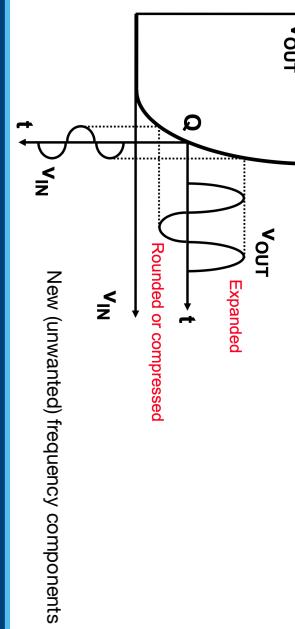
Distortion in elementary transistor circuits

3

What it is

Distortion is the result of amplitude dependency

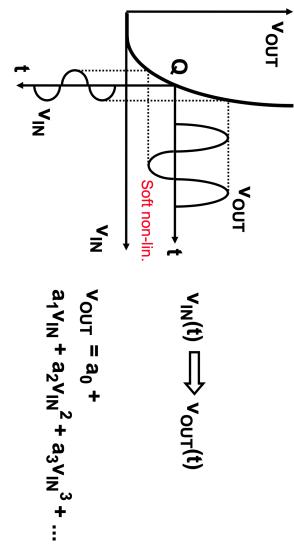
Quiescent point



Distortion in elementary transistor circuits

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Modeling distortion with power series



Distortion in elementary transistor circuits

6

Finding the distortion coefficients

$$y = a_0 + a_1 u + a_2 u^2 + a_3 u^3 + \dots$$

$$a_0 = y \Big|_{u=0} \quad a_1 = \frac{dy}{du} \Big|_{u=0}$$

$$a_2 = \frac{1}{2} \frac{d^2y}{du^2} \Big|_{u=0} \quad a_3 = \frac{1}{6} \frac{d^3y}{du^3} \Big|_{u=0}$$

Distortion in elementary transistor circuits

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Harmonic distortion (HD)

$$y = a_0 + a_1 u + a_2 u^2 + a_3 u^3 + \dots$$

$$\text{With } u = U \cos \omega t$$

$$\cos^3 x = 1/4 (3 \cos x + \cos 3x)$$

$$y = a_0 + a_1 u + a_2 u^2 + a_3 u^3 + \dots = a_0 +$$

$$(a_1 + \frac{3}{4} a_3 U^2) U \cos \omega t + \frac{a_2}{2} U^2 \cos 2\omega t + \frac{a_3}{4} U^3 \cos 3\omega t$$

$$HD_2 = \frac{1}{2} \frac{a_2}{a_1} U$$

$$HD_3 = \frac{1}{4} \frac{a_3}{a_1} U^2$$

Distortion in elementary transistor circuits

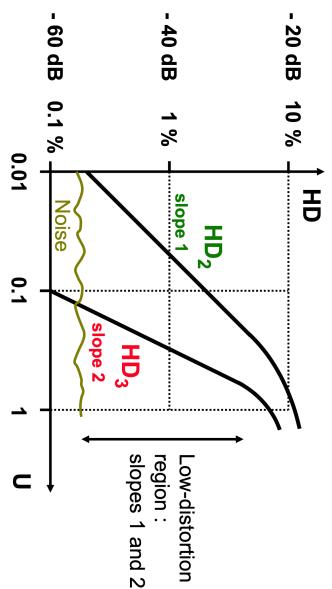
5

HD versus input amplitude

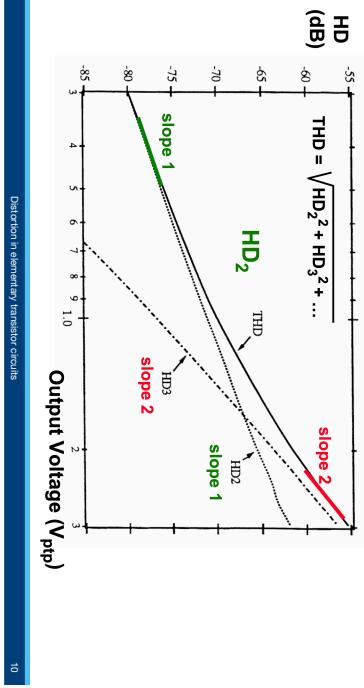
$$y = a_0 + a_1 u + a_2 u^2 + a_3 u^3 + \dots$$

with $u = U (\cos \omega_1 t + \cos \omega_2 t)$

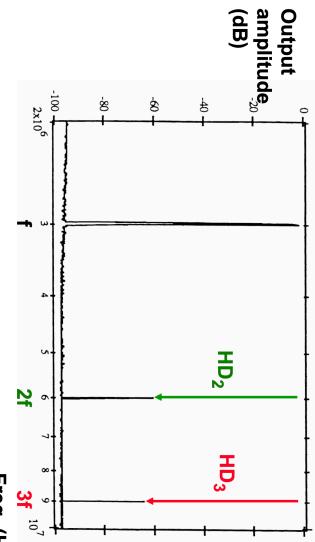
卷之三



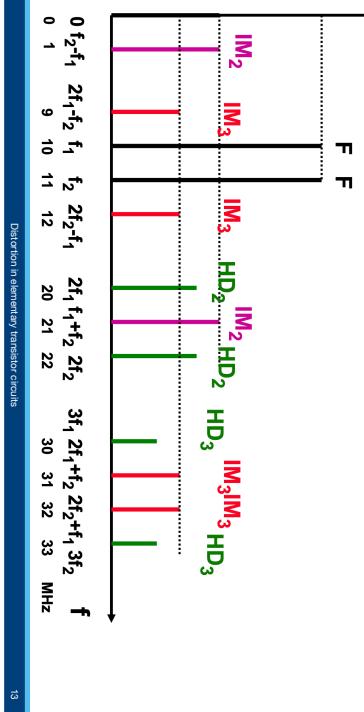
Example: HD of a resistor



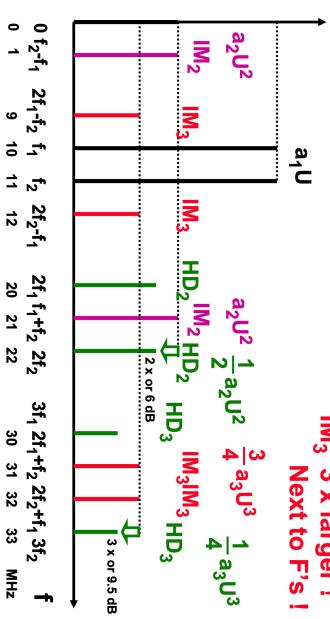
HD in the output spectrum



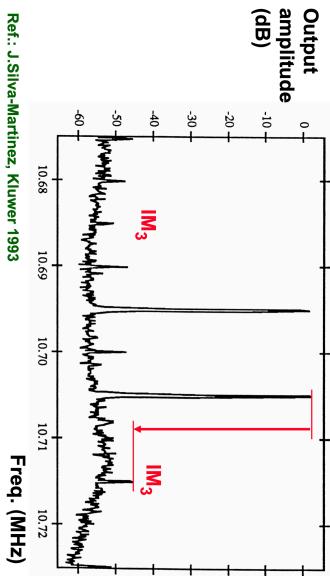
HB and IM in the spectrum



The relevance of IM₃



Example: amplifier output spectrum

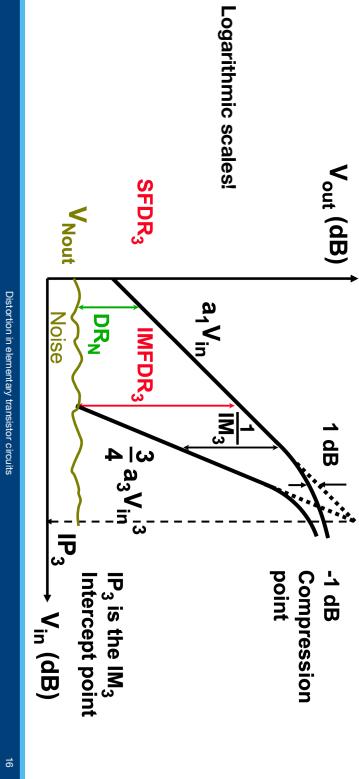


Ref.: J.Silva-Martinez, Kluwer 1993

Distortion in elementary transistor circuits

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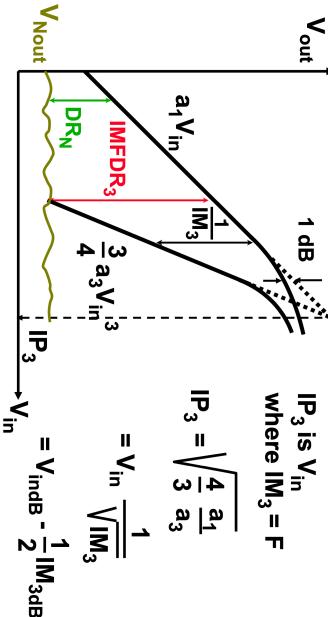
IM_3 versus input amplitude



Distortion in elementary transistor circuits

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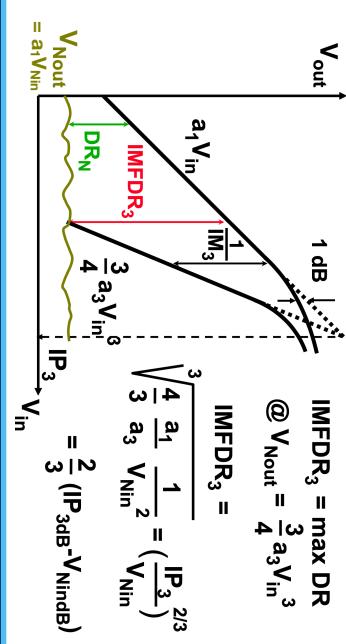
Relation between IP_3 and IM_3



Distortion in elementary transistor circuits

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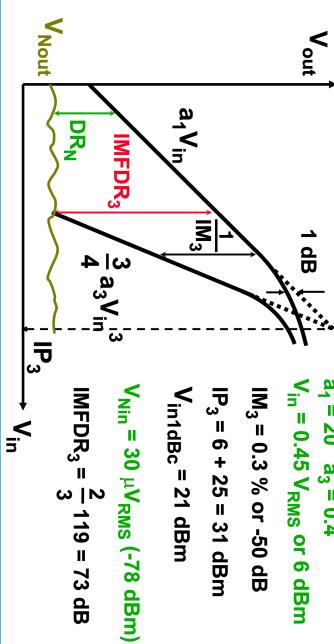
Relationship between $V_{\text{in}1\text{dBc}}$ and IP_3



Distortion in elementary transistor circuits

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Exercise



Distortion in elementary transistor circuits

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Outline

- Definitions and metrics of distortion
- Distortion in components**

- MOST**

- BJT
- Passive components

- Distortion reduction

- Distortion in OPAMPS

- Summary

Distortion of MOST current

$$I_{DS} = K(V_{GS} - V_T)^2 \quad K = K' \frac{W}{L}$$

$$I_{DS} + i_{ds} = K(V_{GS} + v_{gs} - V_T)^2$$

$$i_{ds} = K(V_{GS} + v_{gs} - V_T)^2 - K(V_{GS} - V_T)^2$$

$$i_{ds} = 2K(V_{GS} - V_T)v_{gs} + KV_{GS}^2 \quad \text{or} \quad i_{ds} = g_1v_{gs} + g_2v_{gs}^2 + g_3v_{gs}^3 + \dots$$

$$IM_2 = \frac{g_2}{g_1} v_{gs} = \frac{V_{GS}}{2(V_{GS} - V_T)} \quad \& \quad IM_3 = 0$$

$$g_1 = 2K(V_{GS} - V_T) \quad g_2 = K \quad g_3 = 0$$

Definitions

$$i_{ds} = K(v_{gs} - V_T)^2 \quad K = K' \frac{W}{L}$$

$$I_{DS} + i_{ds} = K(V_{GS} + v_{gs} - V_T)^2$$

$$i_{ds} = K(V_{GS} + v_{gs} - V_T)^2 - K(V_{GS} - V_T)^2$$

$$i_{ds} = 2K(V_{GS} - V_T)v_{gs} + KV_{GS}^2 \quad \text{or} \quad i_{ds} = g_1v_{gs} + g_2v_{gs}^2 + g_3v_{gs}^3 + \dots$$

$$i_{ds} : \text{DC component}$$

$$i_{ds} : \text{the DC + ac component}$$

$$i_{ds} : \text{the ac component}$$

$$i_{ds} : \text{the amplitude of the ac component}$$

Normalization of signals

$$i_{ds} = 2K(V_{GS} - V_T)v_{gs} + KV_{GS}^2 \quad i_{ds} = K(v_{gs} - V_T)^2$$

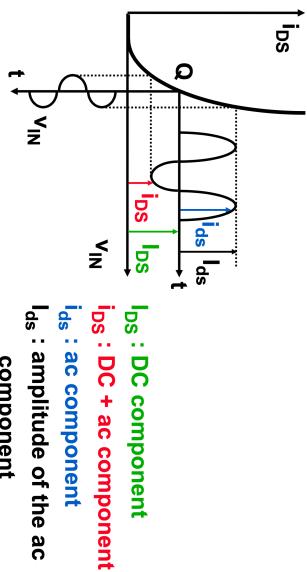
$$\text{or } y = a_1u + a_2u^2 + a_3u^3 + \dots$$

$$y = \frac{i_{ds}}{I_{DS}} = \frac{2v_{gs}}{V_{GS} - V_T} + \frac{1}{4} \left(\frac{2v_{gs}}{V_{GS} - V_T} \right)^2$$

$$y = \frac{i_{ds}}{I_{DS}} = u + \frac{1}{4}u^2 \quad U = \frac{V_{GS}}{(V_{GS} - V_T)/2}$$

y is the relative current swing !

Definitions - graphical



Example

The peak value of V_{gs} is $V_{gsp} = 100 \text{ mV}$

(then $V_{gsRMS} = 100/\sqrt{2} = 71 \text{ mVRMS}$)

if $V_{GS} - V_T = 0.5 \text{ V}$ then $V_{gsp}/[2(V_{GS} - V_T)] = 0.1$

gives $IM_2 = 10\%$ ($HD_2 = 5\%$) & $IM_3 = 0$

The relative current swing $U = 0.1/0.25 = 0.4$!

More MOST distortion components

In general

$$i_{ds} = g_m v_{gs} + K_2 g_m v_{gs}^2 + K_3 g_m v_{gs}^3 + \dots$$

$$g_o v_{ds} + K_2 g_o v_{ds}^2 + K_3 g_o v_{ds}^3 + \dots$$

$$g_{mb} v_{bs} + K_2 g_{mb} v_{bs}^2 + K_3 g_{mb} v_{bs}^3 + \dots$$

$$K_2 g_m \& g_{mb} v_{gs} v_{bs} + K_3 g_m \& g_{mb} v_{gs}^2 v_{bs} + \dots$$

$$+ K_3 g_m \& g_{mb} v_{gs} v_{bs}^2 + \dots$$

+ ...

v_{gs} v_{ds} v_{bs}

Distortion in elementary transistor circuits

$i_{ds} = g_m v_{gs} + K_2 g_m v_{gs}^2 + K_3 g_m v_{gs}^3 + \dots$

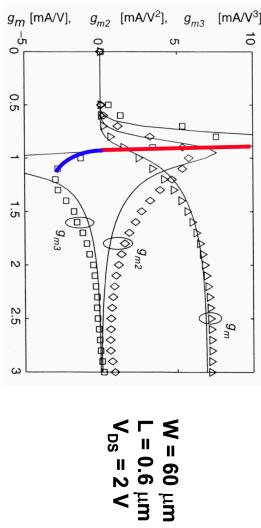
non-linear transconductance

non-linear output resistance

non-linear body transconductance

MOST biasing for no HD₃

Very steep $g_{m3} \rightarrow$ very sensitive!



Ref. Fager JSSC Jan. 2004, 24-33

$i_{ds} = g_m v_{gs} + K_2 g_m v_{gs}^2 + K_3 g_m v_{gs}^3 + \dots$

+ ...

v_{gs} v_{ds} v_{bs}

Distortion in elementary transistor circuits

$i_{ds} = g_m v_{gs} + K_2 g_m v_{gs}^2 + K_3 g_m v_{gs}^3 + \dots$

non-linear transconductance

non-linear output resistance

non-linear body transconductance

Distortion of a MOST diode

$$i_{ds} = K (v_{ds} - V_T)^2$$

$$y = \frac{i_{ds}}{i_{ds}} = \frac{2 v_{ds}}{V_{ds} - V_T} + \frac{1}{4} \left(\frac{2 v_{ds}}{V_{ds} - V_T} \right)^2$$

$$y = \frac{i_{ds}}{i_{ds}} = u + \frac{1}{4} u^2$$

$$U = \frac{V_{ds}}{(V_{ds} - V_T)/2}$$

Same as for a MOST transistor amplifier!

Distortion in elementary transistor circuits

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MOST biasing for no HD₃

$$g_m = \frac{w_i}{V_T} s_i v_s - g_{m\text{sat}} = WC_{ox} V_{sat}$$

$$g_m' = \frac{w_i}{V_T} s_i v_s$$

$$g_m''' = \frac{w_i}{V_T} s_i v_s$$

$$g_m'' = \frac{w_i}{V_T} s_i v_s$$

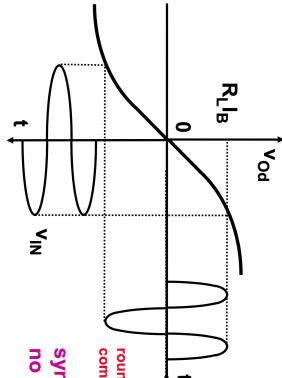
$g_m''' = 0$ at $V_{GS} = V_T$?

$$Note that: g_m = \frac{I_B}{V_{GS} - V_T} = K' \frac{W}{L} (V_{GS} - V_T)$$

Distortion in elementary transistor circuits

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MOST differential pair



even order distortion:
same amplitude and sign
→ removed in differential signal

uneven order distortion:
uneven amplitude but different sign
→ maintained in differential signal

Distortion in elementary transistor circuits

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Distortion in a MOST differential pair

$$y = \frac{i_{od}}{I_B} = \frac{v_{id}}{V_{GS} - V_T} \sqrt{1 - \frac{1}{4} \left(\frac{v_{id}}{V_{GS} - V_T} \right)^2}$$

v_{id} is the differential input voltage

i_{od} is the differential output current ($g_m v_{id}$) or twice the circular current $g_m v_{id} / 2$

I_B is the total DC current in the pair

$$Note that: g_m = \frac{I_B}{V_{GS} - V_T} = K' \frac{W}{L} (V_{GS} - V_T)$$

Distortion in elementary transistor circuits

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Distortion in a MOST differential pair

$$y = \frac{i_{od}}{I_B} = \frac{V_{id}}{V_{GS}V_T} \sqrt{1 - \frac{1}{4} \left(\frac{V_{id}}{V_{GS}V_T} \right)^2}$$

$|IM_3|$ result of current limitation
→ compression

$$y = \frac{I_{od}}{I_B} = U \sqrt{1 - \frac{1}{4} U^2} \approx U - \frac{1}{8} U^3$$

$$\sqrt{1-x} \approx 1 - \frac{x}{2}$$

$$IM_2 = 0$$

$$IM_3 = \frac{3}{32} U^2$$

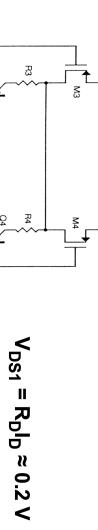
U is the relative current swing

$$IP_3 = 4 \sqrt{\frac{2}{3}} (V_{GS} - V_T) \approx 3.3 (V_{GS} - V_T)$$

Distortion in elementary transistor circuits

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MOST in linear region



$$V_{DS1} = R_D I_D \approx 0.2 \text{ V}$$

$$I_{DS1} = \beta_1 V_{DS1} (V_{GS1} - V_T)$$

$$g_{m1} = \beta_1 V_{DS1} \text{ is constant}$$

Low distortion !

Ref. Alimi,JSSC, Dec.-92, pp.1905-1915

Distortion in elementary transistor circuits

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Distortion of BJT current

$$I_{CE} = I_S \exp\left(\frac{V_{BE}}{kT_e/q}\right)$$

I_{CE} DC component
 I_{CE} DC + ac component

$$I_{CE} + i_{ce} = I_S \exp\left(\frac{V_{BE} + V_{be}}{kT_e/q}\right)$$

i_{ce} ac component
 i_{ce} the ac component

$$1 + y = \exp\left(\frac{V_{be}}{kT_e/q}\right)$$

$$\approx \exp(u) = 1 + u + \frac{u^2}{2} + \frac{u^3}{6} + \dots \quad \text{if } u \ll 1$$

Distortion in elementary transistor circuits

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Distortion of BJT current

$$y \approx u + \frac{u^2}{2} + \frac{u^3}{6} + \dots$$

$$U = \frac{V_{be}}{kT_e/q}$$

is the non-linear equation

y is the relative current swing !

$$a_1 = 1$$

$$a_2 = 1/2$$

$$a_3 = 1/6$$

$$IM_3 = \frac{3}{4} \frac{a_3}{a_1} U^2 = \frac{1}{8} \left(\frac{V_{be}}{kT_e/q} \right)^2$$

Distortion in elementary transistor circuits

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Example

1. Relative current swing is 10 %

$$y_p = 0.1 \text{ gives } IM_2 = 5 \% \text{ (HD}_2 = 2.5\%)$$

$$IM_3 = 0.125 \% \text{ (HD}_3 = 0.04 \%)$$

As a result $V_{be,p} = y_p (kT_e/q) = 2.6 \text{ mV}_p$ (1.8 mV_{RMS})

$$IP_3 = \sqrt[3]{8} (kT_e/\alpha) = 74 \text{ mV}_p \text{ or } 50 \text{ mV}_{RMS} \text{ or } -13 \text{ dBm}$$

2. $V_{be,p} = 100 \text{ mV}$

then $y_p = 0.1/0.026 \approx 4$ (must be $\ll 1$!!)
gives $IM_2 = ??$ Too high distortion !!

• Distortion in components

- MOST
- BJT

- Passive components
- Distortion reduction
- Distortion in OPAMPs
- Summary

Distortion in a BJT diode

$$i_D = I_S \exp\left(\frac{V_D}{kT_e/q}\right) \quad y \approx u + \frac{u^2}{2} + \frac{u^3}{6} + \dots$$

$$y = \frac{i_d}{I_b} = u + \frac{u^2}{2} + \frac{u^3}{6} \quad U = \frac{V_d}{kT_e/q}$$

Same as for a Bipolar transistor amplifier!

Distortion in elementary transistor circuits

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Distortion in a BJT differential pair

$$y = \frac{i_{od}}{I_B} = \tanh \frac{V_{id}}{2kT_e/q} \quad \tanh x = \frac{e^x - e^{-x}}{e^x + e^{-x}}$$

$$\approx x - \frac{1}{3}x^3$$

$$y = \frac{i_{od}}{I_B} \approx U - \frac{1}{3}U^3 \quad U = \frac{V_{id}}{2kT_e/q}$$

$$|M_2 = 0 \quad |M_3 = \frac{1}{4}U^2 \quad |P_3 = 4kT_e/q$$

U is the relative current swing

||M₃ is result of current limitation AND intrinsic third order distortion||

Distortion in elementary transistor circuits

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Outline

- Definitions and metrics of distortion
- **Distortion in components**
 - MOST
 - BJT
 - Passive components
 - Distortion reduction
 - Distortion in OPAMPs
 - Summary

Distortion in resistors and capacitors

$$R = R_0 (1 + a_1 V + a_2 V^2 + \dots) \quad [\approx \text{JFET with large } V_P]$$

For diffused resistors : $a_1 \approx 5 \text{ ppm/V}$
 $a_2 \approx 1 \text{ ppm/V}^2$

$$C = C_0 (1 + a_1 V + a_2 V^2 + \dots)$$

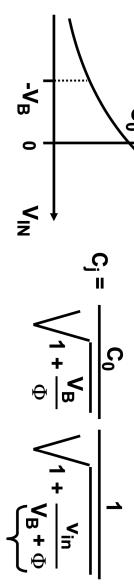
For poly-poly caps : $a_1 \approx 20 \text{ ppm/V}$
 $a_2 \approx 2 \text{ ppm/V}^2$

Distortion in elementary transistor circuits

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Non-linear depletion capacitance

$$C_J = \frac{C_0}{\sqrt{1 - \frac{V_B}{\Phi}}} \quad V_{IN} = V_B + V_{IN}$$



$$C_J = \frac{C_0}{\sqrt{1 + \frac{V_B}{\Phi}}} \sqrt{\frac{1}{1 + \frac{V_{IN}}{\sqrt{V_B + \Phi}}}}$$

$$C_J = C_{0B} (1 + x)^{-1/2} = C_{0B} (1 - 1/2 x + 3/8 x^2 - 5/16 x^3 + ..)$$

Distortion in elementary transistor circuits

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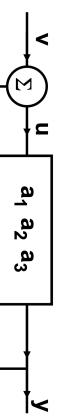
Outline

- Definitions and metrics of distortion
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Distortion in elementary transistor circuits

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Feedback distortion coefficients



$$v = v - Fy$$

$$\begin{aligned} y &= a_1 u + a_2 u^2 + a_3 u^3 \\ y &= d_1 v + d_2 v^2 + d_3 v^3 \end{aligned}$$

elim. u elim. y

Distortion in elementary transistor circuits

$$\begin{aligned} u &= v - Fy \\ y &= \left[\begin{array}{l} \text{coeff } v : d_1 \\ \text{coeff } v^2 : d_2 \\ \text{coeff } v^3 : d_3 \end{array} \right] \end{aligned}$$

elim. v : d_1 coeff v^2 : d_2 coeff v^3 : d_3

For large T: $\frac{a_3 a_1 - 2 a_2^2}{a_1^2} \frac{1}{T} = \frac{a_3}{a_1} \left(1 - \frac{2 a_2^2}{a_1 a_3} \right) \frac{1}{T}$

MOST: $a_3 = 0$: a_2 dominant

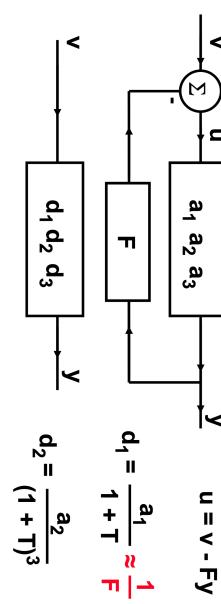
Bipolar: $a_1 = 1$ $a_2 = 1/2$ $a_3 = 1/6$: a_2 dominant

Dif. pair: $a_2 = 0$: a_3 dominant

Distortion in elementary transistor circuits

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Distortion reduction by feedback



$$d_1 = \frac{a_1}{1+T} \approx \frac{1}{F}$$

$$d_2 = \frac{a_2}{(1+T)^3}$$

Loop gain $1+T = 1+a_1 F$
u is $(1+T)$ times smaller than **v** : $d_3 = \frac{a_3(1+T) \cdot 2F a_2^2}{(1+T)^5}$
v is reduced by loop gain $(1+T)$

Distortion in elementary transistor circuits

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IM with feedback

$$IM_{2f} = \frac{d_2}{d_1} V = \frac{a_2}{a_1} \frac{V}{(1+T)^2} = \frac{a_2}{a_1} \frac{1}{(1+T)} \frac{V}{(1+T)}$$

reduction by loop gain reduction in current swing

$$IM_{3f} = \frac{3}{4} \frac{d_3}{d_1} V^2 = \frac{3}{4} \left[\frac{a_3}{a_1} \frac{1}{(1+T)} - \left(\frac{a_2}{a_1} \right)^2 \frac{2T}{(1+T)^2} \right] \frac{V^2}{(1+T)^2}$$

compression expansion reduction in current swing

IM_{2f} with emitter degeneration

$$T = g_m R_E = \frac{V_{RE}}{kT_e/q} \quad \frac{a_2}{a_1} = \frac{1}{2}$$

$$IM_{2f} = \frac{1}{2} \frac{1}{(1+T)^2} \frac{V_{in}}{kT_e/q} = \frac{1}{(1+T)} \frac{U}{2}$$

$$U = \frac{1}{(1+T)} \frac{V_{in}}{kT_e/q} \text{ is the relative current swing}$$

IM_{2f} decreases linearly with T for constant U !

Distortion in elementary transistor circuits

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IM_{3f} with emitter degeneration

$$IM_{3f} = \frac{1-2T}{(1+T)^2} \frac{U^2}{8} \quad \frac{a_2}{a_1} = \frac{1}{2} \quad \frac{a_3}{a_1} = \frac{1}{6}$$

$$U = \frac{1}{(1+T)} \frac{V_{in}}{kT_e/q} \text{ is the relative current swing}$$

Null for T = 0.5

IM_{3f} also decreases with T for constant U
for large T !!

Distortion in elementary transistor circuits

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IM_{3f} for large T

$$IM_{3f} = \frac{3}{4} \frac{a_3}{d_1} V^2 = \frac{3}{4} \left[\underbrace{\frac{a_3}{a_1} \frac{1}{(1+T)} - \left(\frac{a_2}{a_1} \right)^2 \frac{2T}{(1+T)^2}}_{\overbrace{(1+T)^2}^{(1+T)^2}} \right] \frac{V^2}{(1+T)^2}$$

For large T: $\frac{a_3 a_1 - 2 a_2^2}{a_1^2} \frac{1}{T} = \frac{a_3}{a_1} \left(1 - \frac{2 a_2^2}{a_1 a_3} \right) \frac{1}{T}$

MOST: $a_3 = 0$: a_2 dominant

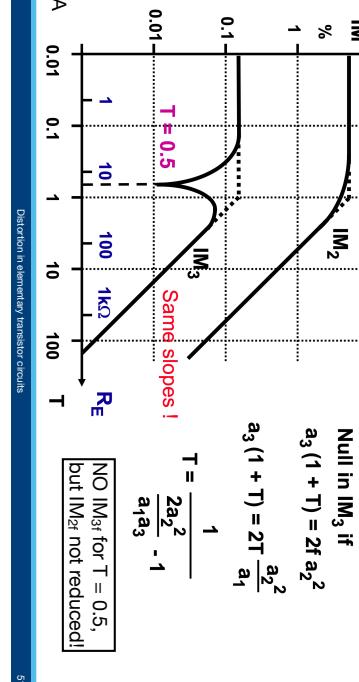
Bipolar: $a_1 = 1$ $a_2 = 1/2$ $a_3 = 1/6$: a_2 dominant

Dif. pair: $a_2 = 0$: a_3 dominant

Distortion in elementary transistor circuits

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Emitter degeneration distortion versus T



Emitter degeneration for large T

$$U = \frac{1}{T} \frac{V_{in}}{kT_e/q} = \frac{V_{in}}{R_E I_{CE}}$$

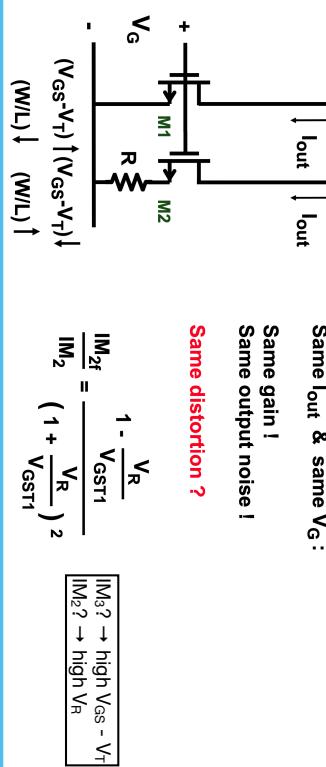
$$IM_{2T} = \frac{U}{2T} = \frac{V_{in}}{kT_e/q} \frac{1}{2T^2} = \frac{V_{in} kT_e/q}{2(R_E I_{CE})^2}$$

$$IM_{3T} = \frac{U^2}{4T} = \left(\frac{V_{in}}{kT_e/q}\right)^2 \frac{1}{4T^3} = \frac{V_{in}^2 kT_e/q}{4(R_E I_{CE})^3}$$

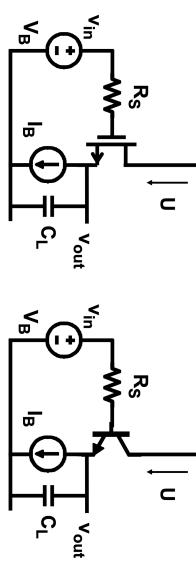
Distortion in elementary transistor circuits

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High $V_{GS} - V_T$ or source degeneration?



Distortion in followers



Distortion in elementary transistor circuits

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Degeneration of differential pair



$|IP_3| \approx 3.3 (V_{GS} - V_T)(1 + g_{m1}R)^2$ HD_3/n^2 $n = 1 + g_{m1}R$
 $HD_3 = -60 \text{ dB for } V_{id} = 1 \text{ V requires } V_{GS} - V_T = 0.38 \text{ V and } g_{m1}R = 3 \text{ !!}$

Distortion in elementary transistor circuits

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Source degeneration reduces distortion

$$T = g_m R_S = \frac{V_{RS}}{(V_{GS} - V_T)/2} \quad \frac{a_2}{a_1} = \frac{1}{4} \quad a_3 = 0$$

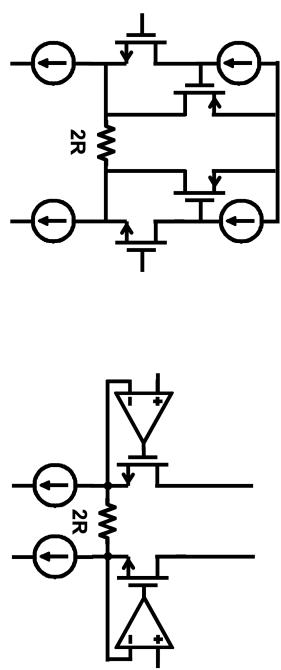
$$U = \frac{1}{(1+T)} \frac{V_{in}}{(V_{GS} - V_T)/2} \quad \text{is the relative current swing}$$

$$IM_{2T} = \frac{1}{4} \frac{U}{T} \approx \frac{V_{in}}{(V_{GS} - V_T)/2} \frac{1}{4T^2} = \frac{V_{in}(V_{GS} - V_T)/2}{4(R_S I_{DS})^2}$$

$$IM_{3T} = \frac{T}{(1+T)^2} \frac{3U^2}{32} \approx \frac{V_{in}^2}{(V_{GS} - V_T)^2/4} \frac{3}{32T^3} = \frac{3V_{in}^2(V_{GS} - V_T)/2}{32(R_S I_{DS})^3}$$

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More feedback reduces distortion



Additional local FB

Distortion in elementary transistor circuits

More FB with opamps

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Condition for zero $|IM_3|$

$$i_{out} = 2(i_{BS1} - i_{BS2})$$

$$\frac{i_{DS}}{I_B} = U - \frac{1}{8}U^3 \quad U = \frac{V_{id}}{V_{GS} - V_T} \quad |IM_3| = \frac{3}{32}U^2$$

$$|IM_3| \approx \frac{3}{32} \left(\frac{V_{id}}{V_{GS1} - V_T} \right)^2 \frac{1 - \alpha v^3}{1 - \alpha v}$$

$$|IM_3| \approx 0 \text{ if } v_{00} = \alpha^{-1/3}$$

at which point $i_{out} = g_{m1} V_{id} (1 - \alpha^{2/3})$

Distortion in elementary transistor circuits

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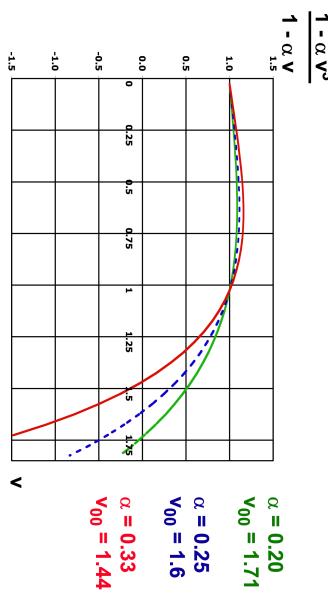
Outline

- Definitions and metrics of distortion
- Distortion in components
- Distortion reduction**
 - Feedback
 - Cancellation
- Distortion in OPAMPS
- Summary

Distortion in elementary transistor circuits

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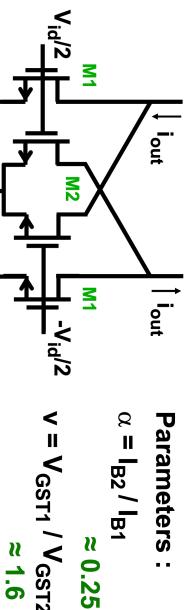
Zero $|IM_3|$ for different α



Distortion in elementary transistor circuits

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Cancelling distortion by subtraction



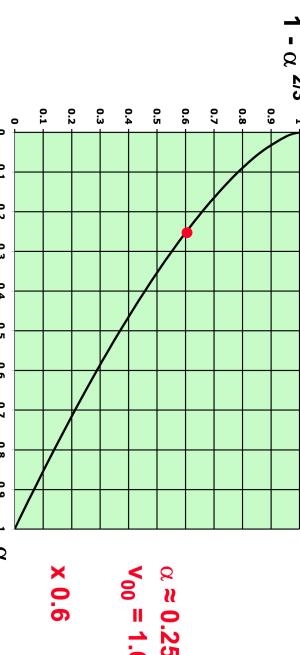
$$I_{B1} = I_{B2}$$

$$|IM_3| \approx 0 \text{ if } v = \alpha^{-1/3}$$

Distortion in elementary transistor circuits

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Subtracting currents reduces signal



Distortion in elementary transistor circuits

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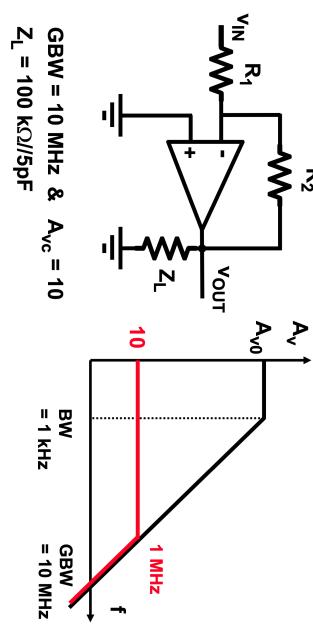
Outline

- Definitions and metrics of distortion
- Distortion in components
- Distortion reduction
- Distortion in OPAMPS**
- Summary

Distortion in elementary transistor circuits

63

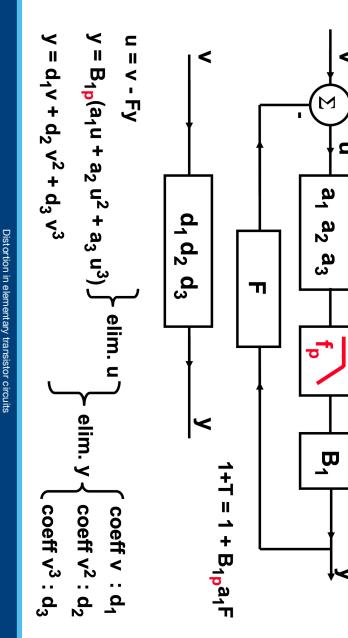
Miller CMOS OTA with feedback



Distortion in elementary transistor circuits

64

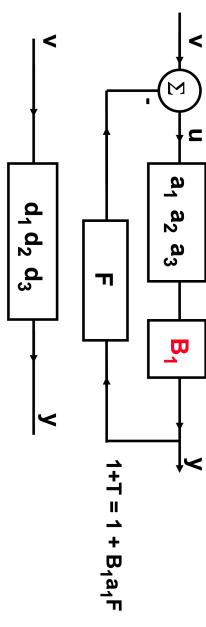
|M_{2f} and |M_{3f} of first stage with f_p



Distortion in elementary transistor circuits

65

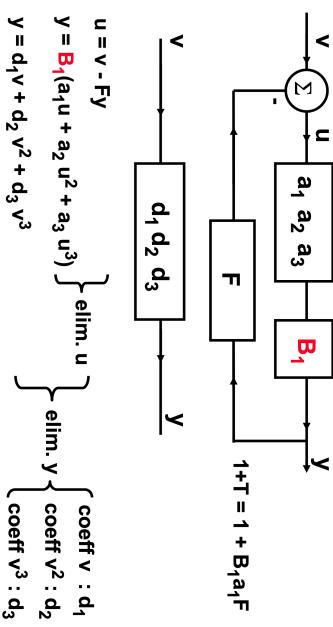
Distortion in first stage



Distortion in elementary transistor circuits

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|M_{2f} and |M_{3f} of first stage with f_p



Distortion in elementary transistor circuits

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$$|M_{2f}| = \frac{d_2}{a_1} \frac{V}{(1+\tau)^2} = \frac{a_2}{a_1} \frac{1}{(B_1 a_1 F)^2} V$$

$$|M_{3f}| = \frac{3}{4} \frac{a_3}{a_1} \frac{1}{(1+\tau)} \frac{V^2}{(1+\tau)^2} = \frac{3}{4} \frac{a_3}{a_1} \frac{1}{(B_1 a_1 F)^3} V^2$$

Same as before but with different Loop gain :

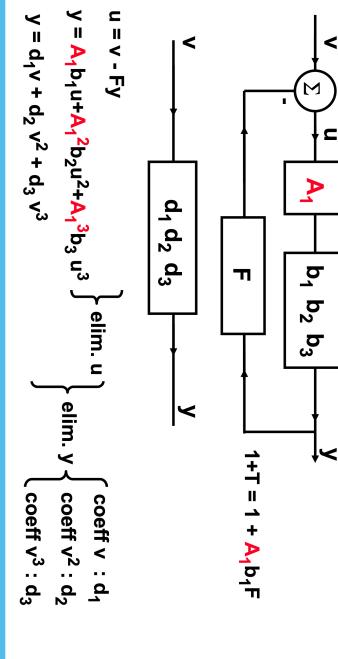
$$1+\tau = 1 + B_1 a_1 F$$

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Distortion in elementary transistor circuits

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Distortion in second stage



69

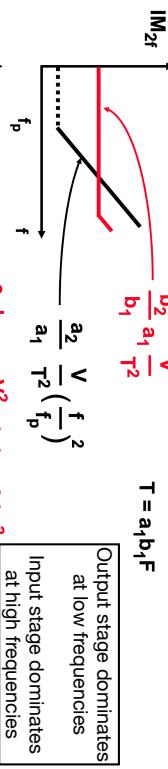
|IM_{2f}| and |IM_{3f}| of second stage

$$\begin{aligned} |IM_{2f}| &= \frac{b_2}{b_1} \frac{V}{(1+T)^2} = \frac{b_2}{b_1} \frac{A_1}{(A_1 b_1 F)^2} V \\ |IM_{3f}| &= \left| \frac{3}{4} \left(\frac{b_2}{b_1} \right)^2 \frac{2T}{(1+T)^2} \frac{V^2}{(1+T)^2} \right| \\ &\text{Single trans.} \\ &= \frac{3}{4} \frac{b_2^2}{b_1^2} \frac{2A_1^2}{(A_1 b_1 F)^3} V^2 \end{aligned}$$

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Distortion in elementary transistor circuits

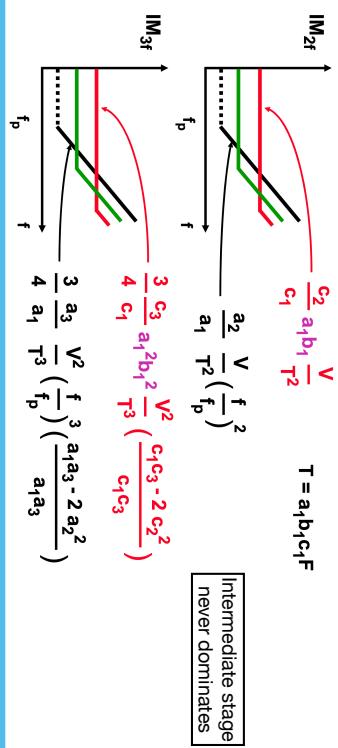
|IM_{2f}| and |IM_{3f}| of both stages



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Distortion in elementary transistor circuits

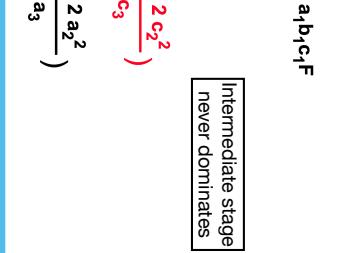
|IM_{2f}| and |IM_{3f}| with three stages



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Distortion in elementary transistor circuits

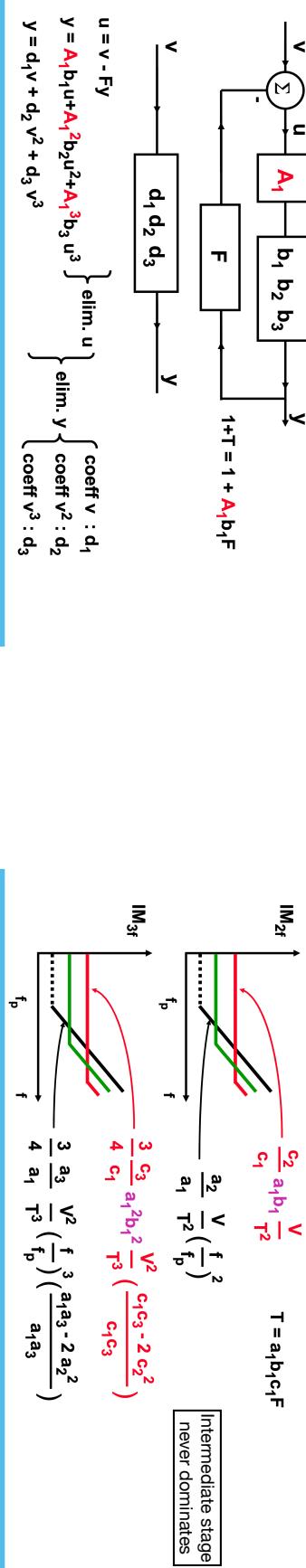
Example



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Distortion in elementary transistor circuits

Signal swing at low frequencies



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Distortion in elementary transistor circuits

Outline

$|IM_{2f}$ and $|IM_{3f}$ at low frequencies

Distortion generation by nonlinear output stage :

$$U_3 = g_{m3} V_m / I_{DS3} = 0.1$$

$$|IM_2| = U_3/4 = 0.25 \cdot 0.1 = 2.5 \%$$

Distortion reduction by feedback :

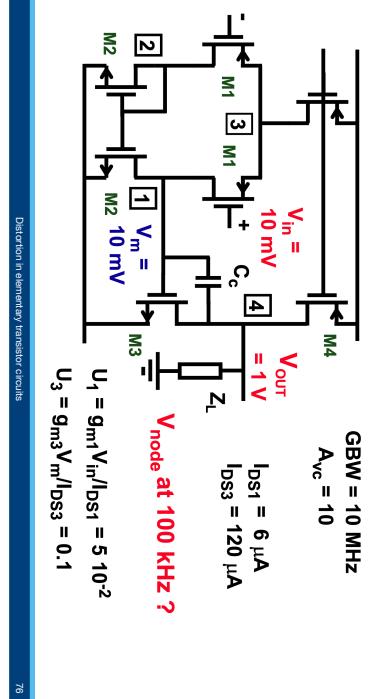
$$T = 1000 \quad |IM_{2f}| = 2.5 \% / 1000 = 0.0025 \% \text{ Negligible!}$$

- Definitions and metrics of distortion
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Distortion in elementary/Immosistor circuits

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Signal swings at high frequencies



Distortion in elementary/Immosistor circuits

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Guidelines for low distortion

- Reduce relative signal swings
- Use feedback
- Use distortion cancellation
- Use differential circuits

Distortion in elementary/transistor circuits

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$|IM_2$ and $|IM_3$ without feedback

Distortion generation by nonlinear output stage :

$$U_3 = g_{m3} V_m / I_{DS3} = 0.1$$

$$|IM_2| = U_3/4 = 0.25 \cdot 0.1 = 2.5 \%$$

Distortion generation by nonlinear input stage :

$$U_1 = g_{m1} V_m / I_{DS1} = 0.05$$

$$|IM_3| = U_1^2/10 = 0.0025/10 = 0.025 \% \text{ Negligible!}$$

Distortion reduction by feedback :

$$T = 10 \quad |IM_{2f}| = 2.5 \% / 100 = 0.25 \%$$

Distortion in elementary/transistor circuits

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	$U_p = V_{ip} / V_{ref}$	$ IM_2 \times U_p $	$ IM_3 \times U_p ^2$	V_{ref}
BJT	1/2	1/8		$kT_{e/q}$
MOST	1/4	0		$(V_{GS} - V_T)/2$
BJT differential pair	0	1/4	$2kT_{e/q}$	
MOST differential pair	0	3/32	$V_{GS} - V_T$	

Distortion in elementary/transistor circuits

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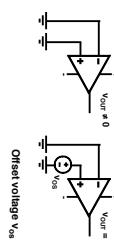
IM₂ and IM₃ with feedback ($\Gamma > 5$)

$U_p = V_{tp}/V_{ref}$	$IM_2 \times U_p$	$IM_3 \times U_p^2$	V_{ref}
BJT	$1/2\Gamma$	$1/4\Gamma$	$kT_e/q \times \Gamma$
MOST	$1/4\Gamma$	$3/32\Gamma$	$(V_{GS} - V_T)/2 \times \Gamma$
BJT differential pair	0	$1/4\Gamma$	$2kT_e/q \times \Gamma$
MOST differential pair	0	$3/32\Gamma$	$V_{GS} - V_T \times \Gamma$

Distortion in elementary transistor circuits

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Definition of offset



Offset voltage V_{GS}

References

P.Wambacq, W.Sansen : Distortion analysis of analog Integrated Circuits, Kluwer Ac. Publ. 1998

W.Sansen : "Distortion in elementary transistor circuits"

IEEE Trans. CAS II Vol 46, No 3, March 1999, pp.315-324

J. Silva-Martinez, et.al: High-performance CMOS continuous-time filters, Kluwer Ac. Publ. 1993

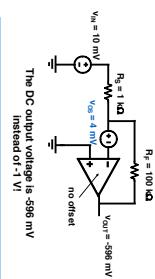
B. Hermes, T. Saether: Design criteria for low-distortion in feedback opamp circuits, Kluwer Ac. Publ. 2003

G. Palumbo, S. Pennisi: Feedback amplifiers, Kluwer Ac. Publ. 2002

Distortion in elementary transistor circuits

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Offset introduces gain errors



The DC output voltage is -598 mV instead of -1 V

Offset leads to reduced yield in ADCs



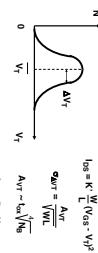
Offset and CMRR



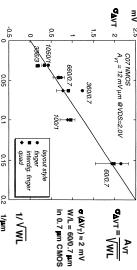
Table of contents

- Random offset and CMRR.
- Systematic offset and CMRR.
- Total CMRR and frequency dependency
- Good layout practices
- Accuracy limit of analog circuits

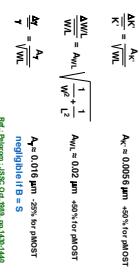
Offset is the result of mismatch



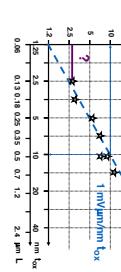
Standard deviation is a function of the area



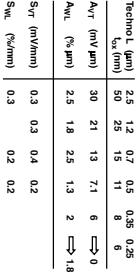
Other MOST mismatch parameters



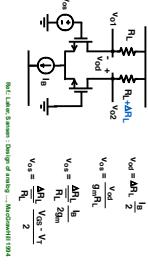
A_V as a function of technology node



nMOST mismatch coefficients

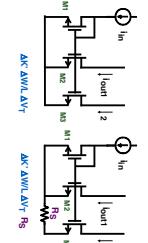


Random offset in a differential pair



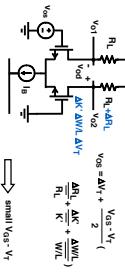
11

Other sources of offset



65

Random offset in a differential pair



Re: Lasker, Saxon : Design of analog ... McGraw-Hill 1974

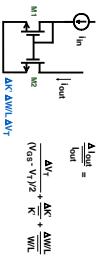
MOST drain current mismatch

$$\frac{\Delta \text{LOS}}{\text{LOS}} = \frac{\Delta \theta}{\Delta V_T} \frac{\text{LOS}}{V_T}$$

$$\sigma^2 \left(\frac{\Delta \text{LOS}}{\text{LOS}} \right) = \sigma^2 \left(\frac{\Delta \theta}{\Delta V_T} \right) + \sigma^2 (\Delta V_T)$$

$$= \frac{1}{n} \sigma_{\theta}^2 + \frac{4}{n} \sigma_{V_T}^2$$

Random offset in a current mirror

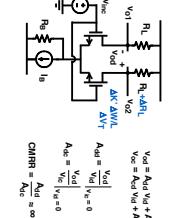


Rat, Lakor, Sanson : Design of analog ... McGrawHill 1994

MOST drain current mismatch in WI and SI

MOST drain current mismatch in WI
and SI

CMRR_i in a differential pair



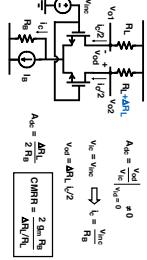
11

Relation between random offset and CMRR_i

$$\begin{aligned} V_{od} &= AV_I + \frac{V_{os} \cdot V_T}{2} \left(\frac{\Delta R_L}{R_L} + \frac{\Delta K'}{K} + \frac{\Delta W_L}{W_L} \right) \\ CMRR_i &= \frac{\frac{2\Delta R_L}{R_L} + \frac{\Delta K'}{K} + \frac{\Delta W_L}{W_L}}{\frac{V_{os} \cdot V_T}{2 \cdot 2g_m R_L}} = \frac{4g_m R_L}{V_{os} \cdot V_T} \\ V_{os} \cdot CMRR_i &= \frac{V_{os} \cdot V_T}{2} \cdot 2g_m R_L = V_T R_L = 5 \dots 15 \text{ V} \\ V_{od} \cdot CMRR_i &= 10 \text{ V} \end{aligned}$$

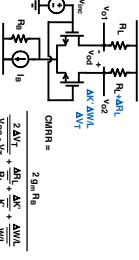
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CMRR_i in a differential pair



11

CMRR_i in a differential pair



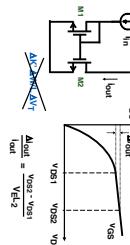
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- * Good layout practices
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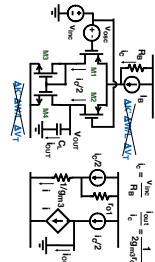
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Systematic offset in a current mirror



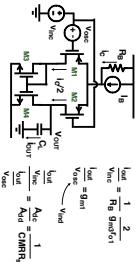
11

$CMRR_s$ in the basic OTA



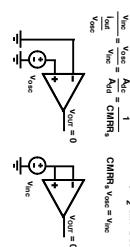
12

$CMRR_s$ in the basic CMOS OTA



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$CMRR_s$ in the basic CMOS OTA



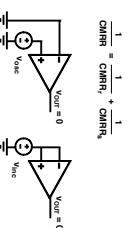
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- * Random offset and CMRR
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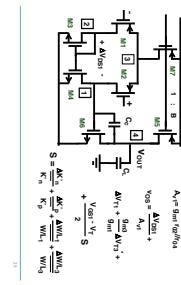
Total CMRR



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Total offset of the Miller OIA

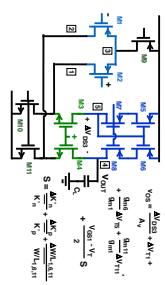


$$\Delta V_{T1} = \frac{\Delta V_{DS1}}{A_{V1}} + \frac{V_{DS1}}{g_{m1}} \Delta V_{T3} + \frac{V_{DS1} - V_T}{2} S$$

- Random offset and CMRR,
 - Systematic offset and CMRR,
 - Total CMRR and frequency dependency
 - **Good layout practices**
 - Accuracy limit of analog circuits

Table of contents

Total offset of the folded-cascode OTA



$$V_{OS} = \frac{\Delta V_{DSI}}{A_V} + \Delta V_I$$

$$+ \frac{g_{m5}}{g_{m1}} \Delta V_{T3} + \frac{g_{m1115}}{g_{m11}}$$

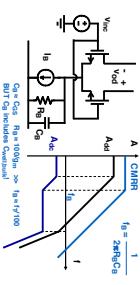
$$+ \frac{V_{GS1} - V_{T1}}{2}$$

$$\equiv \frac{\Delta K_n}{K_n} + \frac{\Delta K_p}{K_p} + \frac{\Delta W}{W}$$

- 1. Equal nature**
 - Equal temperature
 - Large area
 - Minimum distance
 - Some orientation
 - Same area/perimeter ratio
 - Round shape
 - Centrotric layout
 - End dummies
 - B/T better than MOST

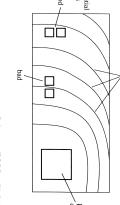
Good layout practices for low offset

CMRR as a function of frequency



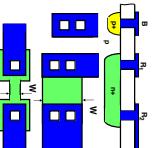
1. Equal nature
 - 2. Equal temperature**
 3. Large area
 4. Minimum distance
 5. Same orientation
 6. Same area/perimeter ratio
 7. Round shape
 8. Centroidal layout
 9. End dummies
 10. BJT better than MOST

On same isotherm



Solomon, JSSC Dec 74, 314-332

Layout of an integrated resistor



Ref.: Lake, Sansen
Design of analog
MacGraw-Hill 1994

Good layout practices for low OISet

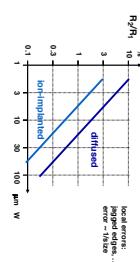
6. Same area/perimeter ratio
 7. Round shape
 8. Centroidic layout
 9. End dummies
 10. BJT better than MOST

Resistor technology parameters

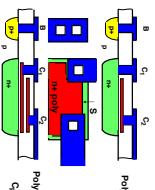
Process	Type	ΔG°	ΔS°	ΔH°	Reference
Benz	benzene	190	0	0	150
ether	ether	10	0	0	100
propanone	ketone	1.4	0	0	100
acetone	ketone	2.0	0	0	100
isopropanol	alcohol	2.8	0	0	100
acetate	ester	0.1	0	0	100
C6H6	benzene	250	0	0	100
toluene	benzene	22.8	0	0	100
p-xylene	benzene	15.0	0	0	100
acetone	ketone	50.0	0	0	100
isopropanol	alcohol	50.0	0	0	100
acetate	ester	200	0	0	100
Tolu	benzene	20	0	0	100

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Misfit as a function of resistor area



Layout of an integrated capacitor

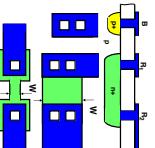


$$C_{\text{par}} \approx \frac{1}{6 \dots 15} C_{\text{pp}}$$

Good layout practices for low OIS net

6. Same area/perimeter ratio
 7. Round shape
 8. Centroidic layout
 9. End dummies
 10. BJT better than MOST

Layout of an integrated resistor



Ref.: Lake, Sansen
Design of analog
MacGraw-Hill 1994

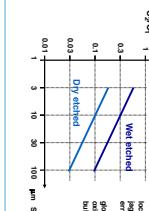
Good layout practices for low OIS net

6. Same area/perimeter ratio
 7. Round shape
 8. Centroidic layout
 9. End dummies
 10. BJT better than MOST

Capacitor technology table

	Process	Type	Age ^a	Age ^b	Age ^c	Age ^d	Age ^e
Reactor	Ce-40	metamorphic	11	13	0.33	2	90
	Ce-20	metamorphic	10	22	0.33	0.5	2
CMOS	100-nm	70	0.02	0.02	0.02	0.02	0.02
	90-nm	70	0.02	0.02	0.02	0.02	0.02
	80-nm	66	0.02	0.02	0.02	0.02	0.02
	70-nm	66	0.02	0.02	0.02	0.02	0.02
	65-nm	53	0.02	0.02	0.02	0.02	0.02
	55-nm	53	0.02	0.02	0.02	0.02	0.02
	45-nm	53	0.02	0.02	0.02	0.02	0.02
	32-nm	53	0.02	0.02	0.02	0.02	0.02
	28-nm	53	0.02	0.02	0.02	0.02	0.02
	22-nm	53	0.02	0.02	0.02	0.02	0.02
	18-nm	53	0.02	0.02	0.02	0.02	0.02
	14-nm	53	0.02	0.02	0.02	0.02	0.02
	10-nm	53	0.02	0.02	0.02	0.02	0.02
	7-nm	53	0.02	0.02	0.02	0.02	0.02
	5-nm	53	0.02	0.02	0.02	0.02	0.02
	3-nm	53	0.02	0.02	0.02	0.02	0.02
	2-nm	53	0.02	0.02	0.02	0.02	0.02
	1-nm	53	0.02	0.02	0.02	0.02	0.02
	0.5-nm	53	0.02	0.02	0.02	0.02	0.02
	0.3-nm	53	0.02	0.02	0.02	0.02	0.02
	0.2-nm	53	0.02	0.02	0.02	0.02	0.02
	0.1-nm	53	0.02	0.02	0.02	0.02	0.02
	0.05-nm	53	0.02	0.02	0.02	0.02	0.02
	0.02-nm	53	0.02	0.02	0.02	0.02	0.02
	0.01-nm	53	0.02	0.02	0.02	0.02	0.02
	0.005-nm	53	0.02	0.02	0.02	0.02	0.02
	0.002-nm	53	0.02	0.02	0.02	0.02	0.02
	0.001-nm	53	0.02	0.02	0.02	0.02	0.02
	0.0005-nm	53	0.02	0.02	0.02	0.02	0.02
	0.0002-nm	53	0.02	0.02	0.02	0.02	0.02
	0.0001-nm	53	0.02	0.02	0.02	0.02	0.02
	0.00005-nm	53	0.02	0.02	0.02	0.02	0.02
	0.00002-nm	53	0.02	0.02	0.02	0.02	0.02
	0.00001-nm	53	0.02	0.02	0.02	0.02	0.02
	0.000005-nm	53	0.02	0.02	0.02	0.02	0.02
	0.000002-nm	53	0.02	0.02	0.02	0.02	0.02
	0.000001-nm	53	0.02	0.02	0.02	0.02	0.02
	0.0000005-nm	53	0.02	0.02	0.02	0.02	0.02
	0.0000002-nm	53	0.02	0.02	0.02	0.02	0.02
	0.0000001-nm	53	0.02	0.02	0.02	0.02	0.02
	0.00000005-nm	53	0.02	0.02	0.02	0.02	0.02
	0.00000002-nm	53	0.02	0.02	0.02	0.02	0.02
	0.00000001-nm	53	0.02	0.02	0.02	0.02	0.02
	0.000000005-nm	53	0.02	0.02	0.02	0.02	0.02
	0.000000002-nm	53	0.02	0.02	0.02	0.02	0.02
	0.000000001-nm	53	0.02	0.02	0.02	0.02	0.02
	0.0000000005-nm	53	0.02	0.02	0.02	0.02	0.02
	0.0000000002-nm	53	0.02	0.02	0.02	0.02	0.02
	0.0000000001-nm	53	0.02	0.02	0.02	0.02	0.02
	0.00000000005-nm	53	0.02	0.02	0.02	0.02	0.02
	0.00000000002-nm	53	0.02	0.02	0.02	0.02	0.02
	0.00000000001-nm	53	0.02	0.02	0.02	0.02	0.02

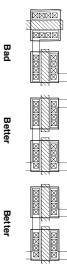
Mismatch as a function of capacitor area



Good layout practices for low offset

2. Equal temperature
 3. Large area
 4. Minimum distance
 - 5. Same orientation**
 6. Same area/perimeter ratio
 7. Round shape
 8. Centroide layout
 9. End dummies
 10. BJT better than MOST

Matching of transistor pair



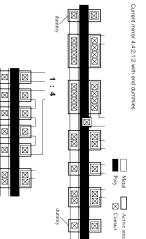
Good layout practices for low offset

1. Equal nature
 2. Equal temperature
 3. Large area
 - 4. Minimum distance**
 5. Same orientation
 6. Same area/perimeter ratio
 7. Round shape
 8. Centroidal layout
 9. End dummies
 10. BJT better than MOST

Good layout practices for low offset

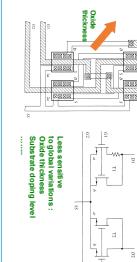
- 1. Equal nature
 - 2. Equal temperature
 - 3. Large area
 - 4. Minimum distance
 - 5. Same orientation
 - 6. Same area/perimeter ratio**
 - 7. Round shape
 - 8. Centroidal layout
 - 9. End dummies
 - 10. BJT better than MOST

Matching of current mirrors



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Centroide layout of a differential pair



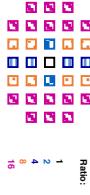
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Good layout practices for low offset

1. Equal nature
2. Equal temperature
3. Large area
4. Minimum distance
5. Same orientation
6. Same area/perimeter ratio
7. Round shape
8. Centrode layout
9. End dummies
10. BJT better than MOST

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Centroide layout of a pactor bank



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Good layout practices for low offset

1. Equal nature
2. Equal temperature
3. Large area
4. Minimum distance
5. Same orientation
6. Same area/perimeter ratio
7. Round shape
8. Centrode layout
9. End dummies
10. BJT better than MOST

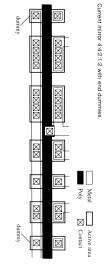
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Good layout practices for low offset

1. Equal nature
2. Equal temperature
3. Large area
4. Minimum distance
5. Same orientation
6. Same area/perimeter ratio
7. Round shape
8. Centrode layout
9. End dummies
10. BJT better than MOST

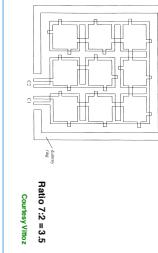
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Matching of current mirrors



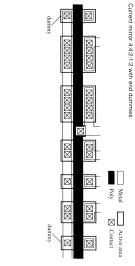
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Matching of capacitors



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Offset for MOST and BiJT



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Table of Contents

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- * Systematic offset and CMRR_c
- * Total CMRR and frequency dependency
- * Good layout practices
- * Accuracy limit of analog circuits

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Good layout practices for low offset

1. Fractal nature
2. Equal temperature
3. Large area
4. Minimum distance
5. Same orientation
6. Same area/perimeter ratio
7. Round shape
8. Centroid layout
9. End dummies
10. **BiJT better than MOST**

Limits because of mismatch

$$\frac{1}{(\text{Accuracy})^2} \approx \sigma^2 \left(\frac{\Delta V_{DS}}{I_{DS}} \right)^2 \approx \frac{4 K_b T^2}{W_L (V_{GS} - V_T)^2}$$

$$\text{Speed} = f_T = \frac{2 I_{DS}}{2 \pi W L 2 \beta C_{ox} (V_{GS} - V_T)} \approx \frac{V_{DD}}{2}$$

$$\frac{\text{Speed} \times (\text{Accuracy})^2}{\text{Power}} = \frac{1}{C_o V_{AVT}^2} \sim \frac{1}{I_{DS}}$$

= technological constant

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Limits because of noise

$$S/N = \frac{V_{pp}^2/2}{4kT_{R}BW}$$

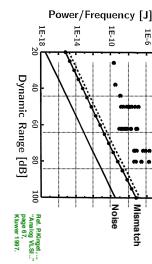
$$SN = \frac{V_{pp}^2B}{kT/C}$$

$$P_{min} = \frac{V_{pp}^2}{R}$$

$$P_{min} \approx V_{DD}BWV_{pp}C$$

$$P_{min} \approx kT_{R}BW S/N$$

Speed-accuracy-power trade-off



The challenge of technology scaling

