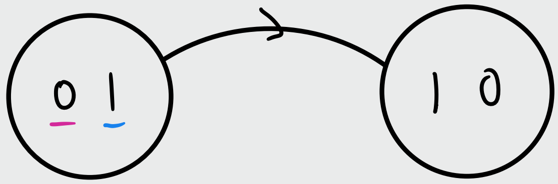
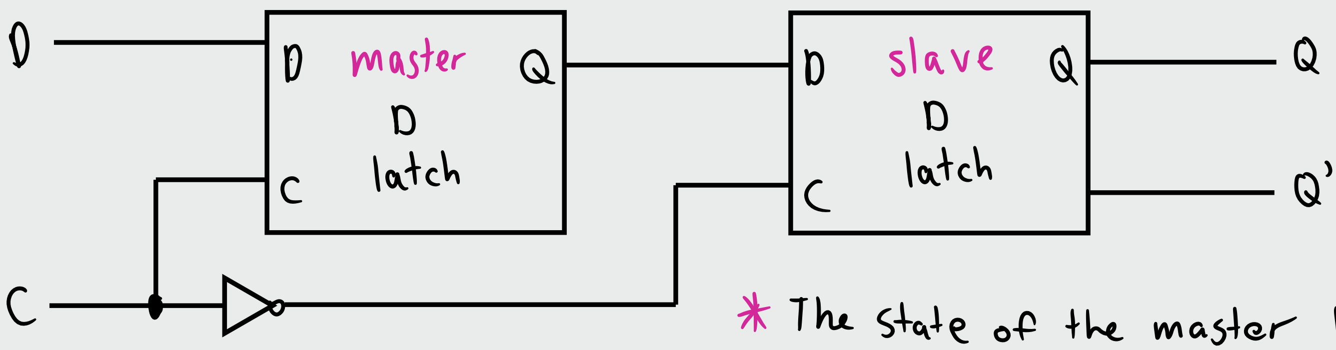


flip flop A

flip flop B

Each f/f must change state instantly at the same time, otherwise we might end up at the wrong state

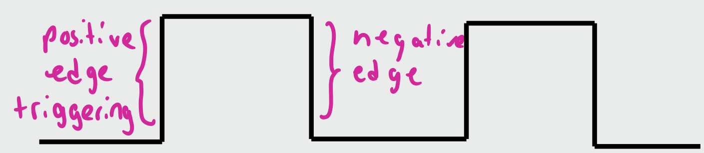
We can use a <u>master-slave</u> approach to make sure that changes propagate instantly.



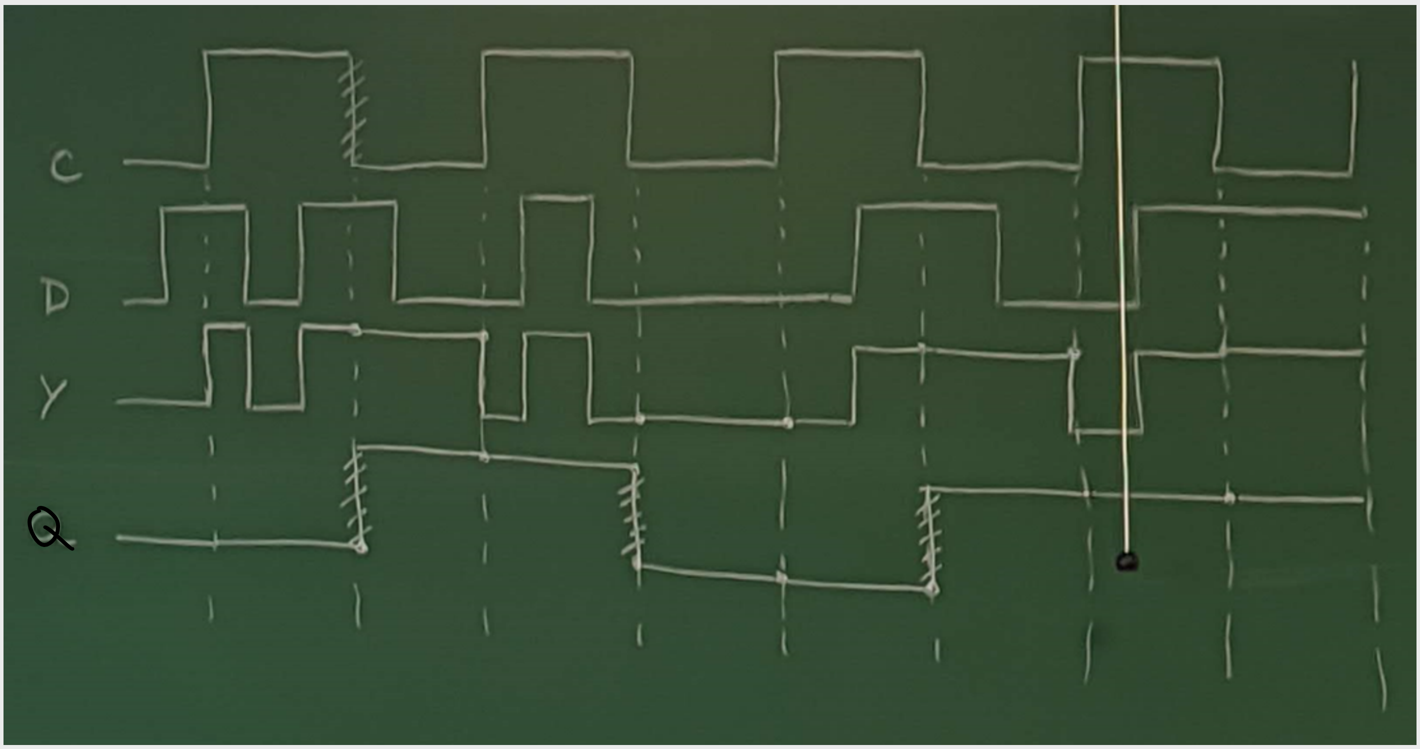
* The state of the master becomes the input of the slave

The clock behaves as such:

	clock = 1	clock = 0
If D is	0,1,1,0,1,0,1	0,1,1,0,1,0,1
Y becomes	0,1,1,0,1,0,1	1,1,1,1,1,1,1
Q:	0,1,1,0,1,0,1 (no change)	1...



When D and C are 1 the state of the master becomes 1. the only way to change the value of the circuit (master) is for C to change from 1 to 0 (negative edge)

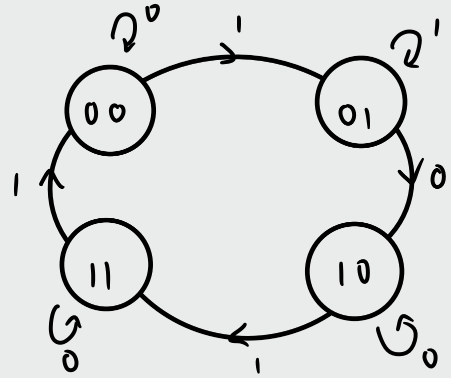


When clock is 1, y is a copy of the input
When clock is 0, y doesn't change

Q is a copy of y when clock is 0, no change when clock is 1

Problem statement: Design the clocked sequential circuit for the below specification using JK flip flops.

0 → 1 by a 1
1 → 2 by a 0
2 → 3 by a 1
3 → 0 by a 1



JK Excitation table

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(b) JK

Present State $Q(t)$		Input	Next state $Q(t+1)$		f/f inputs			
A	B	X	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

Kmaps

J_A

A \ BX	00	01	11	10
0				1
1	X	X	X	X

$J_A = BX'$

K_A

A \ BX	00	01	11	10
0	X	X	X	X
1			1	

$K_A = BX$

J_B

A \ BX	00	01	11	10
0				
1				

K_B

A \ BX	00	01	11	10
0				
1				

$J_A = BX'$ $K_A = BX$