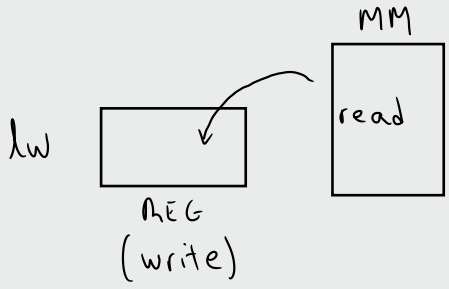
Execution Cycles

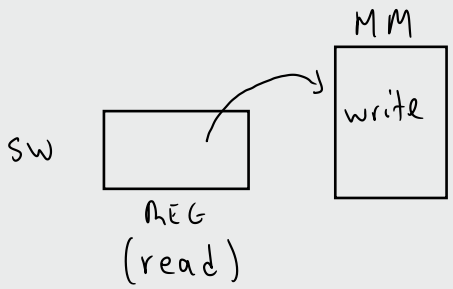
- Fetch Instruction, update the PC register
- Instruction memory (read only)
  get in with an address
  the address is stored in the PC register
  get out with the instruction
  PC register is updated [PC + 4]
- Decode
  The instruction is parsed into fields (R-format has OPCODE 000000)
  get the source data
  Register file (2 read ports and 1 write port)

  Understand the implementation of the read and write ports (B56 on Patterson)

- Execute
  ALU: compute logical and arithmetic operations
  output: result of the operation, it can represent target address (lw, sw),
    check for zero

  Write-back or memory address
  Data memory or register file
  Write-back: R-format
  memory access: lw and sw





Datapath for R-format

sout = shift amount
fct = function counter