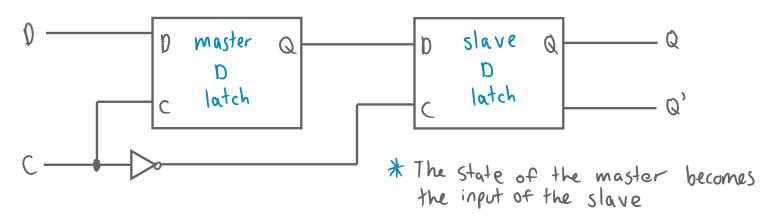
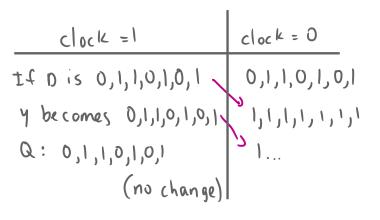


flip flop A Each f/f must change state instantly at the same time, otherwise we might end up at the wrong state

We can use a <u>master-slave</u> approach to make sure that changes propagate instantly.

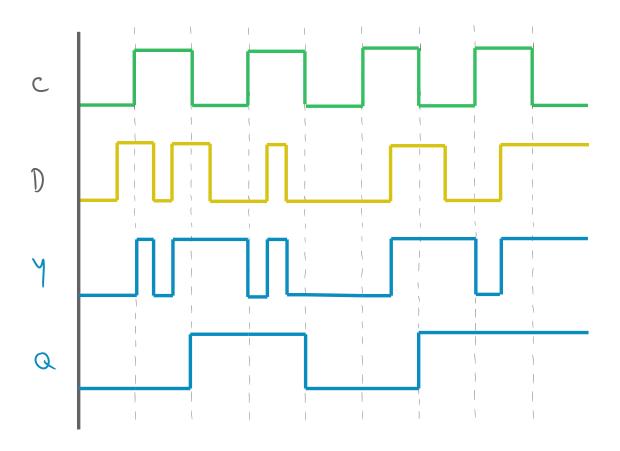


The clock behaves as such:





When D and C are 1 the state of the master becomes 1. The only way to change the value of the circuit (master) is for C to change from 1 to 0 (negative edge)



Given C and D, we can determine Y and Q by considering the following:

Y: output of the master f/f

Q: output of the slave f/f

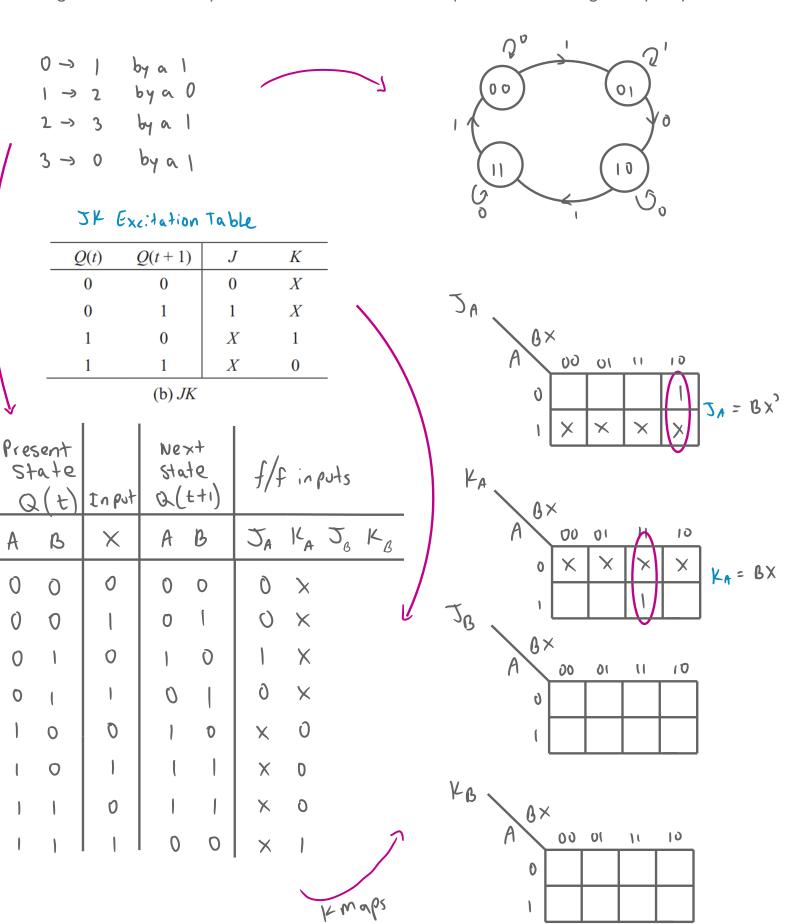
Behavior of Y:

- When clock is 1, Y is a copy of D
- When clock is 0, Y doesn't change

Behavior of Q:

- When clock is 0, $\ensuremath{\mathsf{Q}}$ is a copy of Y
- When clock is 1, Q doesn't change

Design the clocked sequential circuit for the below specification using JK flip flops.



 $J_A = B \times'$ $K_A = B \times$

