Memory Hierarchy, Address Decoding, and RAM Expansion

Memory Structure

· Memory composition: Memory is built from the smallest unit (memory cell) up to larger structures. - A memory cell stores 1 bit - 8 cells = 1 byte - 4 bytes = 1 word (in MIPS) - words can be grouped into blocks · Access Pattern; - Building: from cell - byte - word - block - Accessing: from block > word > byte > cell (big to small) Read: uses MUX Write: In order to get to a specific location: uses decoders Memory Unit: Size and Structure · Represented as 2" × m: - K = address size (number of bits needed for addressing) - M = word size (number of bits per word) · A memory unit includes: - Read/write control line - Input and output data lines - select line (for chip selection in multi-chip setups) · Addressing Modes - Byte Addressing (eg. in MIPS): each address points to a byte - Word Addressing: each address points to a word RAM: Types and Characteristics · Static RAM (SRAM) - Faster, more expensive - Used in cache memory - Doesn't need refreshing '
- Stores data using flip-flops - More reliable for frequent and fast access · Dynamic RAM (DRAM) - Slower, cheaper - Used in most main memory systems - Stores data using capacitors that leak charge - Needs periodic refreshing (read then re-write the value to restore it) - Less expensive and denser than SRAM, allowing for higher capacity

Expanding RAM with an Array of RAM Chips

Given a RAM configuration $1K \times 16$, we want to:

- Increase the RAM capacity 10 times
- Access word 3079 (draw the circuit and indicate the settings to accommodate this task)

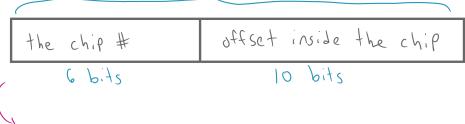
To increase the capacity 10 times, we'll put 10 chips together > Co to Cq
To access word 3079, we consider that each RAM chip holds 1024 words, so
to access word 0-1023, we need to access Co. To access word 1024, we
need to access C,

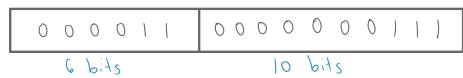
$$3079 = 3 \times 1024 + 7 = 2 \times 1024 + 1024 + 7$$

$$2'' + 2'' + 7$$

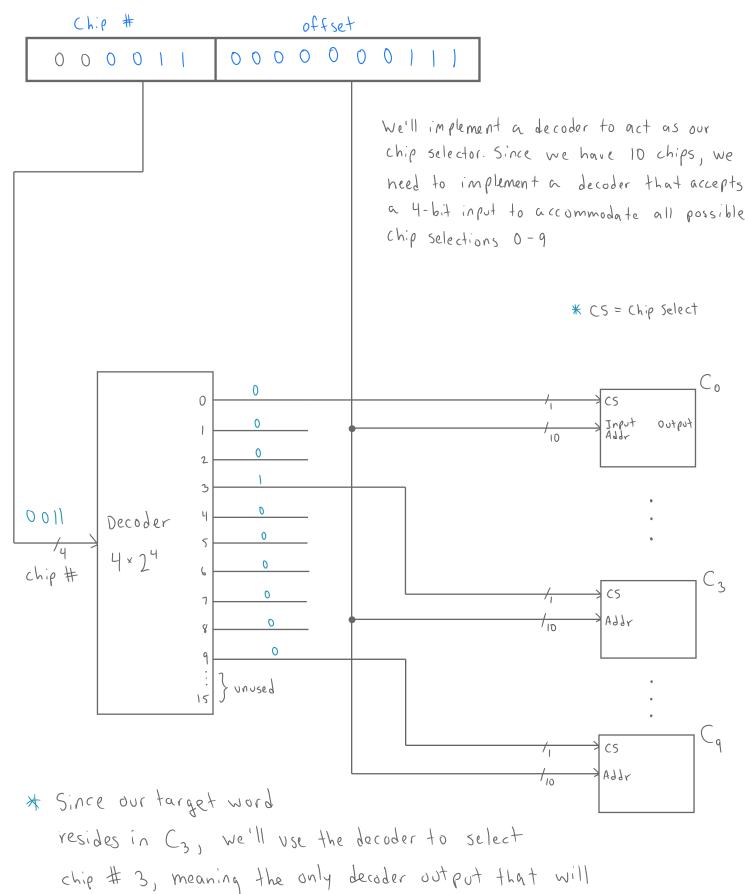
By examining our RAM config, $14 \times 16 = 2^{10} \times 16$, we can see that we need 10 bits to accommodate the offset. Since we have 16-bit words, we can assume a 16-bit address

Address structure: 16 bits





our Address to access word 3079:



be I will be line 3, which leads to C3