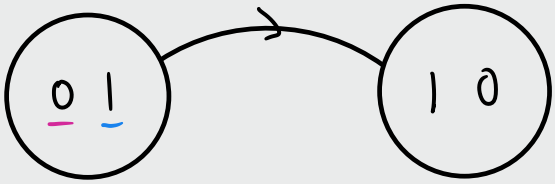
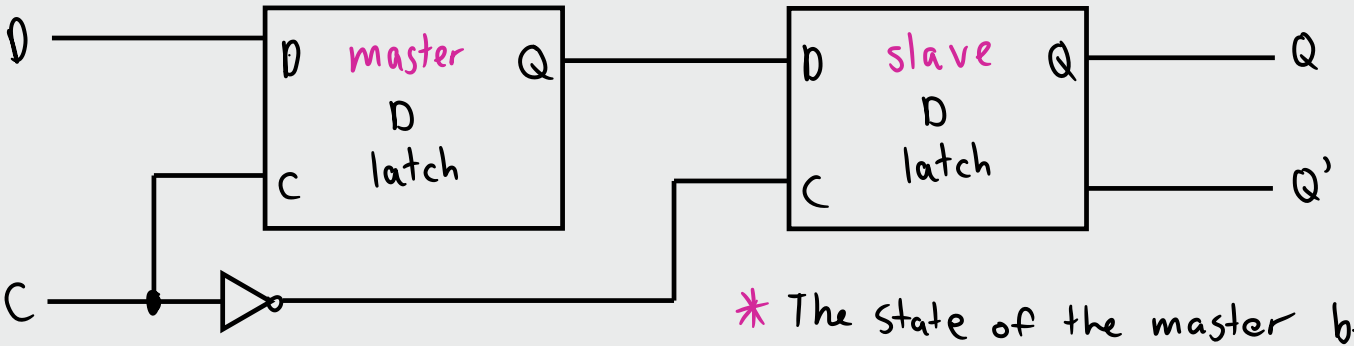


flip flop A

flip flop B

Each f/f must change state instantly at the same time, otherwise we might end up at the wrong state

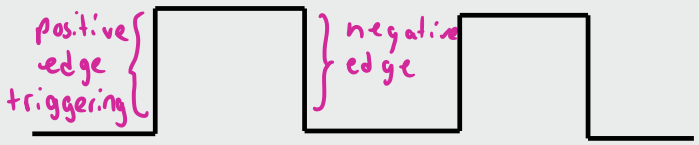
We can use a master-slave approach to make sure that changes propagate instantly.



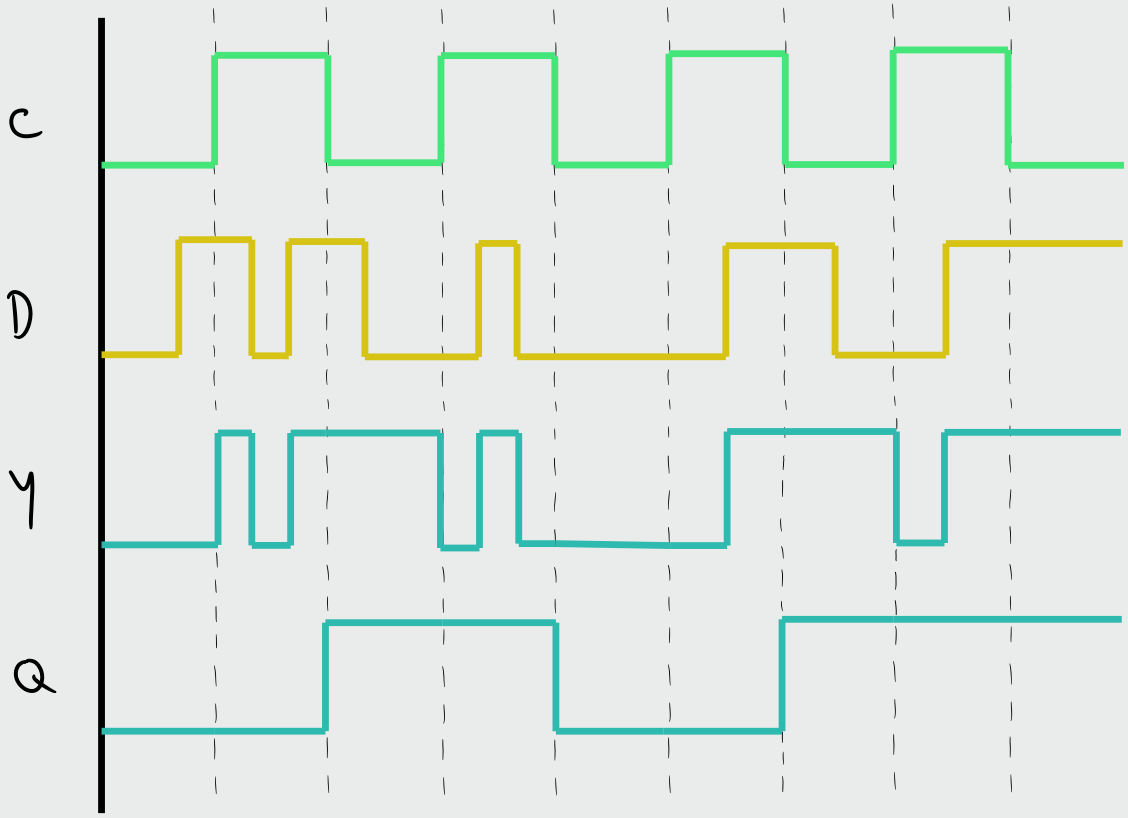
* The state of the master becomes the input of the slave

The clock behaves as such:

clock = 1	clock = 0
If D is 0,1,1,0,1,0,1	0,1,1,0,1,0,1
y becomes 0,1,1,0,1,0,1	1,1,1,1,1,1,1
Q: 0,1,1,0,1,0,1	1...
(no change)	



When D and C are 1 the state of the master becomes 1.
the only way to change the value of the circuit (master) is for C to change from 1 to 0 (negative edge)



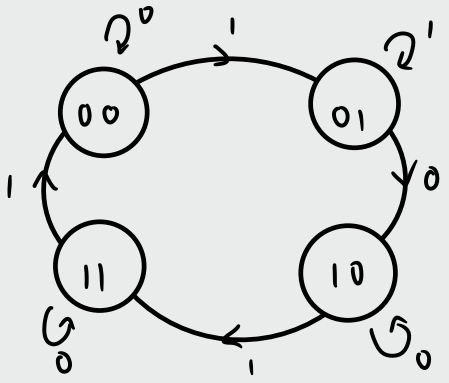
Y: output of the master f/f
Q: output of the slave f/f

Behavior of Y:
When clock is 1, Y is a copy of the input D
When clock is 0, Y doesn't change

Behavior of Q:
When clock is 0, Q is a copy of Y
When clock is 1, Q doesn't change

Problem statement: Design the clocked sequential circuit for the below specification using JK flip flops.

$0 \rightarrow 1$ by a 1
$1 \rightarrow 2$ by a 0
$2 \rightarrow 3$ by a 1
$3 \rightarrow 0$ by a 1



JK Excitation Table

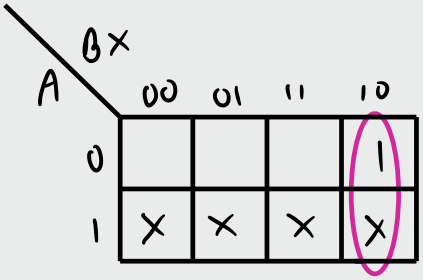
$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(b) JK

Present State Q(t)		Input	Next state Q(t+1)		f/f inputs			
A	B	X	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

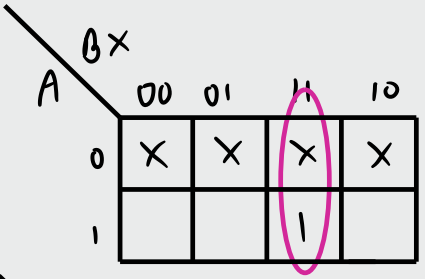
K maps

J_A



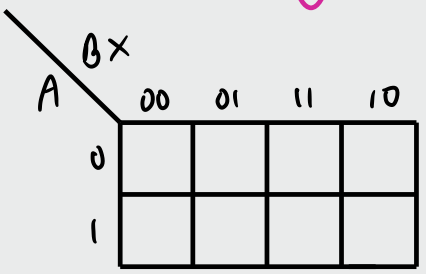
$J_A = BX'$

K_A

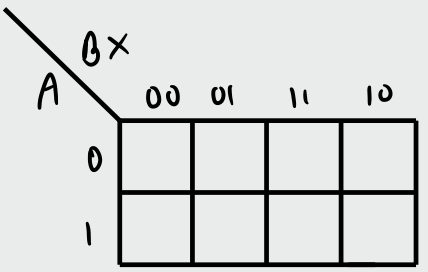


$K_A = BX$

J_B



K_B



$J_A = BX'$ $K_A = BX$