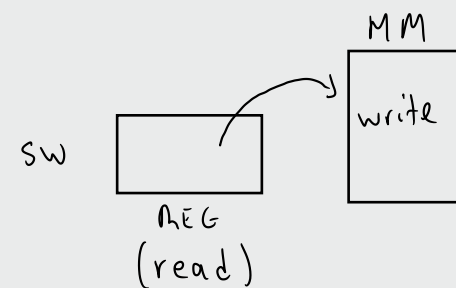
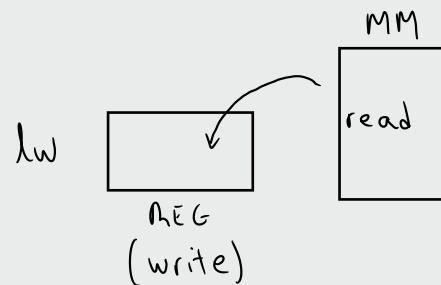


## Execution Cycles

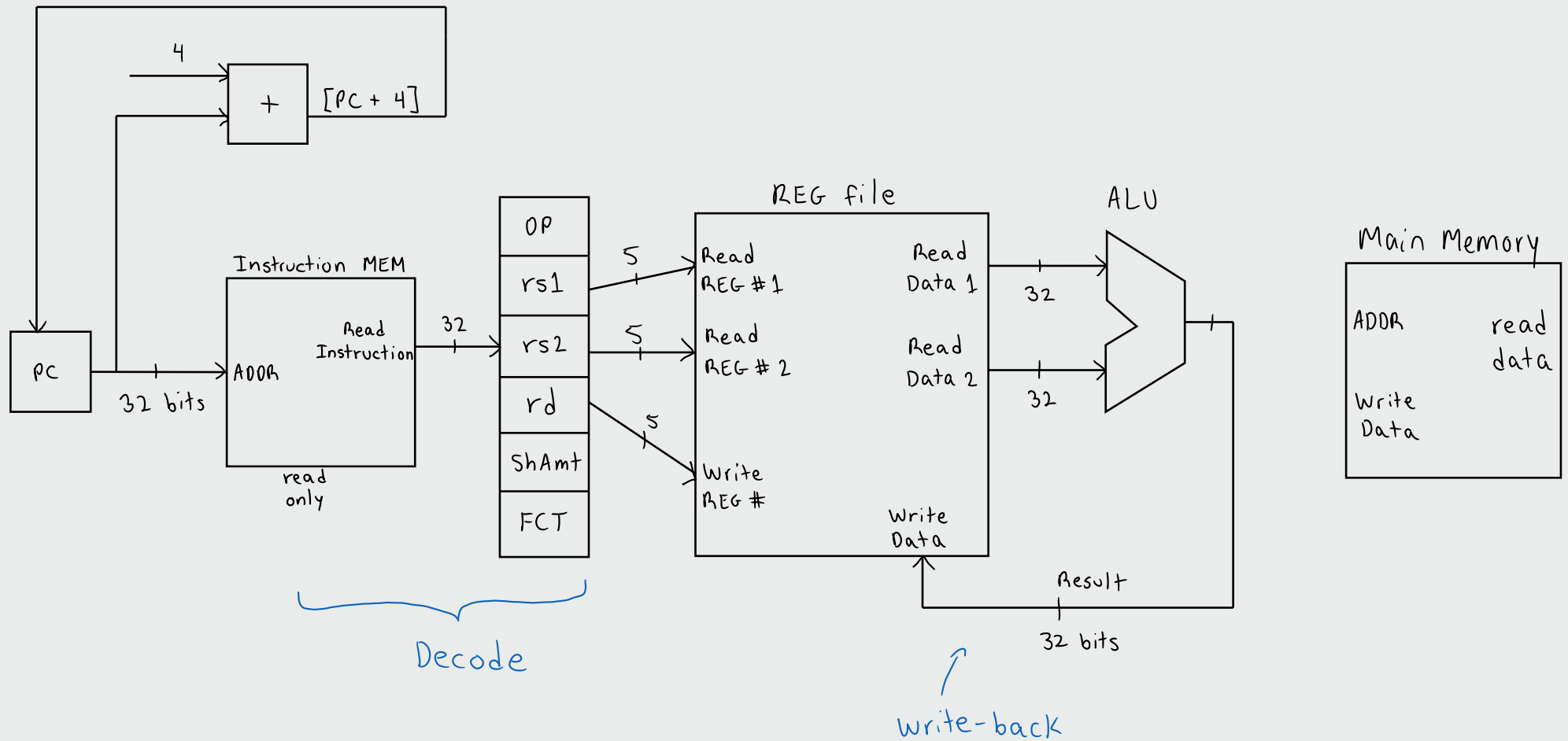
- Fetch instruction, update the PC register  
Instruction memory (read only)  
Get in with an address  
The address is stored in the PC register  
Get out with the instruction  
PC register is updated  $[PC + 4]$
- Decode  
The instruction is parsed into fields (R-format has OPcode 000000)  
Get the source data  
Register file (2 read and 1 write port)
- \* Must understand the implementation of the read and write ports (B56 on Patterson)
- Execute  
ALU: compute logical and arithmetic operations  
Output: result of the operation, it can represent target address (lw, sw)  
check for zero
- Write back/memory access  
Data memory or register file  
Write-back: R-format  
Memory access: lw and sw

## Instructions to cover

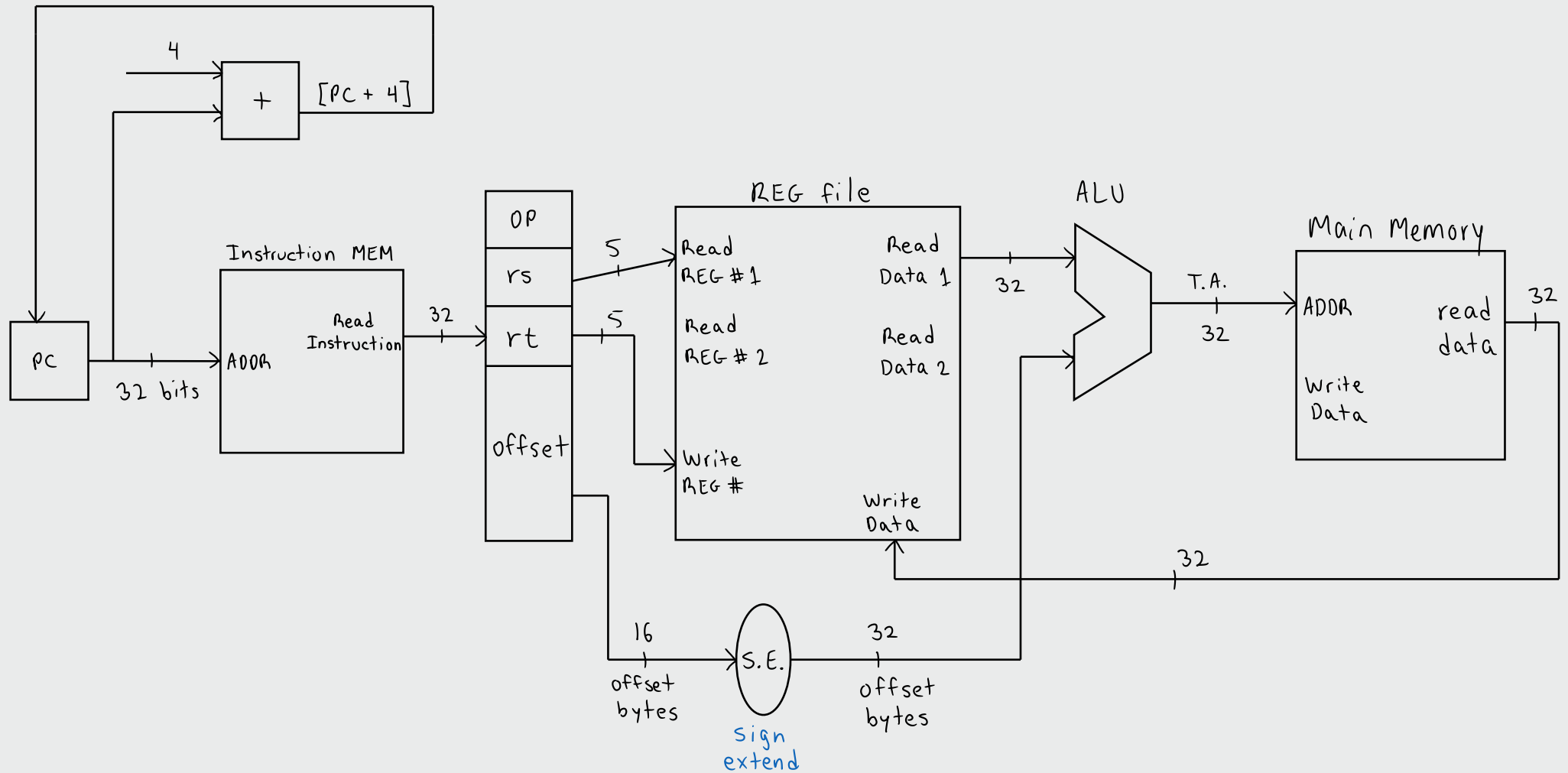
- R-format
- Load word
- Store word
- beq
- J



# Datapath for R-format



## Datapath for lw (load word)



# Datapath for beg

