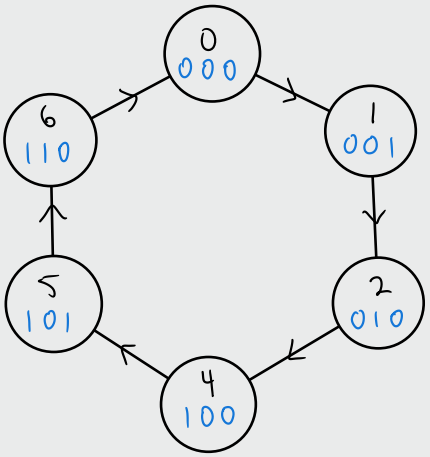
Problem statement: Implement the sequential circuit needed for the following sequence (using T f/f)

0 → 1 → 2 → 4 → 5 → 6



$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

(d) T

T flip flop

Excitation table

	Q(t)			Q(t+1)					
	A	B	C	A	B	C	T_A	T_B	T_C
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
2	0	1	0	1	0	0	1	1	0
4	1	0	0	1	0	1	0	0	1
5	1	0	1	1	1	0	0	1	1
6	1	1	0	0	0	0	1	1	0

T_A

A \ BC	00	01	11	10
0			X	1
1			X	1

$T_A = B$

T_B

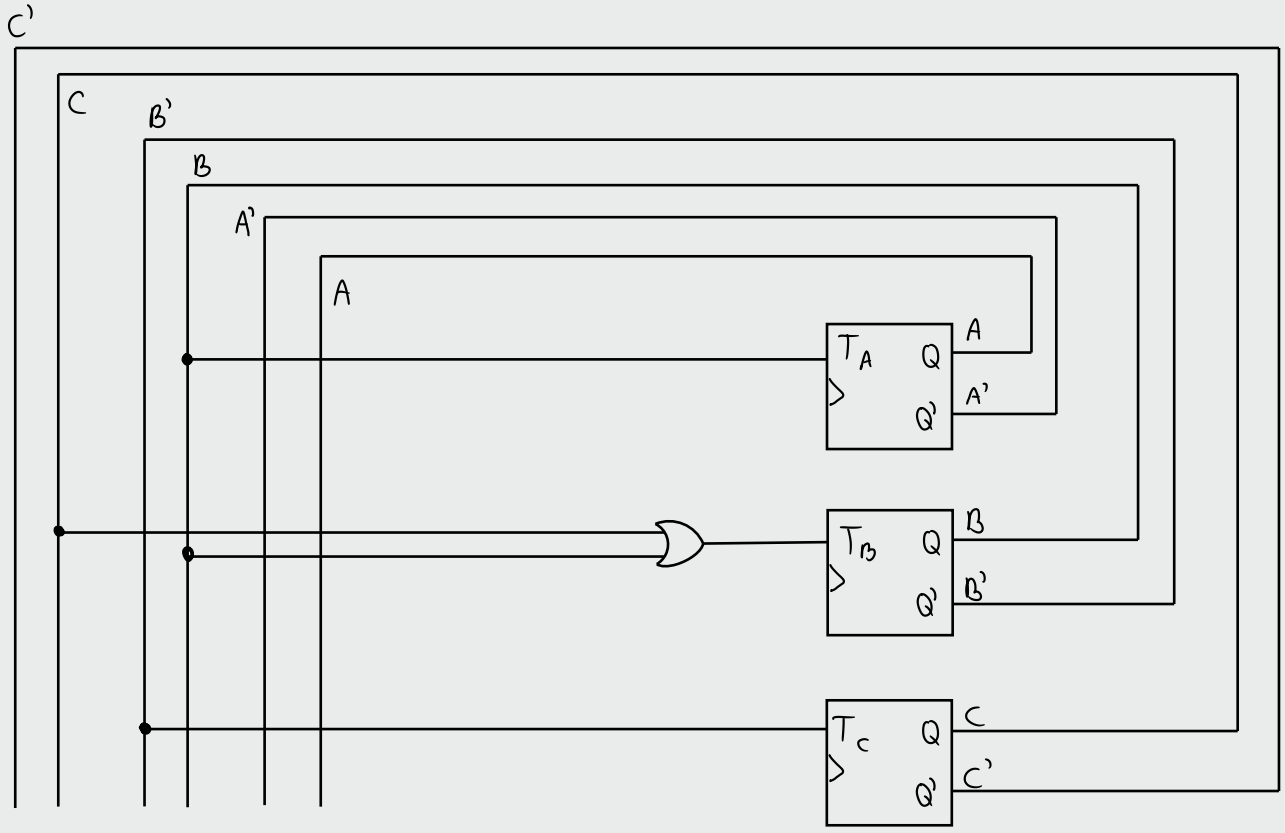
A \ BC	00	01	11	10
0		1	X	1
1		1	X	1

$T_B = B + C$

T_C

A \ BC	00	01	11	10
0	1	1	X	
1	1	1	X	

$T_C = B'$



T	$Q(t+1)$
0	$Q(t)$
1	$Q'(t)$

T flip flop characteristic table

Unused State 011

A	B	C
0	1	1
↓	↓	↓
1	0	1

$T_A = B = 1$ ⇒ toggle

$T_B = B + C = 1 + 1 = 1$ ⇒ toggle

$T_C = B' = 0$ ⇒ no change

Since the invalid states transition to valid states (011 → 100 and 111 → 001), then this circuit is self correcting

Unused State 111

A	B	C
1	1	1
↓	↓	↓
0	0	1

$T_A = B = 1$ ⇒ toggle

$T_B = B + C = 1 + 1 = 1$ ⇒ toggle

$T_C = B' = 0$ ⇒ no change