

1 **Reference Data**

V	_		Kelei ence i	Data
RV32I BASE	INTE	GER INSTRUCTIONS, in al	phabetical order	
MNEMONIC	FMT	NAME	DESCRIPTION (in Verilog)	NOTE
add	R	ADD	R[rd] = R[rs1] + R[rs2]	
addi	I	ADD Immediate	R[rd] = R[rs1] + imm	
and	R	AND	R[rd] = R[rs1] & R[rs2]	
andi	I	AND Immediate	R[rd] = R[rs1] & imm	
auipc	U	Add Upper Immediate to PC	$R[rd] = PC + \{imm, 12'b0\}$	
beq	SB	Branch EQual	if(R[rs1]==R[rs2) PC=PC+{imm,1b'0}	
bge	SB	Branch Greater than or Equal	if(R[rs1]>=R[rs2) PC=PC+{imm,1b'0}	
bgeu	SB	$Branch \geq Unsigned$	if(R[rs1]>=R[rs2) PC=PC+{imm,1b'0}	2)
blt	SB	Branch Less Than	if(R[rs1] <r[rs2) pc="PC+{imm,1b'0}</td"><td></td></r[rs2)>	
bltu	SB	Branch Less Than Unsigned	if(R[rs1] <r[rs2) pc="PC+{imm,1b'0}</td"><td>2)</td></r[rs2)>	2)
bne	SB	Branch Not Equal	if(R[rs1]!=R[rs2) PC=PC+{imm,1b'0}	
csrrc	I	Cont./Stat.RegRead&Clear	$R[rd] = CSR; CSR = CSR \& \sim R[rs1]$	
csrrci	I	Cont./Stat.RegRead&Clear Imm	R[rd] = CSR;CSR = CSR & ~imm	
csrrs	I	Cont./Stat.RegRead&Set	$R[rd] = CSR; CSR = CSR \mid R[rs1]$	
csrrsi	Ī	Cont./Stat.RegRead&Set Imm	R[rd] = CSR; CSR = CSR imm	
csrrw	I	Cont./Stat.RegRead&Write	R[rd] = CSR; CSR = R[rs1]	
csrrwi	I	Cont./Stat.Reg Read&Write	R[rd] = CSR; $CSR = IRISI$	
		Imm	Ritaj Corc, Corc IIIIII	
ebreak	I	Environment BREAK	Transfer control to debugger	
ecall	I	Environment CALL	Transfer control to operating system	
fence	I	Synch thread	Synchronizes threads	
fence.i	I	Synch Instr & Data	Synchronizes writes to instruction	
		2,	stream	
jal	UJ	Jump & Link	$R[rd] = PC+4; PC = PC + \{imm, 1b'0\}$	
jalr	I	Jump & Link Register	R[rd] = PC+4; $PC = R[rs1]+imm$	
lb	I	Load Byte	R[rd] =	3)
		and the state of t	{24'bM[](7),M[R[rs1]+imm](7:0)}	4)
lbu	I	Load Byte Unsigned	$R[rd] = \{24'b0,M[R[rs1]+imm](7:0)\}$,
lh	I	Load Halfword	$R[rd] = {16'bM[](15),M[R[rs1]+imm](15:0)}$	
lhu	I	Load Halfword Unsigned	$R[rd] = \{16'b0,M[R[rs1]+imm](15:0)\}$	4)
lui	U	Load Upper Immediate	$R[rd] = \{imm, 12'b0\}$	
lw	I	Load Word	$R[rd] = \{M[R[rs1]+imm](31:0)\}$	
or	R	OR	$R[rd] = R[rs1] \mid R[rs2]$	
ori	I	OR Immediate	$R[rd] = R[rs1] \mid imm$	4)
sb	S	Store Byte	M[R[rs1]+imm](7:0) = R[rs2](7:0)	
sh	S	Store Halfword	M[R[rs1]+imm](15:0) = R[rs2](15:0)	
sll	R	Shift Left	R[rd] = R[rs1] << R[rs2]	
slli	I	Shift Left Immediate	$R[rd] = R[rs1] \ll imm$	
slt	R	Set Less Than	R[rd] = (R[rs1] < R[rs2]) ? 1 : 0	
slti	I	Set Less Than Immediate	R[rd] = (R[rs1] < imm) ? 1 : 0	
sltiu	I	Set < Immediate Unsigned	R[rd] = (R[rs1] < imm) ? 1 : 0	
sltu	R	Set Less Than Unsigned	R[rd] = (R[rs1] < R[rs2]) ? 1 : 0	
sra	R	Shift Right Arithmetic	R[rd] = R[rs1] >> R[rs2]	
srai	I	Shift Right Arith Imm	R[rd] = R[rs1] >> imm	2)
srl	R	Shift Right (Word)	R[rd] = R[rs1] >> R[rs2]	2)
srli	I	Shift Right Immediate	$R[rd] = R[rs1] \gg imm$	5)
sub, subw	R	SUBtract (Word)	R[rd] = R[rs1] - R[rs2]	5)
sw	S	Store Word	M[R[rs1]+imm](31:0) = R[rs2](31:0)	
xor	R	XOR	$R[rd] = R[rs1] \wedge R[rs2]$	
xori	I	XOR Immediate	$R[rd] = R[rs1] \land imm$	

Notes: 1) Operation assumes unsigned integers (instead of 2's complement)

- 2) The least significant bit of the branch address in jalr is set to 0

 3) (signed) Load instructions extend the sign bit of data to fill the 32-bit register

 4) Replicates the sign bit to fill in the leftmost bits of the result during right shift

 5) Multiply with one operand signed and one unsigned

- The Single version does a single-precision operation using the rightmost 32 bits of a 64bit F register
- Classify writes a 10-bit mask to show which properties are true (e.g., -inf, -0,+0, +inf,
- denorm, ...)

 8) Atomic memory operation; nothing else can interpose itself between the read and the write of the memory location

 The immediate field is sign-extended in RISC-V

Instruction	ALUOp1	ALUOp0
R-format	1	0
lw	0	0
sw	0	0
beq	0	1

ALU control lines	Function
0000	AND
0001	OR
0010	add
0110	subtract

CORE INSTRUCTION FORMATS

	31	27	26	25	24	20	19	15	14	12	11	7	6	0
R		funct7			rs	s2	r	s1	fur	nct3	re	i	Opco	ode
I		imı	m[11	:0]			r	sl	fur	ict3	re	i	Opco	ode
\mathbf{s}		imm[11:5	5]		rs	s2	r	sl	fur	nct3	imm	[4:0]	opco	de
SB		imm[12 10	:5]		rs	s2	r	sl	fur	nct3	imm[4	:1 11]	opco	de
U				ir	nm[31	:12]	5.0				re	i	opco	de
UJ			in	nm[20	0 10:1	11 19	:12]				re	i	opco	de

OPCODES IN NUMERICAL ORDER BY OPCODE

1	OPCODES IN					
The composition The compos	MNEMONIC	FMT	OPCODE	FUNCT3	FUNCT7 OR II	
1						
Second Process Seco						
Thu	lw	I	0000011	010		03/2
fence I 0001111 000 0F/0 fence.i I 0001111 001 0F/1 addi I 0010011 000 13/0 slli I 0010011 010 13/1/00 slli I 0010011 010 13/2 sltiu I 0010011 010 13/2 sltiu I 0010011 100 13/2 sltiu I 0010011 100 13/4 srli I 0010011 100 13/5/20 srai I 0010011 101 0000000 13/5/20 ori I 0010011 110 110 13/6 srai I 0010011 111 111 13/7 ssb S 0100011 000 23/0 sh S 0100011 000 23/0 sh S 0100011 001 23/1 sw S 0100011 010 23/2 sh S 0100011 010 000000 33/0/00 sub R 0110011 000 0100000 33/0/00 slt R 0110011 001 0000000 33/2/00 slt R 0110011 010 0000000 33/2/00 slt R 0110011 010 0000000 33/4/00 sra R 0110011 101 0000000 33/4/00 sra R 0110011 101 0000000 33/5/00 sra R 0110011 101 0000000 33/5/00 sra R 0110011 101 0000000 33/5/00 sra R 0110011 110 0000000 33/5/00 sra R	lbu	I		100		03/4
fence.i I 0001111 001 0F/1 addi I 0010011 000 13/0 slli I 0010011 001 0000000 13/1/00 slti I 0010011 010 13/2 sltiu I 0010011 011 13/3 xori I 0010011 101 0000000 13/5/00 srai I 0010011 101 0100000 13/5/20 ori I 0010011 101 13/6 13/6 andi I 0010011 001 23/0 23/0 23/0 sh S 0100011 001 23/1 23/1 23/1 23/2 add R 0110011	lhu	I	0000011	101		03/5
addi I 0010011 000 13/0 slli I 0010011 001 0000000 13/1/00 slti I 0010011 011 13/2 scri I 0010011 100 13/4 srai I 0010011 101 0000000 13/5/00 srai I 0010011 101 0100000 13/5/20 ori I 0010011 110 13/6 andi I 0010011 111 13/7 sb S 0100011 111 13/7 sb S 0100011 101 13/7 sb S 0100011 101 23/0 sh S 0100011 001 23/1 sw S 0100011 001 23/2 add R 0110011 000 0000000 33/0/20 sub R 0110011 001 0000000 33/1/00 <td>fence</td> <td>I</td> <td>0001111</td> <td></td> <td></td> <td>0F/0</td>	fence	I	0001111			0F/0
slli I 0010011 001 0000000 13/1/00 slti I 0010011 010 13/2 sltiu I 0010011 011 13/3 svori I 0010011 100 13/4 srli I 0010011 101 0000000 13/5/00 srai I 0010011 101 0100000 13/5/20 ori I 0010011 110 13/6 andi I 0010011 111 13/7 sb S 0100011 000 23/0 sh S 0100011 001 23/2 add R 0100011 000 000000 33/0/00 sub R 0110011 000 000000 33/0/00 sub R 0110011 000 000000 33/1/00 sl1 R 0110011 010 000000 33/2/00 slt R 011001	fence.i	I	0001111	001		0F/1
slti I 0010011 010 13/2 sltiu I 0010011 011 13/3 xori I 0010011 101 13/4 xrli I 0010011 101 0000000 13/5/00 srai I 0010011 101 0100000 13/5/20 ori I 0010011 110 13/6 andi I 0010011 111 13/7 sb S 0100011 000 23/0 sh S 0100011 001 23/1 sw S 0100011 001 23/2 add R 0110011 000 000000 33/000 sw S 0100011 000 000000 33/000 sub R 0110011 000 000000 33/2/00 sl1 R 0110011 010 000000 33/2/00 sltu R 0110011 010	addi	I	0010011	000		13/0
sltiu I 0010011 011 13/3 xori I 0010011 100 13/4 srli I 0010011 101 0000000 13/5/00 srai I 0010011 101 0100000 13/5/20 ori I 0010011 110 13/6 andi I 0010011 111 13/7 sb S 0100011 000 23/0 sh S 0100011 001 23/1 sw S 0100011 001 23/2 add R 0110011 000 0000000 33/0/00 sub R 0110011 000 0000000 33/0/00 sub R 0110011 000 0000000 33/0/00 sub R 0110011 010 0000000 33/2/00 slt R 0110011 01 0000000 33/3/00 slt R 0110011	slli	I	0010011	001	0000000	13/1/00
xori I 0010011 100 13/4 srli I 0010011 101 0000000 13/5/00 srai I 0010011 101 0100000 13/5/20 ori I 0010011 110 13/6 andi I 0010011 111 13/7 sb S 0100011 000 23/0 sh S 0100011 001 23/1 sw S 0100011 001 23/2 add R 0110011 000 0000000 33/0/00 sub R 0110011 001 000000 33/0/20 sub R 0110011 001 000000 33/1/00 sub R 0110011 010 000000 33/2/00 slt R 0110011 011 000000 33/3/00 xor R 0110011 101 0000000 33/5/00 sra R </td <td>slti</td> <td>Î</td> <td>0010011</td> <td>010</td> <td></td> <td>13/2</td>	slti	Î	0010011	010		13/2
xori I 0010011 100 13/4 srli I 0010011 101 0000000 13/5/00 srai I 0010011 101 0100000 13/5/20 ori I 0010011 110 13/6 andi I 0010011 111 13/7 sb S 0100011 000 23/0 sh S 0100011 001 23/1 sw S 0100011 001 23/2 add R 0110011 000 0000000 33/0/00 sub R 0110011 000 000000 33/0/00 sub R 0110011 001 000000 33/0/00 sub R 0110011 001 000000 33/3/00 slt R 0110011 011 000000 33/3/00 slt R 0110011 101 0000000 33/3/00 sra R </td <td>sltiu</td> <td>I</td> <td>0010011</td> <td>011</td> <td></td> <td>13/3</td>	sltiu	I	0010011	011		13/3
srai I 0010011 101 0100000 13/5/20 ori I 0010011 110 13/6 andi I 0010011 111 13/7 sb S 0100011 000 23/0 sh S 0100011 001 23/1 sw S 0100011 000 000000 33/0/00 sub R 0110011 000 010000 33/0/20 sub R 0110011 000 010000 33/0/20 sub R 0110011 001 000000 33/0/20 sub R 0110011 010 0000000 33/2/00 slt R 0110011 011 0000000 33/4/00 sttu R 0110011 101 0000000 33/5/20 sra R 0110011 101 0000000 33/5/20 or R 0110011 110 0000000 33/5/20	xori		0010011	100		13/4
ori I 0010011 110 13/6 andi I 0010011 111 13/7 sb S 0100011 000 23/0 sh S 0100011 001 23/1 sw S 0100011 001 23/2 add R 0110011 000 0000000 33/0/20 sub R 0110011 000 0100000 33/2/20 sl1 R 0110011 010 0000000 33/2/00 slt R 0110011 01 0000000 33/4/00 sltu R 0110011 101 0000000 33/4/00 srl R 0110011 101 0000000 33/4/00 srl R 0110011 101 0000000 33/5/00 srl R 0110011 101 0000000 33/5/00 sra R 0110011 101 0000000 33/5/00	srli	I	0010011	101	0000000	13/5/00
ori I 0010011 110 13/6 andi I 0010011 111 13/7 sb S 0100011 000 23/0 sh S 0100011 001 23/1 sw S 0100011 010 23/2 add R 0110011 000 0000000 33/0/20 sub R 0110011 000 0100000 33/0/20 sub R 0110011 001 0000000 33/1/00 sub R 0110011 001 0000000 33/1/00 sub R 0110011 010 0000000 33/2/00 slt R 0110011 011 0000000 33/3/00 sor R 0110011 101 0000000 33/5/00 sra R 0110011 101 0000000 33/5/00 sra R 0110011 101 0000000 33/5/00	srai	ī	0010011	101	0100000	13/5/20
andi I 0010011 111 13/7 sb S 0100011 000 23/0 sh S 0100011 001 23/1 sw S 0100011 001 23/2 add R 0110011 000 0000000 33/0/00 sub R 0110011 001 0000000 33/1/00 sl1 R 0110011 001 0000000 33/1/00 slt R 0110011 010 0000000 33/3/00 xor R 0110011 101 0000000 33/4/00 srl R 0110011 101 0000000 33/5/00 srl R 0110011 101 0000000 33/5/00 sra R 0110011 101 0000000 33/5/00 or R 0110011 101 0000000 33/6/00 and R 0110011 101 0000000 33/7/00	ori		0010011	110		13/6
sh S 0100011 001 23/1 sw S 0100011 010 23/2 add R 0110011 000 0000000 33/0/20 sub R 0110011 000 0100000 33/1/00 sl1 R 0110011 011 0000000 33/2/00 slt R 0110011 010 0000000 33/2/00 scor R 0110011 101 0000000 33/5/00 sra R 0110011 101 0000000 33/5/00 sra R 0110011 101 0100000 33/5/20 or R 0110011 101 0100000 33/5/20 or R 0110011 110 0000000 33/6/00 and R 0110011 110 0000000 33/7/00 lui U 0110111 11 0000000 33/7/00 beq SB 1100011 00	andi		0010011	111		13/7
sw S 0100011 010 23/2 add R 0110011 000 0000000 33/0/00 sub R 0110011 000 0100000 33/0/20 sl1 R 0110011 001 0000000 33/1/00 slt R 0110011 010 0000000 33/3/00 scor R 0110011 101 0000000 33/5/00 srl R 0110011 101 0000000 33/5/00 sra R 0110011 101 0000000 33/5/00 sra R 0110011 101 0100000 33/5/00 or R 0110011 110 0000000 33/6/00 and R 0110011 110 0000000 33/7/00 lui U 011011 11 0000000 33/7/00 beq SB 1100011 001 63/0 bne SB 1100011	sb		0100011			
add R 0110011 000 0000000 33/0/00 sub R 0110011 000 0100000 33/1/00 sll R 0110011 001 0000000 33/1/00 slt R 0110011 010 0000000 33/1/00 slt R 0110011 010 0000000 33/2/00 sltu R 0110011 011 0000000 33/3/00 xor R 0110011 101 0000000 33/4/00 srl R 0110011 101 0000000 33/5/00 sra R 0110011 101 0000000 33/5/20 or R 0110011 101 0100000 33/5/20 or R 0110011 110 0000000 33/5/20 blu U 0110111 37	sh	S	0100011	001		23/1
sub R 0110011 000 0100000 33/0/20 sl1 R 0110011 001 0000000 33/1/00 slt R 0110011 010 0000000 33/2/00 sltu R 0110011 011 0000000 33/4/00 scor R 0110011 101 0000000 33/5/00 srl R 0110011 101 0000000 33/5/00 sra R 0110011 101 0100000 33/5/20 or R 0110011 110 0000000 33/7/00 and R 0110011 11 0000000 33/7/00 lui U 0110111 11 0000000 33/7/00 beq SB 1100011 000 63/0 bne SB 1100011 001 63/1 blt SB 1100011 100 63/6 bge SB 1100011 11 63/6	SW	S	0100011	010		23/2
sll R 0110011 001 0000000 33/1/00 slt R 0110011 010 0000000 33/2/00 sltu R 0110011 011 0000000 33/3/00 xor R 0110011 100 0000000 33/4/00 srl R 0110011 101 0000000 33/5/00 sra R 0110011 110 0100000 33/5/20 or R 0110011 110 0000000 33/6/00 and R 0110011 111 0000000 33/7/00 lui U 0110111 11 0000000 33/7/00 beq SB 1100011 000 63/0 bne SB 1100011 001 63/1 blt SB 1100011 100 63/4 bge SB 1100011 110 63/6 bgeu SB 1100011 11 63/6	add	R	0110011	000	0000000	33/0/00
slt R 0110011 010 0000000 33/2/00 sltu R 0110011 011 0000000 33/3/00 xor R 0110011 100 0000000 33/4/00 srl R 0110011 101 0000000 33/5/00 sra R 0110011 101 0100000 33/5/20 or R 0110011 110 0000000 33/6/00 and R 0110011 111 0000000 33/7/00 lui U 011011 11 0000000 33/7/00 beq SB 1100011 000 63/0 bne SB 1100011 001 63/1 blt SB 1100011 100 63/4 bge SB 1100011 110 63/6 bgeu SB 1100011 11 63/7 jalr I 110011 000 67/0	sub	R	0110011	000	0100000	33/0/20
sltu R 0110011 011 0000000 33/3/00 xor R 0110011 100 0000000 33/4/00 srl R 0110011 101 0000000 33/5/00 sra R 0110011 101 0100000 33/5/20 or R 0110011 110 0000000 33/6/00 and R 0110011 111 0000000 33/7/00 lui U 0110111 37 beq SB 1100011 000 63/0 bne SB 1100011 001 63/1 blt SB 1100011 100 63/4 bge SB 1100011 110 63/5 bltu SB 1100011 110 63/6 bgeu SB 1100011 11 63/7 jalr I 1100111 000 67/0	sll	R	0110011	001	0000000	33/1/00
xor R 0110011 100 0000000 33/4/00 srl R 0110011 101 0000000 33/5/00 sra R 0110011 101 0100000 33/5/20 or R 0110011 110 0000000 33/6/00 and R 0110011 111 0000000 33/7/00 lui U 0110111 37 beq SB 1100011 000 63/0 bne SB 1100011 001 63/1 blt SB 1100011 100 63/4 bge SB 1100011 101 63/5 bltu SB 1100011 110 63/6 bgeu SB 1100011 111 63/7 jalr I 1100111 000 67/0	slt	R	0110011	010	0000000	33/2/00
srl R 0110011 101 0000000 33/5/00 sra R 0110011 101 0100000 33/5/20 or R 0110011 110 0000000 33/6/00 and R 0110011 111 0000000 33/7/00 lui U 0110111 000 63/0 beq SB 1100011 001 63/1 bht SB 1100011 100 63/4 bge SB 1100011 101 63/5 bltu SB 1100011 110 63/6 bgeu SB 1100011 11 63/7 jalr I 1100111 000 67/0	sltu	R	0110011	011	0000000	33/3/00
sra R 0110011 101 0100000 33/5/20 or R 0110011 110 0000000 33/6/00 and R 0110011 111 0000000 33/7/00 lui U 0110111 37 beq SB 1100011 000 63/0 bne SB 1100011 001 63/1 blt SB 1100011 100 63/4 bge SB 1100011 110 63/6 bgeu SB 1100011 11 63/7 jalr I 110011 000 67/0	xor	R	0110011	100	0000000	33/4/00
or R 0110011 110 0000000 33/6/00 and R 0110011 111 0000000 33/7/00 lui U 0110111 0000000 33/7/00 beq SB 1100011 000 63/0 bne SB 1100011 001 63/1 blt SB 1100011 100 63/4 bge SB 1100011 101 63/5 bltu SB 1100011 110 63/6 bgeu SB 1100011 111 63/7 jalr I 1100111 000 67/0	srl	R	0110011	101	0000000	33/5/00
and lui R 0110011 01011 111 0000000 33/7/00 37 beq SB 1100011 000 63/0 63/0 63/1 bne SB 1100011 001 63/1 63/1 blt SB 1100011 100 63/4 bge SB 1100011 101 63/5 bltu SB 1100011 110 63/6 bgeu SB 1100011 111 63/7 jalr I 1100111 000 67/0	sra	R	0110011	101	0100000	33/5/20
lui U 0110111 37 beq SB 1100011 000 63/0 bne SB 1100011 001 63/1 blt SB 1100011 100 63/4 bge SB 1100011 101 63/5 bltu SB 1100011 110 63/6 bgeu SB 1100011 111 63/7 jalr I 1100111 000 67/0	or	R	0110011	110	0000000	33/6/00
beq SB 1100011 000 63/0 bne SB 1100011 001 63/1 blt SB 1100011 100 63/4 bge SB 1100011 101 63/5 bltu SB 1100011 110 63/6 bgeu SB 1100011 111 63/7 jalr I 1100111 000 67/0	and	R	0110011	111	0000000	33/7/00
bne SB 1100011 001 63/1 blt SB 1100011 100 63/4 bge SB 1100011 101 63/5 bltu SB 1100011 110 63/6 bgeu SB 1100011 111 63/7 jalr I 1100111 000 67/0	lui	U	0110111			37
bne SB 1100011 001 63/1 blt SB 1100011 100 63/4 bge SB 1100011 101 63/5 bltu SB 1100011 110 63/6 bgeu SB 1100011 111 63/7 jalr I 1100111 000 67/0	bea	SB	1100011	000		63/0
blt SB 1100011 100 63/4 bge SB 1100011 101 63/5 bltu SB 1100011 110 63/6 bgeu SB 1100011 111 63/7 jalr I 1100111 000 67/0						
bge SB 1100011 101 63/5 bltu SB 1100011 110 63/6 bgeu SB 1100011 111 63/7 jalr I 1100111 000 67/0						
bltu SB 1100011 110 63/6 bgeu SB 1100011 111 63/7 jalr I 1100111 000 67/0						
bgeu SB 1100011 111 63/7 jalr I 1100111 000 67/0						
jalr I 1100111 000 67/0						
	jal	ÚJ	1101111	00F0F0F0		6F

REGISTER NAME, USE, CALLING CONVENTION

/A
(4)
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			_
REGISTER	NAME	USE	SAVER
x0	zero	The constant value 0	N.A.
x1	ra	Return address	Caller
x2	sp	Stack pointer	Callee
x 3	gp	Global pointer	
x4	tp	Thread pointer	22
x5-x7	t0-t2	Temporaries	Caller
x8	s0/fp	Saved register/Frame pointer	Callee
x9	s1	Saved register	Callee
x10-x11	a0-a1	Function arguments/Return values	Caller
x12-x17	a2-a7	Function arguments	Caller
x18-x27	s2-s11	Saved registers	Callee
x28-x31	t3-t6	Temporaries	Caller
f0-f7	ft0-ft7	FP Temporaries	Caller
f8-f9	fs0-fs1	FP Saved registers	Callee
f10-f11	fa0-fa1	FP Function arguments/Return values	Caller
f12-f17	fa2-fa7	FP Function arguments	Caller
f18-f27	fs2-fs11	FP Saved registers	Callee
f28-f31	ft8-ft11	R[rd] = R[rs1] + R[rs2]	Caller