

Given a cache hierarchy with 8 words with a cache access time of 5 ns and a memory access time of 50ns, and the following set of memory accesses representing the tag and index: 22, 28, 31, 22, 16, 13, 31, 8, 5, 13, 8, and 5.

- a) If the cache is a direct-mapped cache, show the sequence for accessing the cache and calculate the total access time. Draw the final cache table
- b) If the cache is a 2-way set associative cache, show the sequence for accessing the cache and calculate the total access time.
- c) Determine which cache has the better performance and by how much.

22= 10110 28=11100 31= 11111 16= 10000 13= 01101 8=01000 5=00101

Direct	+	3×50s+9	x (2+20) = 210m
Index	\/	Tag	Memory
000	1 KY	10701	m(1638)
001	N	and the state of t	
014	1/4		
011	N		
100.	NM	1)	m (28)
109.	MY	61-100-101-100	m(13>5013+5)
110	MY	10	m(sz)
(()	172	l N	m(31)

2 (min), 13 (min), 31 (min), 28 (HH), 16 (min), 13 (min), 31 (Hil), 8 (min), 28 (min),

Index	V	Tag	Memors	Y	Tag	Memory
00	7	11131003010	M(23-016-28	Y	111-> 100	M(20->/6
01	5	1001110110110	M(13+5+13-)T	7	1106 1006110	m(13-)5-113
10	Y	101	M(21"	N		1,73
1 (1)	14	And the state of t	m(31	IN		

27 (Miss), 78 (Miss), 31 (Miss), 22 (Hit), 16 (Miss), 18 (Miss), 31 (Hit), 8 (Miss), 5 (Miss)

Average Memory Access Time

Given a Level-1 cache with a hit rate of 95%, a cache access time of 5 ns, and a memory access time of 100ns, find the average memory access time

The processor in the Example is given a L2 cache with a hit rate of 85%, and a cache access time of 7ns. Find the average memory access time

$$0.05$$
 30.0 0.05 $(50.2 \times 10.2 \times 10.6)$ $(7474106)) $= 6.1 \times 10$ $= 6.1 \times 10$$

The processor in the Example is given a L3 cache with a hit rate of 80%, and a cache access time of 10ns. Find the average memory access time