

1. Given the following RISC-V Code and the following set of latencies with dependencies, and a branch delay slot of 1 cycle

Type	Instruction producing result	Instruction using result	Stalls
1	FP ALU operation	Another FP Operation	3
2	FP ALU operation	Store double	2
3	Load double	FP ALU operation	1
4	Load double	Store double	1
5	Integer operation	Integer operation	1

Loop:

```
LD    F0, 0(R1)
ADDD  F4, F0, F2
SD    0(R1), F4
ADDI  R1, R1, -8
BNEZ  R1, Loop
NOP   ;delayed branch slot
```

First, determine the stalls require to implement the code. Then, perform out-of-order execution to improve the run time.

Show the execution of a single issue Tomasulo algorithm in the form of status tables for the above code sequence for one iterations of the above loop.

Assume the following

- There are 1 FP ADD/SUB unit, 1 FP MULT units, 2 load buffers and 2 store buffers
- FP ADD/SUB take 2 cycles, multiplication takes 10 cycles, divides take 40 cycles and load/stores take 2 cycles for execution
- Function units are not pipelined and there is no forwarding between function units; results are communicated by the CDB
- If two instructions complete at the same time one of them will wait to write result on CDB

[illegible]

Consider the following RISC-V code

LD	F2,	0(R1)	
MULTD	F4,	F0,	F2
SD	F4,	0(R1)	
SUBI	R1,	R1,	#8
BNE	R1,	R0,	Loop

Show the execution of a single issue Tomasulo algorithm in the form of status tables for the above code sequence for two iterations of the above loop.

Assume the following

- There are 1 FP ADD/SUB unit, 2 FP MULT units, 2 load buffers and 2 store buffers
- FP ADD/SUB take 2 cycles, multiplication takes 4 cycles, divides take 16 cycles and load/stores take 1 cycle for execution
- First load takes 8 clocks (L1 cache miss), all other lw/sw takes 1 clock (hit)
- Function units are not pipelined and there is no forwarding between function units; results are communicated by the CDB
- SUBI, BEQZ are integer instructions that each take 1 clock cycle to execute
- If two instructions complete at the same time one of them will wait to write result on CDB

[illegible]