Assume that three I/O devices are connected to a 32-bit, 10 MIPS CPU. The first device is a floppy drive with a transfer rate of 25KB/sec over a 16-bit bus. The second device is a keyboard that must be polled thirty times per second. The third device is a hard drive with a maximum transfer rate of 1MB/sec. It has a 32-bit bus. Assuming that the polling operation requires 20 instructions for each I/O device, determine the percentage of CPU time required to poll each device.

Consider the following code segment, with the values MAX = 10^6 and WSIZE = 5 and the following data:

- Read from x and w takes 20 cycles
- t+= takes 5 cycles
- Write to y takes 10 cycles
- Each i++ and j++ take 5 cycles
- Each comparison takes 5 cycles
- Write to a register takes 1 cycle.
- L1 cache hits require 5 cycles
- Cache miss penalty is 10 cycles

```
for( i = 0; i < MAX; ++i ){
        t = 0;
        for( j = 0; j < WSIZE; ++j ){
                t += x[i+j]*w[j];
                y[i] = t;
        }
}
```

a) Without any modifications, how many cycles does the code segment take?

b) Discuss the opportunities for reduction of cycle times and determine the improvement in performance when implemented in SIMD with 8 processors.

Given the following RISC-V Code and the following set of latencies with dependencies, and a branch delay slot of 1 cycle

Type	Instruction producing result	Instruction using result	Stalls
1	FP ALU operation	Another FP Operation	3
2	FP ALU operation	Store double	2
3	Load double	FP ALU operation	1
4	Load double	Store double	1
5	Integer operation	Integer operation	1

```
Loop:
        LD    F0, 0(R1)
        ADDD  F4,F0,F2
        SD    0(R1), F4
        ADDI  R1,R1,-8
        BNEZ  R1,Loop
        NOP   ;delayed branch slot
```

First, determine the stalls require to implement the code. Then, perform out-or-order execution to improve the run time.