Given the following parameters for memory

- L1 cache hit = 1 clock cycles, hit 95% of accesses
- L2 cache hit = 10 clock cycles, hit 60% of L1 misses
- DRAM = 200 clock cycles (≈100 nanoseconds)
- Disk = 20,000,000 clock cycles (≈10 milliseconds)

a) Derive the Average Memory Access Time without paging

b) Derive the Average Memory Access Time with paging for a Memory Hit Rate of 99%?

c) Derive the Average Memory Access Time with paging for a Memory Hit Rate of 99.9999%?

What percentage of time will a 20 MIPS processor spend in the busy wait loop of an 80-character line printer when it takes 1 msec to print a character and a total of 565 instructions need to be executed to print an 80 character line. Assume that two instructions are executed in the polling loop.

Consider a 20 MIPS processor with several input devices attached to it, each running at 1000 characters per second. Assume that it takes 17 instructions to handle an interrupt. If the hardware interrupt response takes 1μsec, what is the maximum number of devices that can be handled simultaneously?