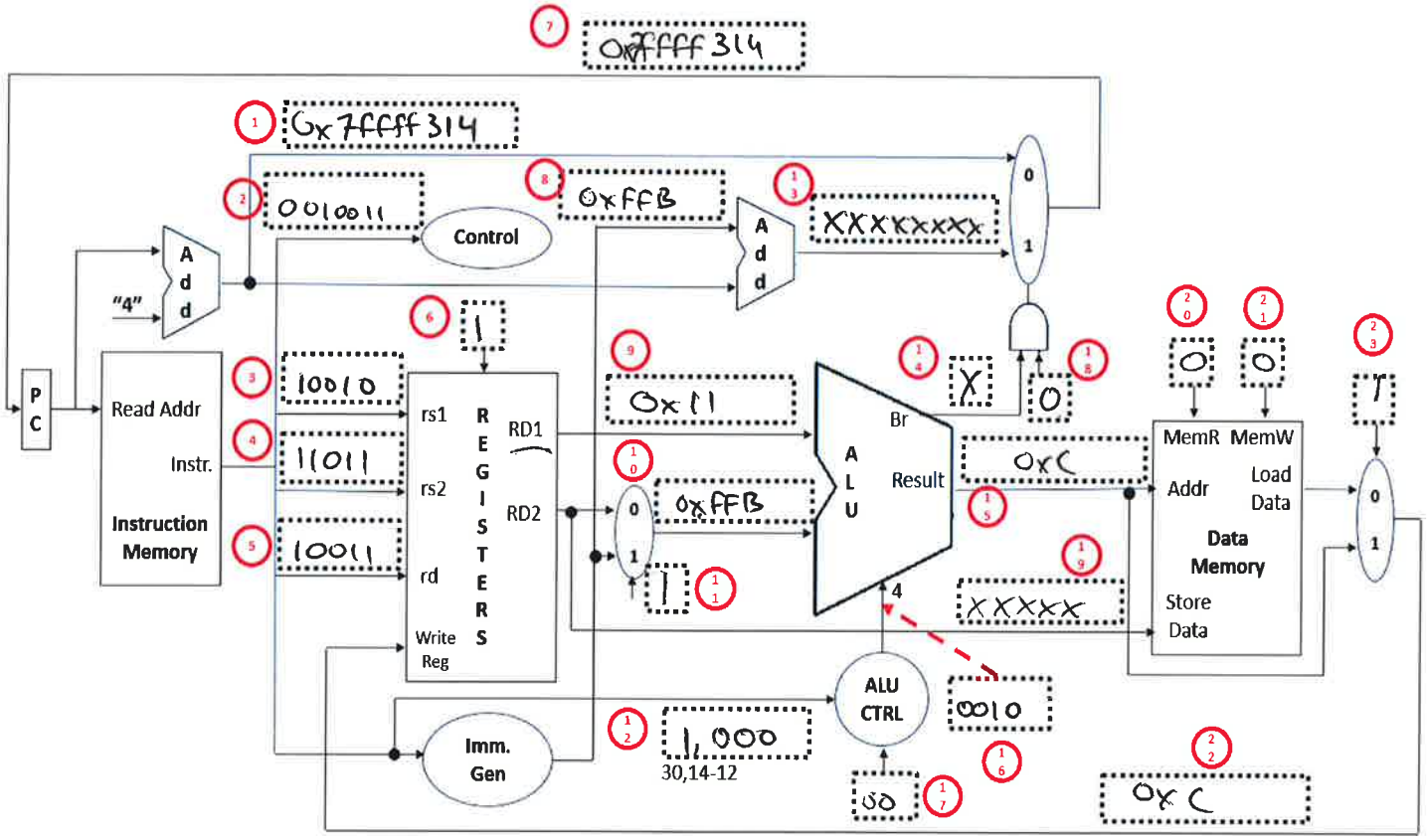
Given the following RISC-V instruction and register / data memory values, perform the following tasks. First, translate the given RISC-V instruction to its binary encoding. Second, show the propagation of signals through the reduced Single-Cycle datapath that calculate the result of the instruction. You are permitted and encouraged to refer to the RISC-V Green sheet while completing the problem. The values of the registers / memory are the values at the beginning of the instruction.

- PC: `0x7ffff310`
- Instruction: `addi x19, x18, -5`
- Register `x18` contains `0x00000011`
- Register `x19` contains `0x0000001A`

00101
11010
11011 → B

RISC-V Encoding: 0xFFB | 10010 | 000 | 10011 | 0010011



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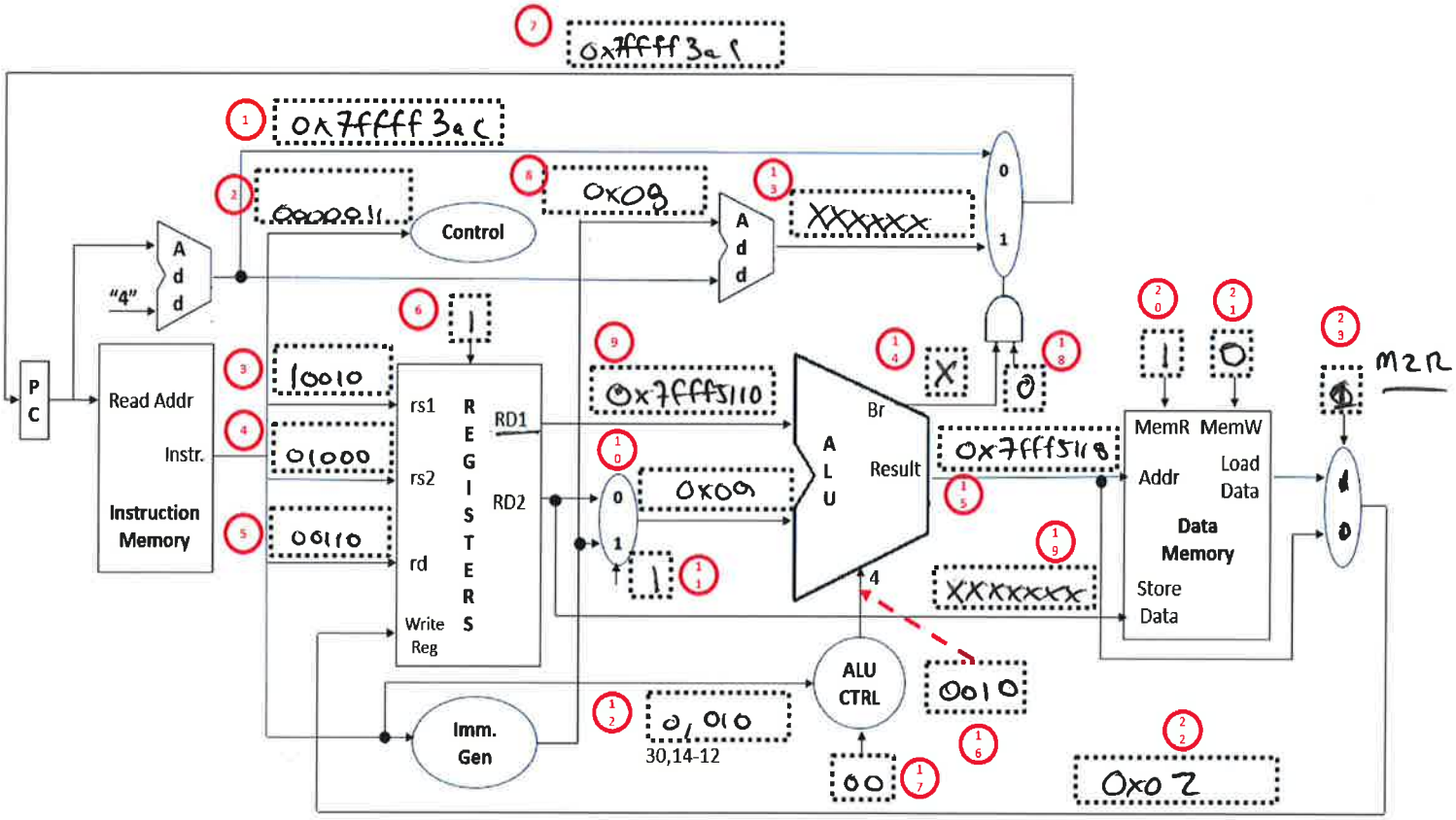
- PC: `0x7ffff3a8`
- Instruction: `lw x6, 8(x18)`
- Register `x18` contains `0x7fff5110`
- Register `x6` contains `0x0000001A`
- Data Memory at `0x7fff5110` contains `0x00000000`
- Data Memory at `0x7fff5114` contains `0x00000001`
- Data Memory at `0x7fff5118` contains `0x00000002`
- Data Memory at `0x7fff511c` contains `0x00000003`

RISC-V Encoding:

0x08	10010	010	00110	0000011



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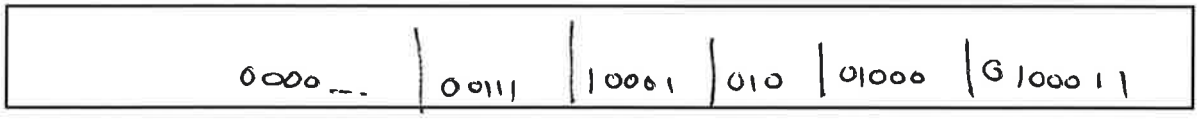
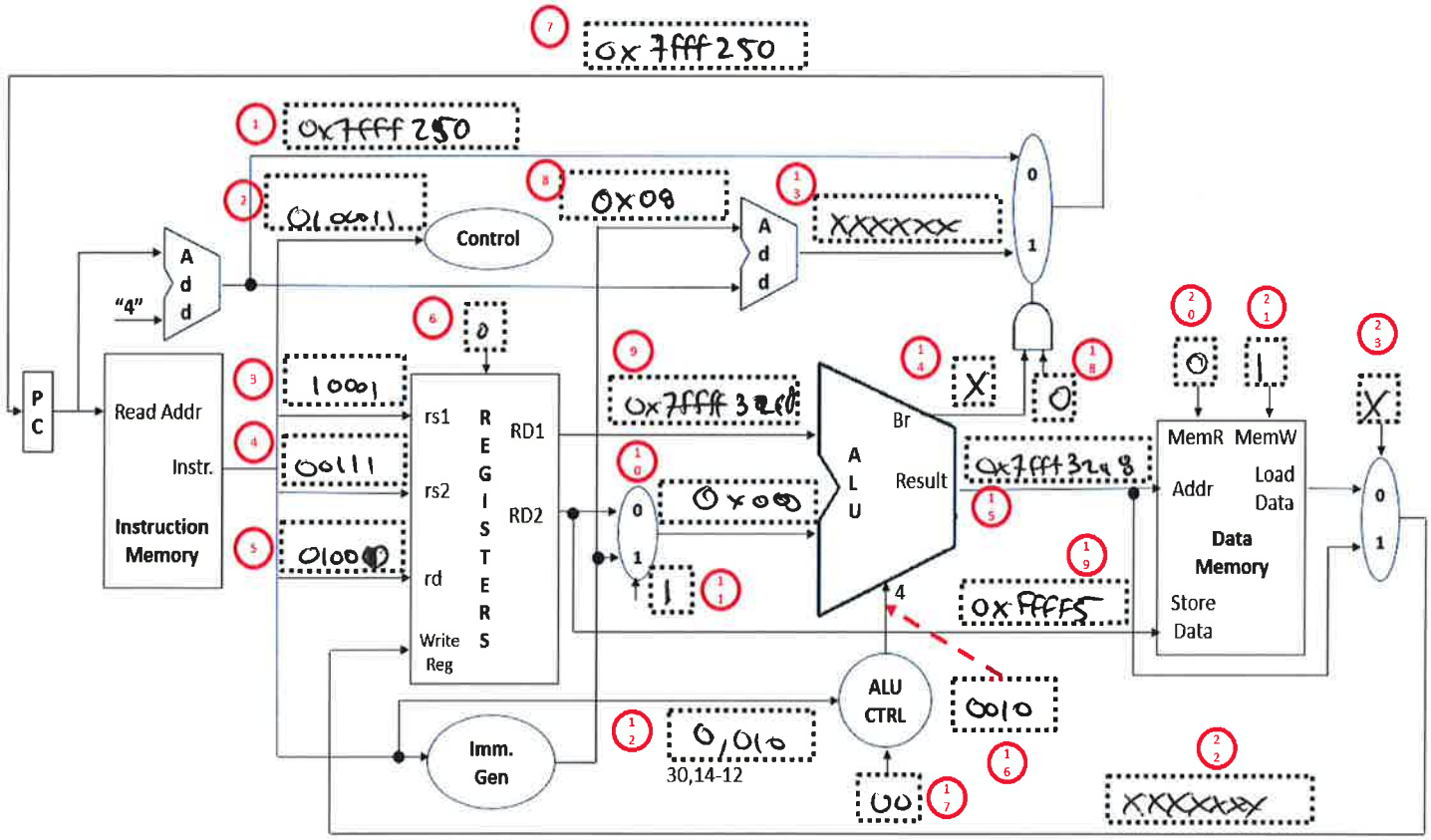
- PC: `0x7ffff24c`
- Instruction: `sw x7, 8(x17)`
- Register `x17` contains `0x7fff32a0`
- Register `x7` contains `0xFFFFFFF5`
- Data Memory at `0x7fff32a0` contains `0x00000000`
- Data Memory at `0x7fff32a4` contains `0x00000001`
- Data Memory at `0x7fff32a8` contains `0x00000002`
- Data Memory at `0x7fff32ac` contains `0x00000003`

RISC-V Encoding:





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- PC: `0x7ffff300`
- Instruction: `beq x21, x22, 24` → 11000
- Register `x21` contains `0x00000008`
- Register `x22` contains `0x00000008`

RISC-V Encoding:

0	000000	10110	10101	000	1100	0	1100011