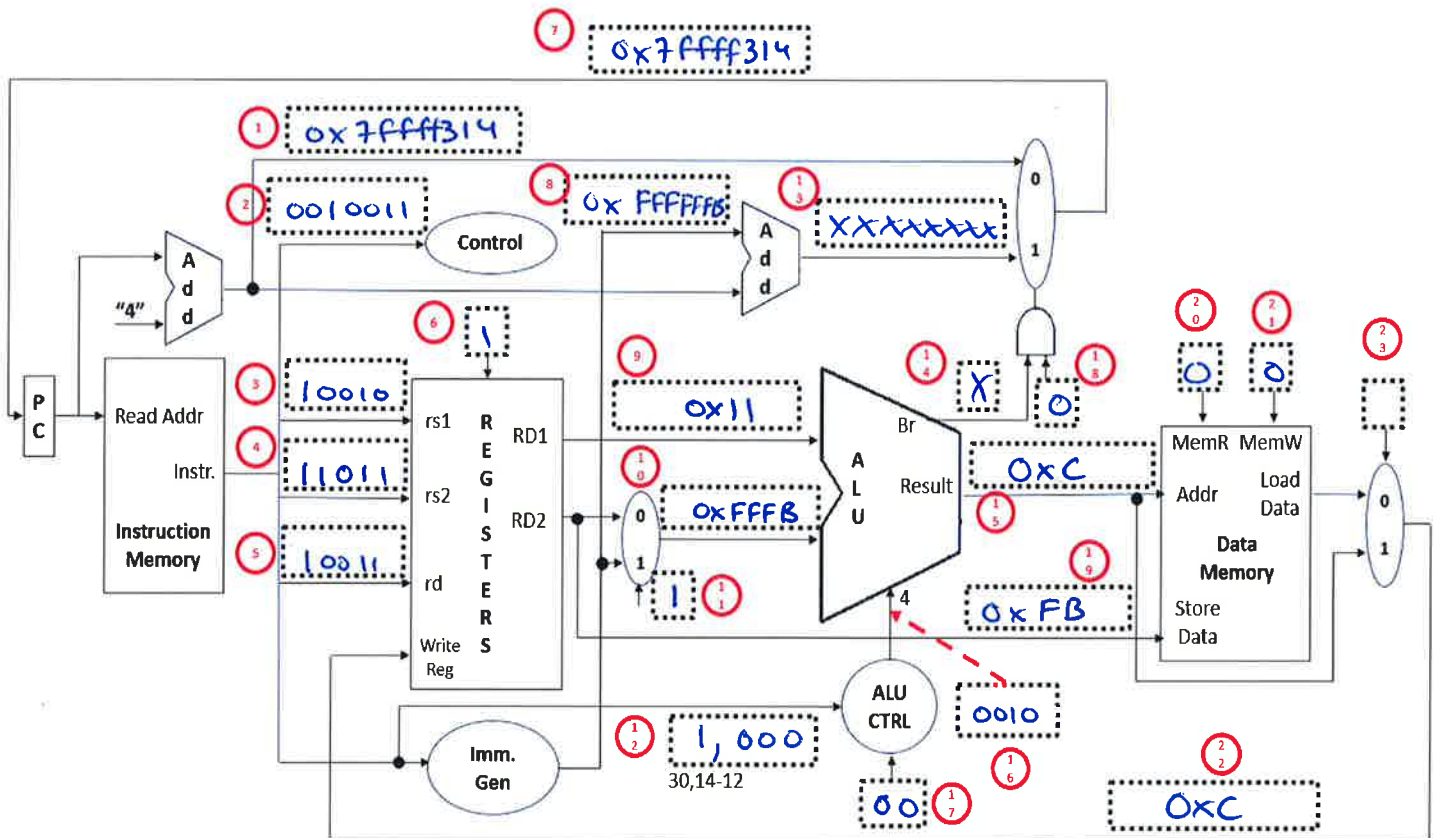Given the following RISC-V instruction and register / data memory values, perform the following tasks. First, translate the given RISC-V instruction to its binary encoding. Second, show the propagation of signals through the reduced Single-Cycle datapath that calculate the result of the instruction. You are permitted and encouraged to refer to the RISC-V Green sheet while completing the problem. The values of the registers / memory are the values at the beginning of the instruction.

- PC: 0x7ffff310
- Instruction: addi x19, x18, -5
- Register x18 contains 0x00000011
- Register x19 contains 0x0000001A

0 0101
1 1010
1 1011 → B

RISC-V Encoding:

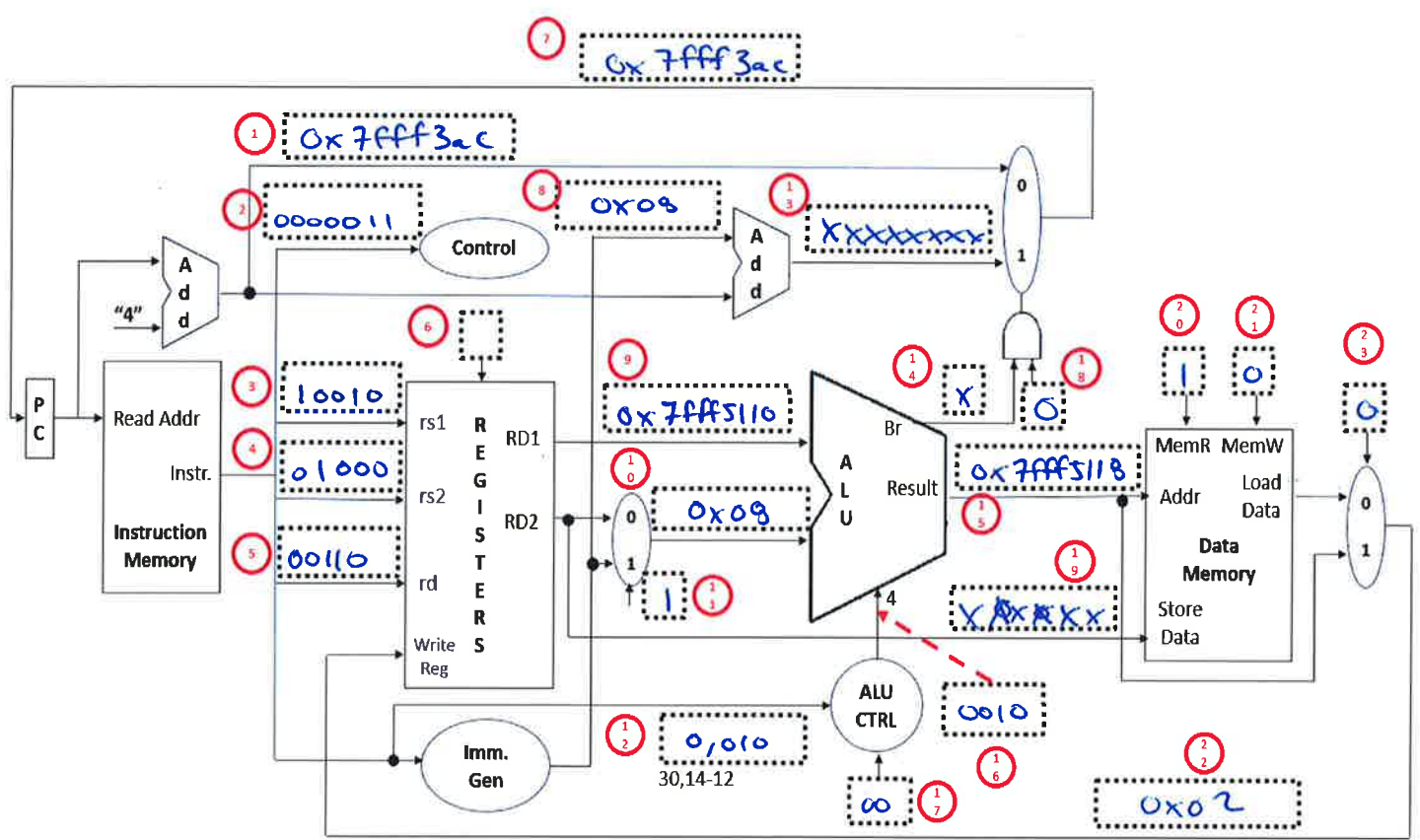1111 1111 1011 | 10010 | 000 | 10011 | 0010011 |

Given the following RISC-V instruction and register / data memory values, perform the following tasks. First, translate the given RISC-V instruction to its binary encoding. Second, show the propagation of signals through the reduced Single-Cycle datapath that calculate the result of the instruction. You are permitted and encouraged to refer to the RISC-V Green sheet while completing the problem. The values of the registers / memory are the values at the beginning of the instruction.

- PC: 0x7ffff3a8
- Instruction: lw x6, 8(x18)
- Register x18 contains 0x7fff5110
- Register x6 contains 0x0000001A
- Data Memory at 0x7fff5110 contains 0x00000000
- Data Memory at 0x7fff5114 contains 0x00000001
- Data Memory at 0x7fff5118 contains 0x00000002
- Data Memory at 0x7fff511c contains 0x00000003

RISC-V Encoding:

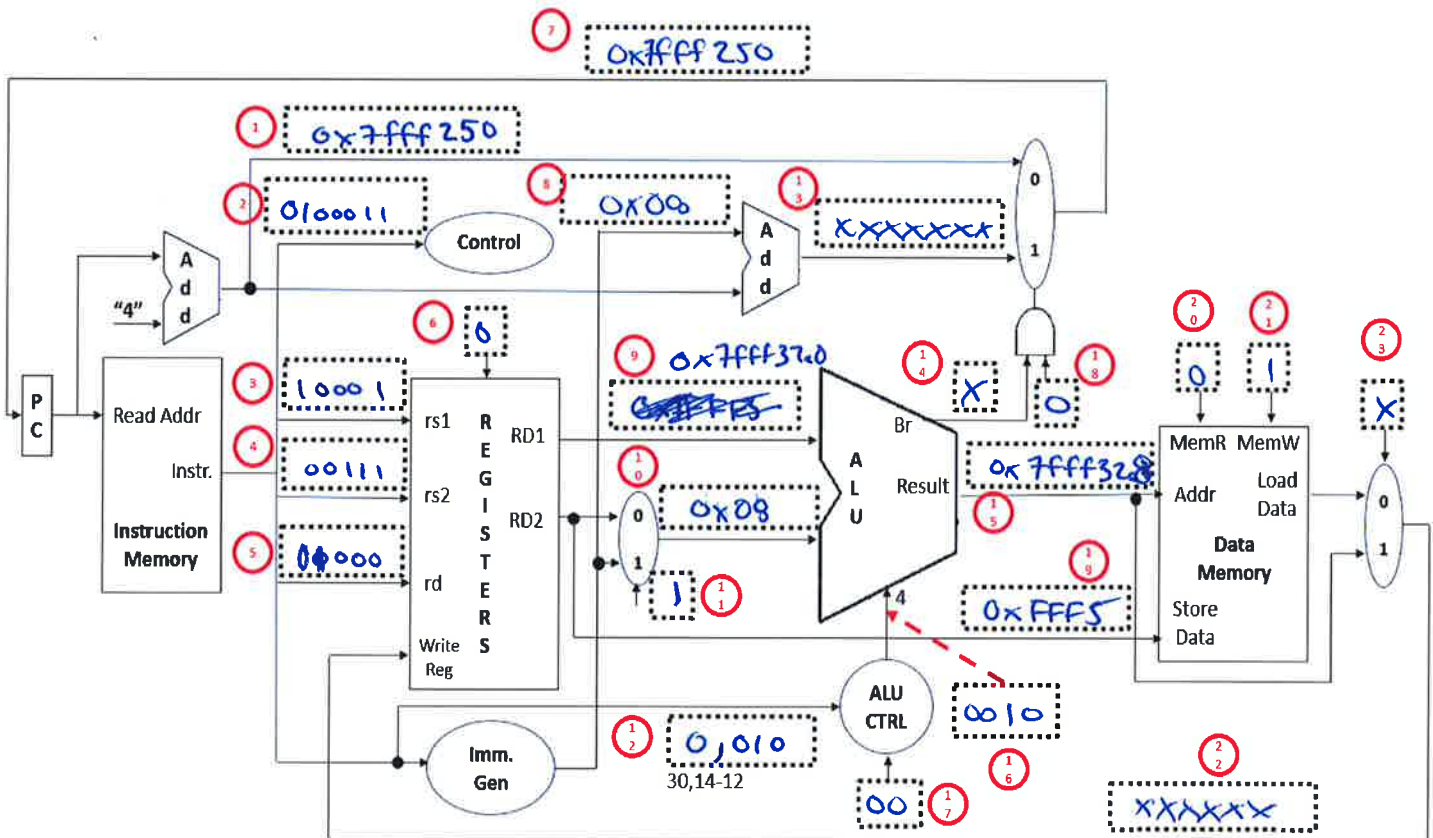000000001000 | 10010 | 010 | 00110 | 0000011

Given the following RISC-V instruction and register / data memory values, perform the following tasks. First, translate the given RISC-V instruction to its binary encoding. Second, show the propagation of signals through the reduced Single-Cycle datapath that calculate the result of the instruction. You are permitted and encouraged to refer to the RISC-V Green sheet while completing the problem. The values of the registers / memory are the values at the beginning of the instruction.

- PC: 0x7ffff24c
- Instruction: sw x7, 8(x17)
- Register x17 contains 0x7fff32a0
- Register x7 contains 0xFFFFFFF5
- Data Memory at 0x7fff32a0 contains 0x00000000
- Data Memory at 0x7fff32a4 contains 0x00000001
- Data Memory at 0x7fff32a8 contains 0x00000002
- Data Memory at 0x7fff32ac contains 0x00000003

1000

RISC-V Encoding:

| 0000000 | 00111 | 10001 | 010 | 1000 | 0100011 |

Given the following RISC-V instruction and register / data memory values, perform the following tasks. First, translate the given RISC-V instruction to its binary encoding. Second, show the propagation of signals through the reduced Single-Cycle datapath that calculate the result of the instruction. You are permitted and encouraged to refer to the RISC-V Green sheet while completing the problem. The values of the registers / memory are the values at the beginning of the instruction.

- PC: 0x7ffff300
- Instruction: beq x21, x22, 24
- Register x21 contains 0x00000008
- Register x22 contains 0x00000008

1100⊄ ⟹ 1100

RISC-V Encoding:

| 0‾000000 | 10110 | 10101 | 000 | 1100‾0 | 11 000 11 |
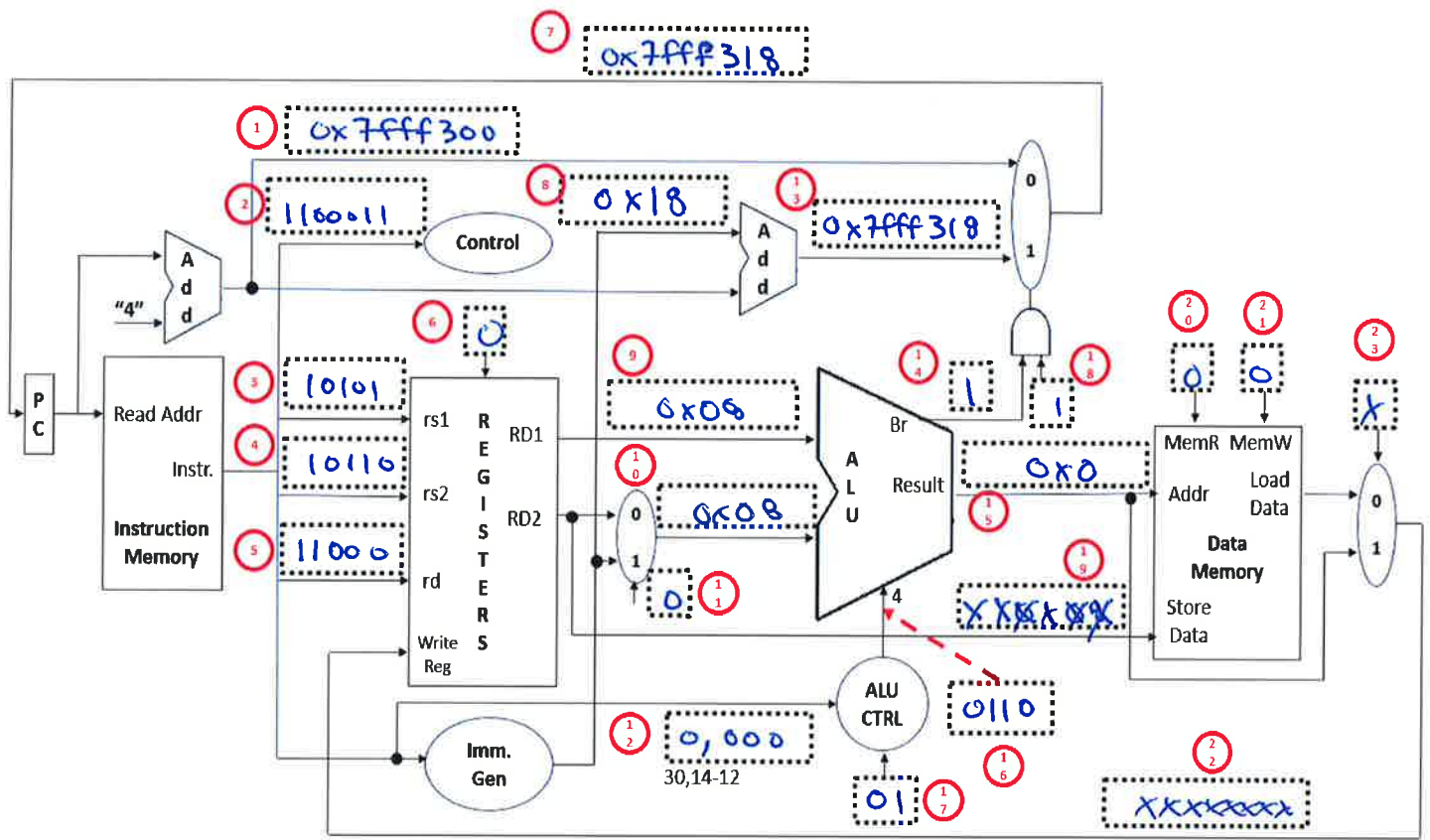
Given the following RISC-V instruction and register / data memory values, show the propagation of signals through the reduced Single-Cycle datapath that calculate the result of the instruction. You are permitted and encouraged to refer to the RISC-V Green sheet while completing the problem.

- PC: 0x7ffff200
- Instruction: bne x21, x22, 48
- Register x21 contains 0x0000001c
- Register x22 contains 0x0000001c

1 1 0 0 0 0

RISC-V Encoding:

0 | 000001 | 10110 | 10101 | 001 | 1000 1 0 | 1100011

⑦ 0x7fff 204

① 0x7fff 204

② 1 1000 11

⑧ 0x~~3002~~ 30

⑬ 0x7fff 30

Control

A d d

A d d

"4"

⑥ 0

③ 10101

④ 10110

⑤ 1000 0

P C

Read Addr

Instr.

Instruction Memory

rs1

rs2

rd

Write Reg

R E G I S T E R S

RD1

RD2

Imm. Gen

30,14-12

⑨ 0x1C

⑩ 0x1C

⑪ 0

⑫ 0 1001

Br

A L U

Result

ALU CTRL

⑭ 0

⑱ 1

⑮ 0x0

⑯ 0110

⑰ 0 1

⑲ 0x0

MemR MemW

Addr

Data Memory

Store Data

Load Data

②⓪ 0

②① 0

②③ ✗

XXXXXXX

②② XXX XXXXX

0

1