Name: _____ ID: _____

Department of Computer Science and Engineering

CSE340: Computer Architecture

Spring 2013

Quiz-1

Full Marks:15 Time: 20 Mins

1. Define **ISA** and **ABI.** **2**

2. **Encode the MIPS instruction sub $16,$17,$18 and sw $16,40($17) also find their type.** **3**
   [sub= 000000 100010,sw=011011]

3. Write MIPS instruction for the expression **f=(g+h)-(i+j),** using minimum number of Register. **3**

4. What type instruction is **JAL**? How would you represent **JAL 513** in the register? What would be the value in **$ra/$31?** **3**

5. In general you can store **16-bit** constant in a register, but if you would need to store **27- bit** constant, how would you do this? Give an example. **4**

Name: _____ ID: _____

Department of Computer Science and Engineering

CSE340: Computer Architecture

Spring 2013

Quiz-1

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Name: _____ ID: _____

Department of Computer Science and Engineering

CSE340: Computer Architecture

Fall 2014

Quiz-1

Full Marks:15 Time: 20 Mins

1. Show that: $A \oplus (B \oplus C) = A \oplus (B\bar{C} + \bar{B}C)$. Using Boolean expression. **6**

2. Using T-FF design a counter that can count from decimal 0 to 10 in binary**.** **9**

Name: _____ ID: _____ Section: ____

Department of Computer Science and Engineering

CSE340: Computer Architecture

Fall 2015

Quiz-1, A

Full Marks: 15 Time: 20 Mins

1. Design a conditional shift register and explain its operation. **15**

Name: _____ ID: _____ Section: ____

Department of Computer Science and Engineering

CSE340: Computer Architecture

Fall 2015

Quiz-1, B

Full Marks: 15 Time: 20 Mins

1. Design a "Conditional Sum" adder and explain its operation. **15**

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Department of Computer Science and Engineering

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Fall 2015

Quiz-1, C

Full Marks: 15 Time: 20 Mins

1. Let's assume you have four inputs **A, B, C, D** and output **F**. **F** is high when decimal equivalent of the inputs are even. Simplify **F** using sum of product expression and draw the logic circuit. **15**

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Quiz-1, D

Full Marks: 15 Time: 20 Mins

1. Design a PLA for the expression given below: **15**

a. $f_1 = A.\bar{B} + \bar{A}.B.\bar{C}$

b. $f_2 = A.\bar{B} + A.B.C$

c. $f_3 = \bar{A}.B.\bar{C} + A.B.C$

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Quiz-1, E

Full Marks: 15 Time: 20 Mins

1. Let's assume you have four inputs **A, B, C, D** and output **F**. **F** is high when decimal equivalent of the inputs are odd. Simplify **F** using sum of product expression and draw the logic circuit. **15**

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Quiz-1

Full Marks:15 Time: 20 Mins

1. Define **compiler** and **assembler.** **2**

2. Encode the MIPS instruction **addi $16,$17, 18** and **lw $16,40($17)** also find their type**.** **3**

3. Write MIPS instruction for the expression **f=(g-h)+(i-j),** using minimum number of Register. **3**

4. What type instruction is **JAL**? What value does $**ra**/**$31** stores**?** **3**

5. Convert ***blt $s1,s2****, Exit* into equivalent MIPS code. [blt= branch if less than] **4**

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Quiz-1

Full Marks:15 Time: 20 Mins

1. Design a logic circuit that has four inputs and one output. Output will be HIGH (1) when majority of the inputs are High (1). **15**

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Spring 2015

Quiz-1

Full Marks:15 Time: 20 Mins

1. Design a ripple adder and explain its limitations. Design another adder that overcomes the limitations of a ripple adder. **15**

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Quiz-1

Full Marks:15 Time: 20 Mins

1. Why do you need a D-flip flop? Explain with an example. Design a shift register using D flip flop. **15**

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Quiz-1

Full Marks:15 Time: 20 Mins

1. Consider the function $Y = (A.B) + \overline{(A.C)}.\overline{B}$, draw a combinational logic circuit that implements this function. Also draw the Truth table for this function. **6**

2. Design and explain operation of a circuit built with D flip-flop that can implement left shift, right shift and data store operation. The circuit should also have the provision to clear all flip-flop when required**.** **6**

3. Design an ALU with logical gates. **3**

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Summer 2015

Quiz-1

Full Marks:15 Time: 20 Mins

1. Simplify the Boolean expression and draw logic circuit:

$z = A'BCD + AB'C'D' + AB'CD' + AB'CD + ABC'D' + ABC'D + ABCD' + ABCD$. **15**

Name: _____ ID: _____

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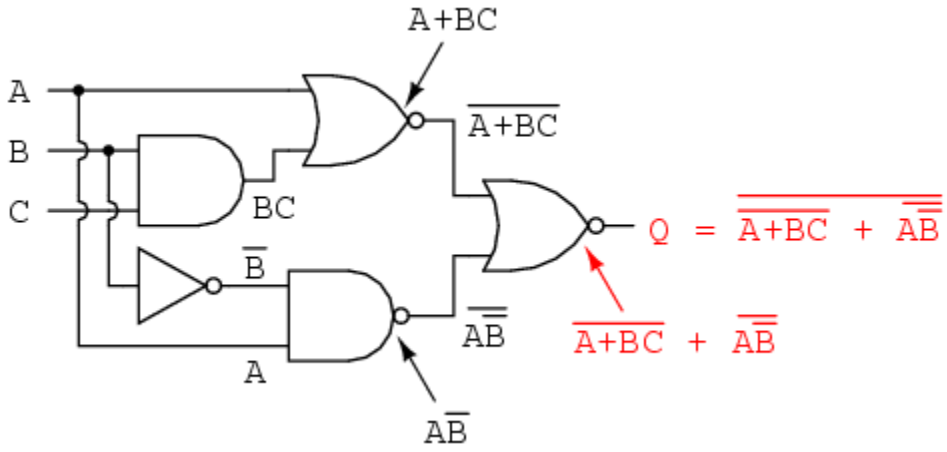
CSE340: Computer Architecture
Summer 2015
Quiz-1
Full Marks:15 Time: 20 Mins

1. Simplify the below circuit and draw the simplified circuit: **15**



Name: _____ ID: _____

Department of Computer Science and Engineering

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Summer 2015

Quiz-1

Full Marks:15 Time: 20 Mins

1. Draw and explain the operation of a counter that can count clock cycle from 0~13 having a falling edge triggered clock and using a T FF. **15**

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Department of Computer Science and Engineering

CSE340: Computer Architecture

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Quiz-1

Full Marks:15 Time: 20 Mins

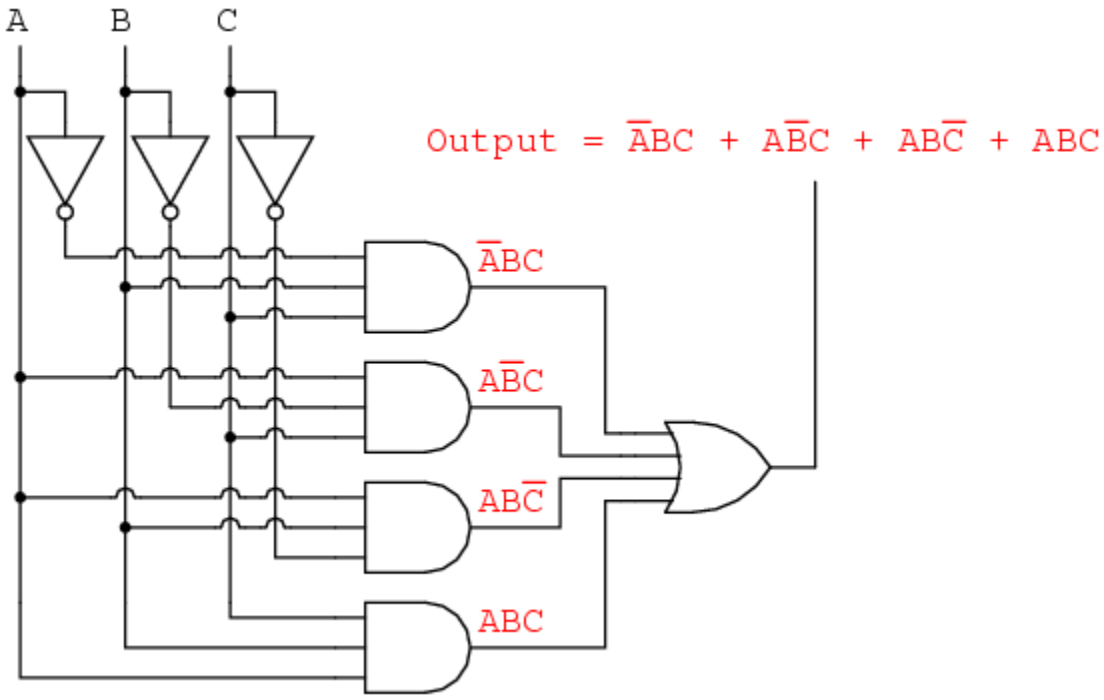
1. Simplify the Boolean expression and draw logic circuit: **15**

$$z = \bar{A}\,C(A + \bar{B} + \overline{D}) + \bar{A}\,B\bar{C}\,\overline{D} + A\bar{B}\,C$$

Name: _____ ID: _____

Department of Computer Science and Engineering
CSE340: Computer Architecture
Summer 2015
Quiz-1
Full Marks:15 Time: 20 Mins

1. Simplify the below circuit and draw the simplified circuit: **15**



Name: _____ ID: _____

Department of Computer Science and Engineering

CSE340: Computer Architecture

Summer 2015

Quiz-1

Full Marks:15 Time: 20 Mins

1. Design a hardware that can execute shift left, shift right, store new data and clear all stored data operation using D FF. Also explain its operation. **15**

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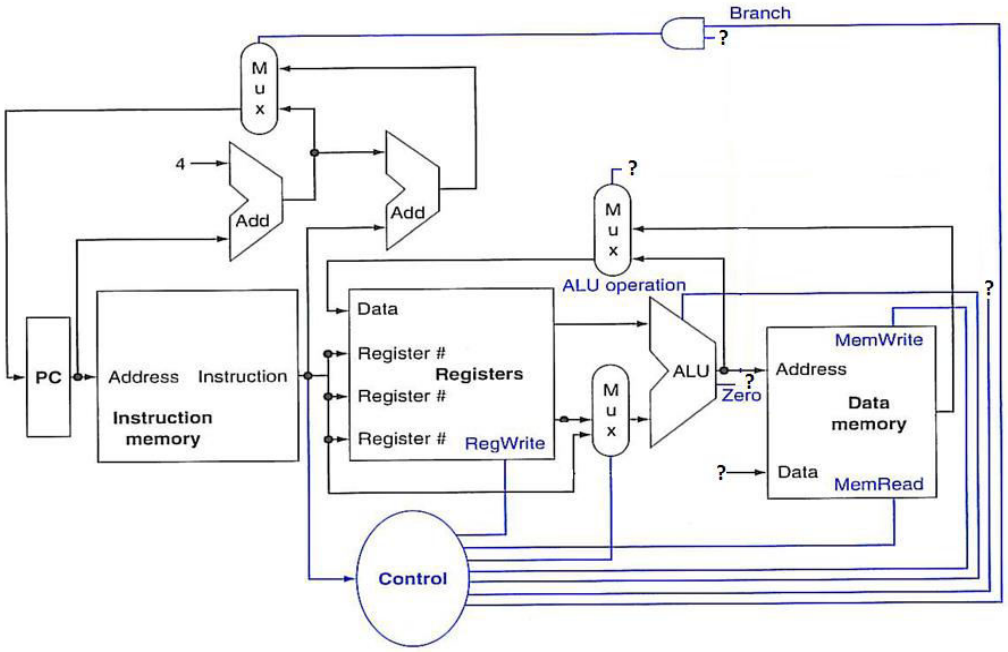
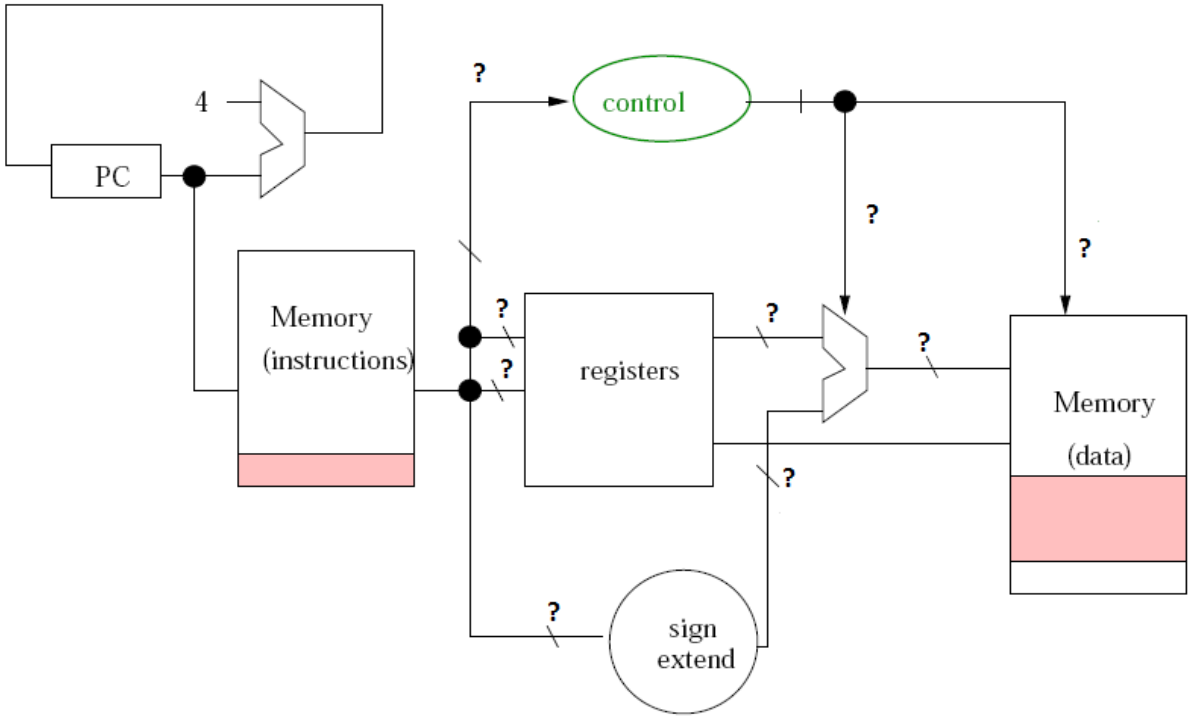
Fall 2013
Quiz-2
Full Marks: 15 Time: 25 Mins

1. Draw the missing links? **3**

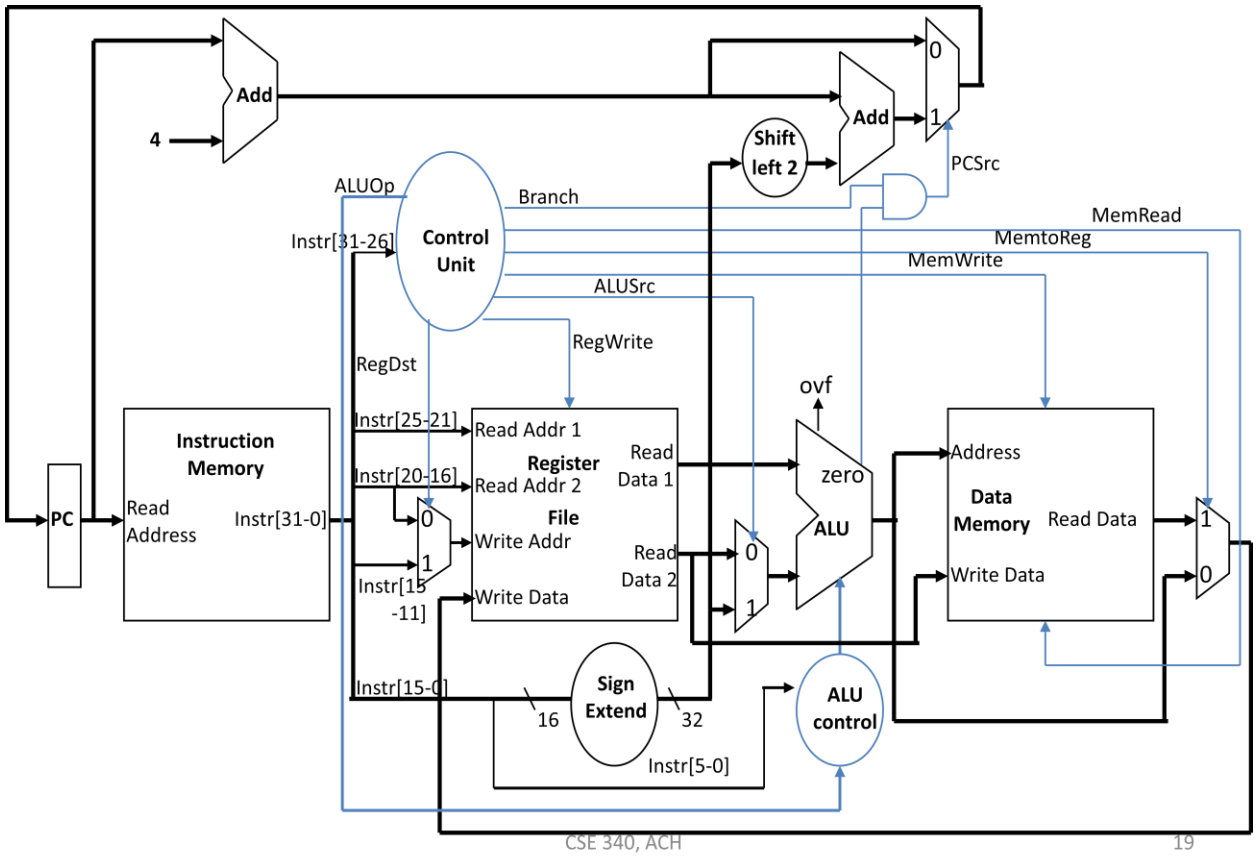


2. What are the advantages and disadvantages of single cycle data path implementation? **3**

3. Following figure shows the datapath for **sw** instruction, label the figure where marked "**?**". **5**



4. For executing lw $16,40($17), circle the appropriate MUX output in the below datapath. 4



Name: _____ ID: _____

Department of Computer Science and Engineering

CSE340: Computer Architecture

Summer 2013

Quiz-2

Full Marks: 15 Time: 25 Mins

1. What do you mean by zero and sign extended? **2**

2. Use Booth's algorithm to multiply **5** by **-3**. **4**

3. **1 00000111 10000000000000000000000** convert this to decimal value using **IEEE754 32-bit** floating point representation. **3**

4. Write Show the **IEEE 754** binary representation of the floating point number **-5/6.** **3**

5. Write Show the **IEEE 754** binary representation of the floating point number **-11.7**. **3**

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Department of Computer Science and Engineering

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Fall 2014

Quiz-2

Full Marks:15 Time: 30 Mins

1. What are the purpose of PC and $sp**.** **2**

2. Encode the MIPS instruction **addi $16,$17, 18** and **lw $16,40($17)** also find their type**.** **3**

3. Write MIPS instruction for the expression **if (i<=10) f=g+h,** using minimum number of Register. **3**

4. Describe how JUMP address is calculated with figure. **4**

5. Convert ***bgt $s1,$s2,*** *Exit* into equivalent MIPS code. [blt= branch if less than] **3**

Name: _____ ID: _____ Section: ____

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CSE340: Computer Architecture

Fall 2015

Quiz-2, A

Full Marks: 15 Time: 20 Mins

1. Define memory hierarchy with diagram. **5**

2. Write MIPS code for the following C code: if (A[5]==10) f=g[6]+C; else f=g[5]+C; 10

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Fall 2015

Quiz-2, B

Full Marks: 15 Time: 20 Mins

1. Draw the diagram of Harvard and Von Neumann Model of computer. **5**

2. Write MIPS code for the following C code: if (A[6]==B) f=g[6]*C; else f=g[5]*C; **10**

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Quiz-2, C

Full Marks: 15 Time: 20 Mins

1. Design a register file having 64 registers with 32-bit each. **5**

2. Write MIPS code for the following C code: if (A[6]==B[5]) f=g[6]-C; else f=g[5]-C;

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Quiz-2, D

Full Marks: 15 Time: 20 Mins

1. Define Multiprocessor system with diagram. **5**

2. Write MIPS code for the following C code: if (A[6]==B[5]) f=g[6]+C; else f=g[5]+C; 10

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Quiz-2, E

Full Marks: 15 Time: 20 Mins

1. Define big endian and little endian addressing with example. **5**

2. Write MIPS code for the following C code: if (A[3]==B[4]) f=g[6]*C; else f=g[5]+C; 10

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Quiz-2

Full Marks: 15 Time: 25 Mins

1. What do you mean by zero and sign extended? **2**

2. **1 00001111 10101000000000000000000** convert this to decimal value using **IEEE754 32-bit** floating point representation. **3**

3. Write Show the **IEEE 754** binary representation of the floating point number **-11.1** using eight bit register have one bit for sign, three bits for exponent and four bits for fraction part. **5**

4. Add $\mathbf{0.5_{ten}}$ and $\mathbf{-0.4365_{ten}}$ IEEE 754 floating point addition. **5**

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Quiz-2

Full Marks: 15 Time: 20 Mins

1. What do you mean by zero and sign extended? **2**

2. Write MIPS instruction for the expression **f=(g*h)+(i*j),** using minimum number of registers. **5**

3. Convert ***bgt $s1,s2****, Exit* into equivalent MIPS code. [bgt= branch if greater than] **3**

4. Encode the following also mention their types: **5**

a. srl $t1,$t2,8.

b. slt $t1,$t2,$t3.

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Department of Computer Science and Engineering
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Quiz-2
Full Marks: 15 Time: 25 Mins

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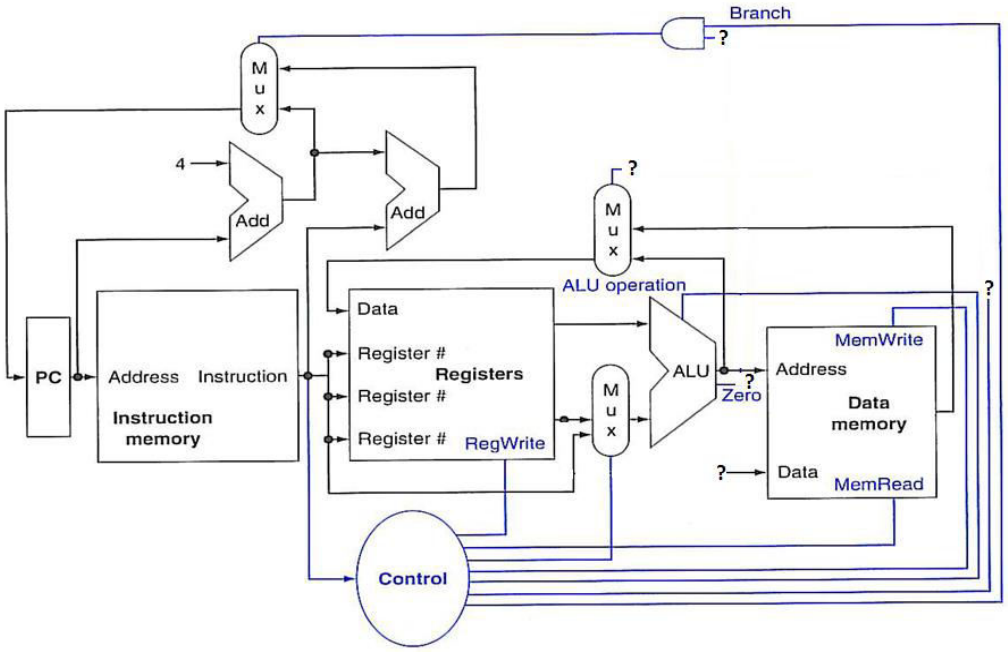

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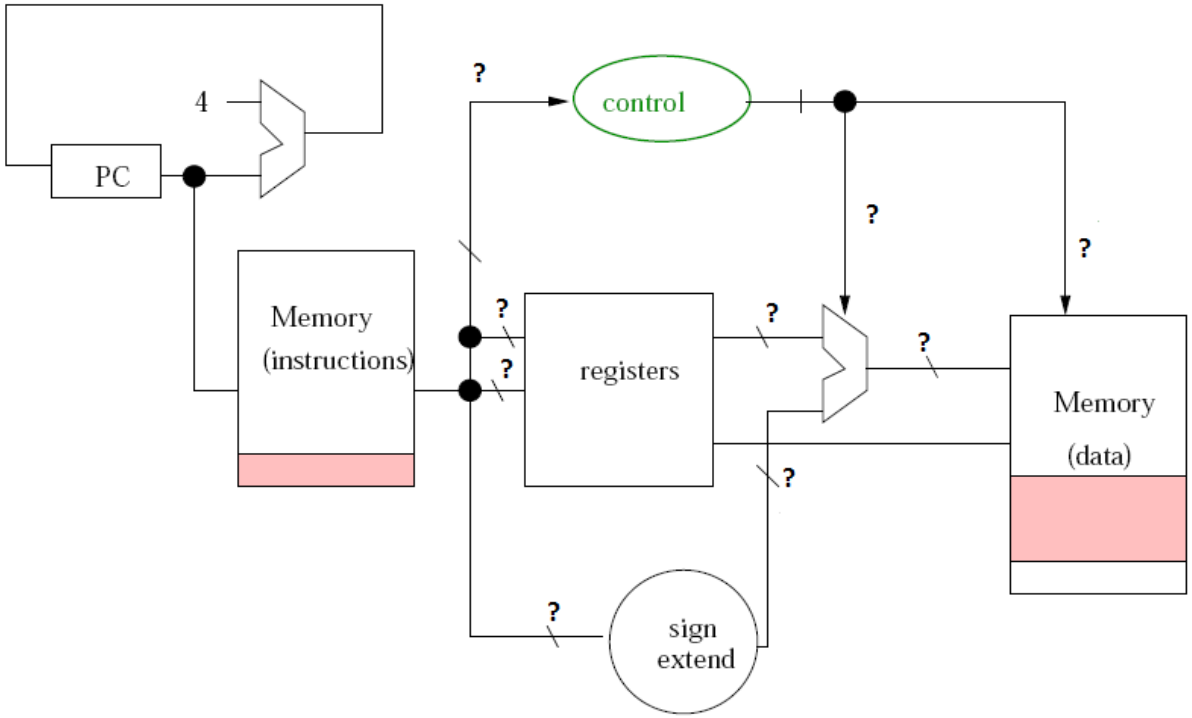

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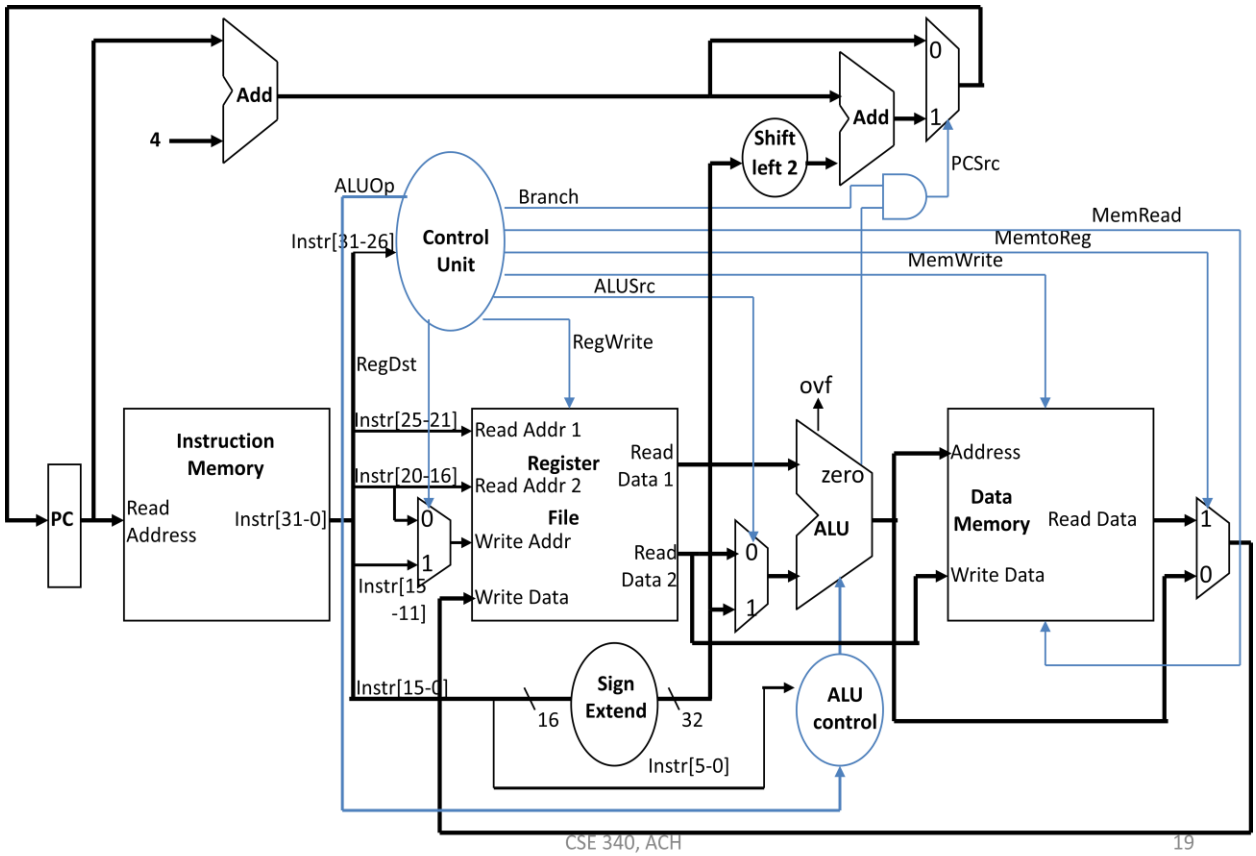

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Quiz-2

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Department of Computer Science and Engineering

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Quiz-2, A

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Name: _____ ID: _____ Section: ____

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Fall 2015

Quiz-2, C

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Name: _____ ID: _____ Section: ____

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Fall 2015

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Fall 2015

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Name: _____ ID: _____

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CSE340: Computer Architecture

Spring 2014

Quiz-2

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