



4. Describe how JUMP address is calculated with figure.

4

5. Convert *bgt \$s1,\$s2, Exit* into equivalent MIPS code. [blt= branch if less than]

3



4. Add  $0.5_{\text{ten}}$  and  $-0.4365_{\text{ten}}$  IEEE 754 floating point addition.

5

**Name:** \_\_\_\_\_

**ID:** \_\_\_\_\_

**Department of Computer Science and Engineering**

# CSE340: Computer Architecture

## Spring 2015

## Quiz-2

**Full Marks: 15 Time: 20 Mins**

1. What do you mean by zero and sign extended? **2**
2. Write MIPS instruction for the expression  $f = (g * h) + (i * j)$ , using minimum number of registers. **5**
3. Convert *bgt \$s1, \$s2, Exit* into equivalent MIPS code. [bgt= branch if greater than] **3**

4. Encode the following also mention their types:

5

a. srl \$t1,\$t2,8.

b. slt \$t1,\$t2,\$t3.

**Name:** \_\_\_\_\_

ID: \_\_\_\_\_

**Department of Computer Science and Engineering**

# CSE340: Computer Architecture

## Summer 2014

## Quiz-2

**Full Marks:15 Time: 20 Mins**

1. Define **compiler** and **assembler**. **2**
2. Encode the MIPS instruction **subi \$16,\$17, 18** and **sw \$16,40(\$17)** also find their type. **3**
3. Write MIPS instruction for the expression **f=(g+h)-(i+j)**, using minimum number of Register. **3**

4. What type instruction is **JAL**? What value does **\$ra/\$31** stores?

**3**

5. Convert ***ble \$s1,\$s2, Exit*** into equivalent MIPS code. [ble= branch if less than or equal]

**4**



Name: \_\_\_\_\_

ID: \_\_\_\_\_

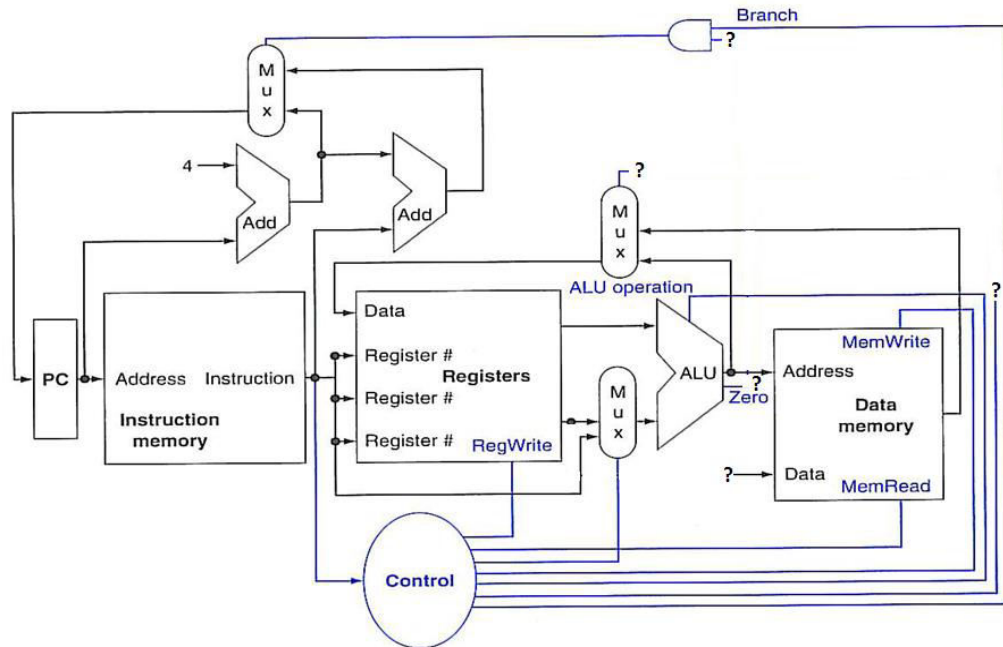
**Department of Computer Science and Engineering**  
**CSE340: Computer Architecture**  
**Summer 2013**

**Quiz-3**

**Full Marks: 15 Time: 25 Mins**

1. Draw the missing links?

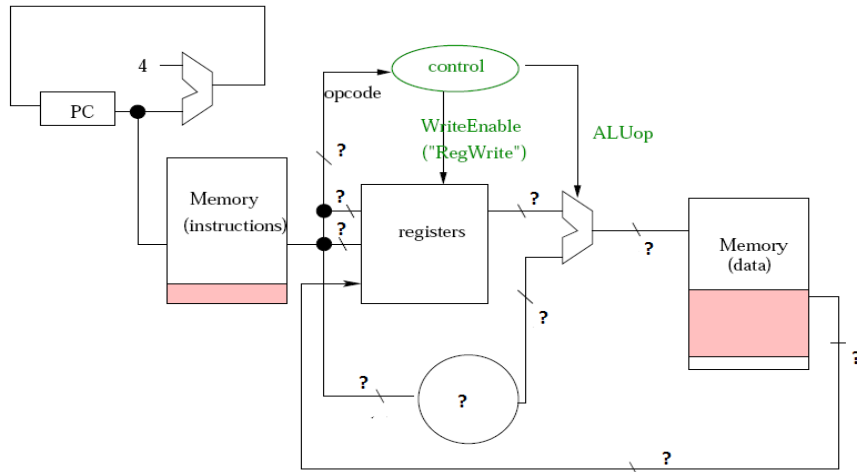
3



2. What do you mean by combinational elements and State elements?

2

3. Following figure shows the datapath for **lw** instruction, label the figure where marked “?”. **5**



4. How address of the next instruction is calculated in **Jump** instruction, explain with appropriate figure. **5**

Name: \_\_\_\_\_

ID: \_\_\_\_\_

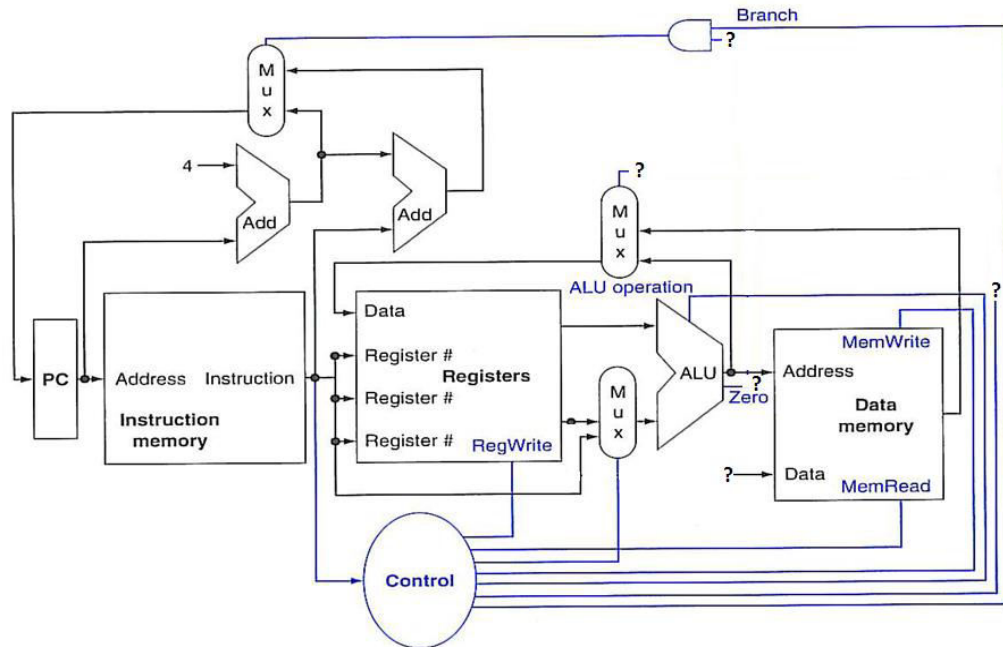
**Department of Computer Science and Engineering**  
**CSE340: Computer Architecture**  
**Summer 2013**

**Quiz-3**

**Full Marks: 15 Time: 25 Mins**

1. Draw the missing links?

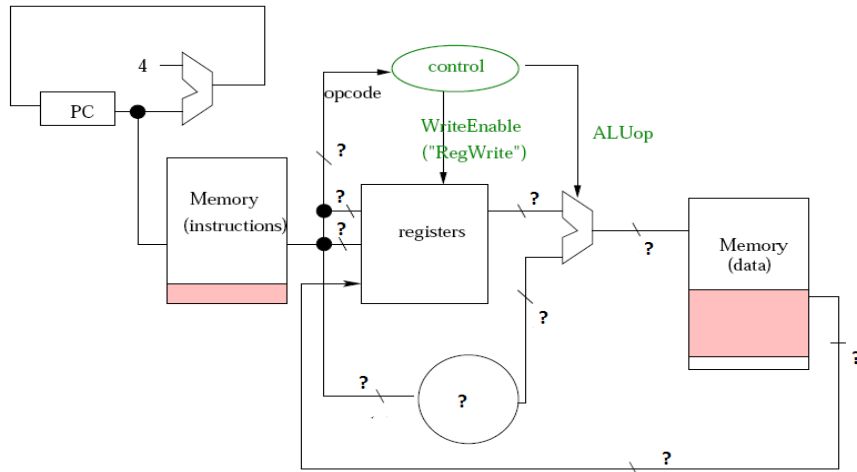
3



2. What do you mean by combinational elements and State elements?

2

3. Following figure shows the datapath for **lw** instruction, label the figure where marked “?”. **5**



4. How address of the next instruction is calculated in **Jump** instruction, explain with appropriate figure. **5**

**Name:** \_\_\_\_\_

**ID:** \_\_\_\_\_

**Department of Computer Science and Engineering**

**CSE340: Computer Architecture**

**Fall 2014**

**Quiz-3**

**Full Marks:15 Time: 30 Mins**

1. Why do you need multiple unites of same component in a single cycle datapath? 2

2. Let  $A = (0\ 1010\ 101)_2$  and  $B = (0\ 1101\ 110)_2$  perform  $(A+B)$  using IEEE754 floating point addition. Also show the decimal equivalent. 4

**3.** What do you mean by Response time, Throughput, CPI and effective CPI?

**4**

**4.** Draw the datapath for instruction: add \$10,\$11,\$12. Also show the dataflow.

**5**

**Name:** \_\_\_\_\_

**ID:** \_\_\_\_\_

**Department of Computer Science and Engineering**

**CSE340: Computer Architecture**

**Summer 2013**

**Quiz-3**

**Full Marks: 15 Time: 25 Mins**

1. State single cycle datapath advantages and disadvantages? 3

2. What do you mean by combinational elements and state elements? 2

3. Explain the five steps of load instruction. 5

4. What is pipelining? What makes Pipelining easy? Why it is hard at the same time?

**5**



Name: \_\_\_\_\_

ID: \_\_\_\_\_

**Department of Computer Science and Engineering****CSE340: Computer Architecture****Spring 2015****Quiz-3****Full Marks: 15 Time: 20 Mins**

1. **1 00001111 101010000000000000000000** convert this to decimal value using **IEEE754 32-bit** floating point representation. **7**

2. Add  **$0.5_{\text{ten}}$**  and  **$-0.4365_{\text{ten}}$**  IEEE 754 floating point addition. Also show the overflow status. **8**

Name: \_\_\_\_\_

ID: \_\_\_\_\_

**Department of Computer Science and Engineering****CSE340: Computer Architecture****Spring 2015****Quiz-3****Full Marks: 15 Time: 20 Mins**

1. **1 00000111 101110000000000000000000** convert this to decimal value using **IEEE754 32-bit** floating point representation. **7**

2. Multiply  **$0.5_{\text{ten}}$**  and  **$-0.4365_{\text{ten}}$**  IEEE 754 floating point addition. Also show the overflow status. **8**

Name: \_\_\_\_\_

ID: \_\_\_\_\_

**Department of Computer Science and Engineering****CSE340: Computer Architecture****Spring 2015****Quiz-3****Full Marks: 15 Time: 20 Mins**

1. Show the **IEEE 754** single precision binary representation of the floating point number **-13.3**. Also show equivalent hex representation of the binary value. **8**

2. Add  **$0.5_{\text{ten}}$**  and  **$0.124_{\text{ten}}$**  IEEE 754 floating point addition. Also show the overflow status. **7**

**Name:** \_\_\_\_\_

**ID:** \_\_\_\_\_

**Department of Computer Science and Engineering**

**CSE340: Computer Architecture**

**Summer 2014**

**Quiz-3**

**Full Marks: 15 Time: 25 Mins**

1. State single cycle datapath advantages and disadvantages? **3**

2. What do you mean by CPU time, CPI and effective CPI? **3**

3. Explain the five steps of load instruction. **4**

4. What is pipelining? What makes Pipelining easy? Why it is hard at the same time?

**5**