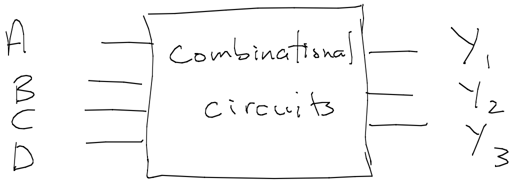
lecture 5

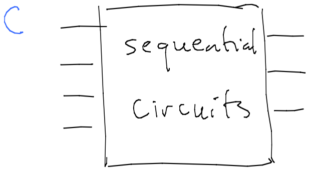
sequential circuits 1

last week



- signals carried on wires
- gate operations take time (e.g. carries in addition)

this week

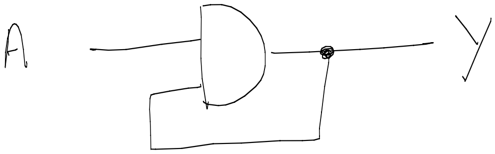


- combinational circuits + memory
- synchronized by a discrete clock C

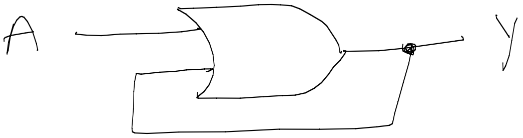
Memory (2 kinds)

- write it down
- repeat to yourself (feedback)

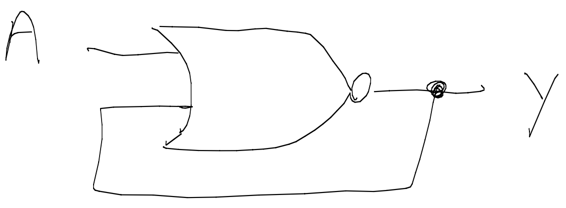
Feedback



A	Y
0	0
1	0 or 1
0 → 1	0
1 → 0	0



A	Y
0	0 or 1
1	1
0 → 1	1
1 → 0	1



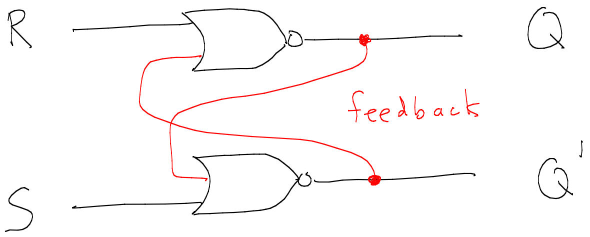
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

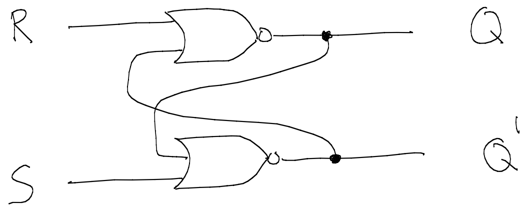
A	Y
0	0 <-> 1 oscillate
1	0

Today

- RS latch
- clocked RS latch
- D latch
- D flipflop, T flip flop
- register

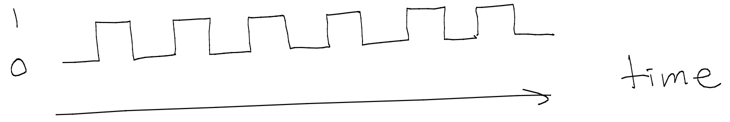
RS latch
('reset' 0, 'set' 1)





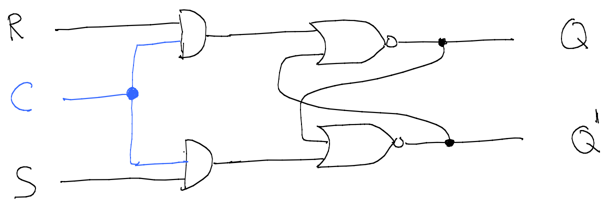
R	S	Q	Q'
0	0	hold previous values	
0	1	1	0
1	0	0	1
1	1	0	0

"Clock"



- doesn't count (just goes ON, OFF, ...)
- electronic implementation not discussed
- typical clock speed today is 3 GHz (10^9 cycles/sec)

Clocked RS latch



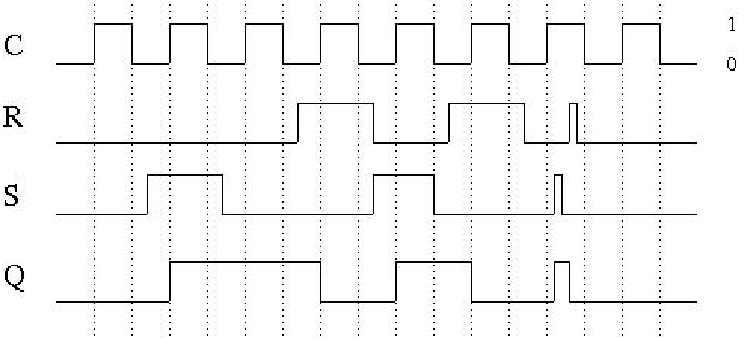
C=0

R	S	Q	Q'
0	0	hold	
0	1		
1	0		
1	1		

C=1

R	S	Q	Q'
0	0	hold	
0	1	1	0
1	0	0	1
1	1	0	0

Example



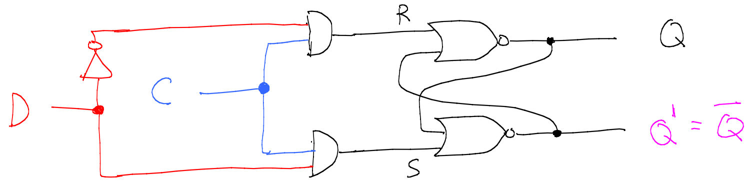
C = 0

R	S	Q	Q'
0	0	hold	
0	1		
1	0		
1	1		

C = 1

R	S	Q	Q'
0	0	hold	
0	1	1	0
1	0	0	1
1	1	0	0

D latch ("D" for data)

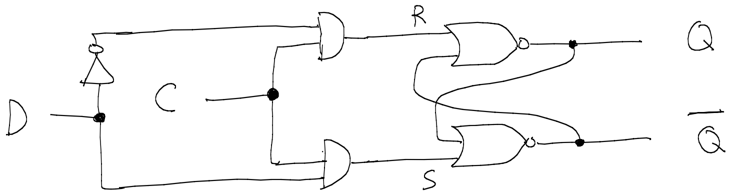


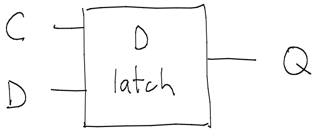
What does this circuit do?

when C = 1, D = 1 ⇒ Q = 1
D = 0 ⇒ Q = 0

when C = 0, hold values of $Q, \overline{Q}$

D latch



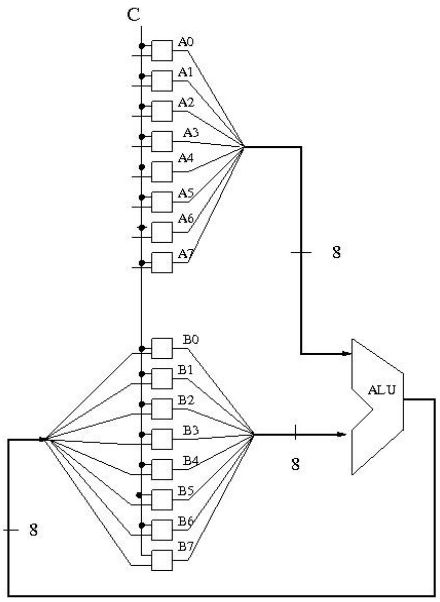


C = 0 ⇒ read only

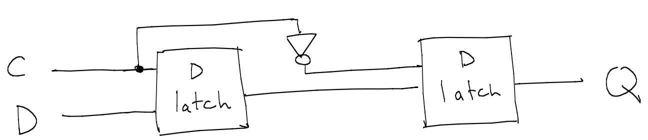
C = 1 ⇒ read and write

- We can hold values in D latches when C = 0.
- But when C = 1, the the circuits are open.
- This becomes a problem when we want feedback in circuits containing D latches

$x = x + y$



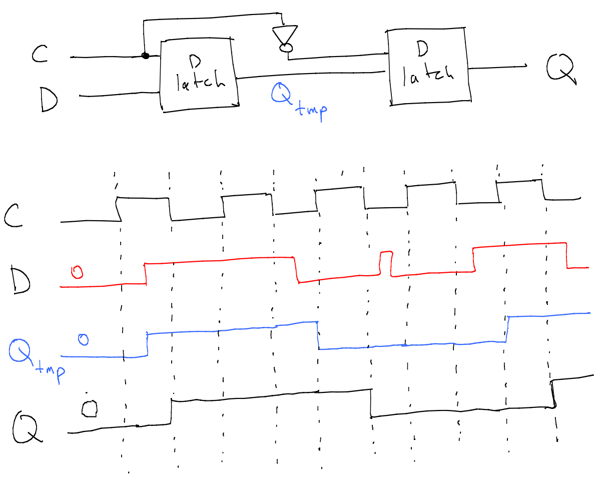
D flip flop



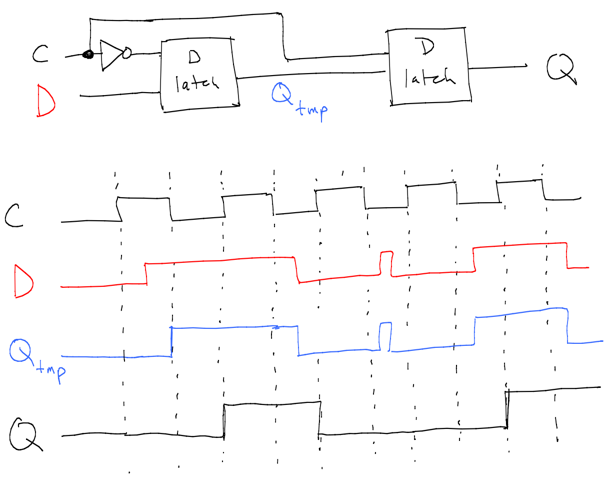
C = 1 ⇒
- write D into first D latch
- Q holds previous value

C = 0 ⇒
- stop writing into 1st D latch
- Copy value from 1st to 2ND D latch, Q takes (possibly) different value

D flip flop (falling edge triggered)

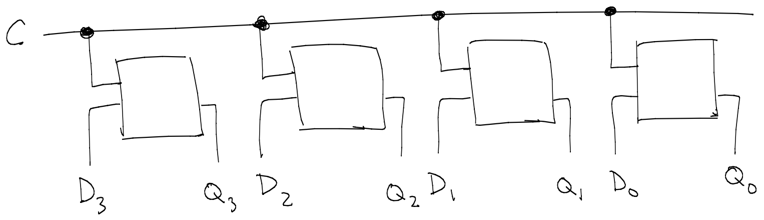


D flip flop (rising edge triggered)

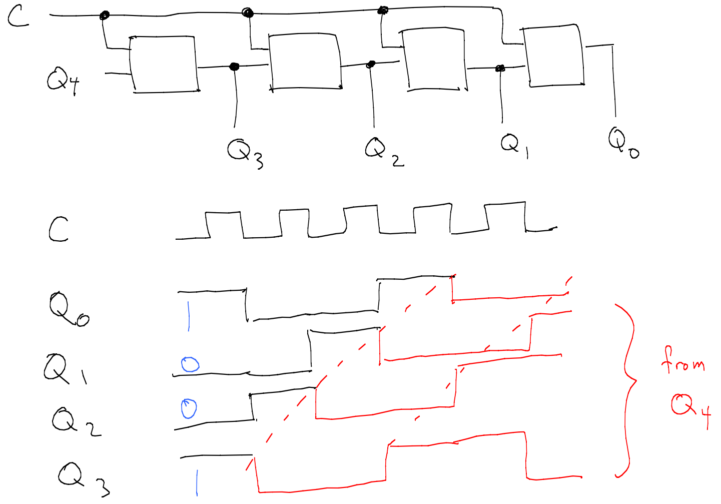


- Clock cycle is long enough to allow all gates to stabilize.
- Clock synchronizes all flip flops, allowing us to treat time as a sequence of discrete R/W steps (hence "sequential circuit")
- From now on, ignore all variations within a clock cycle (e.g. carries in adder)

Register (set of flip flops that are grouped together)



Shift register (falling edge)


C
Q_4
Q_3
Q_2
Q_1
Q_0
C
Q_0
Q_1
Q_2
Q_3
1
0
0
1
from Q_4