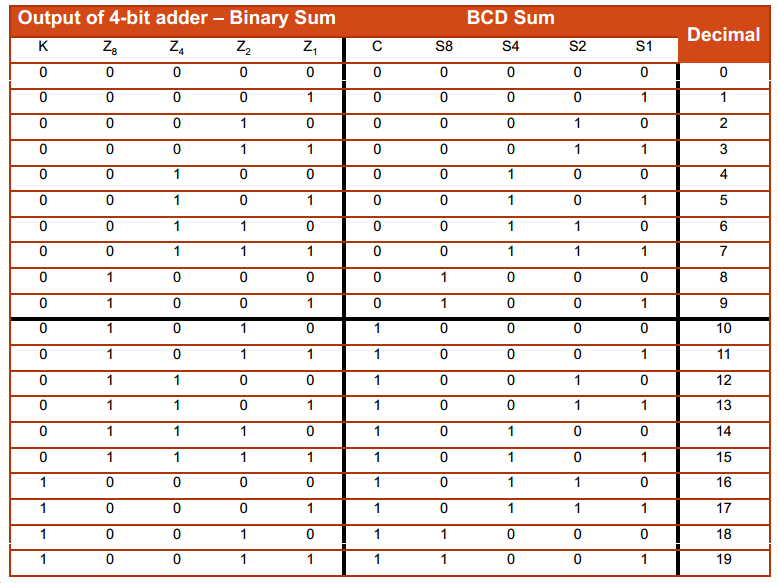
**Assignment 5**

***Question1 : Design a 4 bit parallel BCD adder from 4 bit Binary parallel adders***

Hint:  
A BCD adder is a circuit that adds two BCD numbers and the result is a sum digit in BCD and a carry. As each of the number can range from 0 to 9, therefore along with a carry in (having a value of 1) a 4 bit BCD adder result can range from 0 to 19 (9+9+1). A carry in BCD only occurs when summation of 2 BCD is more than 9. For example, when result is (10)10in decimal, 4 bit binary parallel adder’s result is ‘1010’ whereas BCD parallel adder’s will be ‘1 0000’.

Below is table which shows the correspondence between 4 bit binary adder and BCD adder. Looking at the table below, observe that there is a carry in BCD sum when K (i.e. Carry out of Binary 4 bit parallel adder) is 1 or z8 and z2 is 1 or z8 and z4 is 1.  
  
 Keeping this in mind, at first designa BCD adder by using a 4 bit binary parallel adder then propagate its result through two OR gate and two AND gates to get the Carry out ( C ) and an extra 4 bit binary parallel adder, to find the sum bits (S8 to S1).



***Question 2:***

1. Design a half adder using NAND gates only.
2. Design a quarter adder using NOR gate only (i.e. quarter adder that has only sum, no carry bit )
3. Design a 7 bit Adder-Subtractor for 1’s complement number system.

***Question 3:***  
Design a 16 people voting system where 0 means ‘No’ and 1 means ‘Yes’. It should show number of ‘Yes’ votes and then number of ‘No’ votes.

***Question 4:***

The adder–subtractor circuit has the following values for mode input M and

data inputs A and B .

M A B

(a) 0 0111 0110

(b) 0 1000 1001

(c) 1 1100 1000

(d) 1 0101 1010

(e) 1 0000 0001

In each case, determine the values of the four SUM outputs, the carry C , and overflow V .

***Question 5:***

Assume that the exclusive-OR gate has a propagation delay of 10 ns and that the AND or

OR gates have a propagation delay of 5 ns. What is the total propagation delay time in the

four-bit adder of each bit of sum and carry.

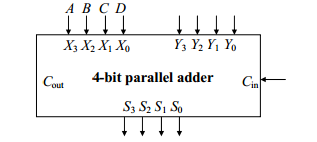
***Question 6:***

Design a 2 bit Magnitude comparator that performs operations such as less than, greater than and equal to between two 2 bit binary numbers. You need to show both equations and circuit diagram.

***Question 7***

You are to design a 4-bit Excess-8 to 2’s complement converter. For example, 0010excess-8 represents the value –6, and hence its corresponding 2’s complement representation is 10102’s. The converter takes in a 4-bit Excess-8 representation ABCD and outputs a 4-bit 2’s complement representation WXYZ.

Supposed you are given only a 4-bit parallel adder and no other logic gate. Implement the converter using this parallel adder. Some of the inputs have been filled in for you, as shown below. Complete the diagram below. Note that the Cout is not used.



|  |  |
| --- | --- |
| Decimal | Excess 8 |
| -8 | 0000 |
| -7 | 0001 |
| -6 | 0010 |
| -5 | 0011 |
| -4 | 0100 |
| -3 | 0101 |
| -2 | 0110 |
| -1 | 0111 |
| 0 | 1000 |
| 1 | 1001 |
| 2 | 1010 |
| 3 | 1011 |
| 4 | 1100 |
| 5 | 1101 |
| 6 | 1110 |
| 7 | 1111 |