**Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID: \_\_\_\_\_\_\_\_\_\_\_\_**

**Department of Computer Science and Engineering**

**FINAL EXAMINATION**

**Summer 2013**

**CSE340: Computer Architecture**

**Total Marks:** **70**  **Time Allowed: 2.20 hrs**

* Answer **ANY SEVEN** questions.
* Return the question with your answer script

Question 1

1. Define Compiler, Assembler and High Level Programming Language. **4.5**
2. Define ISA and ABI. **2**
3. What do you mean by Datapath, Memory hierarchy and Multi processor systems? Explain with appropriate figures. **3.5**

Question 2

1. What are the differences between RICS and CICS Architecture? **2**
2. Encode the following MIPS instructions. For each instruction, you should identify the format type (R, I, or J format): **4.5**
   1. sub $s0,$t0,$t1 # $s0 is register 16 and $t0 is register 8, op=0,function=22hex
   2. beq $s1,$s2,100 # $s1 is register 17 and $s2 is register 18, op=4hex
   3. sb $12, 2($3) # op=28hex
3. In the following code segment f,g,h,i and j are variables. If the five variables f through j corresponds to five registers $s0 through $s4, what is the complied MIPS code for the below C is statement? **3.5**

if (i==j) f=g+h; else f=g-h;

Question 3

1. Explain Big Endian and Little Endian addressing with appropriate figures. **3** **4**
2. Write a MIPS code to sum the series 1+5+9+…+N. You should use minimum number of registers to implement the MIPS code. **4**
3. What do you mean by zero and sign extension? **3**

Question 4

1. Convert **-87.6875** into **IEEE-754** single point floating point representation. Also show the hex equivalent of the representation. **5**
2. 0 00000111 10101100000000000000000 convert this to decimal value using **IEEE754 32-bit** floating point representation. **5**

Question 5

1. **X**=0100 0111 1101 0000 0000 0000 0000 00002 **Y**=1010 1110 1110 0000 0000 0000 0000 00002 representing single precision **IEEE 754** floating-point numbers, Find **X+Y** and **X-Y**. **6**
2. Our favorite program runs in **10** seconds on computer A, which has a **4 Ghz** clock. We are trying to help a computer designer build a computer, B, that will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require **1.2** times as many clocks cycles as computer A for this program. What clock rate should we tell the designer to target? **4**

Question 6

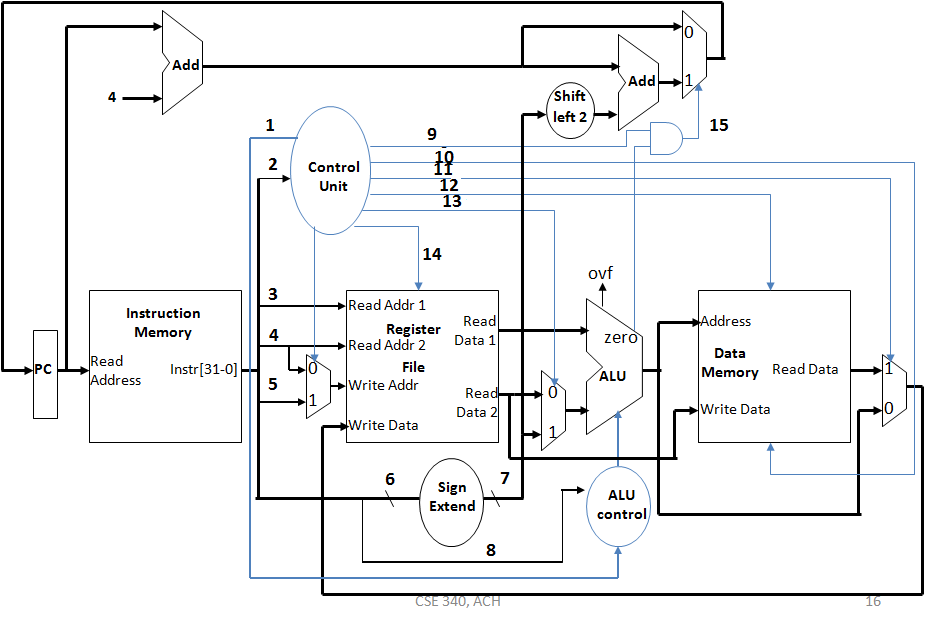
1. Define Combinational elements and State elements. **2**
2. Draw the Datapath for lw instruction and explain the execution steps. **5**
3. Explain Multicycle datapath control unit. **3**

Question 7

1. Compare between single cycle, multi cycle and pipelining processing with necessary diagrams. **4**
2. Explain different pipeline Hazards with appropriate figures. **6**

Question 8

1. Label the diagram where numbered 1 to 15. Write your answer in the answer script. **5**



1. How address of the next instruction is calculated in **Jump** instruction, explain with appropriate figure. **5**