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| No. of Pages | **6** |
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**Department of Computer Science and Engineering**

**FINAL EXAMINATION**

**Spring 2016**

**CSE 340: Computer Architecture**

**Total Marks: 75 Time Allowed: 3 Hours**

* Answer ***Section 1*** in the space provided in the question paper
* Answer ***Section 2 and 3*** in the answer script provided
* At the end of the exam return both your answer scripts along with your question

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_\_

**Section 1 (35 Marks)**

1. Design a single cycle datapath for the instruction addi $5, $6, 10. **3**
2. Consider the instructions: addi (add immediate), mult (multiply two integers), beq (branch if equal), sub (subtract). Explain the operation performed at decode and execution stage for these instructions. **4**
3. Multiply 0.712 and 0.138 using IEEE single precision floating point representation? Also show the status of the result (overflow or underflow). **4**
4. Consider the MIPS code given below. Explain what operations are performed in the given code and why? **4**

mult $t1,$t2

mfhi $s0

mflo $s1

1. Briefly mentioned the techniques of overcoming control hazards. **3**
2. In an ideal world, a processor with an N-stage pipeline would execute with a clock frequency N times faster than a single-cycle (i.e., non-pipelined) processor. Give reasons why the clock frequency of a real pipelined processor would be less than N times faster. **3**
3. Design a PLA for the expression: **5**
4. Explain performance equation. **3**
5. A Program is running on a specific machine (CPU) with the following parameters:

Total executed instruction count: 10,500,000 instructions. Average CPI for the program: 2.3 cycles/instruction. CPU clock rate: 270 MHz (1 MHz = 1 \* 10^6 cycles/sec). What is the execution time for this program? **3**

1. Consider the pseudocode given below, convert this code to sequence of MIPS code. **3**

abs $t2,$t3

This instruction means that register $t2 has a copy of register $t3 if $t3 is positive, and the two’s complement of register $t3 if $t3 is negative.

**Section 2 (Answer any Three) (30 Marks)**

###### Question No.11

1. Convert -59.323 into IEEE754 floating point representation. Consider you have a register which is 16-bit in length and in the register one bit is reserve for sign of the number, following five bits are for exponent and rest for fraction part. Show the equivalent Hex representation of your conversion. **5**
2. Use Booth’s algorithm to multiply 7 and -7. **5**

###### Question No.12

1. Consider the below MIPS code sequence: **5**

add $t4,$t0,$0

loop: sll $t0,$t0,2

slt $t2,$t1,$t0

bne $t2,$0,loop

srl $t3,$t4,2

J Exit

Exit:

Consider $t0 has a value of 4 and $t1 has a value of 64. Trace the code sequence for values of $t0 and $t3.

1. Write a MIPS code for the below sequence of C code: **5**

While (c<10) {

D=b+a[c];

c+=1;

}

Assume c, d, b are in registers $s0, $s1, $s2. Also base address of a is stored in $s3.

Question No. 13

Draw the pipeline for the below MIPS code sequence. Identify all the data hazards in the following sequence of instructions. Identify the line number of the hazards. Mention what are the possible ways of overcoming data hazards with necessary diagrams. **10**

1. addi $5, $5, 4

2. lw $6, 100($5)

3. add $6, $2, $0

4. sw $6, 0($5)

5. xor $7, $7, $1

6. add $8, $8, $9

## Question No. 14

1. What is paging? Explain concept of paging when you have a RAM of 1GB and a HDD of 1TB and your page size is 2 KB. Show the mapping of VPN with RAM and HDD. **6**
2. Consider the code sequence given below: **4**

add $1,$1,$2

add $1,$1,$3

add $1,$1,$4

Give the corrected forwarding control for the above code sequence.

**Section 3 (10 Marks)**

## Question No. 15

1. Let’s consider you have a system that takes four bits (a,b,c,d) as input. Consider inputs starting form (0000) to (1011). These twelve inputs identify the months of a year. For these twelve combinations output F will be high (1) when number of days in the month is 31 else output will be low (0). Also from input (1100) to (1111) output will be low (0), as we have only twelve months in a year. Considering this algorithm: **8**
   * 1. Draw a truth table for F
     2. Using sum of product method simplify F
     3. Design a logic circuit for simplified F
2. Design a conditional sum adder? **2**

THE END