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**Department of Computer Science and Engineering**

**FINAL EXAMINATION**

**Summer 2015**

**CSE 340: Computer Architecture**

**Total Marks: 80 Time Allowed: 2.5 Hours**

* Return the question paper with your answer script

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Section 1(Answer Any Four)

###### Question No.1 (12+3=15)

1. Let’s assume that you are asked to design a 128-bit MIPS computer architecture. Now the specification that you are given is as follows: total number of registers in the register file is 64. Instruction size is 128-bit, Data size 128-bit and has three different types (R, I and J) of instructions are available in the architecture. Show the three different instruction formants leaving OP code and function field empty. Also following 32-bit MIPS architecture model, design a single cycle datapath for this new architecture. Your datapath should indicate the bandwidth of every link.
2. Convert the below given instructions into MIPS pseudo-instructions:
   1. **blt $t1,$t2, Exit** (**blt**--Branch if less than)
   2. **bgt $t1,$t2, Exit** (**bgt**--Branch if greater than)

## Question No. 2 (5+5+5=15)

1. Let’s assume you have a sixteen bit register (bit 15 for sign, bits 14~10 for exponent and remaining bits for fraction). Now show IEEE 754 binary representation of **(-17.612)10**. Also show the Hex equivalent.
2. Add **(5.227)10** and **(1.723)10** using IEEE 754 single precision floating point addition method. Also show decimal equivalents of the result.
3. Compare between Von Neumann and Harvard computer model with necessary block diagrams.

Question No. 3 (9+6)

1. The performance equation can be given by. Define each term of the given equation. For each component identify at least two components that affects each term. For example: technology affects the clock cycle.
2. Write a MIPS assembly code that can sum the following series: **2+4+6+…+30**. Your code should use general register convention discussed in the class and make optimum use of registers.

## Question No. 4 (4+11)

1. Consider the following MIPS assembly code. Assume that we are using the pipeline processor and $a1 is initialized to 4. Print instruction execution sequence by writing the instruction numbers given after “//” of each instruction.

**Loop: lw $t1, 0($a0) //1**

**lw $a0, 0($t1) //2**

**addi $a1,$a1,-1 //3**

**bne $a1, $zero, Loop //4**

**add $v0, $a0, $zero //5**

**addi $sp, $sp, 8 //6**

1. Identify data dependencies in instructions given in 4(a). If there is any data hazard in the pipeline, explain how you can over the hazards with appropriate diagram(s).

Question No. 5 (6+5+4)

1. What is the difference between a branch and a jump instruction? Explain how branch and jump address can be calculated with necessary diagram(s).
2. Consider the instructions below:

**lw $t1, 4(t0)**

**lw $t2,5(t1)**

Let’s $t0 has 0x1234 as base address. Now calculate the memory address from where $t2 will have value from. Draw the figure that shows the senior also show your detail calculation.

1. How can you execute multiply and division operations without using **MULT** or **DIV** instruction. Give one example for each case.

Section 2

## Question No. 6 (10+10)

1. Consider the given circuit below. Truth table for USF is given on the left of the circuit. Generate the truth table for f(a,b,c,d,e).



1. Design a combinational logic circuit using PAL that implements below expressions:



THE END