**Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID: \_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_**

**Department of Computer Science and Engineering**

**CSE340: Computer Architecture   
Fall 2015**

**Quiz-1, A**

**Full Marks: 15 Time: 20 Mins**

1. Design a conditional shift register and explain its operation. **15**

**Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID: \_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_**

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**Quiz-1, B**

**Full Marks: 15 Time: 20 Mins**

1. Design a “Conditional Sum” adder and explain its operation. **15**

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**Quiz-1, C**

**Full Marks: 15 Time: 20 Mins**

1. Let’s assume you have four inputs **A, B, C, D** and output **F**. **F** is high when decimal equivalent of the inputs are even. Simplify **F** using sum of product expression and draw the logic circuit. **15**

**Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID: \_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_**

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**Quiz-1, D**

**Full Marks: 15 Time: 20 Mins**

1. Design a PLA for the expression given below: **15**

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**Quiz-1, E**

**Full Marks: 15 Time: 20 Mins**

1. Let’s assume you have four inputs **A, B, C, D** and output **F**. **F** is high when decimal equivalent of the inputs are odd. Simplify **F** using sum of product expression and draw the logic circuit. **15**