**Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID: \_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_**

**Department of Computer Science and Engineering**

**CSE340: Computer Architecture   
Spring 2016**

**Quiz-1, A**

**Full Marks: 15 Time: 20 Mins**

1. Design a frequency counter that can count upto 16 using T flip-flop. Also show the frequency diagram. **15**

**Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID: \_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_**

**Department of Computer Science and Engineering**

**CSE340: Computer Architecture   
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**Quiz-1, B**

**Full Marks: 15 Time: 20 Mins**

1. Design a “Conditional Sum” adder and explain its operation. **10**
2. Consider the below Boolean expression and generate the truth table for the expression. **5**



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**Quiz-1, C**

**Full Marks: 15 Time: 20 Mins**

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1. Consider the below Boolean expression and generate the truth table for the expression. Also draw the circuit for the expression. **15**

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**Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID: \_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_**

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**Quiz-1, D**

**Full Marks: 15 Time: 20 Mins**

1. Design a PLA for the expression given below: **15**

**Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID: \_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_**

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**Quiz-1, E**

**Full Marks: 15 Time: 20 Mins**

1. Consider the below Boolean expression and generate the truth table for the expression. Also draw the circuit for the expression. **15**

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