Q1. Do question 4.1 (chapter 4).

```
□-- Homework 8 Question 4p1
   -- Design of Digital Circuits
2
3 L-- Mark Musil
4
5
    -- Translate the following code into an if-then-else
    statement:
6
7
    transmit <= signal a when state = idle else
8
                signal b when state = incoming else
9
                signal c when state = outgoing else
10
                signal d;
11
12
   -- Answer
13
14 □if state = idle then
15
       transmit <= signal a;
16
17 pelsif state = incoming then
18
       transmit <= signal b;
19
20 pelsif state = outgoing then
21
       transmit <= signal c;
22
23 ⊟else
24
        transmit <= signal d;
25
26 end if;
```

Q2. Do question 4.2 (chapter 4).

```
📑 eight_bit_even_parity_checker.vhd 🗵 📙 MyPLL.vhd 🗵 📙 MyPLL_inst.vhd 🗵 📙 q14p1.vhd 🗵 📙 BlinkerTest.txt 🗵 🔒 q24p2.vhd 🗵
 1 □-- Question 4p2
  2 L-- Mark Musil
  3
  4 -- Translate the following code to a when-else st
  5
  6 process (a, b, j, k)
  7
          begin
               if a = "1" and b = "0" then
 8
                   step <= "0100";
 9
               elsif a = "1" then
 10
 11
                  step <= j;
12
               elsif b = "1" then
 13
                  step <= k;
14
               else
15
                   step <= "----";
16
               end if;
17
          end process;
18
19
     -- To a when-else statement
20
21
22
    process (a, b, j, k)
 23
     begin
      step <= "0100" when (a = "1" and b = "0") else
24
                      when a = "1" else
25
              j
 26
                      when b = "1" else
               "----" when others;
27
 28
     end process;
```

Q3. Do question 4.3 (chapter 4).

```
📑 📙 eight_bit_even_parity_checker.vhd 🗵 🔡 MyPLL.vhd 🗵 🔡 MyPLL_inst.vhd 🗵 🛗 q14p1.vhd 🗵 🔡 BlinkerTest.txt 🗵 🔡 q24p2.vhd 🗵 🛗 new 1 🗵
   2 L-- Homework 8 problem 3
   3
   5
      -- Translate the following code to a case-when statement
   7
      with state select
           data <= "0000" when idle | terminate,
   9
                    "1111" when increase,
  10
                    "1010" when maintain,
                    "0101" when decrease,
  11
                    "----" when others;
  12
  13
  14
  15
      -- Answer
  16
  17 □case state is
  when idle | terminate => data <= "0000";
  19
           when increase => data <= "1111";</pre>
           when decrease => data <= "1010";</pre>
  20
  21
           when others => data <= "----";</pre>
  22 end case;
```

Q4. Do question 4.5 (chapter 4).

```
📙 sq_wave_fourier_fn_Musil.txt 🗵 📙 gate_level_example.txt 🗵 📙 my_gate_level_example.vhd 🗵 📙 test_bench_for_decrementer.vhd 🗵 📙 new 1 🗵
  1 ⊟-- Mark Musil
  2 L-- Homework 8 question 4
  4 -- Translate the following code to two with-select-when
     statements
  5
  6
  7 pcase state is
 8
         when idle => a <= "11"; b <= "00";</pre>
         when terminate | increase => a <= "01"; b <= "--";</pre>
  9
 10
         when maintain | decrease => a <= "10"; b <= "11";</pre>
         when others => a <= "11"; b <= "01";</pre>
 11
 12 end case;
 13
 14
 15
     -- Answer
 16
 17
 18
     with state select
        a <= "11" when idle,
 19
               "01" when terminate | increase,
 20
 21
               "10" when maintain | decrease,
 22
              "11" when others;
 23 end case;
 24
 25 with state select
 26 b <= "00" when idle,
 27
              "--" when terminate | increase,
 28
               "11" when maintain | decrease,
 29
               "01" when others;
 30 end case;
 31
```