2 Integrated Circuit Manufacturing: A Technology Resource

2 — IC MANUFACTURING TECHNOLOGIES

While the integrated circuit drives the packaging and assembly, the IC manufacturing process, and associated methodologies, serves as an invaluable technology resource. IC manufacturing is made up of a “Front End” and a “Back End”. The “Front End” encompasses the actual fabrication of the IC and is most often referred to as “Wafer Fab”. The “Back End” covers subsequent packaging, assembly, and testing of the IC. Many of the materials, the processes, procedures, and equipments, particularly those associated with the photolithography, have direct application to relevant packaging and assembly needs.

Areas of application for these types of methodologies supporting current and future IC packaging and assembly include:

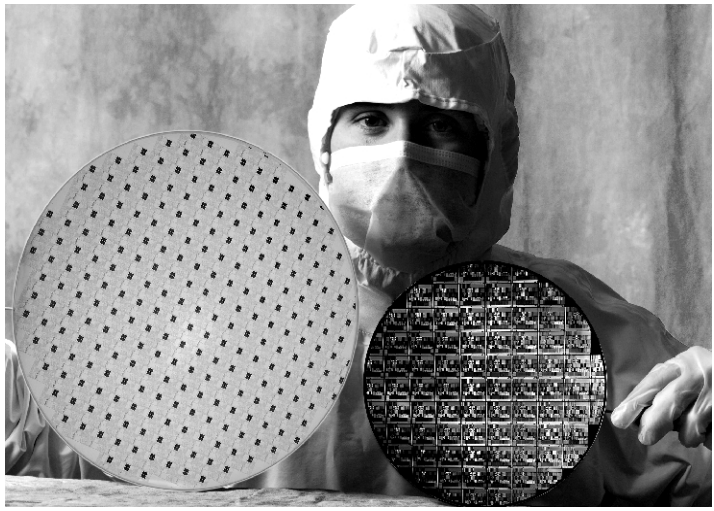
- Wafer bumping for TAB and flip chip,
- Wafer Level Packaging (WLP) for Chip Scale Packages (CSP),
- Interconnect Substrates for MCPs, and
- Level 2 High Density Interconnects, HDI PWBs.

The IC photolithographic process and the above applications share the same basic technology for pattern transfer. The inherent advantages of much of the IC methodologies can best be assessed by first reviewing the various processes emphasizing some of the important “lessons learned” and secondly (and perhaps more importantly) their significance and impact on yields and cost-effective manufacturing.

2.1 — Overview of the IC Manufacturing Processes [1–4]

An IC is fabricated in a wafer format. Multiple ICs are manufactured simultaneously on a single wafer. Today wafers are processed in 6", 8" and 12" diameters (Figure 2-1). When completed, a wafer can contain literally hundreds or thousands of ICs. Larger wafers produce more devices and since the cost to manufacture changes little with size, the cost per IC is less. This of course assumes yields are maintained in the transition from smaller to larger wafers. The switch to the larger wafer, however, is also costly, typically involving a rather significant investment in new process equipment capable of handling the larger size wafers. The current 12" wafer

is projected to remain in place through the next decade. Most major semiconductor houses, which in the U.S. include Intel, Texas Instruments and Freescale Semiconductor (formerly Motorola), are now processing 12" wafers. The 6" and 8" wafers are found in the foundries. Foundries are facilities that provide wafer manufacturing services to “fab-less” ASIC design houses.



(Courtesy IBM Corp.)

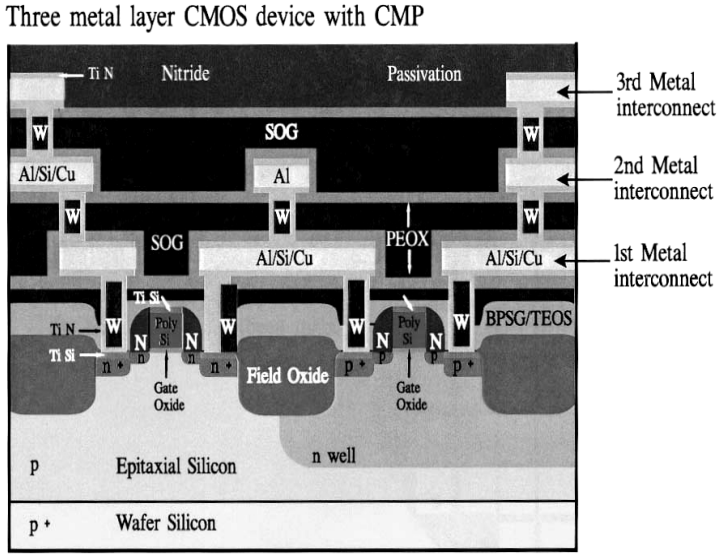
Figure 2-1. A 300 mm (12") and 200 mm (8") Diameter Silicon Wafer

The IC, basically a multilayered structure (Figure 2-2), is fabricated in a sequential process. Controlled impurities that create the active transistors are first embedded in the silicon using processes such as oxidation, ion implantation, and diffusion. This is followed by the deposition of conductor and dielectric materials that form a multilevel conductor network. The network literally interconnects the millions of embedded transistors that may be contained within a single IC. This multilevel conductor network terminates at metallized bond pads on the surface of the IC that allow for access to the outside world when the IC is assembled into a package.

Each layer within the structure shown must be properly defined using a pattern-transfer process wherein an image on a photomask is transferred onto the surface of a wafer. To complete an IC as many as 25 or more photomasks, each containing a different image, are required.

Because of the many steps involved in the manufacture of the IC major problems arise resulting in the loss of functional devices. This adversely affects overall yield of devices and directly impacts manufacturing costs. Devices are lost because of defects and contamination introduced during manufacture.

The processes currently in place have evolved over the years from a continuing and dedicated effort directed towards one objective, that is, *to eliminate or minimize generation of defects and contaminants at each and every step in the manufacturing process and thereby optimize yields.*



(Courtesy PTI Seminars, Inc.)

Figure 2-2. Schematic Cross-Section of a Si Integrated Circuit

Major sources of defects are particulates in the operating environment, the materials and processes themselves, the equipment, and associated fixtures and tooling. In addition, operator involvement during manufacture can be a further contributor to yield loss due to improper dress, procedural errors and mishandling of wafers.

Identification of the various sources of defects and their elimination has resulted in many changes. As IC feature sizes began to rapidly decrease and complexity increased, critical changes were needed. These included, most notably,

- Strict control of the manufacturing environment and operator protocols, and
- Continuing development of "near defect-free" photolithographic processes covering the photomask and the exposure/imaging/printing equipment and tooling.

2.2 — The Manufacturing Environment [5–6]

With decreasing feature size it became obvious that "particulates" contained in normal room air, when inadvertently deposited on the wafer could create a defect that would result in loss of one or many ICs. A "cleanroom" operating environment to control the particulates in the air was essential. The level of control required changed with each generation of IC. *The level of cleanlines, and degree of controls are dictated by the particular process and device requirement, e.g., minimum feature size*. Table 2-1 lists levels of cleanliness for cleanrooms and defines particle sizes and limits. The lower the classification number the higher level of control both as to the size and the number to be found in a given volume of air.

Table 2-1. Cleanroom Classifications [US FED STD 209E Cleanroom Standards]

Maximum Number of Allowable Particle of Indicated Size per ft^3						
Class	0.1 µm	0.2 µm	0.3 µm	0.5 µm	1 µm	5 µm
1	35	7	3			
10	350	75	30	10		
100		750	300	100	10	1
1,000				1,000	100	10
10,000				10,000	1,000	100
100,000				100,000	10,000	1,000

Other sources of contaminants to be controlled include process chemicals, bacteria from process water, metallic ions found in process chemicals. and operator and equipment related static discharge. High purity, high resistivity (18 megohms) deionized water (treated to remove metallic ions) is used extensively during IC manufacturing supporting the many rinsing and cleaning operations. Special plumbing and the use of filters insure removal of damaging particles. In addition, harmful bacterial contamination is removed by an ozone or ultraviolet light exposure treatment. Process chemicals are similarly subjected to much the same types of treatments and controls.

Control of the room temperature (T) and relative humidity (RH) is also an essential part of any cleanroom operating environment. Lack of control of T and RH can adversely effect both materials and equipment and contribute to critical process irregularities. This is of particular significance in the photolithographics area where materials like photosensitive resists and associated processes are affected. And, because resist materials are sensitive to ultraviolet (uv) light, all photolithographic processes are performed in a room with special lighting (yellow lighting) that eliminates unintentional but damaging exposures.

The “Back End” cleanroom requirements however, are quite different. Levels of control are orders of magnitude greater for “Front End” than “Back End”. “Back End” processing is usually maintained in a Class 1000 and higher operating environment. Early cleanrooms were Class 100. Today IC wafer fab is performed in Class 1 cleanrooms. And, to further enhance the level of cleanliness, special processes, e.g. the photolithographic processes, are performed in separate enclosures within the cleanroom (Figure 2-3).

2.2.1 — Operator Protocols

Strict operator protocols were also instituted and incorporated including,

- Special training covering proper handling and storage of wafer,
- The wearing of special cleanroom garments, and
- Well-defined cleanroom operating procedures.

(Courtesy National Semiconductor)

Figure 2-3. A Class 1 Cluster Cell within a Class 10 Cleanroom

(Courtesy IBM Corp.)

Figure 2-4. Robotic Wafer Handling

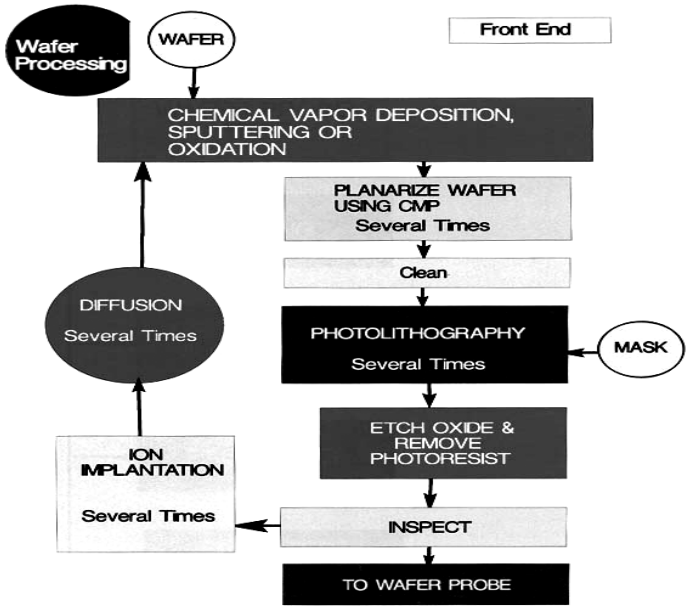
In Wafer Fab operators are required to wear gowns worn specifically to eliminate particulates that could be introduced by the operator and the operator's personal clothing.

Use of "robotics" (Figure 2-4) as well as other automated wafer handling equipment and fixturing are implemented to minimize, wherever possible, operator intervention and potential operator induced damage resulting from mishandling and electrostatic discharge.

2.3 — The Photolithographic Process [7]

The basic manufacturing processes, shown in Figure 2-5, can be grouped as follows:

- Deposition Processes—including Oxidation, Diffusion/Ion Implantation, Chemical, Vapor Deposition (CVD), Sputtering
- Photolithography—Exposure (Printing, Imaging), Developing, and
- Pattern Transfer—including Etching and Plating



(Courtesy PTI Seminars, Inc.)

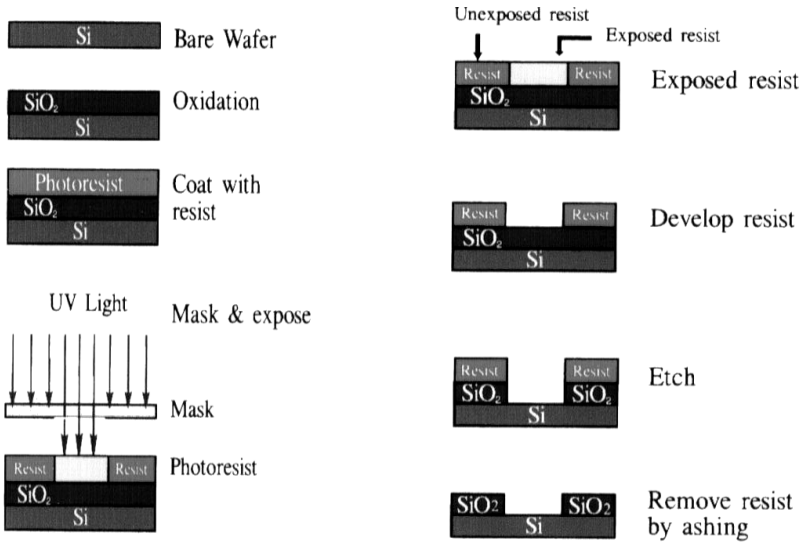
Figure 2-5. Si Wafer Fab, The Front End Processes

Photolithography is a multi-step pattern transfer process that covers:

1. Application of a photosensitive material (photoresist or resist) to a wafer or substrate.
2. Patterning of the resist by exposure to a UV light source through a patterned photomask.
3. Completion of the pattern transfer by immersion of the exposed resist in a developer.
4. Using the patterned resist as a mask for chemical etching of exposed metals or dielectrics, or as a template for selective deposition of a metal by a plating process.

2.3.1 — The Basic Pattern Transfer Process

The IC photolithographic process for pattern transfer is highly sophisticated and has been designed to ensure "near zero defects" and high yield of ICs with feature sizes in the 100-nanometer range. The basic process is shown in Figure 2-6.



(Courtesy PTI Seminars, Inc.)

Figure 2-6. The Basic Pattern Transfer Process

It begins with the application of a photoresist film that when patterned, will function as either an etch mask or as a template, to selectively deposit a metal by plating. Figure 2-6 shows the "etch" or "subtractive" process for patterning a silicon dioxide (SiO_2) layer to be used as a mask for the introduction of impurities into the silicon to form the transistors.

Basic to the process is:

- The photomask,
- The photosensitive resist film, and
- The mask aligner/exposure/printer equipment.

2.3.2 — Photolithographic Tooling—The Photomask/Reticle [8]

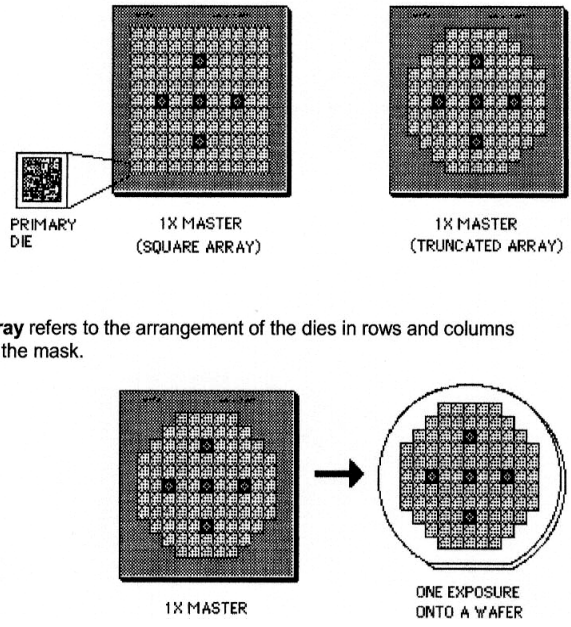
The primary tool and the most critical item in the photolithographic manufacturing process is the photomask. As used in the manufacture of the IC it is typically a high quality, high precision glass or quartz plate. Glass is used because it is not easily damaged and is extremely stable—not susceptible to dimensional changes when subjected to variations in room temperature and relative humidity. Patterned images on the glass mask are an opaque chromium or Al film. The hard surface chrome is highly durable and yields patterns with exceptionally sharp edge acuity insuring well-defined image transfer.

Mask manufacture, therefore, is just as critical as that of the actual IC. The transferred patterns simply *cannot be better* than the patterns on the photomask. As many as 25+ different patterns (photomasks) are typically required to manufacture an integrated circuit. A defective pattern on any mask results in a defective die. Hence each mask must be of the highest quality, and ideally, free of defects to insure the maximum possible yield. Insuring a defect free photomask requires that each and every pattern on a mask be critically inspected. Performed by an operator, it is labor intense and subject to error. Today, automatic optical mask inspection equipment allows for 100% inspection of each and every image on a mask. While all patterns on a multi-image mask may not be completely defect free, the inspection can help identify useable masks that are repairable or are at an acceptable defect level for use in production. The mask manufacturing process sequence is shown in Appendix B.

The mask image is pattern transferred using the same basic processes described in Figure 2-6 with multiple in-process inspections and measurements included to insure precise replication of the image as derived from a computer automated design (CAD) database. All mask manufacturing is accomplished under the same operational enviroment and operator protocols as the IC.

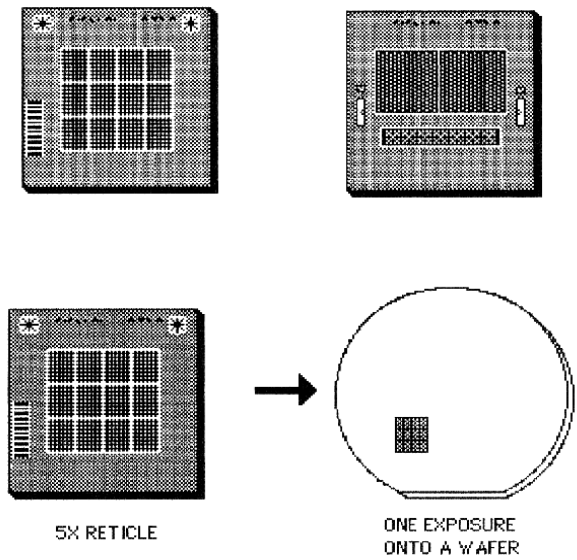
2.3.3 — Types of Photomasks

There are basically two types of photomasks: the array mask and the reticle (Figures 2-7(a) and (b)). The area array mask contains multiple sites each with the same pattern or image.



(Courtesy Photronics)

Figure 2-7(a). An Array Photomask



(Courtesy Photronics, Inc.)

Figure 2-7(b). A Reticle

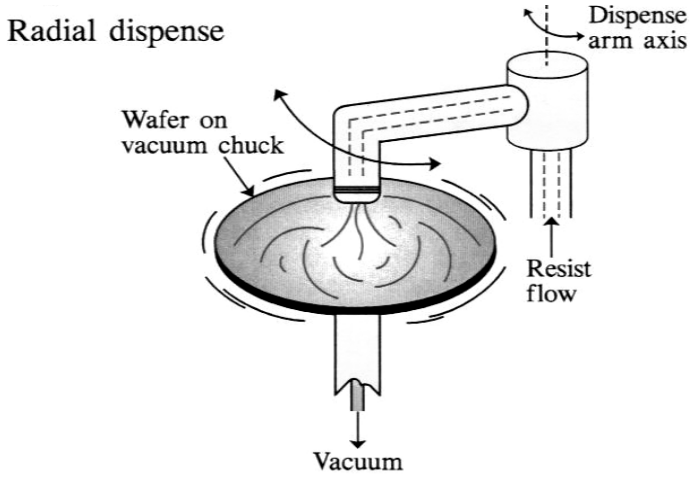
The reticle is a photomask that is specifically intended for use in projection printers, specifically wafer steppers, and contains a single image or a grouping of the same image. The images can be 1X, 2X or 10X of the final feature size to be transferred onto the wafer.

Reticles offer several advantages compared to array masks particularly in regard to inspect for defective images. Since there is only one or a few images, inspection times are significantly reduced. Similarly, with magnified images inspection is further simplified enabling "near-perfect" masks to be presented into manufacturing.

2.3.4 — Photosensitive Materials (Photoresists) [9]

In IC manufacturing the photosensitive film deposited on the Si wafer is liquid and is applied by dispensing. Graphically represented in Figure 2-8, it shows a wafer mounted on a vacuum chuck that can be rotated at very high rpm. The dispensing can be done while the wafer is either stationary (dynamic) or rotating (radial). Similarly the dispensing arm can be fixed or moved across the wafer. The volume of resist dispensed must be sufficient to insure complete coverage of the wafer. Following application the resist is cured to form a hard coating. It is then exposed through a photomask and developed to complete the patterning of the resist. The resist is now ready for the etching process.

When a metal conductor is to be patterned, the final thickness of the resist is critical. As an etch mask it must be of sufficient thickness to insure complete removal of unprotected metal. The final thickness of the resist will be determined by



(Courtesy PTI Seminars, Inc.)

Figure 2-8. Deposition of Liquid Photoresist by Spinning

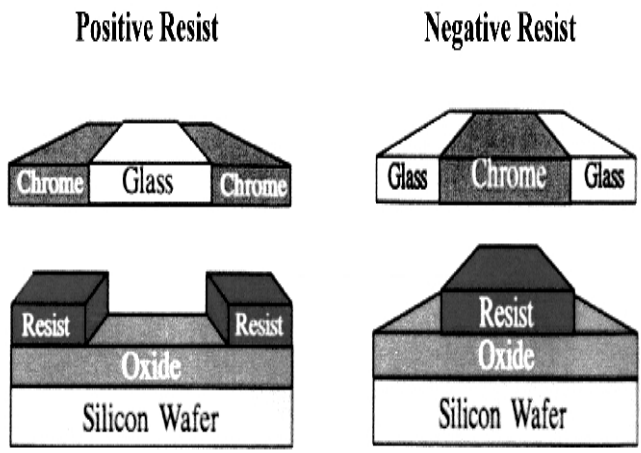
the viscosity of the resist and the rotational speed of the chuck. This thickness is typically the same or slightly greater than the thickness of metal to be etched. For IC metallization, it is normally 1 μm or less in thickness.

There are other alternative resist materials and coating processes available but they are not necessarily employed in the manufacture of the IC. These include spray coating of liquid resist, dry film resist and electrodeposited spray coating. Thicker resist films are better suited for packaging and assembly applications such as bumping and HDI substrates, where metals are several microns thicker than the IC metallization. These are discussed further in Chapter 12.

2.3.5 — Types of Photoresist

There are two types of photoresist materials: a positive acting resist and a negative acting resist. When a positive resist is exposed to uv light of the proper wavelength it undergoes what is referred to as photo-softening and upon developing in a water based solution is completely removed. If a photomask is used during exposure the same pattern on the mask will be transferred to the resist film. With negative resist the reverse takes place. Exposure to uv light results in a photo-hardening or photo-polymerization of the resists. Thus the pattern transferred to the resist will be a reverse tone of the pattern on the mask. The two processes are illustrated graphically in Figure 2-9, and Table 2-2 compares the salient features of each.

Positive resist is used extensively in most IC patterning process, offering several advantages over negative resist, not the least of which is it is environmentally friendly. It also has inherently superior fine feature size capability and is used exclusively whenever line widths less than 1.5 μm are required.



(Courtesy PTI Seminars, Inc.)

Figure 2-9. Positive and Negative Acting Photoresist

Table 2-2. Comparison of Positive and Negative Resists [7]

Positive Resist	Negative Resist
Photo-softening	Photo-hardening
Environmentally Friendly	Biological Hazard
Developer—water based	Developer—solvent based
Fine Line Capability << 1μm	Features < 1μm
Cost—expensive	Cost—low, << positive
Adhesion—poor (requires use of primer)	Adhesion—good (no primer required)

2.3.6 — Exposure Systems for Printing/Imaging

The most common exposure system, (Figure 2-10) consists of an ultraviolet light source and a substrate or wafer holder. When a mask holder and precision stages are added, permitting movement of the substrate and/or photomask for alignment purposes, the system becomes a msk aligner.

Over the years new exposure systems/mask aligners were developed. Each new system addressed elimination of process/equipment generated defects. The various systems used in IC manufacture and the attributes of each follows.

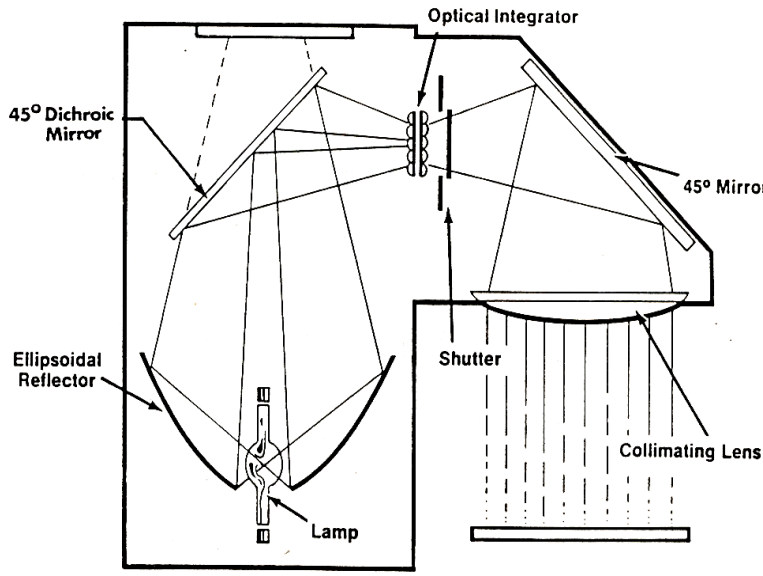
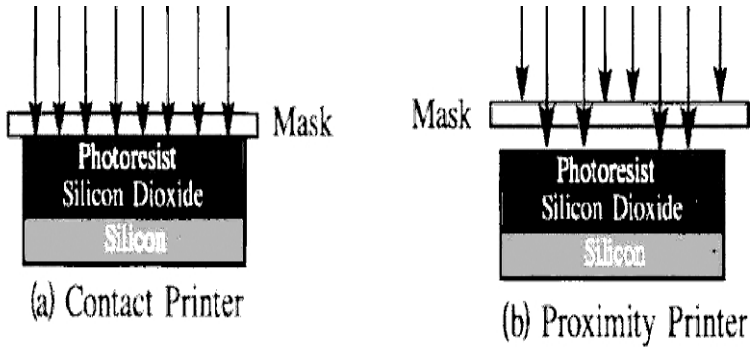


Figure 2-10. The Basic Exposure System [9]

2.3.6.1 — Contact and Proximity Printer

Figure 2-11 schematically illustrates both the contact printer and the proximity or off-contact Printer.

The (contact printer Figure 2-11(a)), was the exposure system in use in early IC manufacturing. For optimum image tranfer from mask to resist, positive contact of mask to the coated wafer is necessary and must be maintained during the entire exposure cycle. This results in damage both to the mask and the resist coating that translates to defective patterns on the wafer and loss of yield.



(Courtesy PTI Seminars, Inc.)

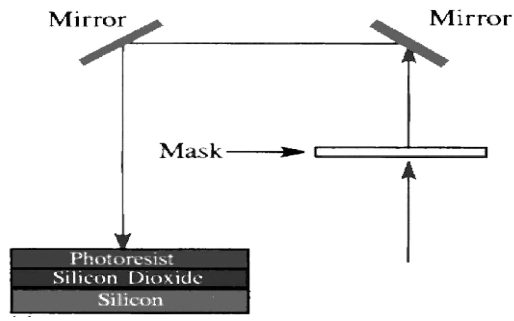
Figure 2-11. (a) Contact Printer; (b) Proximity Printer

To eliminate this problem, the proximity or off-contact printer, (Figure 2-11(b)) was developed. With the mask separated from the wafer (approximately 25µm/ 0.001") damage to the mask and the resist was greatly minimized. However proximity printing resulted in loss of resolution versus contact printing.

2.3.6.2 — The Projection Printer

To address this particular problem, the projection printer, Figure 2-12, was developed.

The projection printer has the photomask completely removed from the wafer. The mask image is optically projected onto the wafer. This is accomplished with greater resolution than achievable with contact printing. The photomask itself is a standard array mask the same as used in contact or proximity printing. The projection printer *totally eliminates* damage to either the mask or the resist coating on the wafer.



(Courtesy PTI Seminars, Inc.)

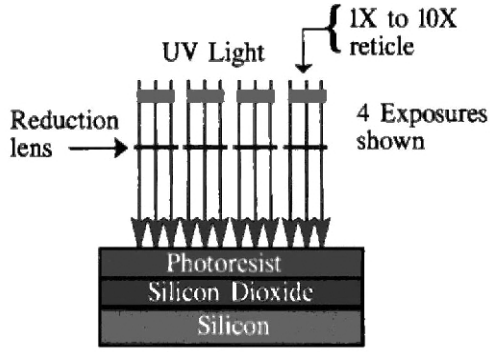
Figure 2-12. Projection Printer

The introduction of a projection printer by Perkin Elmer in the '70s represented a significant advancement in wafer fabrication technology and stands out as a major contributor to the continued development and producibility of ICs with minimum features down to the micron and submicron range, and with exceptionally high yields.

2.3.6.3 — The Wafer Stepper and Step and Scan Projection Systems

Further developments in projection printing are shown in Figure 2-13. In this case, the standard array photomask is replaced by a reticle that contains a single image at 1X. Only one site is exposed to uv at a time. The wafer, which is mounted on a computer controlled x-y table, is programmed to step to the next adjacent site following each exposure. This is repeated until the entire wafer has been exposed. This type of exposure system is known as a "Wafer Stepper".

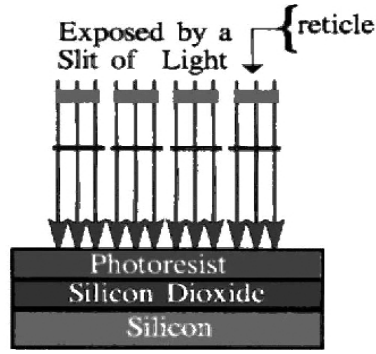
The single image reticle can also be a magnified image up to 10X. Magnified images are optically projected and reduced to 1X at the wafer using a reduction lens inserted in the optical path as shown in the figure.



(Courtesy PTI Seminars, Inc.)

Figure 2-13. The Wafer Stepper Projection System

The "Stepper", in turn, also underwent further development. Since this is a sequential process, it is time-consuming. To overcome this drawback more than one site was added to the reticle and a section of the wafer instead of a single site was being exposed. This "Step and Scan" mode is illustrated in Figure 2-14.



(Courtesy PTI Seminars, Inc.)

Figure 2-14. The Step and Scan Projection System

2.4 — IC Methodologies and Packaging, Assembly, Interconnections

Application of IC process methodologies, aka, the Thin Film process, when applied to packaging, assembly and interconnections, can provide the needed cost-effective, high yield, high density wiring capability. For wafer bumping and WLP, where finished wafers are involved, and where the "added value" is at an absolute maximum, yield loss is untenable and extremely costly. "Near defect-free" processing is therefore essential. When the thin film technology is combined with thick film, cofired ceramic and the laminate PWB manufacturing technologies

(Chapters 13, 14 and 15), it provides for an enhanced capability that effectively extends areas of application for each of the respective technologies.

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