less, synthesis and simulation tool vendors may have optimized package bodies for use with their tools.

Rest assured, however, that there are many more uses for subprograms—some we have explored, others we leave for you to discover—in which the function has not already been standardized or defined.

Problems

7.1. Create an i2std (integer to std_logic_vector) function similar to the one for i2bv function.

7.2. Overload the + operator for operands of type std_logic_vector (see myops package, page 392)

7.3. Compile and synthesize the following design, using the myops package of Listing 7-11.

```
use work.myops.all;
entity add is port(
   a, b: bit_vector(15 downto 0);
   x:    out bit_vector(15 downto 0));
end add;
architecture add of add is
begin
   s <= a + b;
end;
```

7.4. Compile and synthesize the design of Problem 7.3, modified to use Warp's bit_arith package. Compare the results with those of Problem 7.3. Does module generation provide an advantage?

7.5. Create a procedure for decrementing bit_vectors. Also, create an underflow output for the procedure.

7.6. What are the disadvantages of using a procedure versus instantiating a component?

7.7. Rewrite the bv2i function shown in Listing 7-2 to interpret the value on the left of the bit-vector as the MSB.

7.8. Write a procedure to perform a 16-bit even parity check. Synthesize this design for a MAX340 CPLD. Select retain XORs under device options.