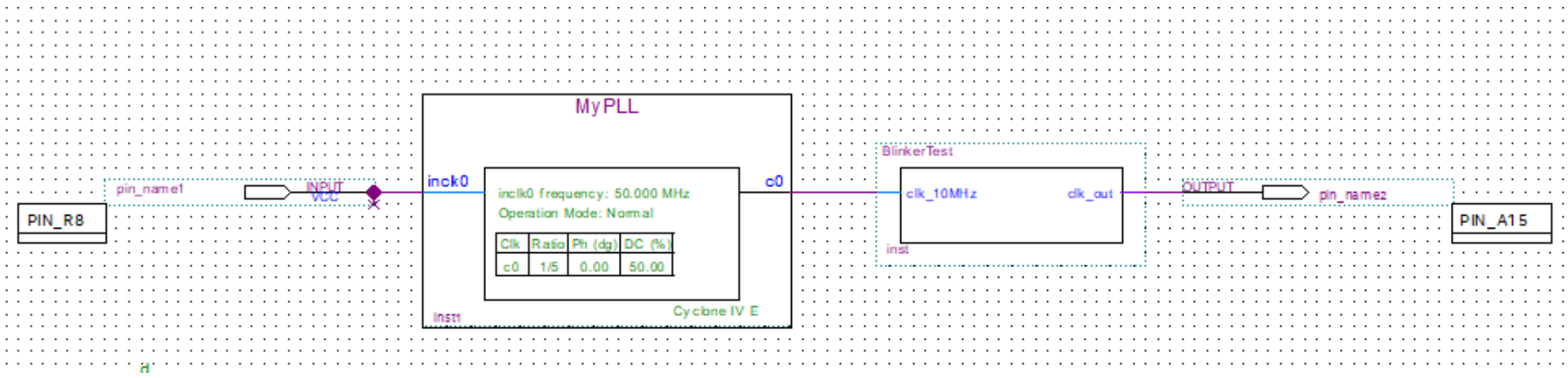
Main Activity

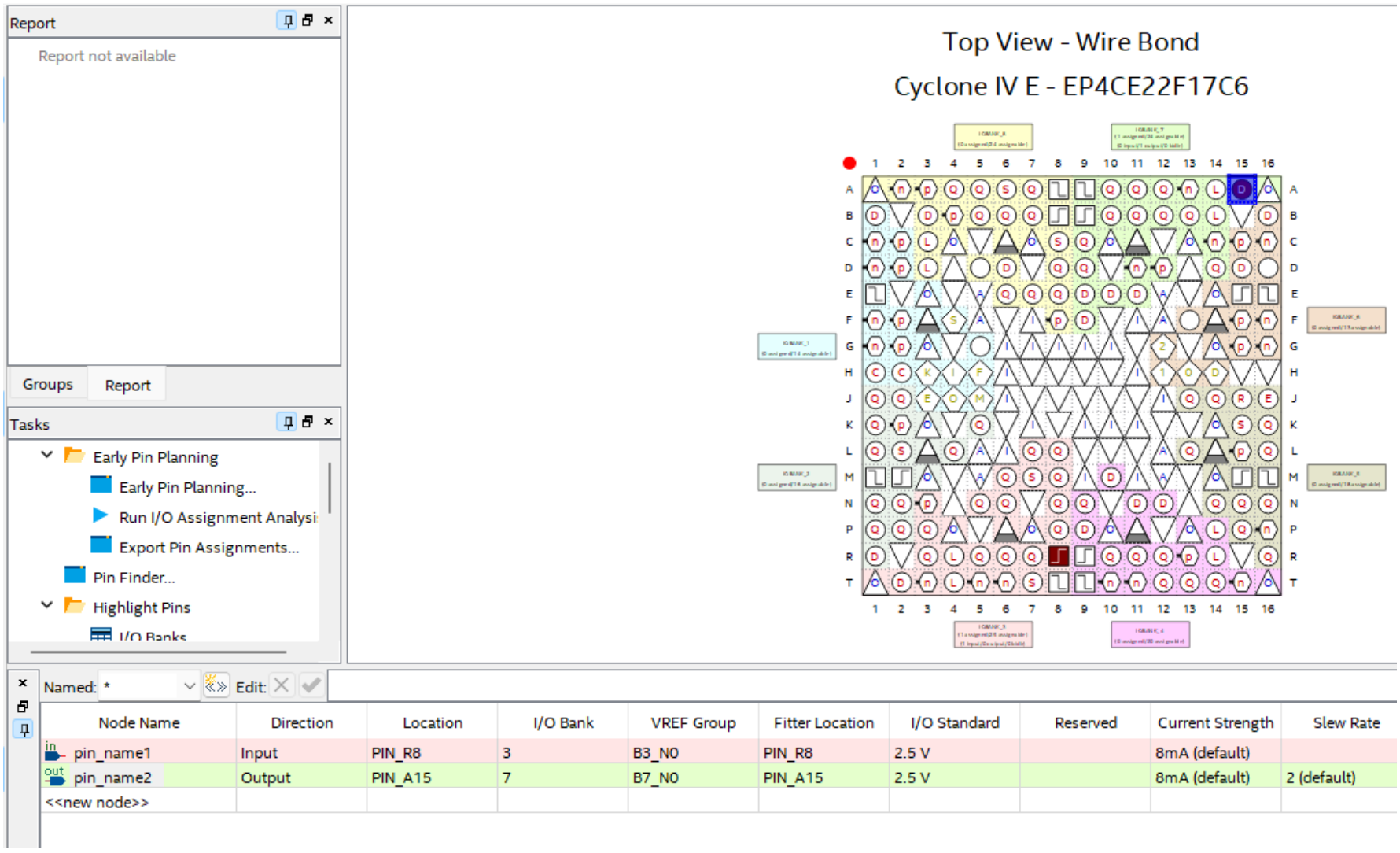
BlinkerTest Code

```
1   -- Library declaration
2
3   library ieee;
4   use ieee.std_logic_1164.all;
5   use ieee.numeric_std.all;
6
7   -- Entity declaration
8
9   entity BlinkerTest is
10     port(
11           clk_10MHz: in std_logic;
12           clk_out: out std_logic
13           );
14  end entity;
15
16  architecture behave of BlinkerTest is
17
18  -- Signal declaration
19
20  signal clk_1Hz: std_logic := '0';
21  signal scaler: integer range 0 to 5000000;
22
23  begin
24
25  -- Process used to scale down the 10 MHz frequency from the PLL to a 1Hz rate.
26
27  clk_1Hz_process: process(clk_10MHz)
28  begin
29     if(rising_edge(clk_10MHz)) then
30           if (scaler  < 5000000) then
31              scaler <= scaler + 1;
32           else scaler <= 0;
33           clk_1Hz <= NOT(clk_1Hz);
34           end if;
35        end if;
36     end process clk_1Hz_process;
37
38  clk_out <= clk_1Hz;
39
40  end behave;
```

BlinkerTest_TopLevel Schematic



Pin Planner Window



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate
in pin_name1	Input	PIN_R8	3	B3_N0	PIN_R8	2.5 V		8mA (default)	
out pin_name2	Output	PIN_A15	7	B7_N0	PIN_A15	2.5 V		8mA (default)	2 (default)
<<new node>>									

Bonus

Problem Statement

For an additional 5 points of bonus credit, I have satisfied the following problem statement.

Modify your BlinkerTest code so that it reads one of the slide switched on the DE0-Nano board and depending on the switch setting makes the LED blink at 1 Hz or 2 Hz rate. This does not require any change to MyPLL but will require changes to both BlinkerTest code and to BlinkerTest_TopLevel schematic. You should send the BlinkerTest code, BlinkerTest_TopLevel schematic and pin planner screen shots to support your bonus activity. These can be in a separate file or in the same file as the main project content.

Approach

In order to modify the BlinkerTest code and ensure that the code changes propagate to the final .sof, I must take the following steps.

1. Modify BlinkerTest with the new functionality: Accept an input from an on board switch and use this input to switch between 1 and 2 Hz.
2. Recompile BlinkerTest
3. Recompile BlinkerTest_TopLevel
4. Compile a .sof output file and program the board for testing.

Record

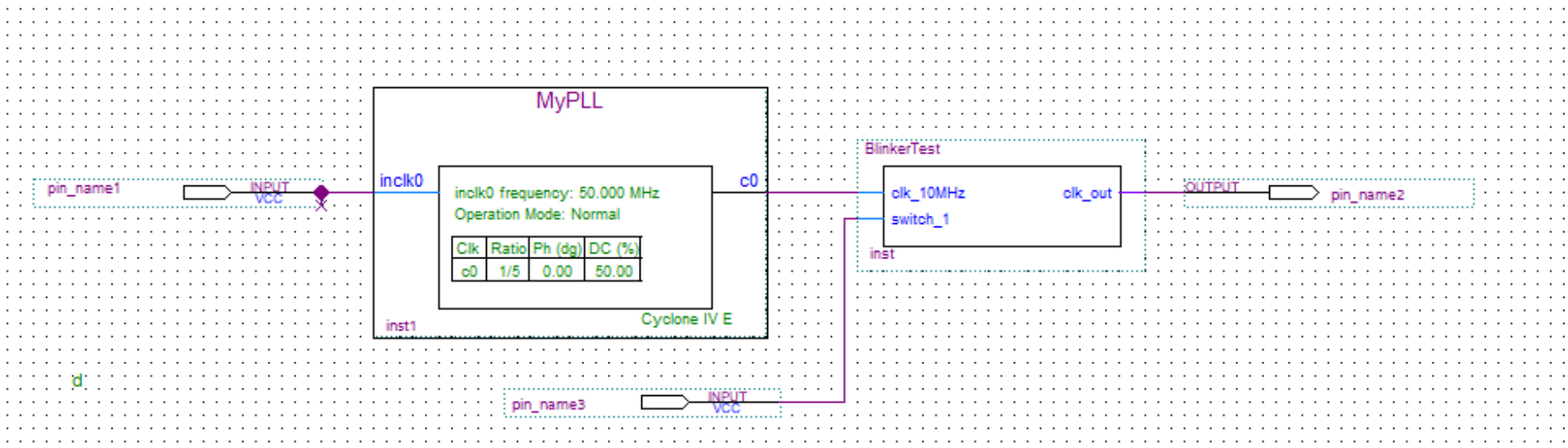
First, I will close the BlinkerTest_TopLevel project and open the BlinkerTest.qpf file. I wrote the following modified code for BlinkerTest.vhd

Modified BlinkerTest Code

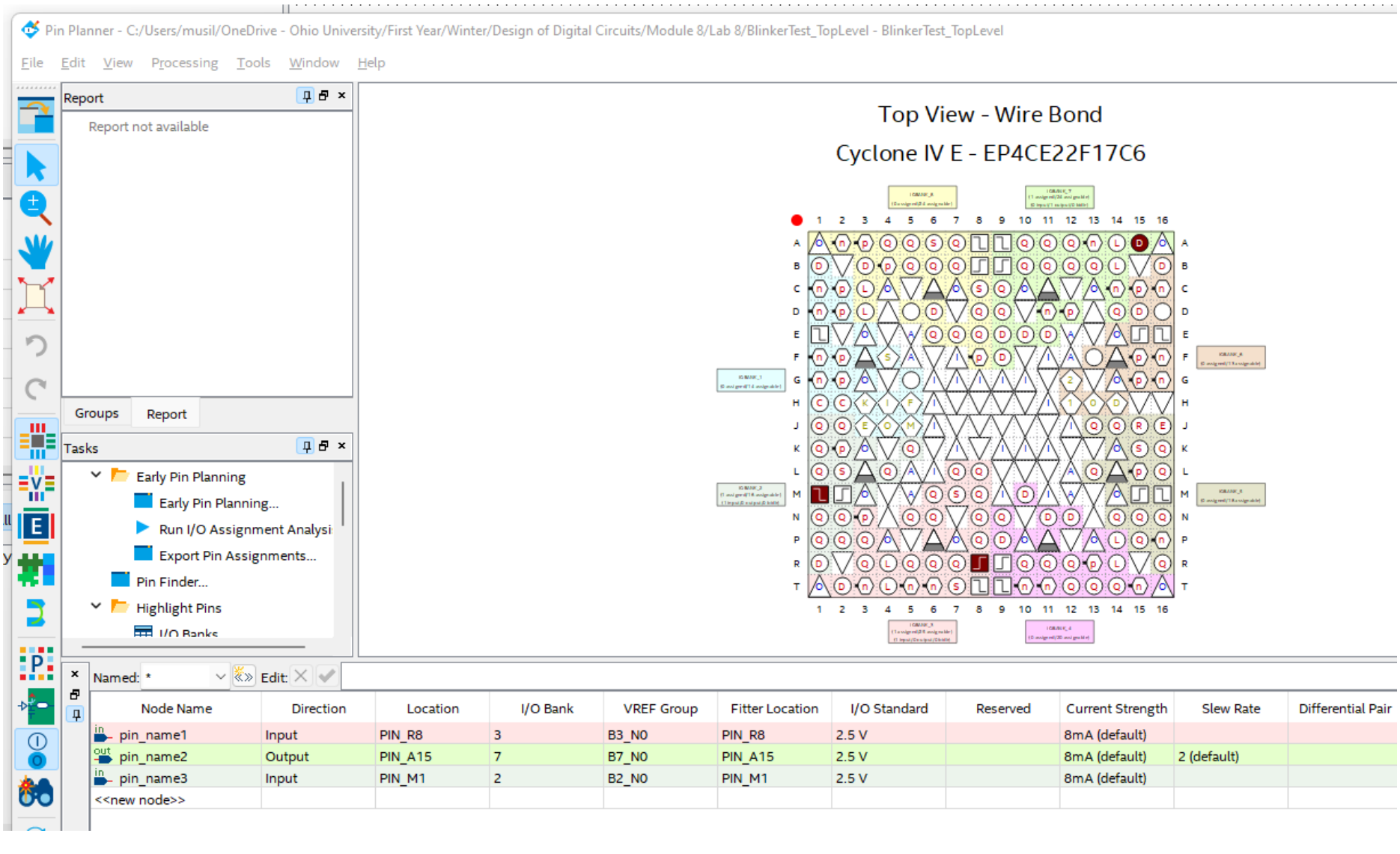
BlinkerTest.vhd

```
1   -- Library declaration
2
3   library ieee;
4   use ieee.std_logic_1164.all;
5   use ieee.numeric_std.all;
6
7   -- Entity declaration
8
9   entity BlinkerTest is
10     port(
11           clk_10MHz: in std_logic;
12           switch_1: in boolean;
13           clk_out: out std_logic
14           );
15  end entity;
16
17  architecture behave of BlinkerTest is
18
19  -- Signal declaration
20
21  signal clk_1Hz: std_logic := '0';
22  signal clk_2Hz: std_logic := '0';
23  signal scaler: integer range 0 to 5000000;
24  signal second_scaler: integer range 0 to 2500000;
25
26  begin
27
28  -- Process used to scale down the 10 MHz frequency from the PLL to a 1Hz rate.
29
30     clk_process: process(clk_10MHz, switch_1) is
31     begin
32        if(rising_edge(clk_10MHz)) then
33
34           if (NOT(switch_1) AND (scaler  < 5000000)) then
35              scaler <= scaler + 1;
36           elsif switch_1 AND (second_scaler < 2500000) then
37              second_scaler <= second_scaler + 1;
38
39        else
40           if NOT(switch_1) then
41              scaler <= 0;
42              clk_1Hz <= NOT(clk_1Hz);
43              clk_out <= clk_1Hz;
44           else if switch_1 then
45              second_scaler <= 0;
46              clk_2Hz <= NOT(clk_2Hz);
47              clk_out <= clk_2Hz;
48           end if;
49        end if;
50     end if;
51     end if;
52     end process clk_process;
53
54
55
56  end behave;
```

Modified BlinkerTest_TopLevel Schematic



Modified Pin Planner



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair
in pin_name1	Input	PIN_R8	3	B3_N0	PIN_R8	2.5 V		8mA (default)		
out pin_name2	Output	PIN_A15	7	B7_N0	PIN_A15	2.5 V		8mA (default)	2 (default)	
in pin_name3	Input	PIN_M1	2	B2_N0	PIN_M1	2.5 V		8mA (default)		
<<new node>>										