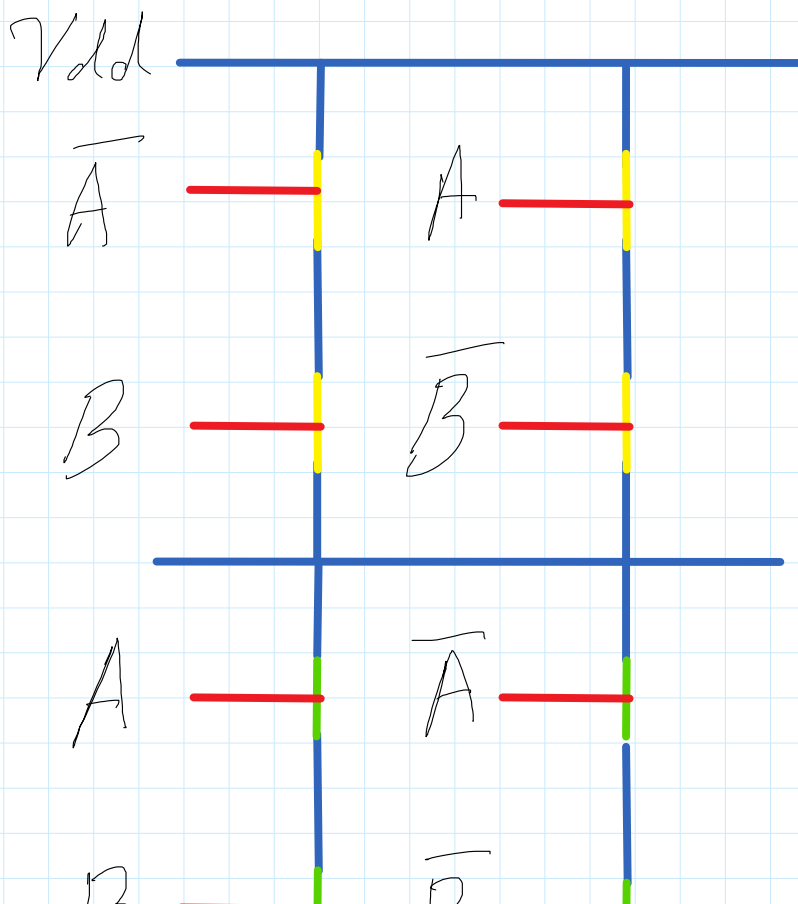
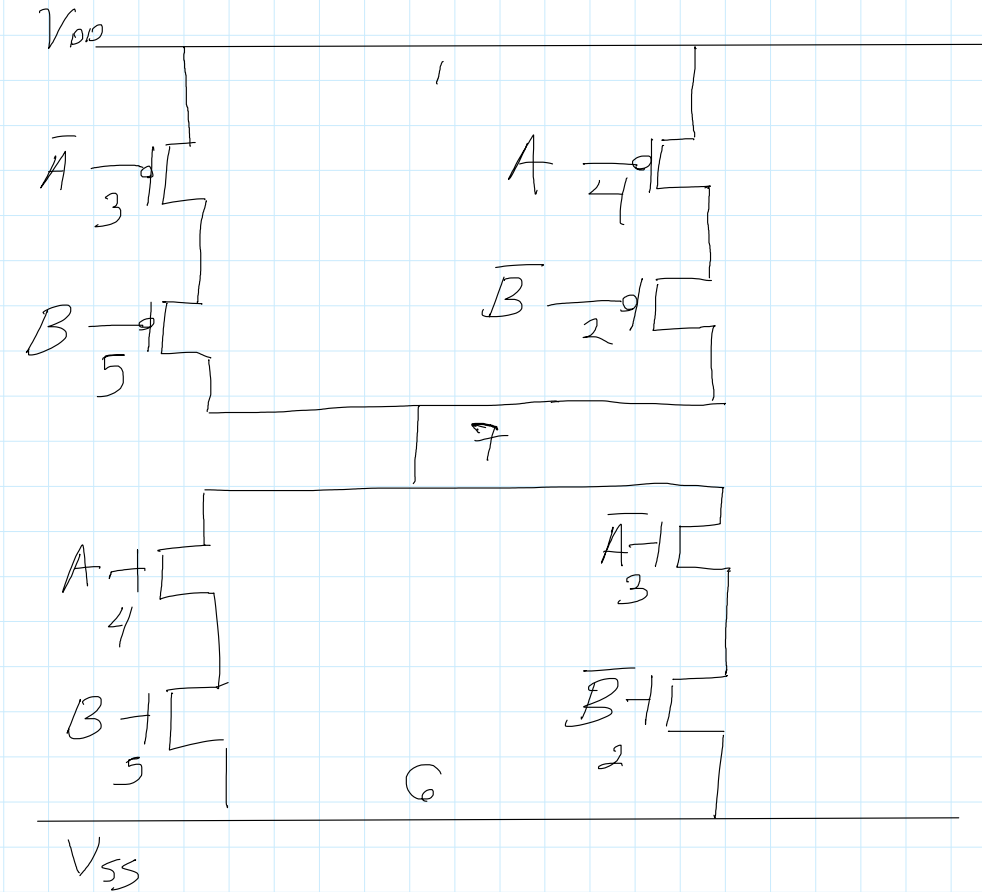
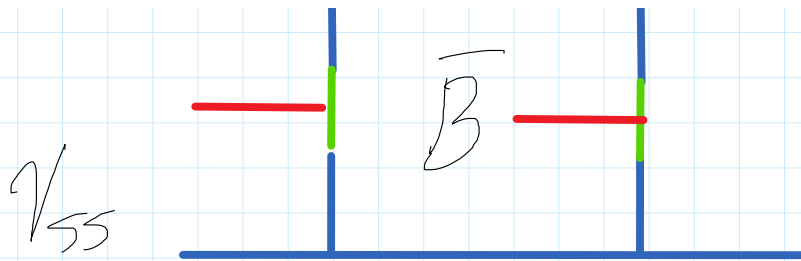
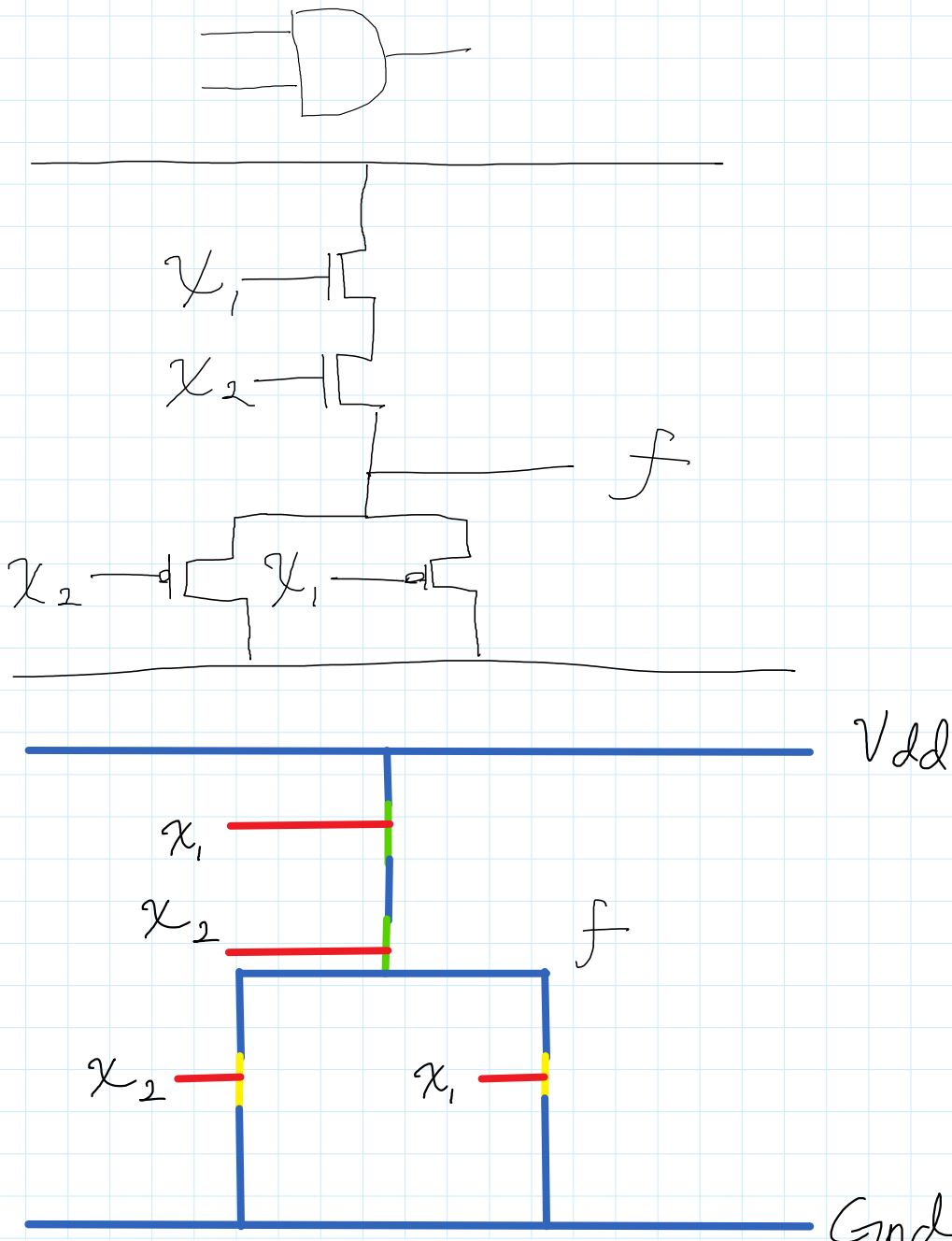
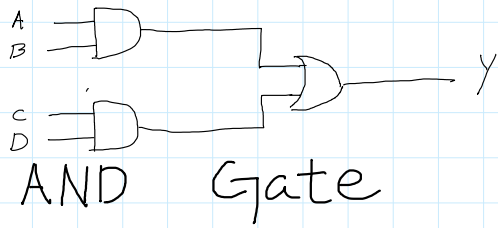


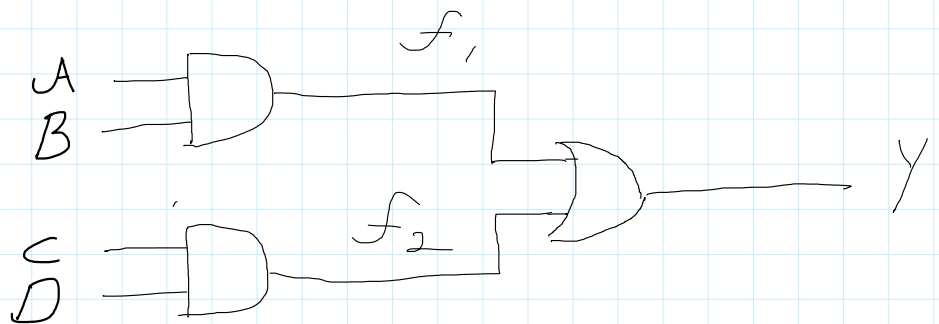
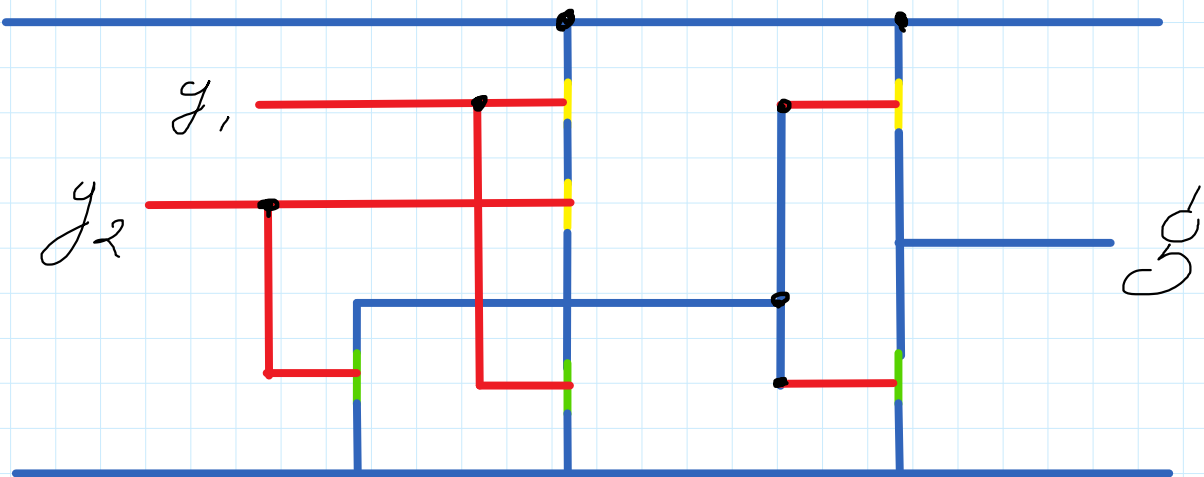
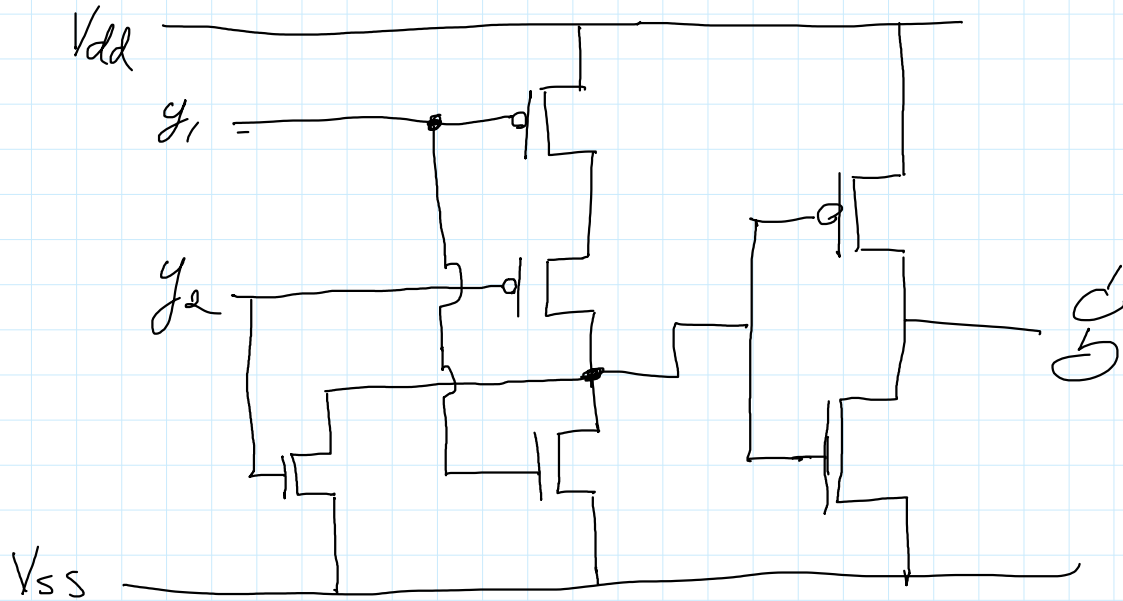
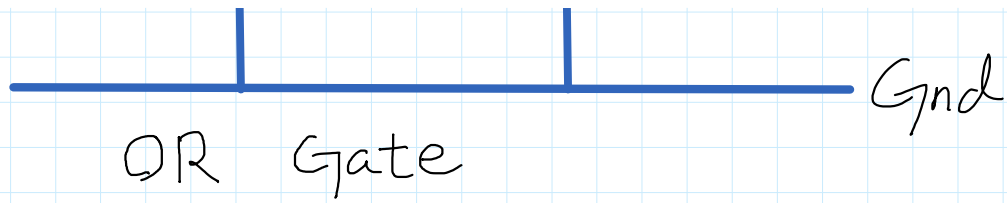
Q1. Sketch a CMOS layout for the XOR function.

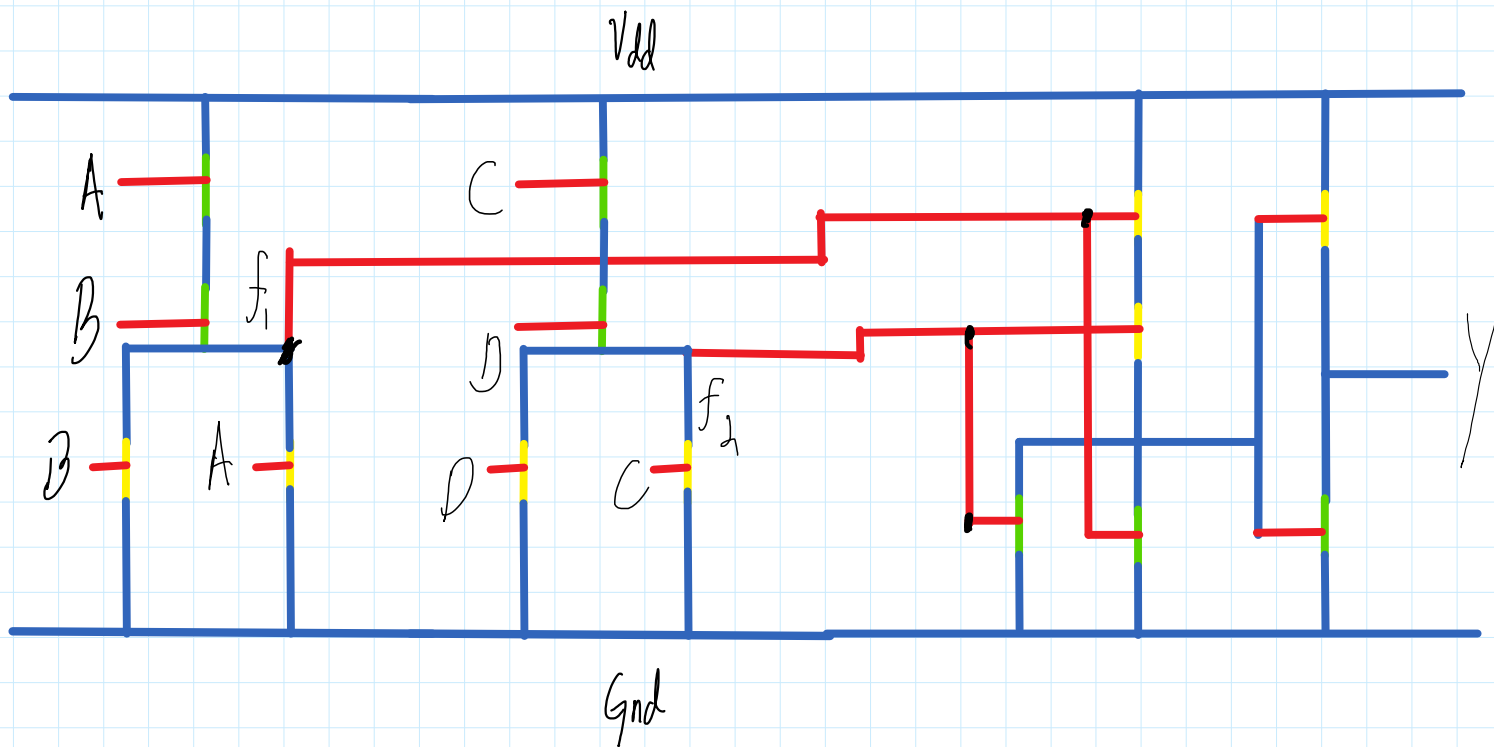




Q2. Sketch CMOS layout for a two 2-input AND gates with their outputs connected to a 2-input OR gate. Do this using both AND and OR gates and then using only NAND gates.







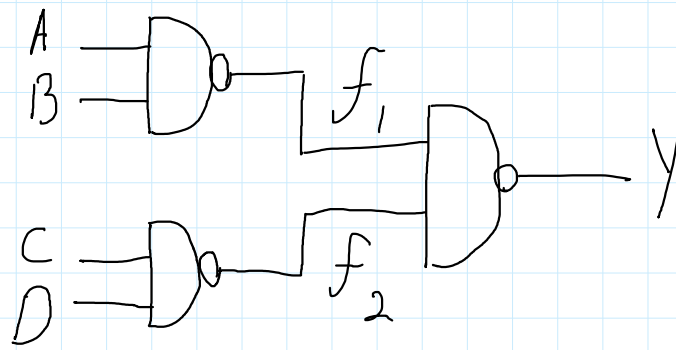
NAND method

$$Y = AB + CD$$

$$\overline{Y} = \overline{AB + CD} = \overline{AB}(\overline{CD})$$

$$Y = \overline{\overline{Y}} = \overline{\overline{AB}(\overline{CD})}$$





NAND Gate

