Module 1 Homework

Problem 4

Explain the differences between continuous-time, discrete-time, and digital signals in terms of mathematical and physical representations.

Continuous-time and discrete-time are mathematical paradigms for viewing the way a signal exists. Digital signals are a data-type and have tangible properties like word-length and floating-point precision. So, it is important to clarify how I have interpreted the prompt and how I will approach the response. The prompt has been be decomposed into several subsections.

1. Discrete time as a representation of the true signal - *Explain the difference between continuous-time and discrete-time mathematical representations.*
2. Comprises made by the ADC - *Briefly review the truncation process and how it relates to effectively processing a real-valued source function.*
3. Physical representations - *Discuss the two modeling pidgin languages used for analog and digital diagramming.*

Discrete time as a representation of the true signal

Figure 1 shows an example of a time domain function with a continuous domain and range.

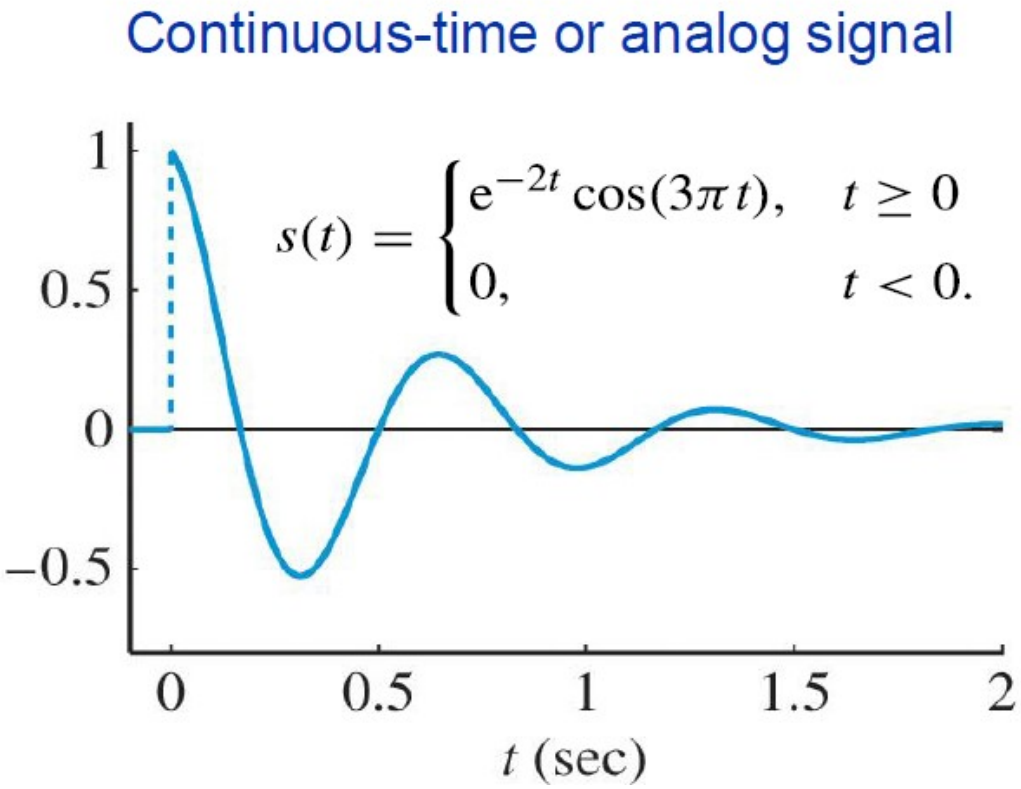

Figure 1: A decaying continuous oscillation.

Such a continuous time domain function is often **mathematically represented** as follows.

$$t \in \mathbb{R} \tag{1}$$

$$f(t) \in \mathbb{C} \tag{2}$$

Some time domain transforms that are regularly performed on continuous time signals include

Fourier Decomposition

$$F = \int_{-\infty}^{\infty} f(t) \cdot e^{-i2\pi ft}\, dt. \tag{3}$$

Convolution

$$g = f * x \tag{4}$$

The same function put forth in the previous subsection can be sampled periodically by altering our input variable.

$$t = nT \tag{5}$$

where t is continuous time, $n < N$ is your sample domain and T is the sampling period. The sample and hold function above will create a discontinuous function of n. Note that this equation 5 does not transform the range of $f(nT)$. This results in the following graphic.

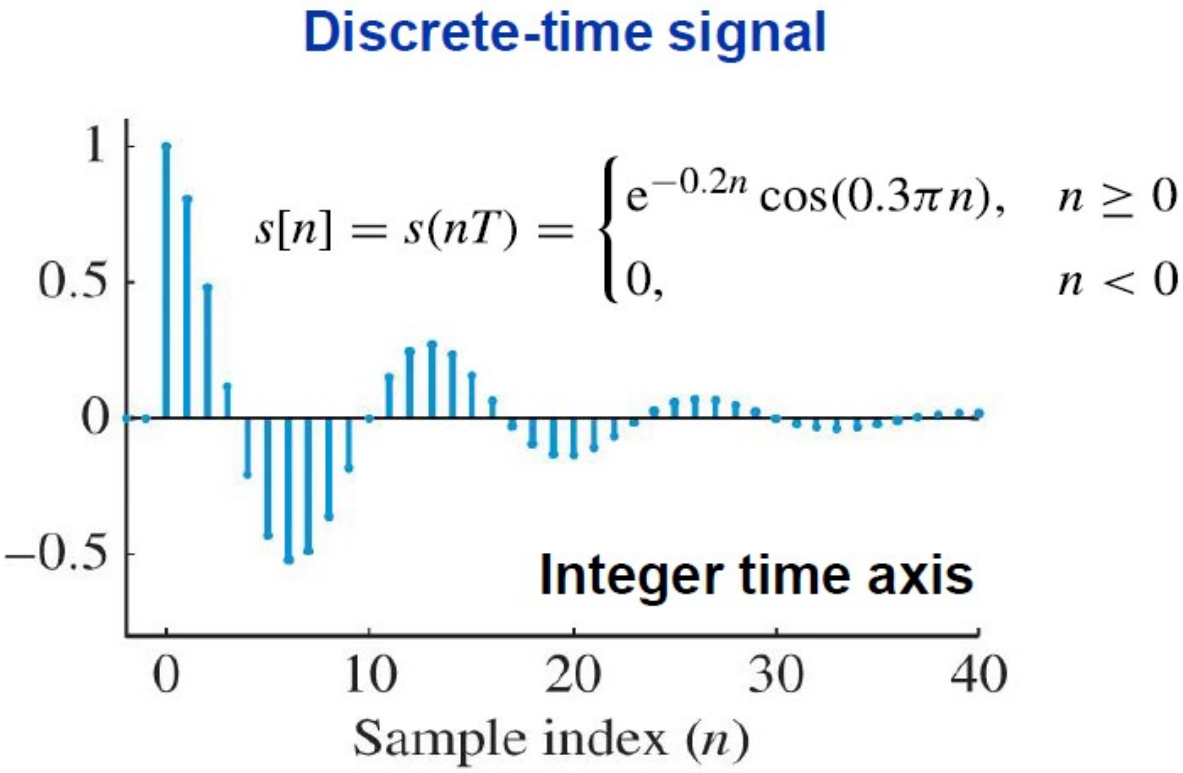

Figure 2: We can realize a function with integer domain and complex range using equation 5.

Comprises made by the ADC

Let's take stock of what we've accomplished in our journey to the digital domain.

- We now have a time-domain function which can be indexed by an integer counter.
- We do NOT have an acceptable input format to our computer.

The issue remains that our discrete-time signal is not usable by a computer, because it is not in floating point representation. In order to accomplish this we will perform two steps.

1. Sample and hold the analog value $f(n * T)$ so that a window of time exists during which the analog to digital converter may read and estimate the value.

2. We will then simulate the results of the limited dynamic range of the analog to digital converter. We will truncate our real-valued function $f(n * T)$ and attain a useful floating point number that can be then handed off.

$f(nT)$ will be sampled using a sample-and-hold circuit.

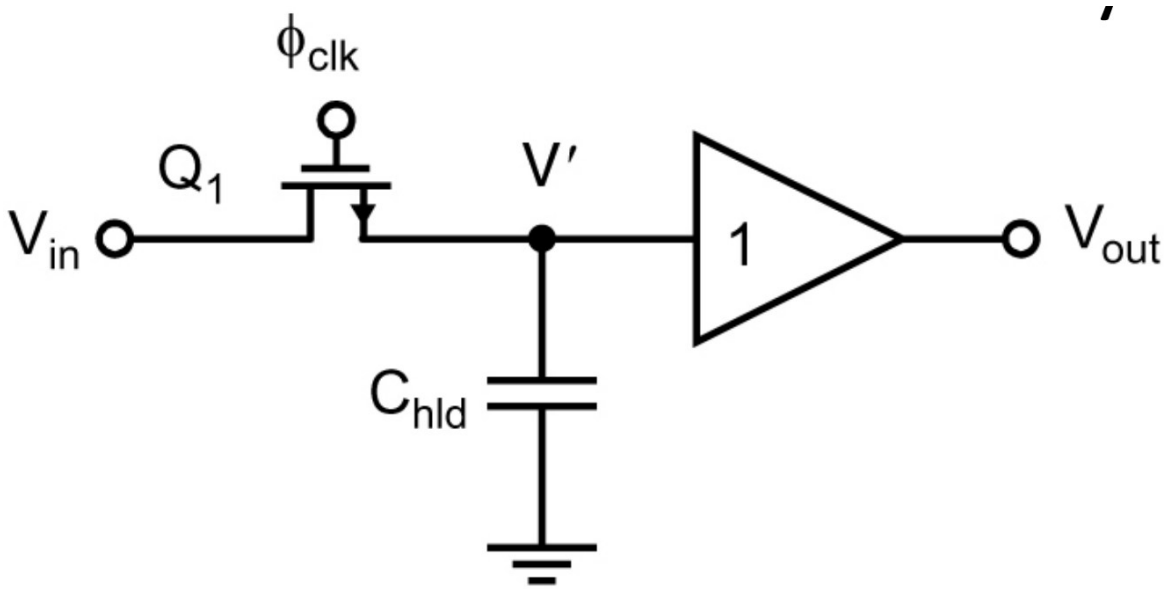

Figure 3: A simple sample and hold circuit used .

This results a staircase pattern at the C_{hld}'s North terminal.

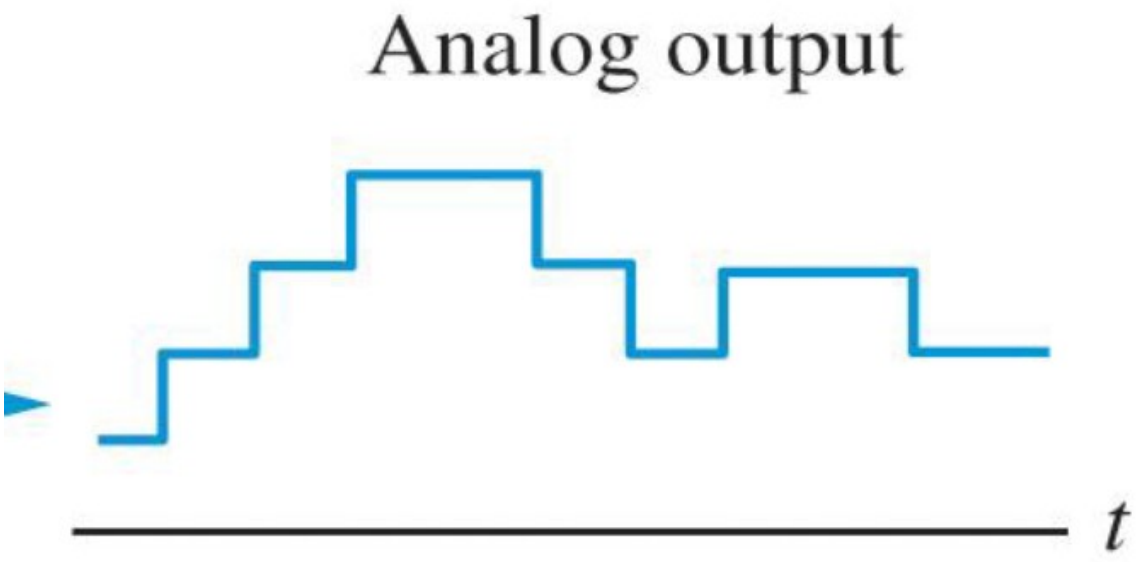

Figure 4: A function which has been sampled and held.

The analog to digital converter reads the samples during the window T and generates a stream of words describing per the following equation.

$$f_{digital}(n) = \frac{2^N V_{In}(t)}{V_{ref}} \tag{6}$$

Physical representations

When digital or analog design are modeled, engineers tend to use proprietary pseudo-modeling languages with pidgin-like vocabulary varying from practitioner to practitioner. So, describing the differences is an inexact pursuit. The critical difference is that analog systems use a standard set of element symbols to represent common components and digital block diagrams tend to use only rectangles. A mixed signal system using both symbolic sets is shown below.

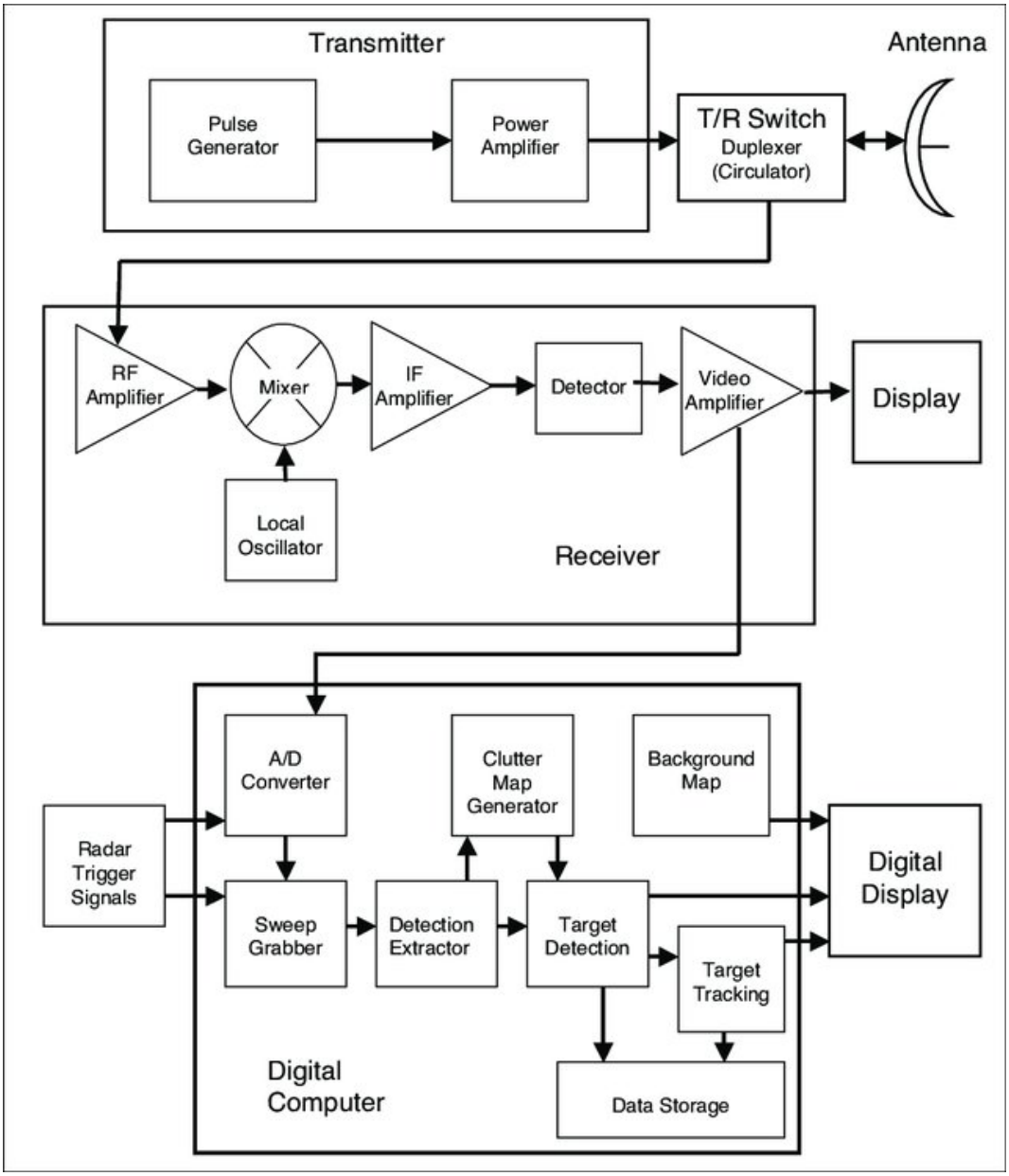

Figure 5: An example of how two separate symbol sets are used.

Problem 8

Why do we need interface systems and where do we need them? Provide a block-diagram description of such systems needed in signal processing.

Sometimes, the phenomena of interest in highly complex and integrated information systems are continuous phenomena. We need interface systems so that we can sample real-valued signals without loss of generality.
Consider a radar receiving as input a time-varying voltage which is a function of the target reflector size and position as well as other properties that are manifested in either the phase or magnitude information encoded in the demodulated quadrature and in-phase sinusoids (I and Q). This radar can be designed as a mixed signal device.

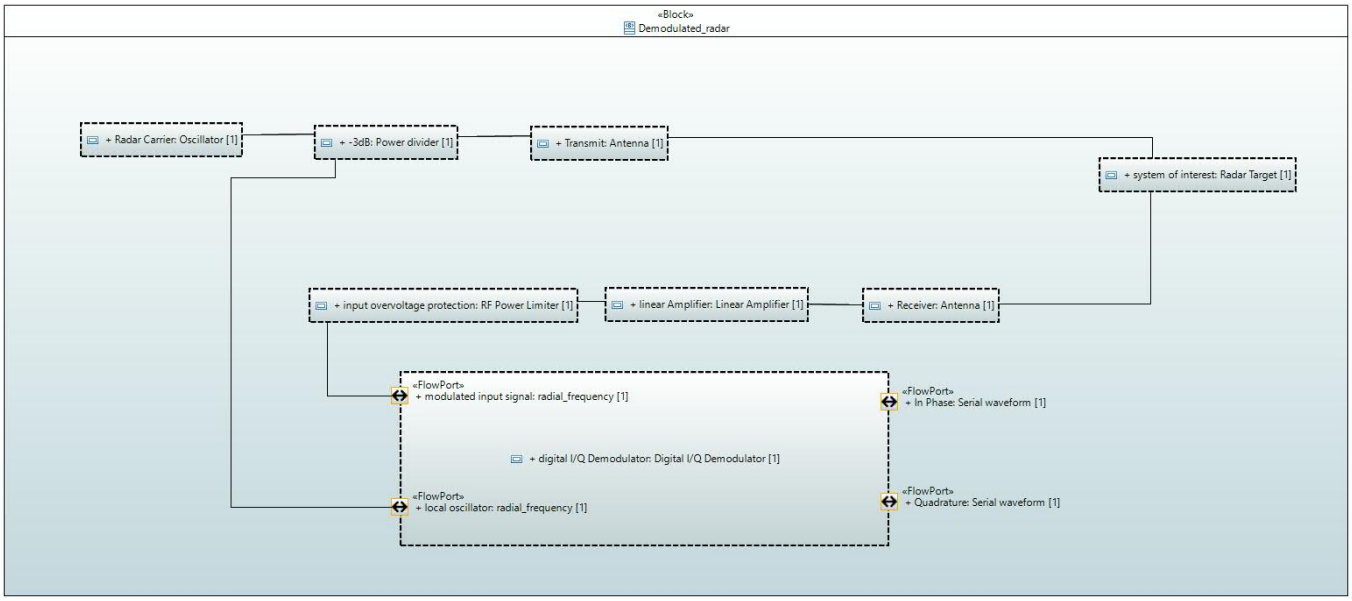

Figure 6: A digital demodulator in context.

My answer to problem 15 will discuss the marked advantages of the such a design. The following internal block diagram shows a design for a digital demodulator.

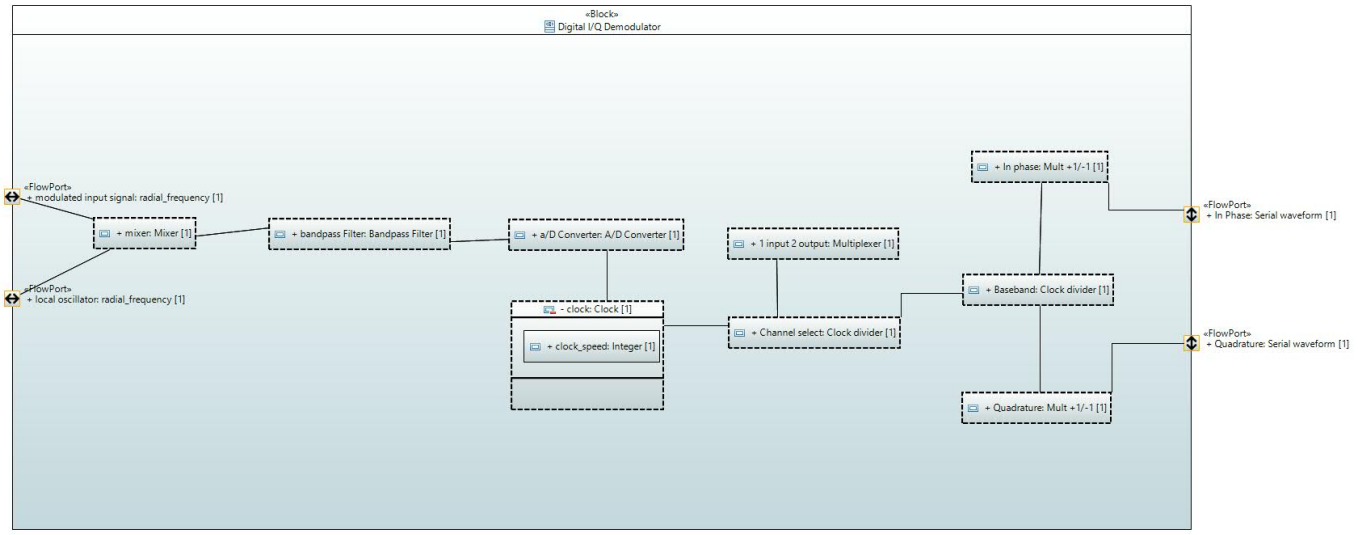

Figure 7: The internal components used to construct a digital IQ demodulator[1]

Problem 15

Why is DSP (digital signal processing) preferred over ASP (analog signal processing)? Are there any disadvantages?

The following example explains the disadvantages of analog signal processing as well as why a signal processing engineer would prefer to use a digital system to accomplish the same task. The following internal block diagram shows the major modules of an ASP radar receiver performing direct IQ demodulation.

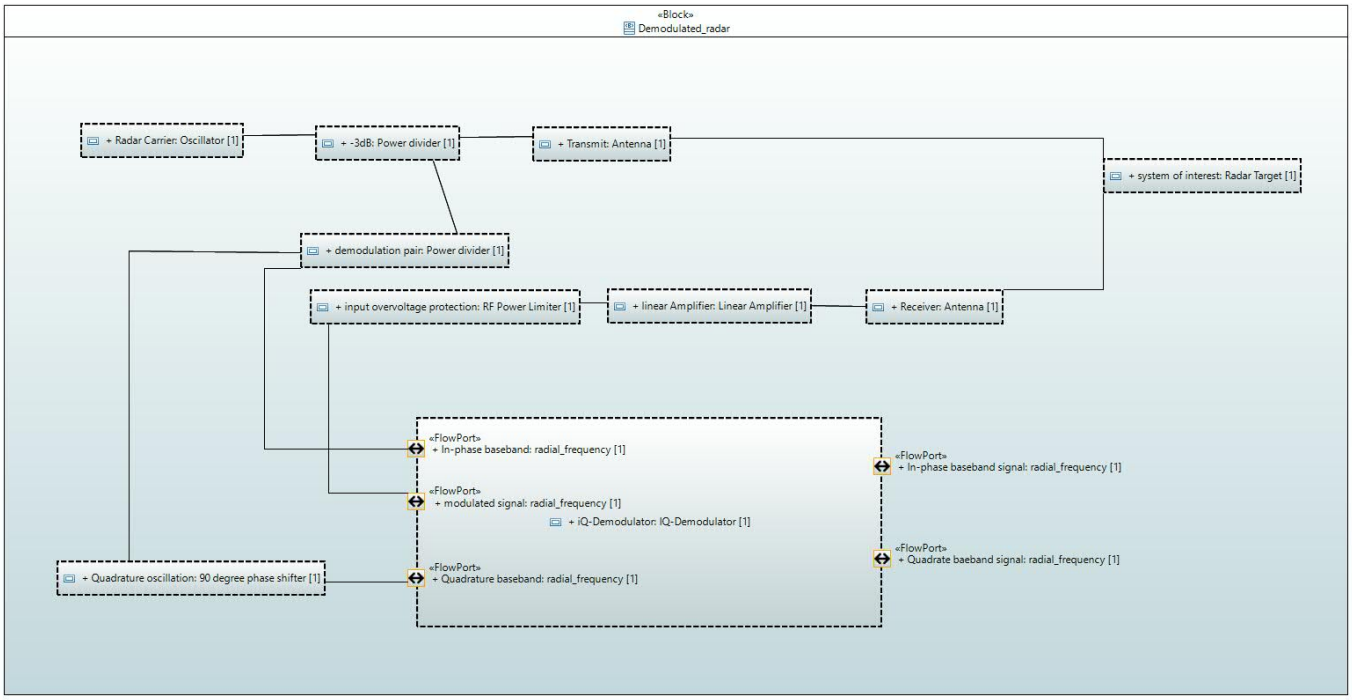

Figure 8: A diagram displaying an analog signal processor accomplishing the task of demodulating the radar return before providing that to the digital filters.

This diagram shows the internals of an analog IQ demodulator.

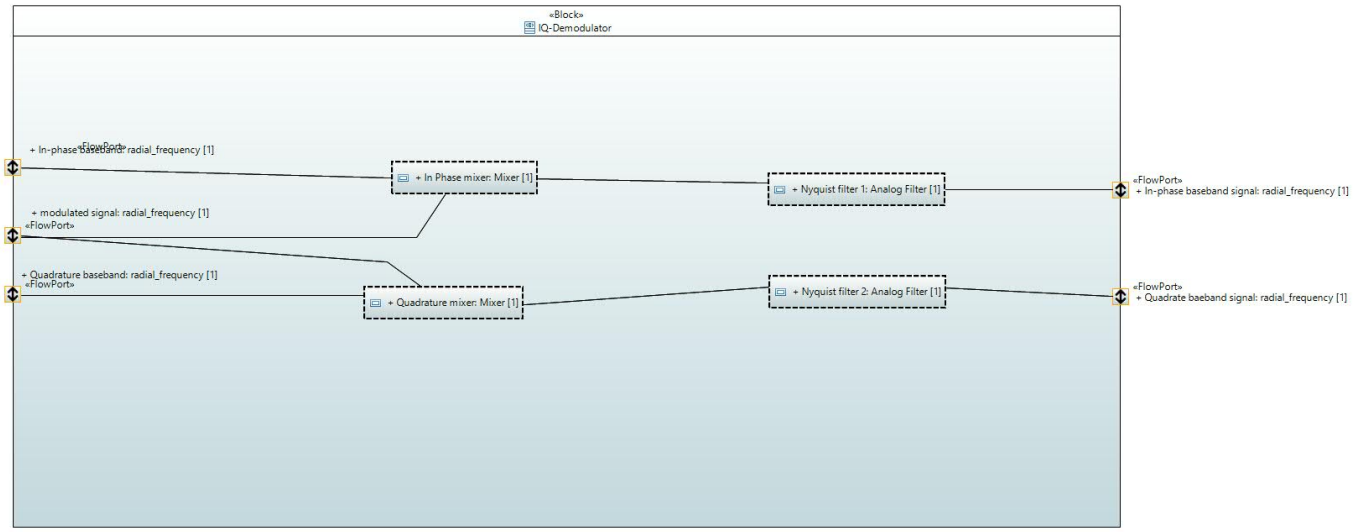

Figure 9: The internal components used to construct an analog IQ demodulator

Reference [1] states that "When implemented with conventional RF components, a number of inherent errors can degrade the I/Q Demodulator performance, including gain balance, quadrature-phase balance, DC offsets, impedance match, and carrier leakage."
Already there are a plethora of issues that have arisen in our relatively simple analog signal processor. All of these problems will manifest themselves as an incorrect estimate on the output of the analog to digital converter. Once, however, the signal has reached the safety of the digital domain, the noise factor decreases substantially for each successive processing stage. In contrast, it is not uncommon for each stage in an analog system to inject noise into its signal on the order of -60dB. Although this is a minimal amount of noise, it is important to recognize that modern systems are expected to derive performance from faint signals at great distances from their transmission point. Cellphones, for example, are expected to provide broadband internet access throughout their roaming area.
To raise the fidelity of our radar receiver, we need to decide which components can be replaced with a digital twin. As a matter of fact, the majority of our system is going to stay as it was designed. The oscillator is, of course, irreplaceable by a digital equivalent. Furthermore, it is worth our resources to keep the linear amplifier and RF power limiter in order to ensure that the analog to digital receiver is operating within its complete dynamic range. Those components (antenna, linear amp, power limiter, oscillator) should all be high quality items that do not significantly impact the signal to noise ratio.
Here is our mixed signal design.

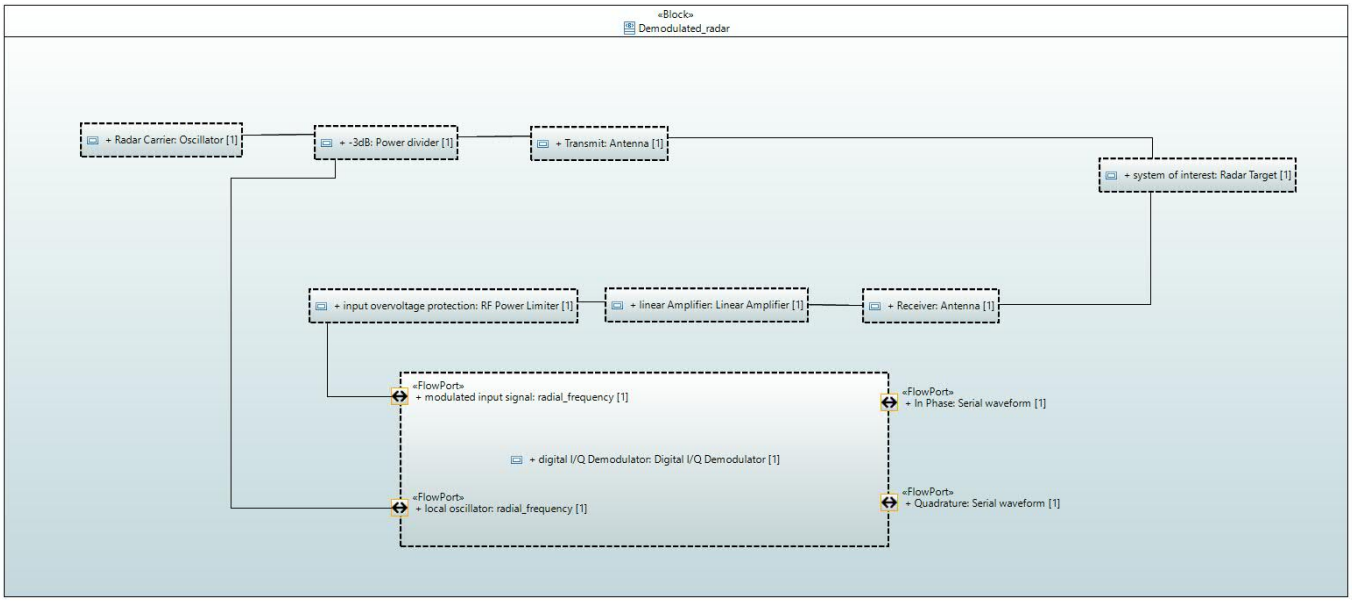

Figure 10: A digital demodulator design.

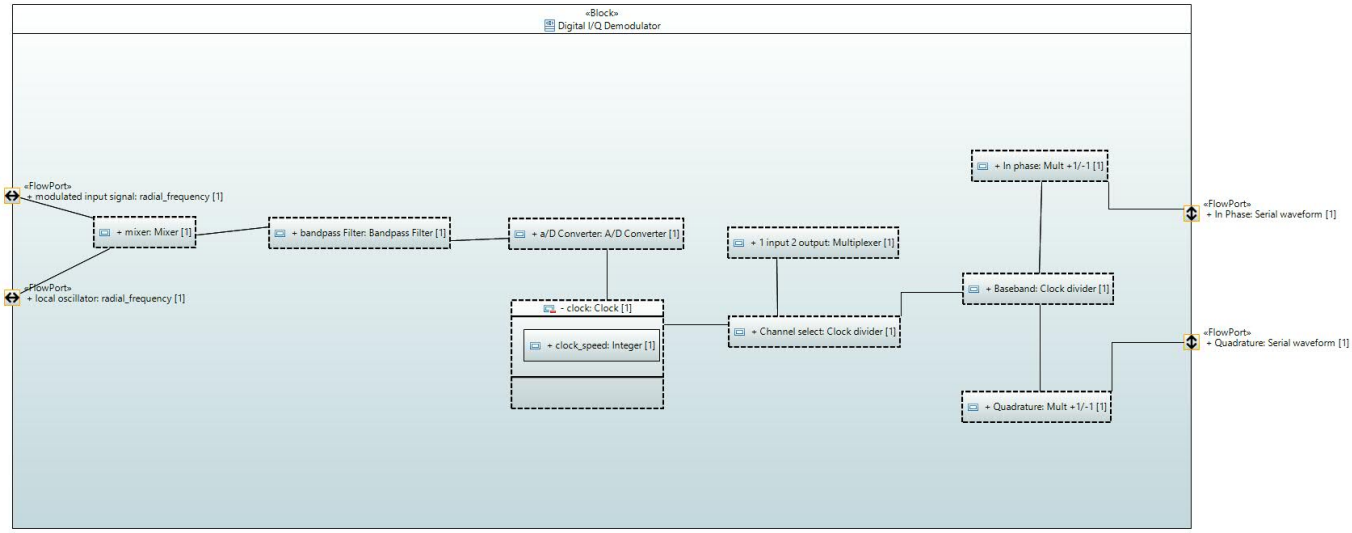

Figure 11: Digital IQ demodulator internals[1]

Notice that in figure there are significantly fewer components than in figure 8. Previously, we reasoned that it is a worthwhile investment to acquire high quality, low noise-factor analog components. These can easily range in the thousands of dollars for a signal packaged RF device. By contrast, the elements used to construct the design in figure are inexpensive at a per-function cost level. It must be ceded that some DSP systems are quite expensive. However, it is important to recognize that DSP processes can be made into monolithic functional packages which results in the same operation (for example demodulation) being performed at a fraction of the price.

Furthermore, the transition to the digital domain opens up more data handling options. Depending on write-speed of the DSP controller, the raw ADC data could be captured and stored concurrent to any real-time signal conditioning that takes

place. As technologies utilizing signal processing increase in frequency, the consumer expects that state of the art functions (such as state space tracking and machine learning) will be present on an average DSP processor. Application level development projects such as tensorflow are designed to perform optimally in dedicated DSP hardware. Integrating with TensorCore is greatly simplified when the TensorCore can be directly mounted to a proprietary digital signal processing circuit board.

Bibliography

[1] C. Ziomek and P. Corredoura, "Digital i/q demodulator*," 1996.