4.11. Build a 16-bit down-counter with synchronous load and asynchronous reset. The outputs are three-state outputs, controlled by two separate signals—one for the lower 8-bits and one for the upper 8-bits. Inputs: `clk`, `reset`, `load`, `data[16:0]`, `upper_enable`, `lower_enable`; output: `count[15:0]`.

4.12. What are the names of the standard VHDL package and function necessary for the following comparison to not always evaluate to false?

```
signal a: std_logic_vector(4 downto 0)
if a= "0011" then...
```

4.13. Find the errors in the following code:

```
architecture has_errors of design
begin
p1: process
   begin
      if clk'event and clk = '1' then
         q <= a or b and c;
      end if;
   end;
end;
```

4.14. Write an entity declaration and architecture body pair for each of the TTL devices in Table 2-1.

4.15. Do all processes require sensitivity lists? Can you declare a clocked process without a sensitivity list?