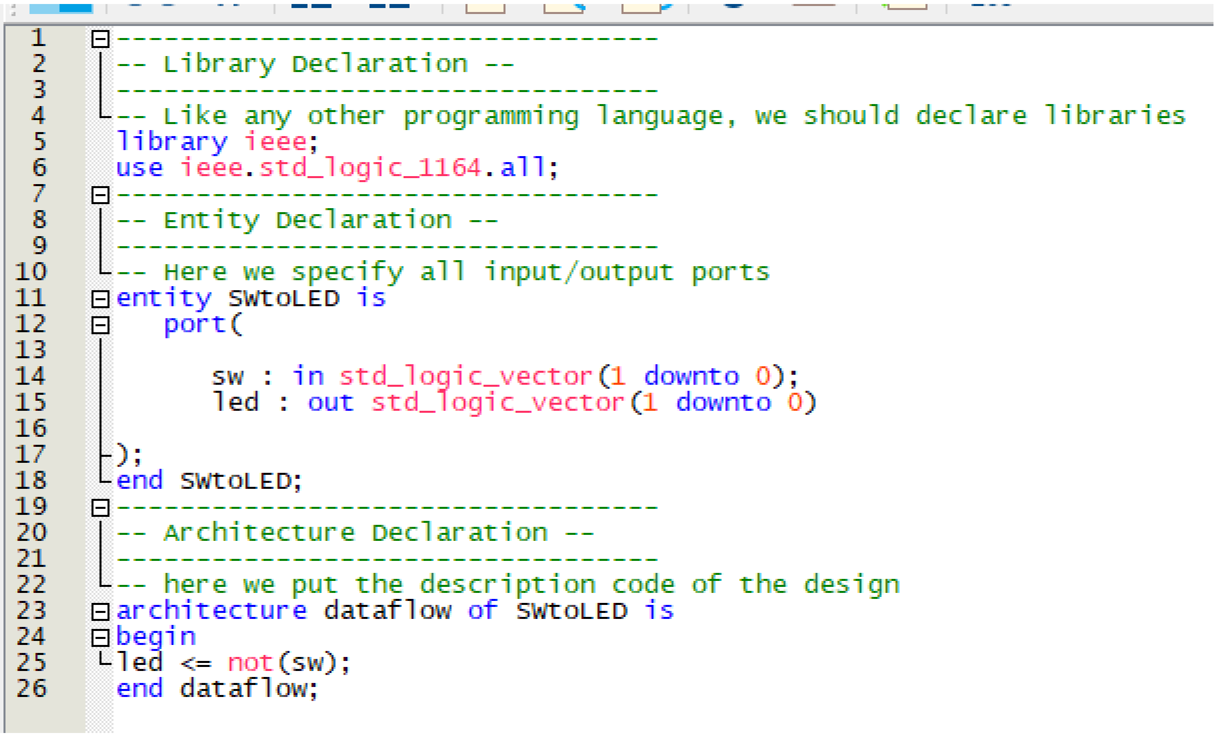
Mark Musil
Ohio University

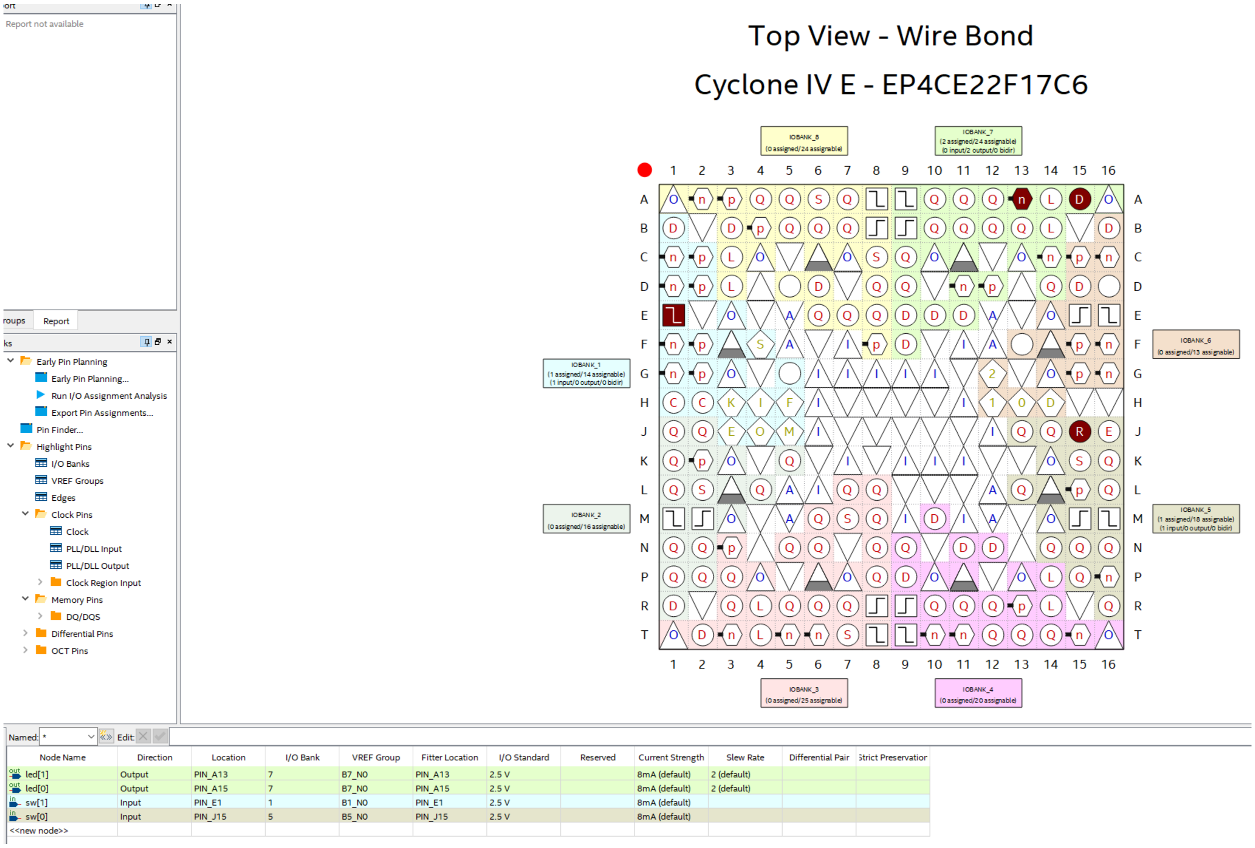
Design of Digital Circuits
Lab 4

February 2022

Part 1

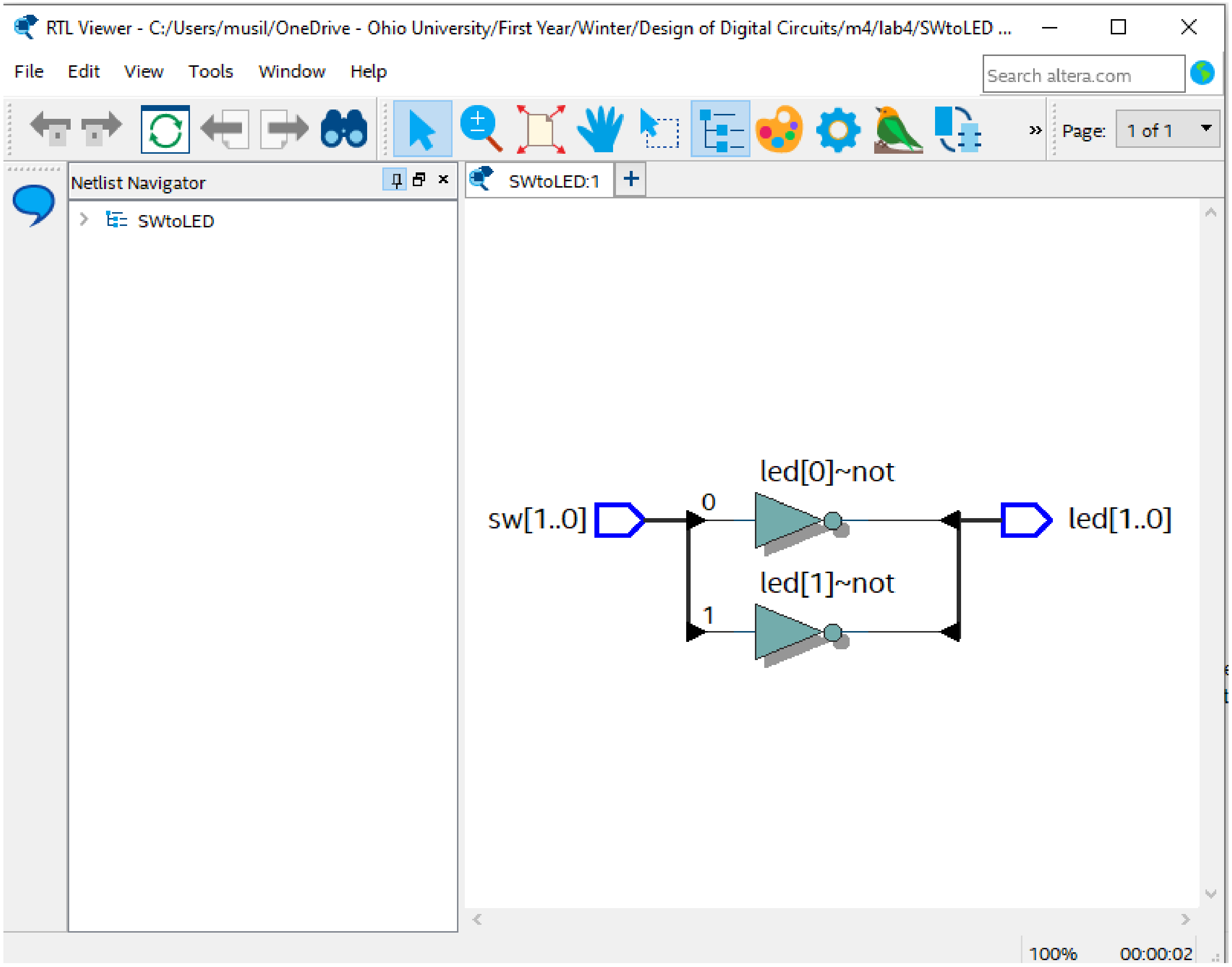


```
------------------------------------
-- Library Declaration --
------------------------------------
-- Like any other programming language, we should declare libraries
library ieee;
use ieee.std_logic_1164.all;
------------------------------------
-- Entity Declaration --
------------------------------------
-- Here we specify all input/output ports
entity SWtoLED is
   port(

         sw : in std_logic_vector(1 downto 0);
         led : out std_logic_vector(1 downto 0)

);
end SWtoLED;
------------------------------------
-- Architecture Declaration --
------------------------------------
-- here we put the description code of the design
architecture dataflow of SWtoLED is
begin
led <= not(sw);
end dataflow;
```

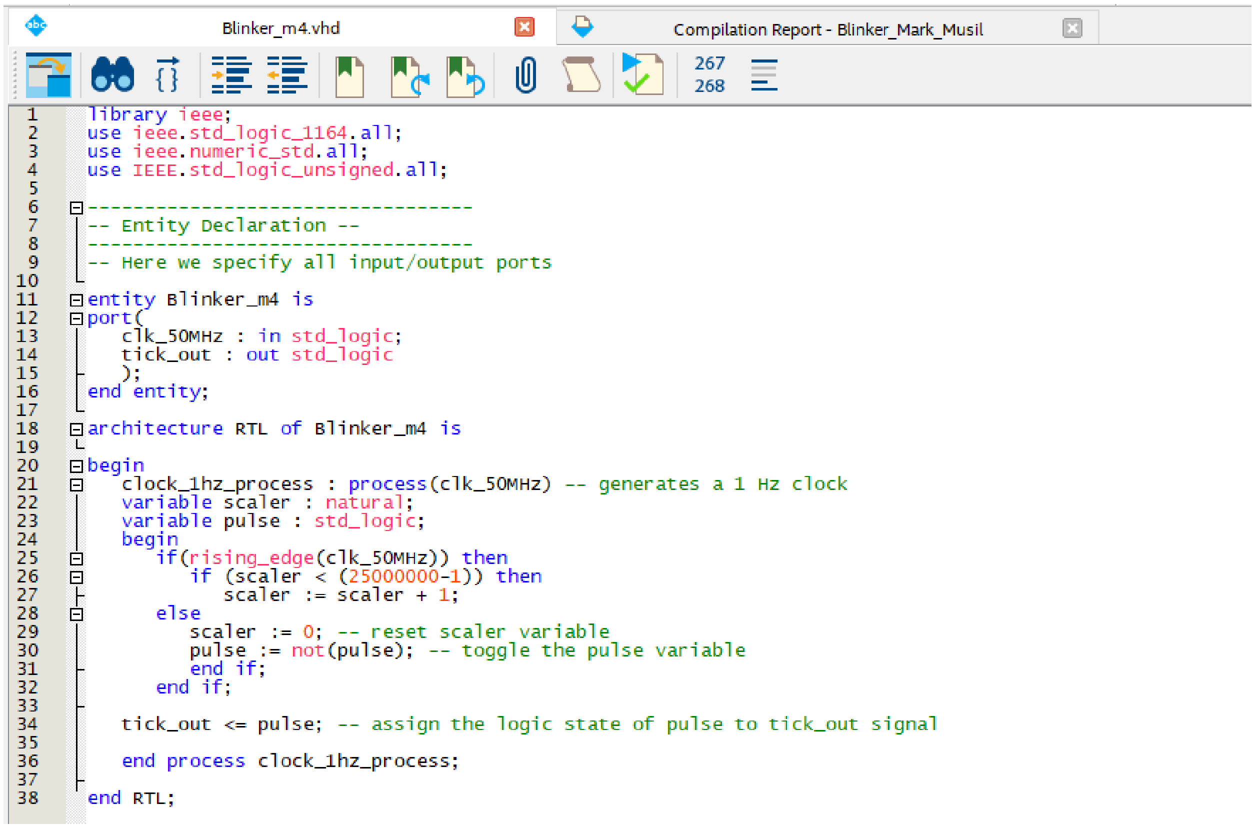


Report not available
Groups
Report
Early Pin Planning
Early Pin Planning...
Run I/O Assignment Analysis
Export Pin Assignments...
Pin Finder...
Highlight Pins
I/O Banks
VREF Groups
Edges
Clock Pins
Clock
PLL/DLL Input
PLL/DLL Output
Clock Region Input
Memory Pins
DQ/DQS
Differential Pins
OCT Pins
Top View - Wire Bond
Cyclone IV E - EP4CE22F17C6
IOBANK_8 (0 assigned/24 assignable)
IOBANK_7 (2 assigned/24 assignable) (0 input/2 output/0 bidir)
IOBANK_1 (1 assigned/14 assignable) (1 input/0 output/0 bidir)
IOBANK_2 (0 assigned/16 assignable)
IOBANK_6 (0 assigned/13 assignable)
IOBANK_5 (1 assigned/18 assignable) (1 input/0 output/0 bidir)
IOBANK_3 (0 assigned/25 assignable)
IOBANK_4 (0 assigned/20 assignable)
Named: *
Edit:

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservatior
led[1]	Output	PIN_A13	7	B7_N0	PIN_A13	2.5 V		8mA (default)	2 (default)		
led[0]	Output	PIN_A15	7	B7_N0	PIN_A15	2.5 V		8mA (default)	2 (default)		
sw[1]	Input	PIN_E1	1	B1_N0	PIN_E1	2.5 V		8mA (default)			
sw[0]	Input	PIN_J15	5	B5_N0	PIN_J15	2.5 V		8mA (default)			
<<new node>>											

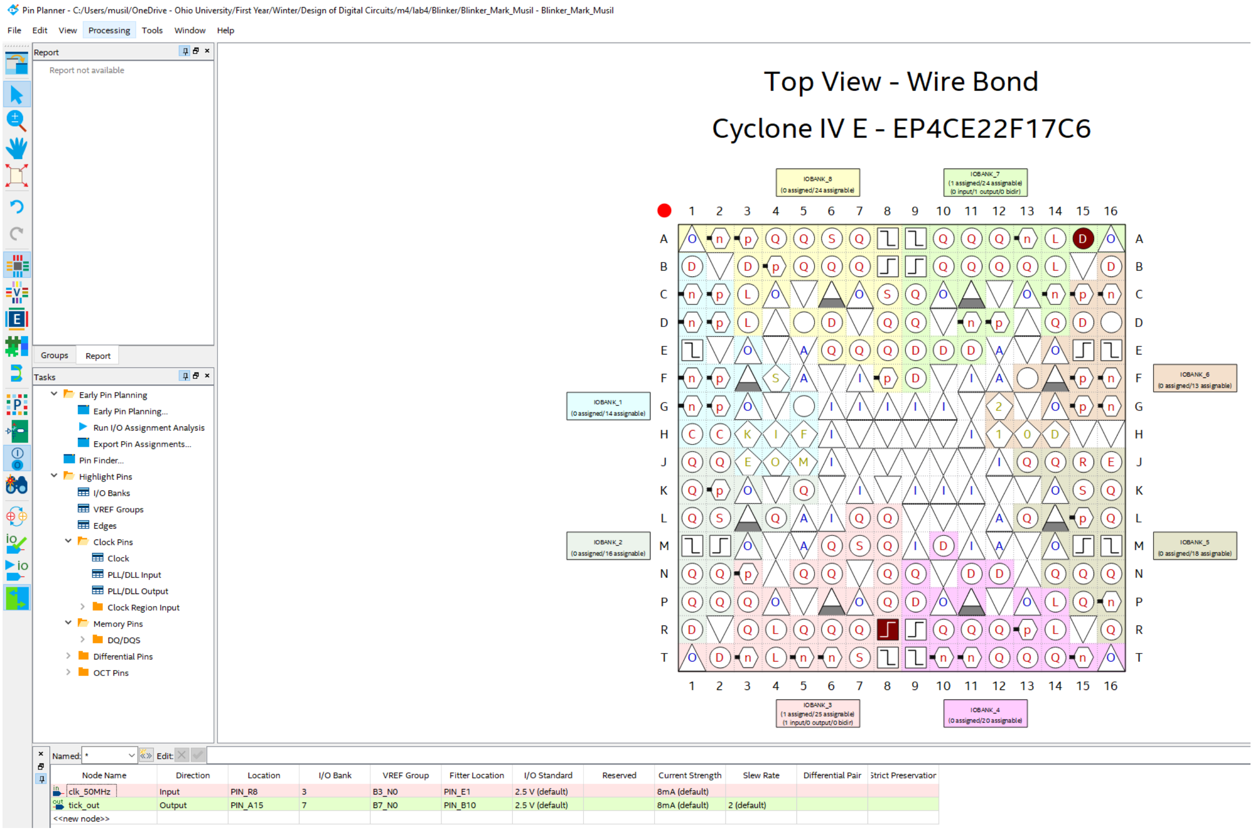

RTL Viewer - C:/Users/musil/OneDrive - Ohio University/First Year/Winter/Design of Digital Circuits/m4/lab4/SWtoLED ...
File
Edit
View
Tools
Window
Help
Search altera.com
Page:
1 of 1
Netlist Navigator
SWtoLED
SWtoLED:1
sw[1..0]
0
1
led[0]~not
led[1]~not
led[1..0]
100%
00:00:02

Part 2



```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use IEEE.std_logic_unsigned.all;

----------------------------------
-- Entity Declaration --
----------------------------------
-- Here we specify all input/output ports

entity Blinker_m4 is
port(
    clk_50MHz : in std_logic;
    tick_out : out std_logic
    );
end entity;

architecture RTL of Blinker_m4 is

begin
    clock_1hz_process : process(clk_50MHz) -- generates a 1 Hz clock
    variable scaler : natural;
    variable pulse : std_logic;
    begin
        if(rising_edge(clk_50MHz)) then
            if (scaler < (25000000-1)) then
                scaler := scaler + 1;
        else
            scaler := 0; -- reset scaler variable
            pulse := not(pulse); -- toggle the pulse variable
            end if;
        end if;

    tick_out <= pulse; -- assign the logic state of pulse to tick_out signal

    end process clock_1hz_process;

end RTL;
```

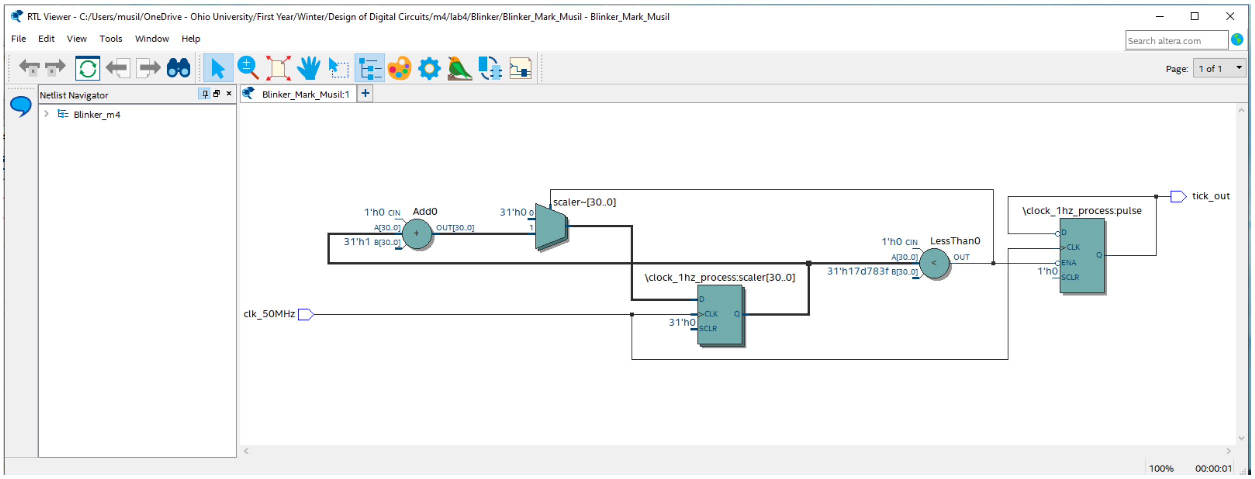
Mark Musil | Design of Digital Circuits | February 2022
Ohio University | Lab 4



Pin Planner - C:/Users/musil/OneDrive - Ohio University/First Year/Winter/Design of Digital Circuits/m4/lab4/Blinker/Blinker_Mark_Musil - Blinker_Mark_Musil

File Edit View Processing Tools Window Help
Report
Report not available
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Run I/O Assignment Analysis
Export Pin Assignments...
Pin Finder...
Highlight Pins
I/O Banks
VREF Groups
Edges
Clock Pins
Clock
PLL/DLL Input
PLL/DLL Output
Clock Region Input
Memory Pins
DQ/DQS
Differential Pins
OCT Pins
Top View - Wire Bond
Cyclone IV E - EP4CE22F17C6
IOBANK_8 (0 assigned/24 assignable)
IOBANK_7 (1 assigned/24 assignable) (0 input/1 output/0 bidir)
IOBANK_1 (0 assigned/14 assignable)
IOBANK_2 (0 assigned/16 assignable)
IOBANK_6 (0 assigned/13 assignable)
IOBANK_5 (0 assigned/18 assignable)
IOBANK_3 (1 assigned/25 assignable) (1 input/0 output/0 bidir)
IOBANK_4 (0 assigned/20 assignable)
Named: * Edit:

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservation
clk_50MHz	Input	PIN_R8	3	B3_N0	PIN_E1	2.5 V (default)		8mA (default)			
tick_out	Output	PIN_A15	7	B7_N0	PIN_B10	2.5 V (default)		8mA (default)	2 (default)		
<<new node>>											



RTL Viewer - C:/Users/musil/OneDrive - Ohio University/First Year/Winter/Design of Digital Circuits/m4/lab4/Blinker/Blinker_Mark_Musil - Blinker_Mark_Musil