Module 5: Identifiers, signals, constants, variables and types in VHDL

Learning objectives:

Study of the following topics -

Valid and invalid identifiers in VHDL
VHDL reserved words
Data objects in VHDL: signals, constants and variables
Data types in VHDL
Sub-types in VHDL

This module deals with core concepts related to data objects in VHDL. Unlike software programming languages, VHDL has an additional data object called signal which enables it to model the behavior of electrical circuits. Also discussed are VHDL's reserved words, rules for selecting valid identifier names and types of data objects.

First go through the Powerpoint slides and the videos and then complete the associated reading assignments for this module.

Reading assignments

The required reading for understanding module 5 topics is listed below. Use the book: VHDL for Programmable Logic by Kevin Skahill for this purpose.

Read the following sections from chapter 3:

3.4 (Identifiers, Data Objects, Data Types, and Attributes)

3.5 (Common Errors)

Also, go through the supplementary reading document in the supplementary readings folder and take a look at the engineering documents in the zip archive in that folder. There is no need to actually read them in any detail.

There is no homework assignment with this module but there is a lab assignment which you should read, complete and submit, as usual.