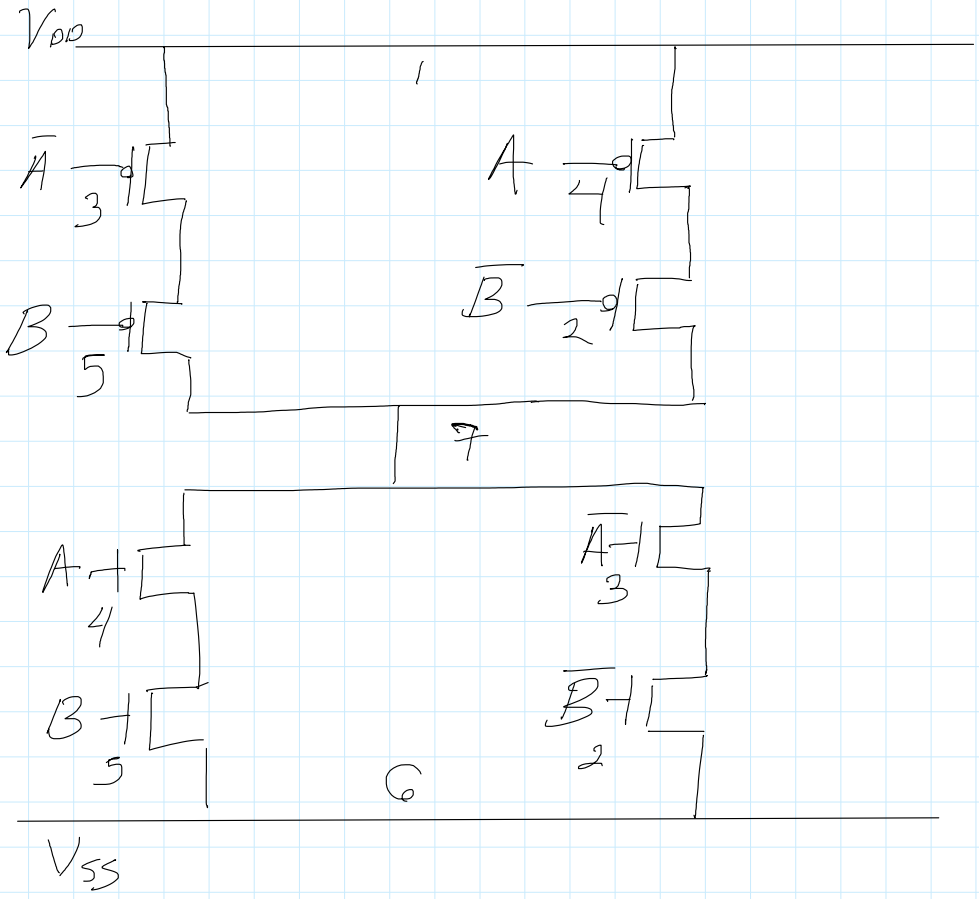
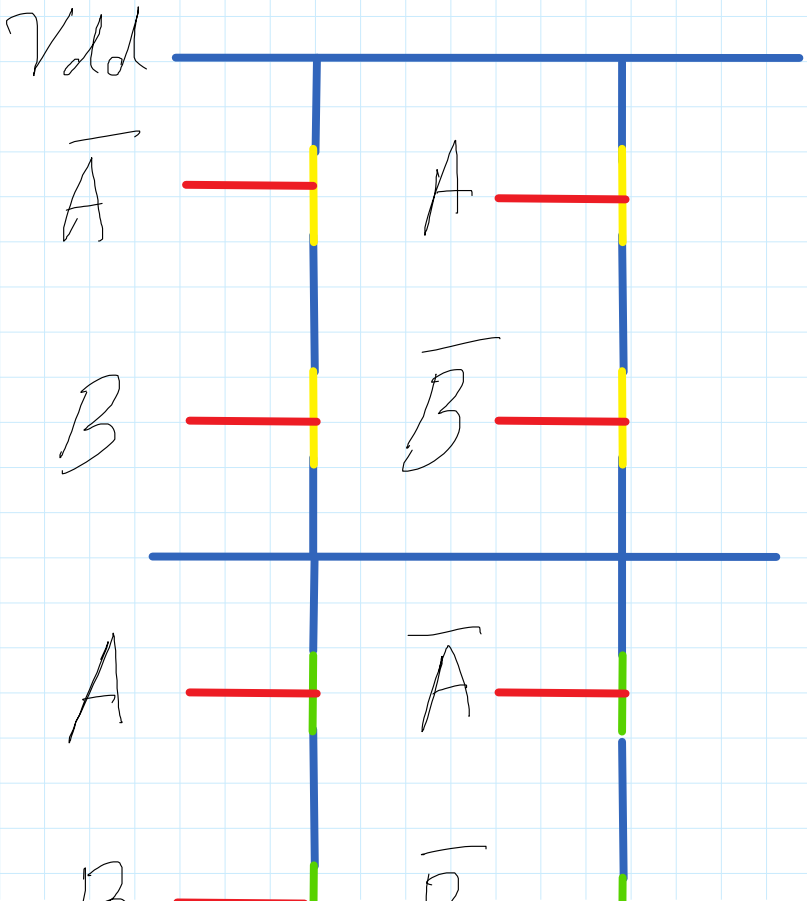
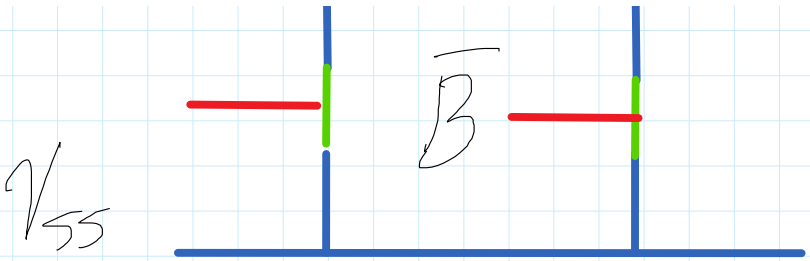
Module 13

Wednesday, April 13, 2022 6:29 AM

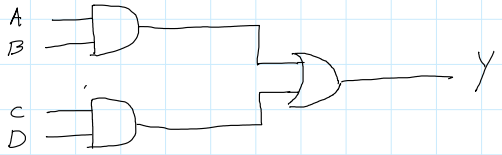
Q1. Sketch a CMOS layout for the XOR function.



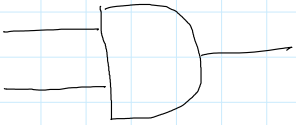


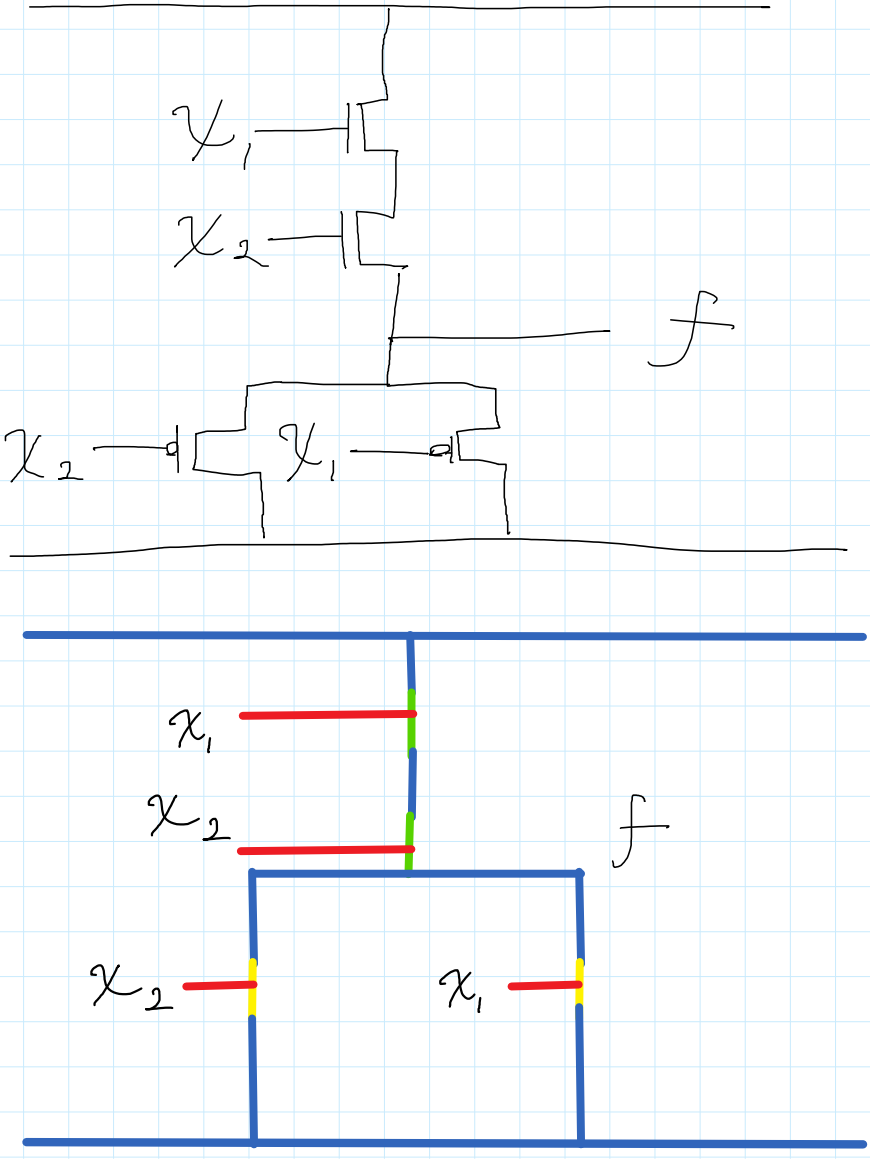


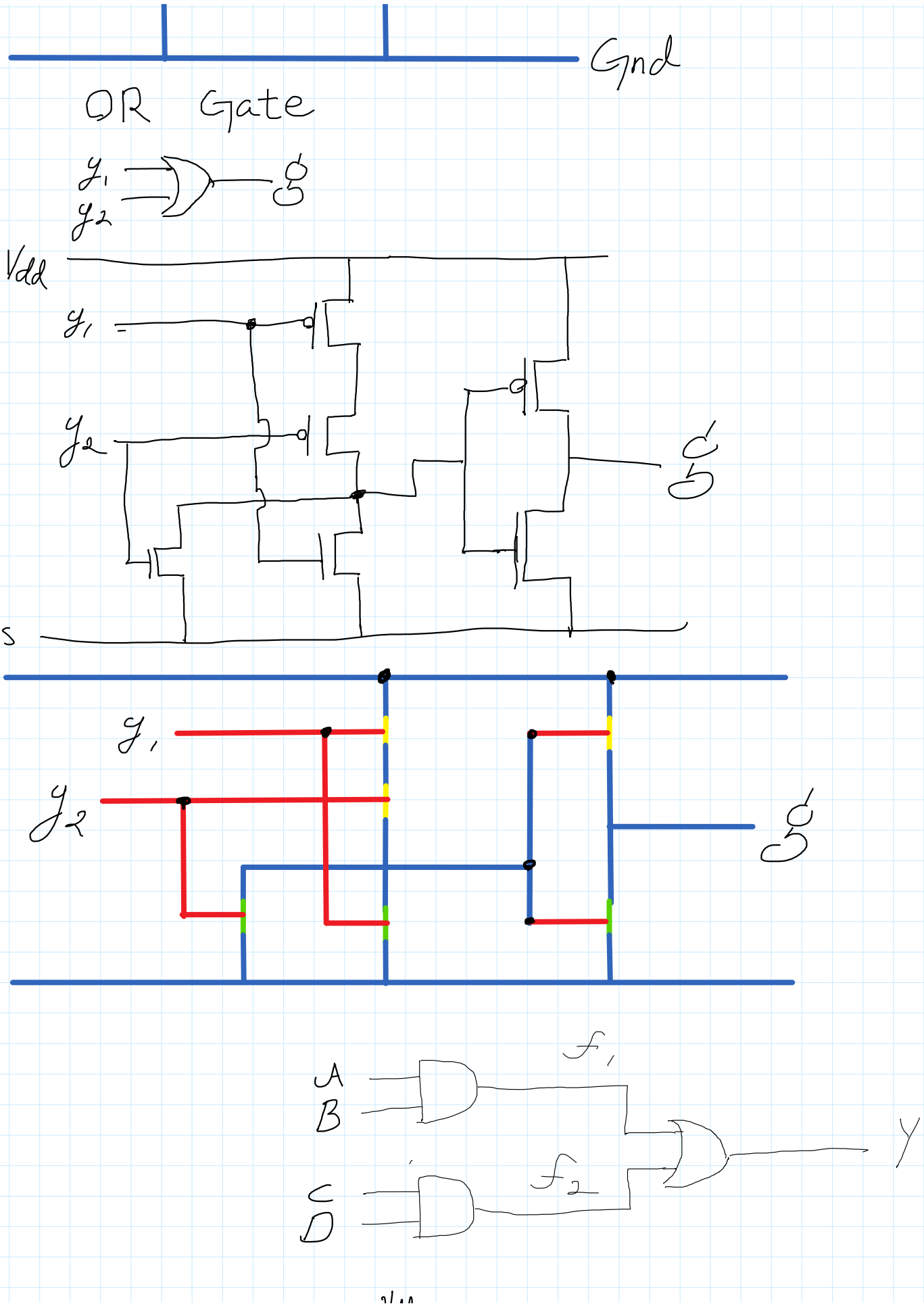
Q2. Sketch CMOS layout for a two 2-input AND gates with their outputs connected to a 2-input OR gate. Do this using both AND and OR gates and then using only NAND gates.

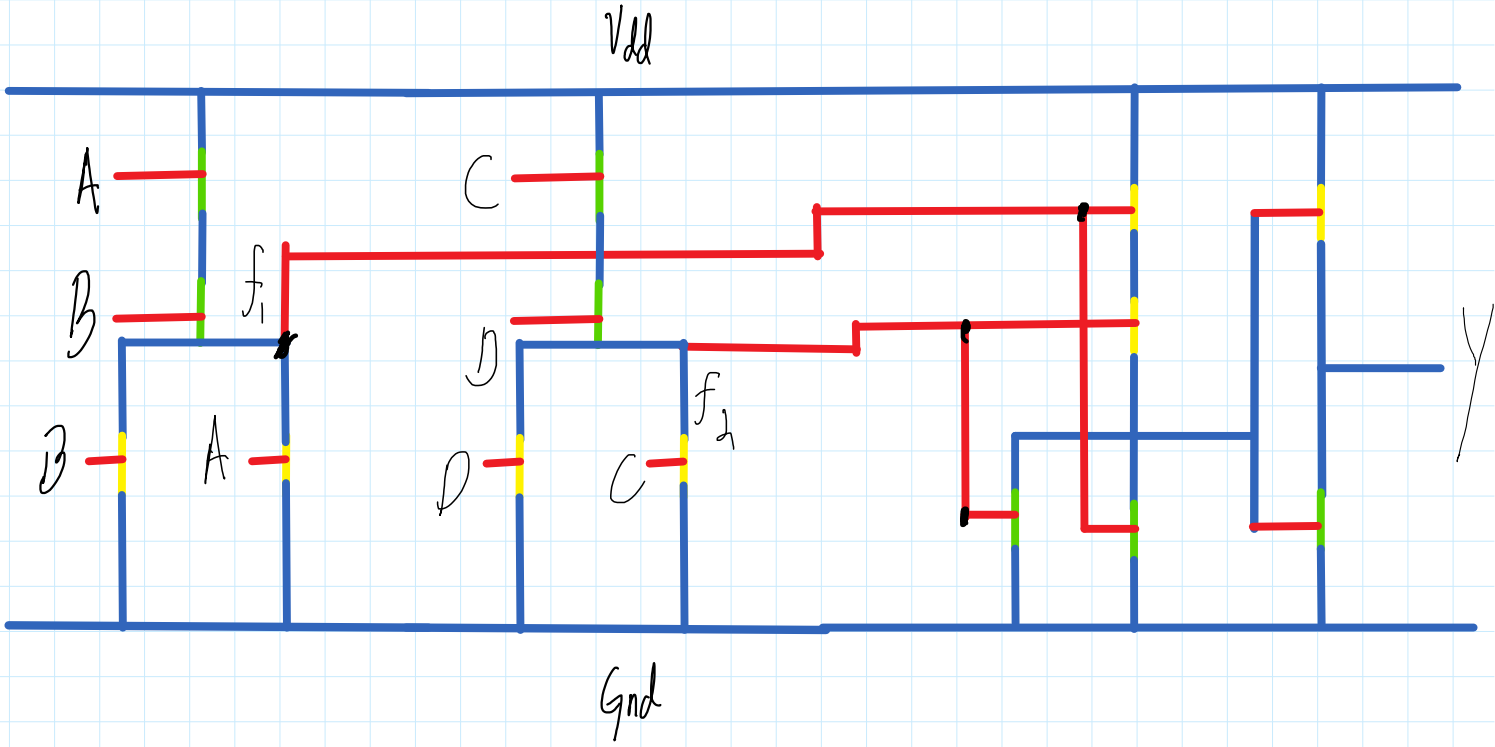


AND Gate






Gnd
OR Gate
y_1
y_2
$\bar{S}$
Vdd
y_1
y_2
$\bar{S}$
Vss
y_1
y_2
$\bar{S}$
A
B
C
D
f_1
f_2
Y

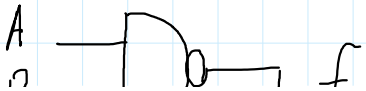


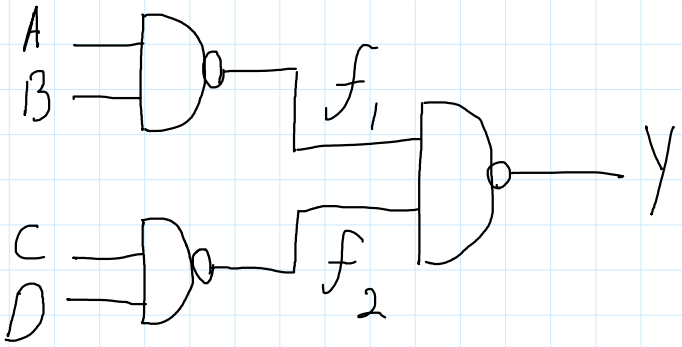
NAND method

$$y = AB + CD$$

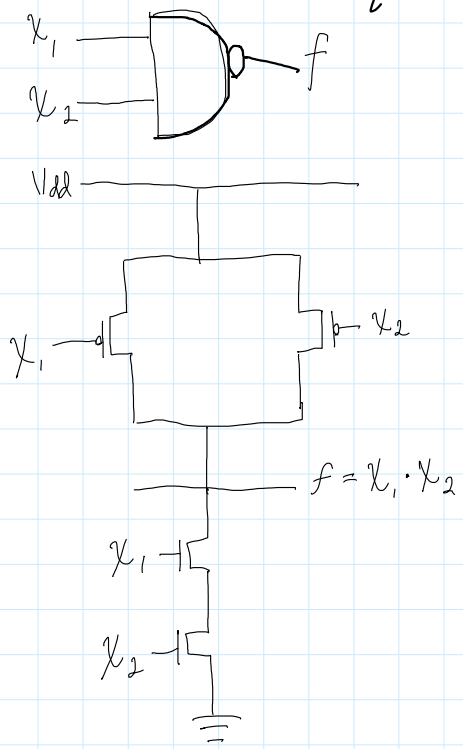
$$\overline{y} = \overline{AB + CD} = \overline{AB}\,\overline{(CD)}$$

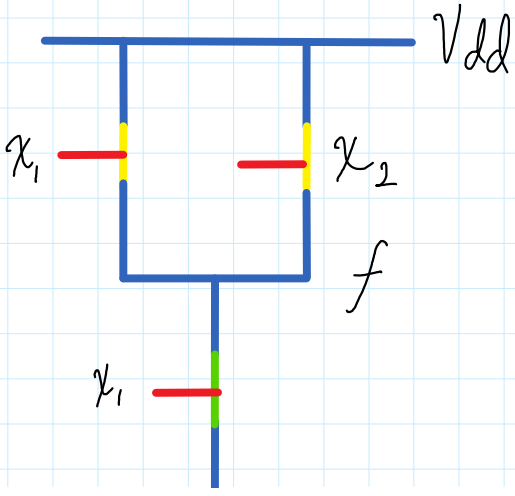
$$y = \overline{\overline{y}} = \overline{\overline{AB}\,\overline{(CD)}}$$

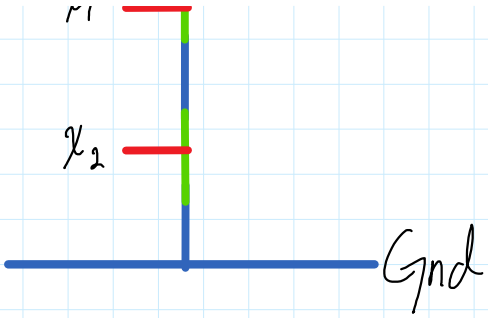


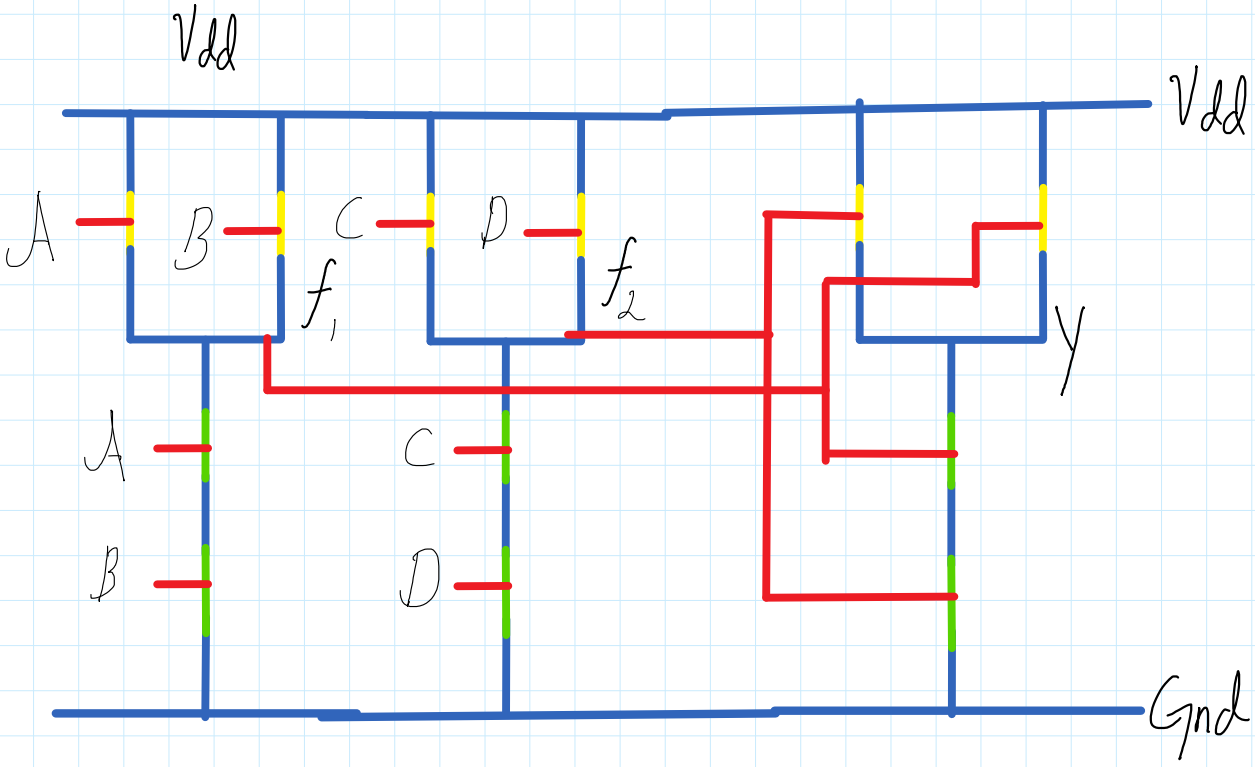


NAND Gate






x_2
Gnd


Vdd
Vdd
A
B
C
D
f_1
f_2
Y
A
B
C
D
Gnd