Project 1

VHDL Code

Top level entity

AOI.vhd

```
1  ----------------------------------
2  -- Entity Declaration --
3  ----------------------------------
4  -- here we describe the I/O of the design
5  entity AOI is
6  port(
7      i1, i2, i3, i4 : in bit;
8      z : out bit
9      );
10 end entity;
11 ----------------------------------
12 -- Architecture Definition --
13 ----------------------------------
14 -- here we put the description code of the design
15 architecture structural of AOI is
16 signal temp1, temp2 : bit; -- these are (internal) signals that carry outputs from 2 Comp1 components to the inputs of the
17
18 component comp1 port(a, b : in bit; c : out bit); end component; -- declaration of Comp1 (written on a single line)
19 component comp2 port(a, b : in bit; c : out bit); end component; -- declaration of Comp2 (written on a single line)
20
21 begin
22 MyAND1: Comp1
23     port map(a => i1, b => i2, c => temp1);
24 MyAND2: Comp1
25     port map(a => i3, b => i4, c => temp2);
26 MyORINVERT: Comp2
27     port map(temp1, temp2, z);
28 end structural;
29
```

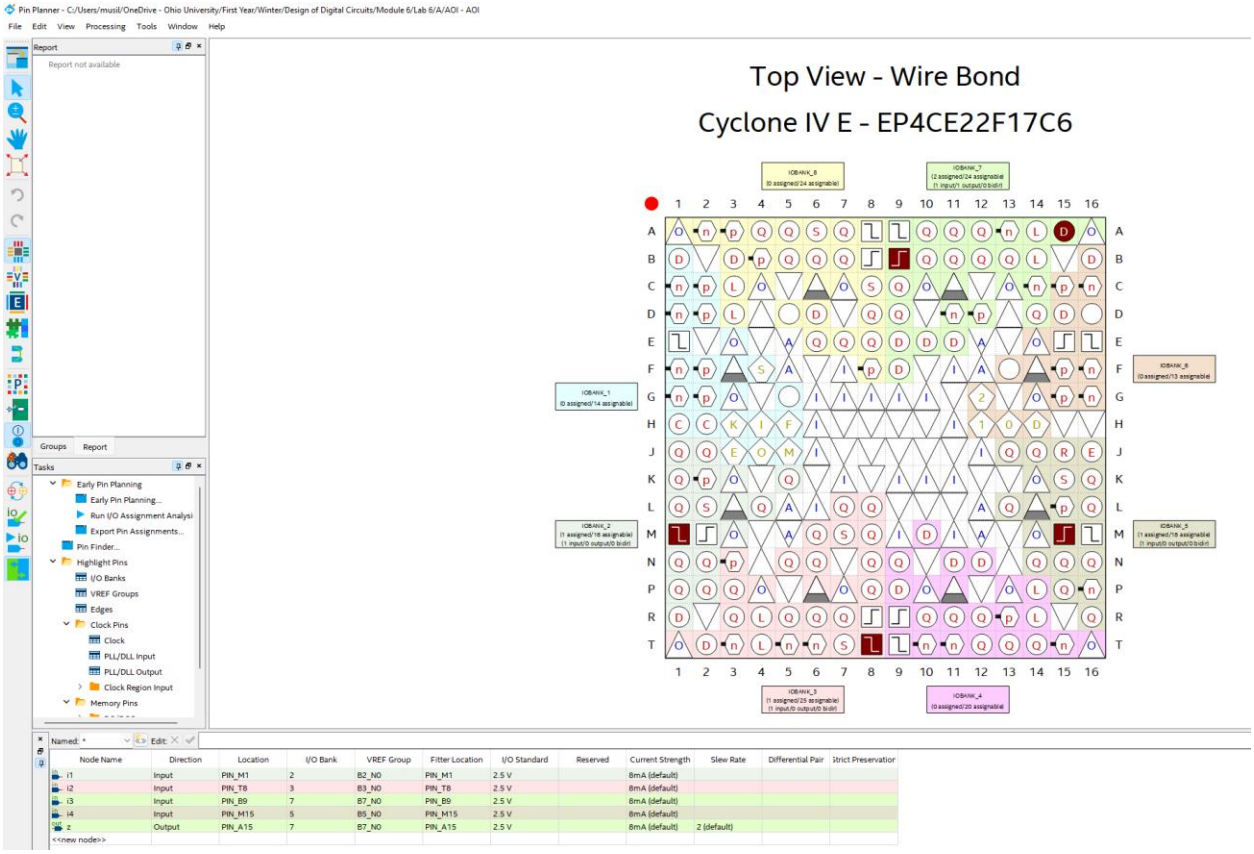
Components

```
1  ----------------------------------
2  -- Entity Declaration --
3  ----------------------------------
4  -- here we describe the I/O of the design
5  entity Comp1 is
6  port(
7      a, b : in bit;
8      c : out bit
9      );
10 end entity;
11
12 ----------------------------------
13 -- Architecture Definition --
14 ----------------------------------
15 -- here we put the description code of the design
16 architecture gate of Comp1 is
17 begin
18     c <= a AND b;
19
20 end gate;
```

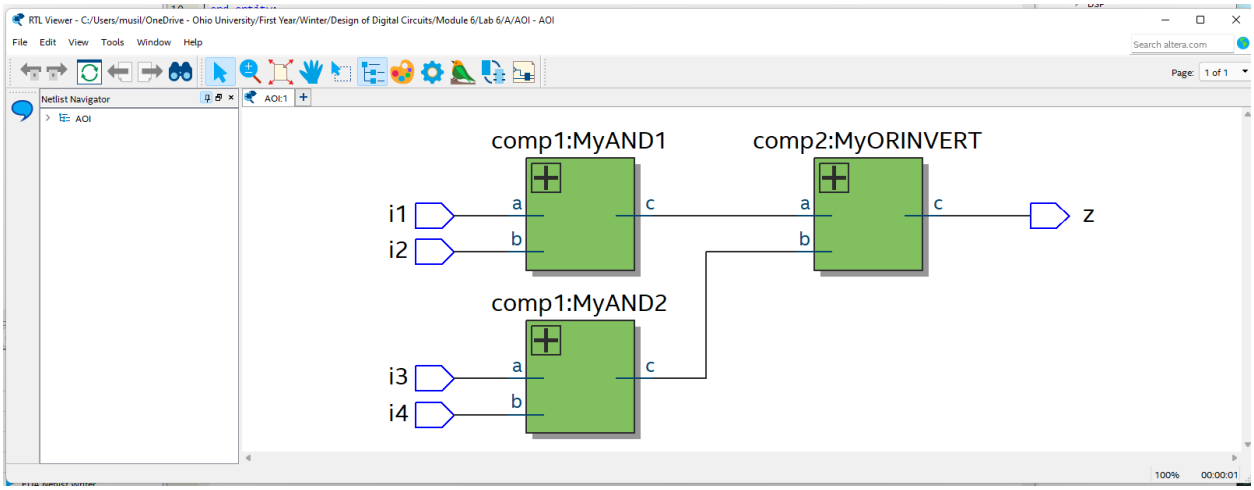
AOI.vhd | Comp1.vhd

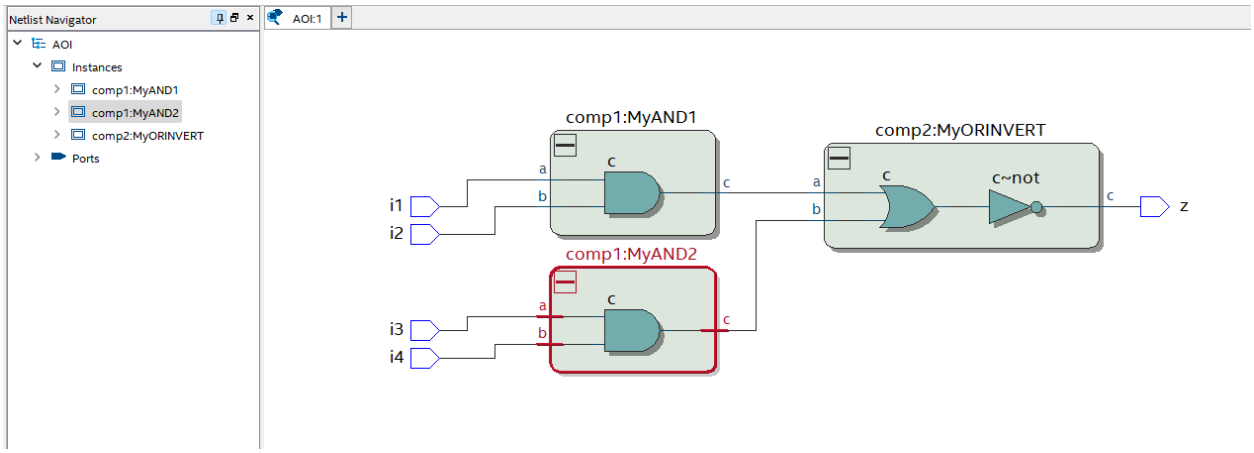
```
1  ----------------------------------
2  -- Entity Declaration --
3  ----------------------------------
4  -- here we describe the I/O of the design
5  entity Comp2 is
6      port(
7          a, b : in bit;
8          c : out bit
9          );
10 end entity;
11 ----------------------------------
12 -- Architecture Definition --
13 ----------------------------------
14 -- here we put the description code of the design
15 architecture gate of Comp2 is
16 begin
17     c <= NOT(a OR b);
18 end gate;
19
```

Pin Planner


Pin Planner - C:/Users/musil/OneDrive - Ohio University/First Year/Winter/Design of Digital Circuits/Module 6/Lab 6/A/AOI - AOI
File Edit View Processing Tools Window Help
Report
Report not available
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Run I/O Assignment Analysis
Export Pin Assignments...
Pin Finder...
Highlight Pins
I/O Banks
VREF Groups
Edges
Clock Pins
Clock
PLL/DLL Input
PLL/DLL Output
Clock Region Input
Memory Pins
Top View - Wire Bond
Cyclone IV E - EP4CE22F17C6
Named: *
Edit:
Node Name | Direction | Location | I/O Bank | VREF Group | Fitter Location | I/O Standard | Reserved | Current Strength | Slew Rate | Differential Pair | Strict Preservation
i1 | Input | PIN_M1 | 2 | B2_N0 | PIN_M1 | 2.5 V | | 8mA (default) | | |
i2 | Input | PIN_T8 | 3 | B3_N0 | PIN_T8 | 2.5 V | | 8mA (default) | | |
i3 | Input | PIN_B9 | 7 | B7_N0 | PIN_B9 | 2.5 V | | 8mA (default) | | |
i4 | Input | PIN_M15 | 5 | B5_N0 | PIN_M15 | 2.5 V | | 8mA (default) | | |
z | Output | PIN_A15 | 7 | B7_N0 | PIN_A15 | 2.5 V | | 8mA (default) | 2 (default) | |
<<new node>>

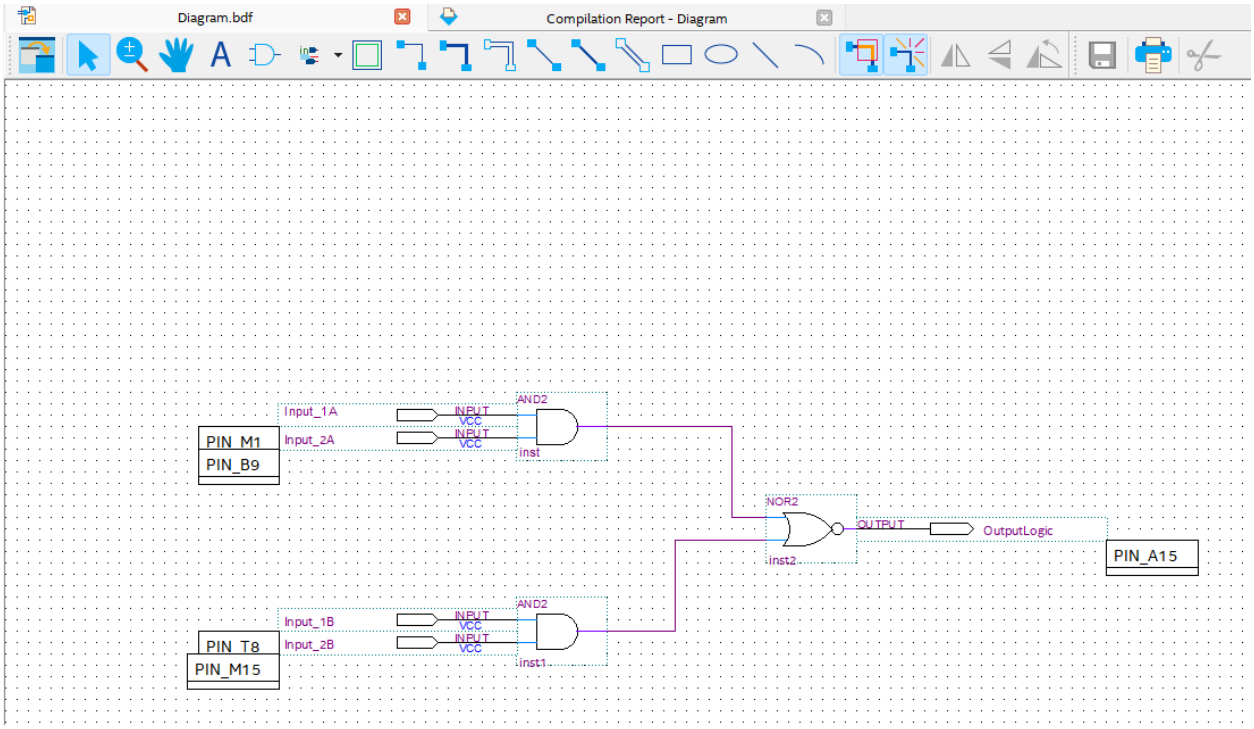
RTL Window


RTL Viewer - C:/Users/musil/OneDrive - Ohio University/First Year/Winter/Design of Digital Circuits/Module 6/Lab 6/A/AOI - AOI
File Edit View Tools Window Help
Netlist Navigator
AOI
AOI:1
comp1:MyAND1
comp2:MyORINVERT
comp1:MyAND2
i1
i2
i3
i4
a
b
c
z
100%
00:00:01

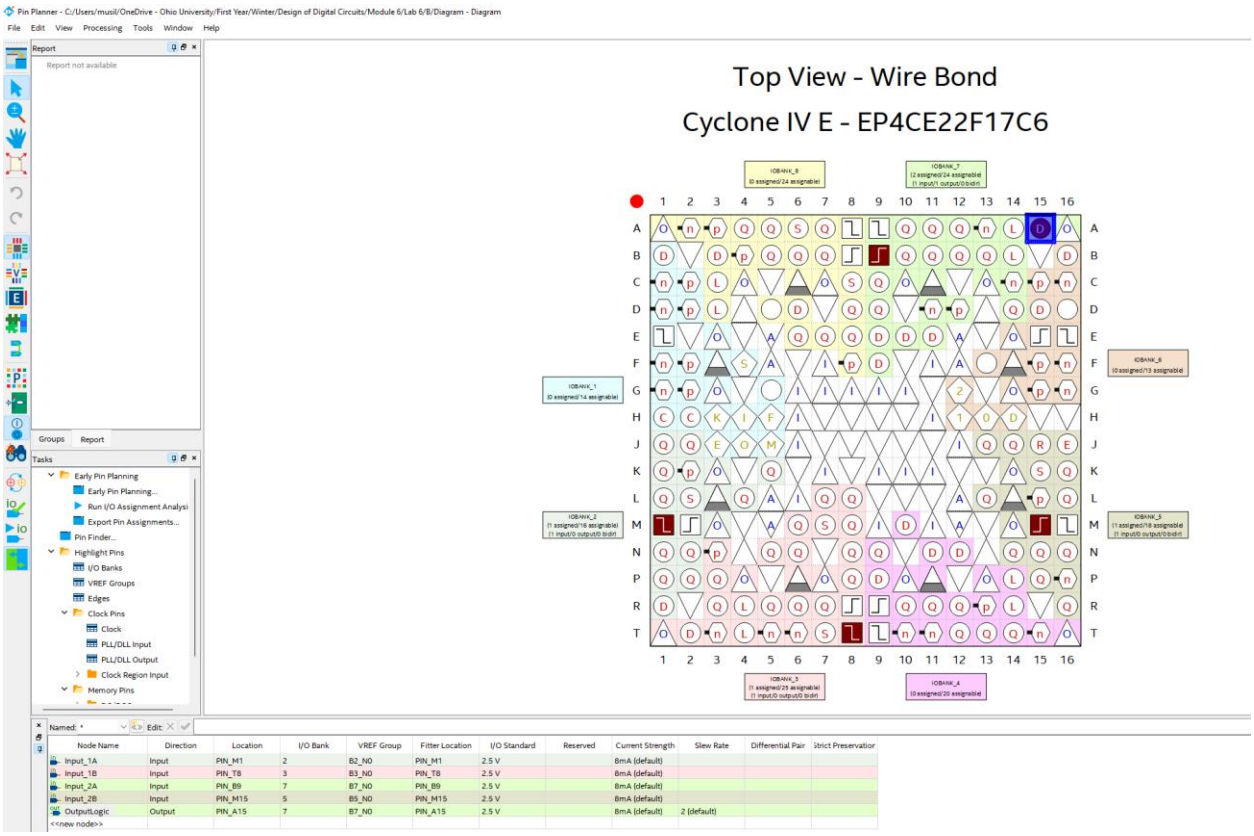

Netlist Navigator
AOI
Instances
comp1:MyAND1
comp1:MyAND2
comp2:MyORINVERT
Ports
AOI:1
comp1:MyAND1
comp2:MyORINVERT
comp1:MyAND2
c~not
i1
i2
i3
i4
a
b
c
z

Project 2

Circuit Diagram



Pin Planner



RTL Window