Module 6: Code reusability: libraries, subprograms and packages in VHDL

Learning objectives:

Study of the following topics -

Reusing code
IEEE libraries
Packages
Subprograms: procedures and functions

This module teaches code reusability topics. Like computer programming languages, VHDL also makes use of procedures and functions. These 'sub-programs' can be written once and used at multiple locations. The concept of libraries and packages is also introduced.

First go through the Powerpoint slides and the videos and then complete the associated reading assignments for this module.

Reading assignments

The required reading for understanding module 6 topics is listed below. Use the book: VHDL for Programmable Logic by Kevin Skahill for this purpose.

Read the following from chapter 7:

Start from the beginning of chapter 7 (Functions and Procedures) and read until you reach section 7.2.5 (Overloading Operators). Skip from there on and go to section 7.3 (Procedures). Start reading until you reach the problems at the end of that chapter and stop there. There are no supplementary reading assignments for this module.

Questions

Q1. Do question 7.1 (chapter 7).

Q2. Do question 7.5 (chapter 7).

Q3. Write a procedure to perform 8-bit even parity check.