Module 9: Design of sequential logic circuits

Learning objectives:

Study of the following topics -

Structure of sequential logic
Flip-flops in VHDL
Resets and presets in VHDL
Three-state outputs in VHDL
Bidirectional signals in VHDL

This module introduces several important topics dealing with sequential logic circuits i.e. circuits containing latches and/or flip-flops. These are also called synchronous logic circuits. The behavior of such circuits is necessarily time-dependent and thus clock signals play a very important role here. All kinds of latches and flip-flops can be easily described in VHDL. Sequential logic circuits such as counters and state machines can also be easily described in VHDL.

First go through the PowerPoint slides and the videos and then complete the associated reading assignments for this module.

Reading assignments

The required reading for understanding module 8 topics is listed below. Use the book: VHDL for Programmable Logic by Kevin Skahill for this purpose.

Read the following section from chapter 4:

4.4 Synchronous Logic – stop when you reach section 4.5 Designing a FIFO.

Note that `if (clk'event and clk = '1')` is an older (but valid) way of saying `if (rising_edge(clk))`

Questions

Q1. Write VHDL code for the following:

1) D-flip-flop 2) T-flip-flop 3) 8-bit wide serial shift register with D-flip-flops

Q2. Do question 4.13 (chapter 4).

Q3. Do question 4.15 (chapter 4).