I have chosen to answer this question in two parts. The first is a table summarizing the key differences in these technologies. This table is followed by a discussion of the various merits of the technologies.

	PAL	**CPLD**	**FPGA**	**ASIC**
Type of logic technology	AND zone coupled with OR zone	Logic blocks consisting of gate arrays, macro cells, and IO Cells	Logic cells which are programmatically interconnected	Programmable Logic Devices using custom masks
Type of memory	Some include Flash EEPROM, others use hard array logic	Built in EEPROM	Volatile, requires external memory	External or memory can be built into the design
Examples of use	Small scale	Boot loader for FPGAs, Address decoders and custom state machines [1]	Small scale digital signal processing applications, testing of designs to be used for ASICS	Cryptocurrency mining (blockchain updates)
Development effort/resources needed	Very inexpensive, can be done by hobbyists/individual engineers	Somewhat involved, may require custom equipment, 1 – 10 engineers	Board design and layout, HDL programming, typically 1 – 10 engineers	Foundry mask production, which could involve hundreds of engineers
Typical Cost of Development	< 100K	< 1 million	> 1 million to < 10 million	>10 million

The computer engineer has many options when a logical function is to be implemented. Each design is impact by its own constraints, but the prudent engineer can always find an effective tool to meet his or her design goals. Options range from the PAL (programmable array logic) approach to the design and production of custom ASICs (application specific integrated circuits). In this technology review I will discuss the merits of the various programmable logic products available today. This review is accompanied by a market survey of Xilinx which I encourage the reader to investigate after finishing this review.

There are four main logic families covered in this review.

- PLD (programmable logic device)
- CPLD (Complex programmable logic device)
- FPGA (field programmable gate array)
- ASIC (application specific integrated circuit)

All four of these classes share the designation of programmable logic device. This means that all of them contain arrays of logic gates along with interconnects. Programming these devices is fundamentally different from programming in the colloquial sense. In software engineering the hardware remains unchanged. By contrast, the logic level programming requires that physical connections by either made or left unconnected. These classes are further split by the memory type. A device can either store connection information or not post shutdown. Hence one can speak of either a volatile (non-storing) or non-volatile (storing).

The first class of devices, PLDS, includes Programmable array logic devices (PAL) as well as programmable logic arrays (PAL). The PAL is good for very simplified logic functions like and encoder or decoder or multiplexer or demultiplexer. In fact, the PLA and PAL are quite similar in their construction as well. The PLA uses programmable AND logic as well as OR logic. PAL devices use only programmable AND logic with fixed OR logic already present.

CPLDs on the other hand contain more numerous logic blocks - small systems that can be used to implement a larger (but still relatively small) logic function on their own. Each logic block consists of a set of gate arrays, macro cells, and I/O cells. This allows for CPLD logic blocks to be used to implement both combinational logic functions and sequential ones. A programmable interconnect connects many logic blocks to route signals between them.

A CPLD is still less complex than an FPGA and so the CLPD is the preferred approach for small circuits of low complexity[1]. CPLDs feature built-in non-volatile EEPROM (electrically erasable programmable read only memory) while FPGA memory is volatile. The pin-to-pin delay on a CPLD is significantly smaller due to simpler architecture. This could be a critical design point for example in high-speed DSP applications.

CPLDs can be used as bootloaders for FPGAs and other programmable systems. CPLDs are often used as address decoders and as custom state machines in digital systems. Due to their small size and low power consumption, CPLDs are ideal for use in portable and handheld digital devices. CPLDs are also used in safety-critical control applications. Major manufacturers of CPLDs are Altera (acquired by Intel), Xilinx (acquired by AMD), Atmel (acquired by Microchip), and Lattice Semiconductor.

An FPGA can be compared to a CLPD. A CPLD contains a few thousand logic gates whereas an FPGA may contain millions. CPLDs and FPGAs are both high-end programmable logic devices that are hard to manufacture. CPLD and FPGA are both good for designing a complete digital system or sub-system. An FPGA will have more capability than a CPLD, and so CLPDs are used for relatively small but fast logic circuits such as display drivers and interleaved analog to digital converter controllers.

The basic functional building block of the FPGAs are its logic cells which are interconnected with wiring within routing channels. The interconnects span three dimensions. Each logic cell contains gates, multiplexers and flip flops. The flip flops take care of any sequential logic capabilities needed. Gates and multiplexers provide combinational logic functionalities. FPGAs are good for situations where the highest logic density is needed on a single chip.

An ASIC is a factory programmable logic device. There may be a variety of uncommitted digital functions available on the chip. Such as gate arrays, communication protocol blocks and data conversion blocks. These resources are then strung together to create a working circuit. ASICs still require making a mask for the top layer wiring. This requires a large amount of capital to create up front. Best for when one needs performance at any cost.

In conclusion, the computer engineer must choose carefully which programmable logic device to implement. Each variety has its niche in which it is the best solution. The discerning engineer must understand these differences and choose accordingly.

Bibliography

[1] E. Robledo, "What is a CPLD (Complex Programmable Logic Device)?," Autodesk, 4 August 2021. [Online]. Available: https://www.autodesk.com/products/fusion-360/blog/cpld-overview/. [Accessed 15 January 2022].