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DESIGN AND DEVELOPMENT OF A CUSTOM ASIC TEST PCB FOR ULTRASONIC COMMUNICATION

Project seminar by

Malte Nilges

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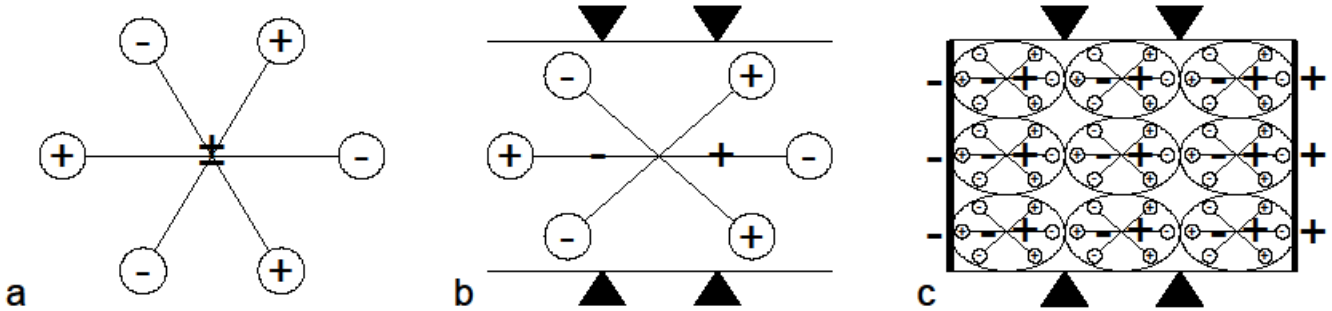
OVERVIEW

- Piezoelectric transducers for sensor communication and energy harvesting



- Aim of this work:
  - Piezo driver platform for data transmission and reception

  → hardware platform (PCB)

  → software platform (FPGA logic)

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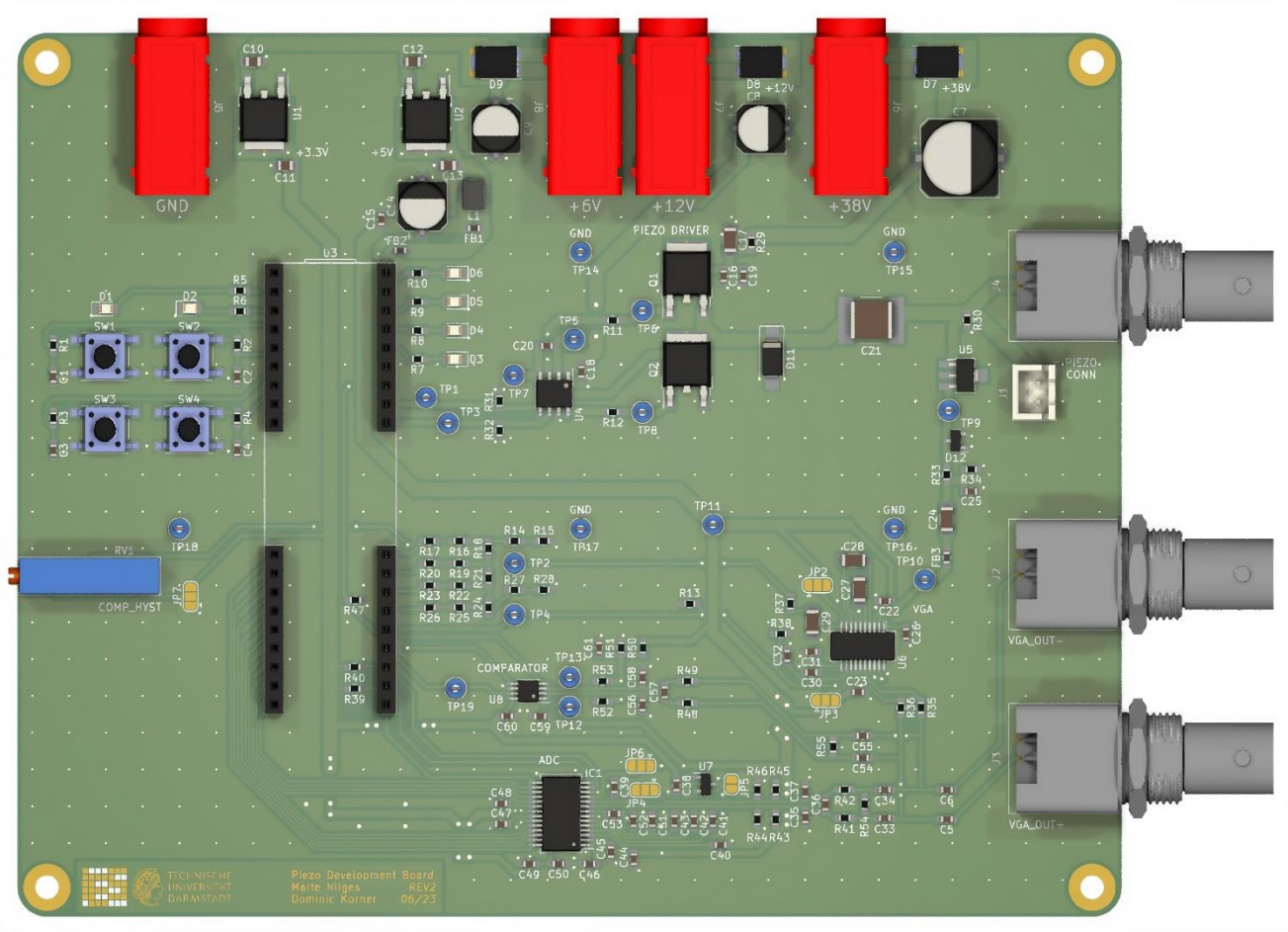
PCB DESIGN



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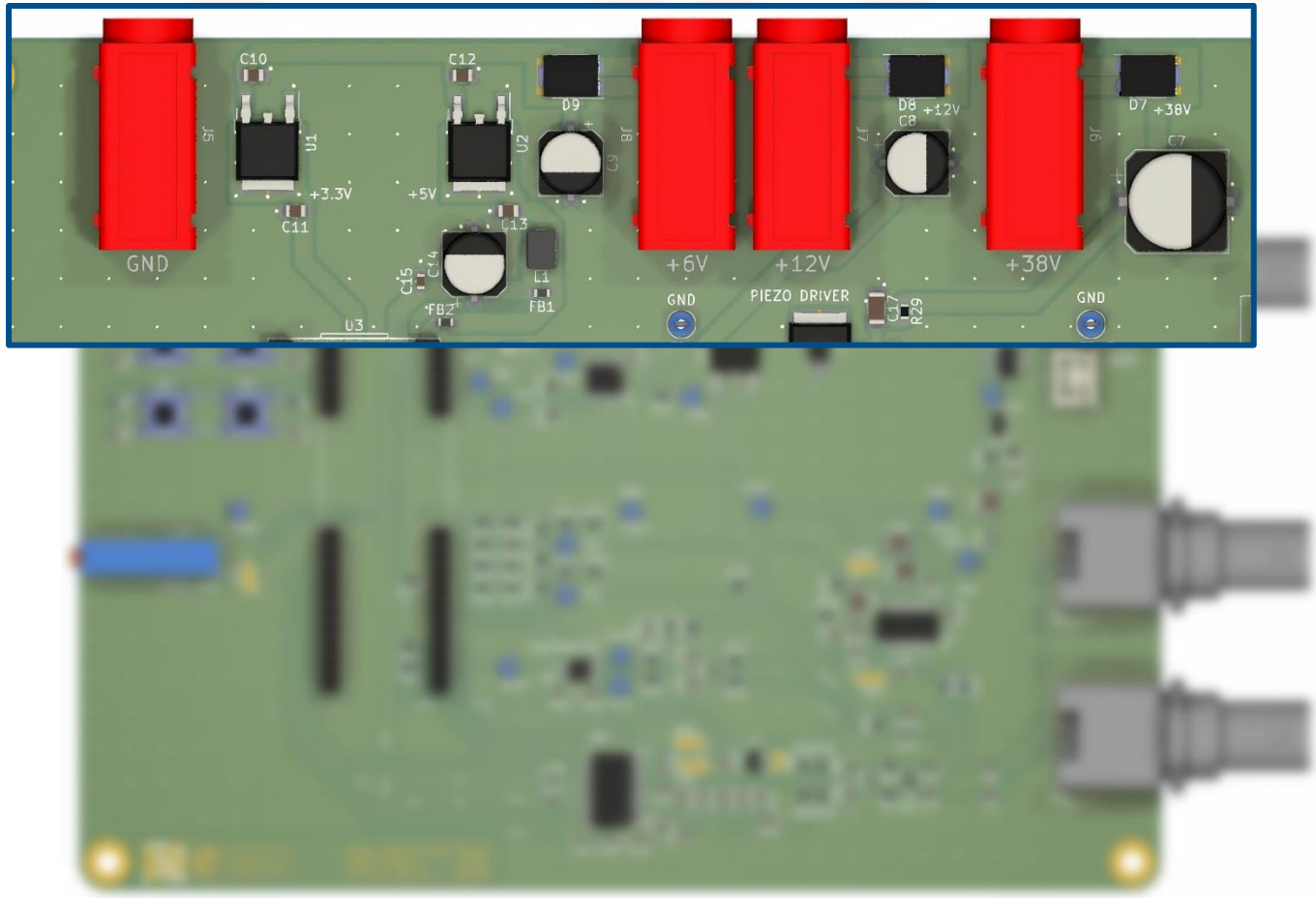
PCB DESIGN

Power stage:

- Rails: 3.3V, 5VA, 5VD, 12V, 38V
- NCP1117 3.3V & 5V LDO
- 3 connectors
- Reverse polarity protection diodes



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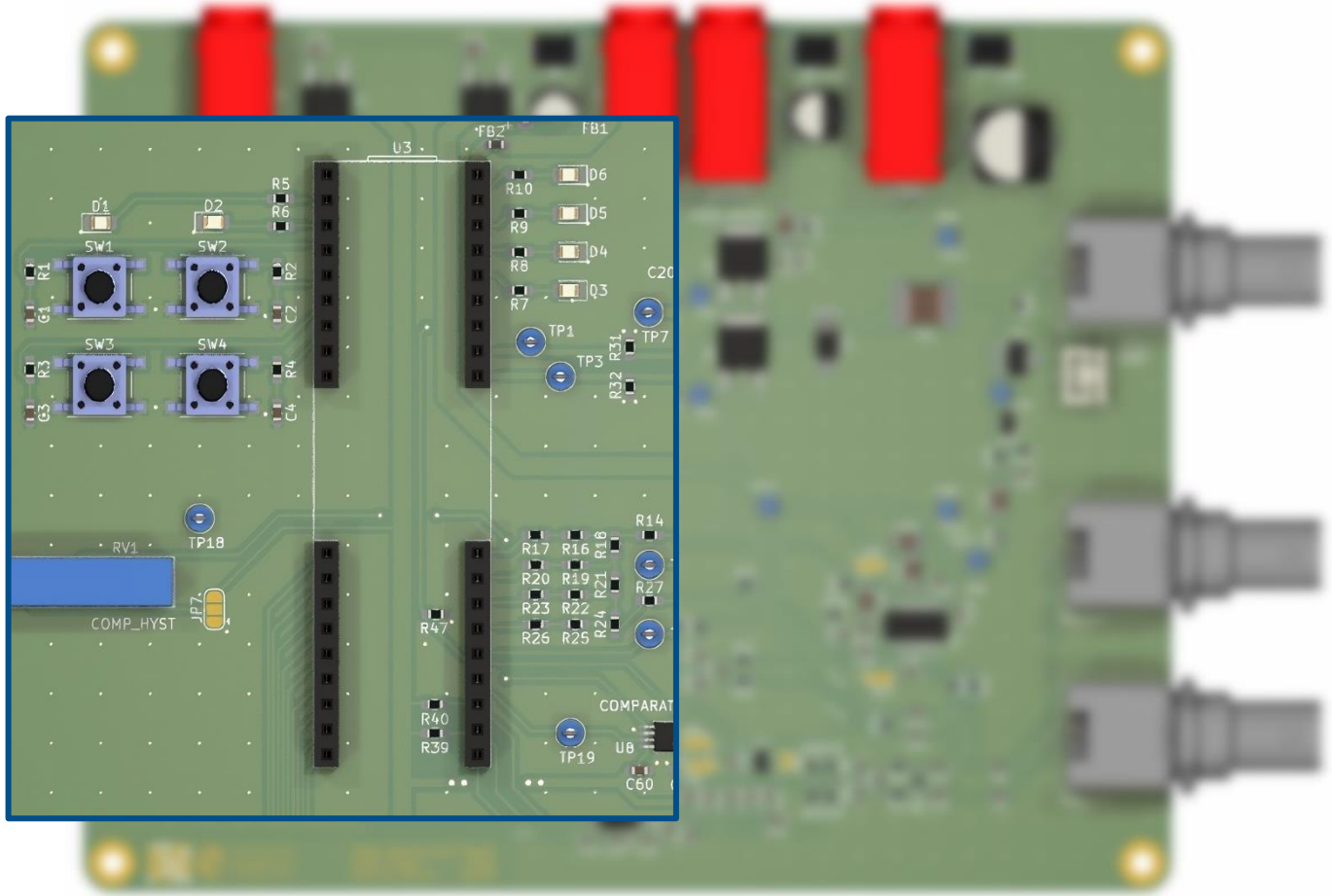
PCB DESIGN

FPGA & I/O:

- CMOD S7 (Spartan XC7S25)
- Push Buttons
- LEDs
- DAC



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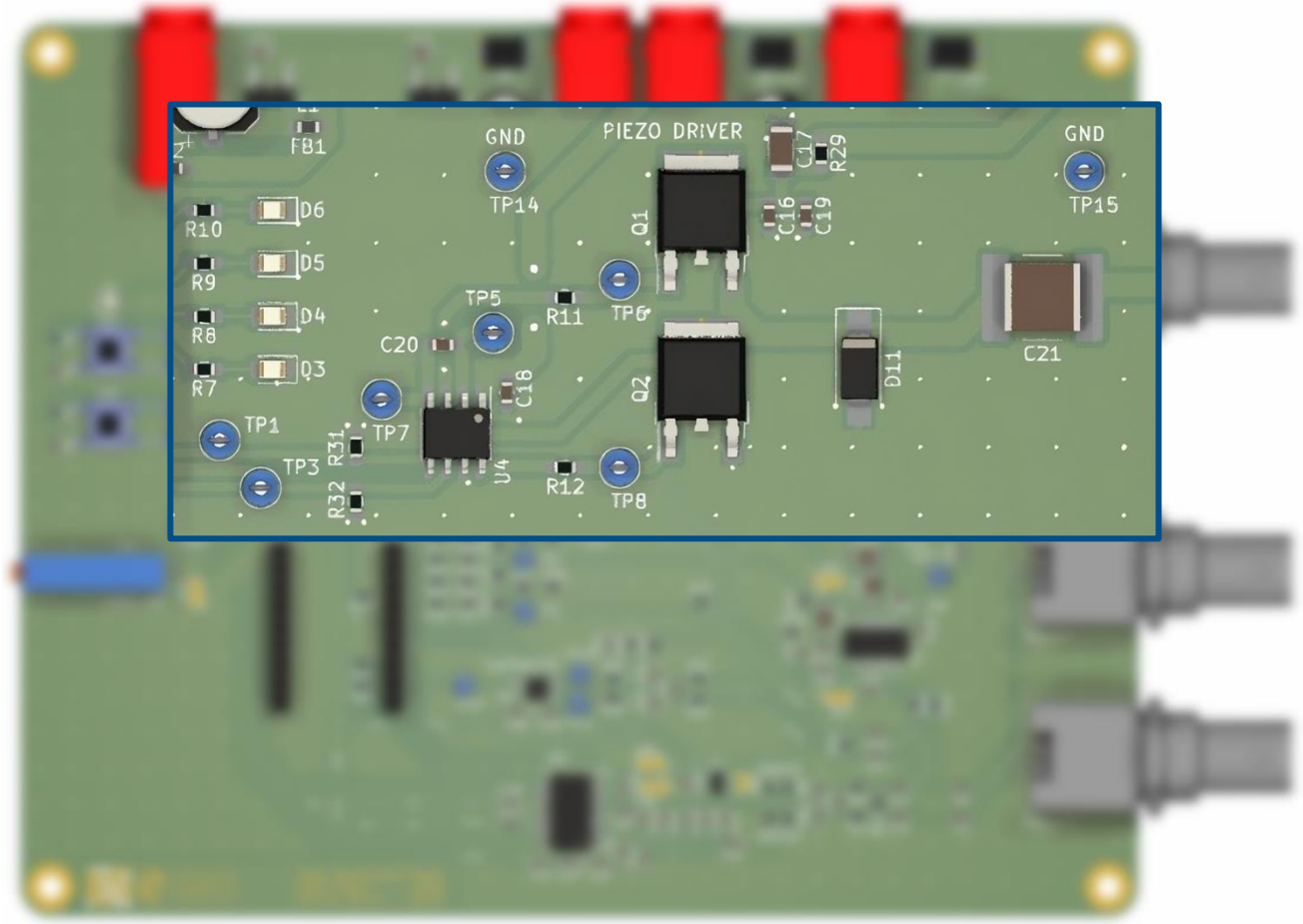
PCB DESIGN

Piezo driver stage:

- MIC4604 half-bridge gate driver
- 2x FDD1600N10ALZ NMOS
- TVS diode
- AC-coupled output



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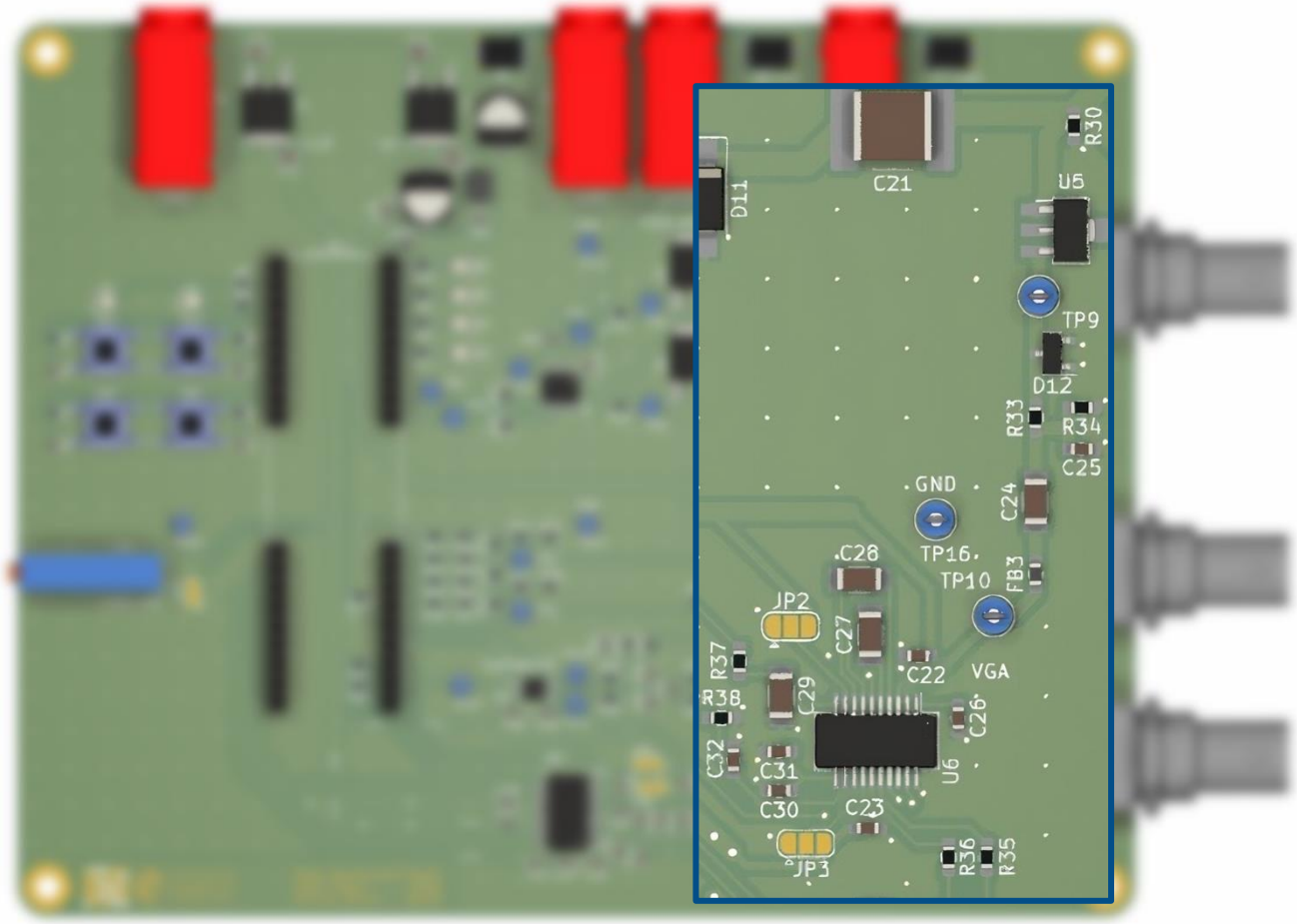
PCB DESIGN

Piezo input & amplifier stage:

- MD0100 T/R switch
- BAV99 protection diodes
- Filtering network
- AD8331 Low-Noise Amplifier with Variable Gain Amplifier



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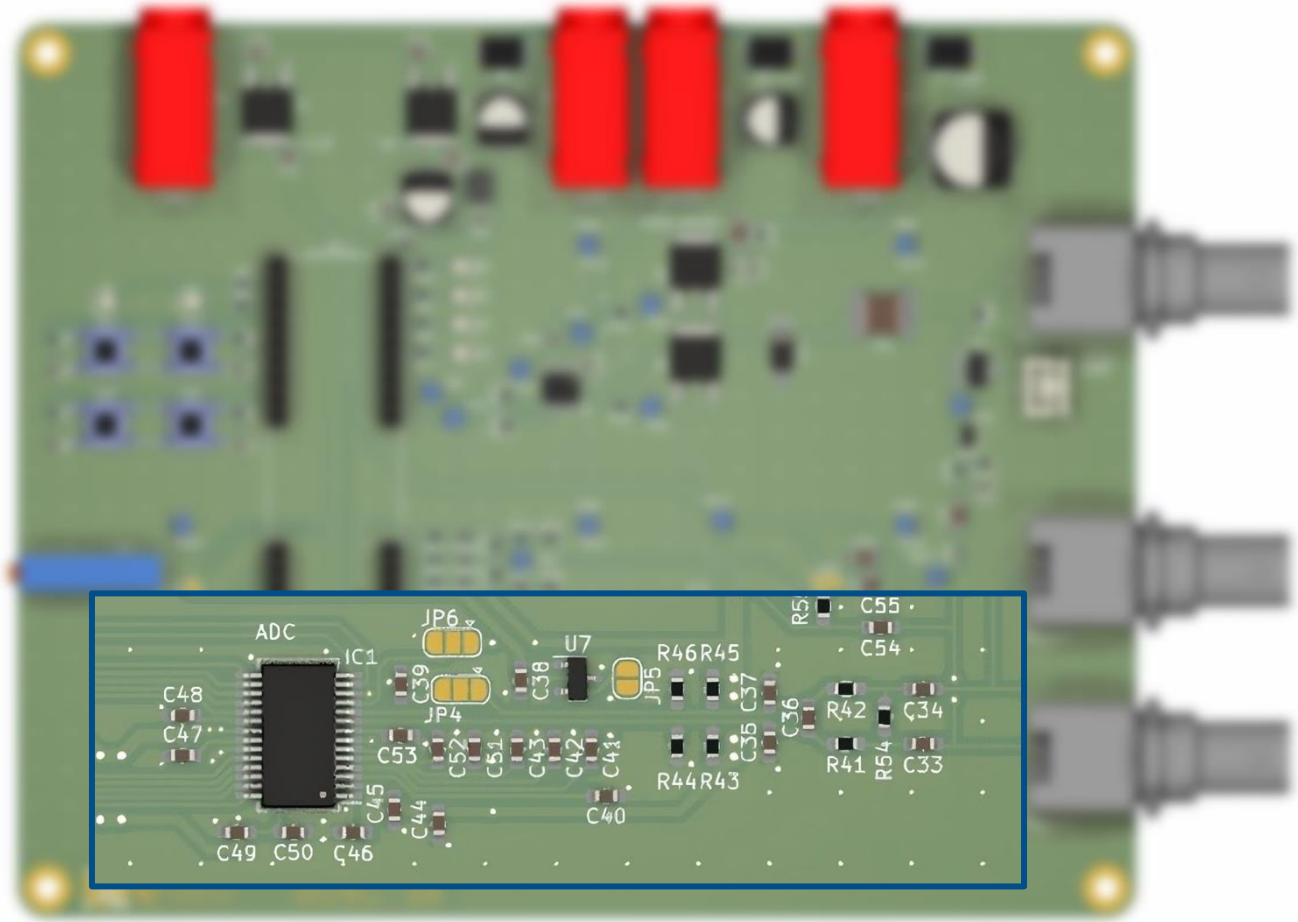
PCB DESIGN

ADC stage:

- AC-coupled
- Low-pass filter network
- MAX1426 10bit 10MHz ADC
- Internal biasing; Vpp,diff = 4V



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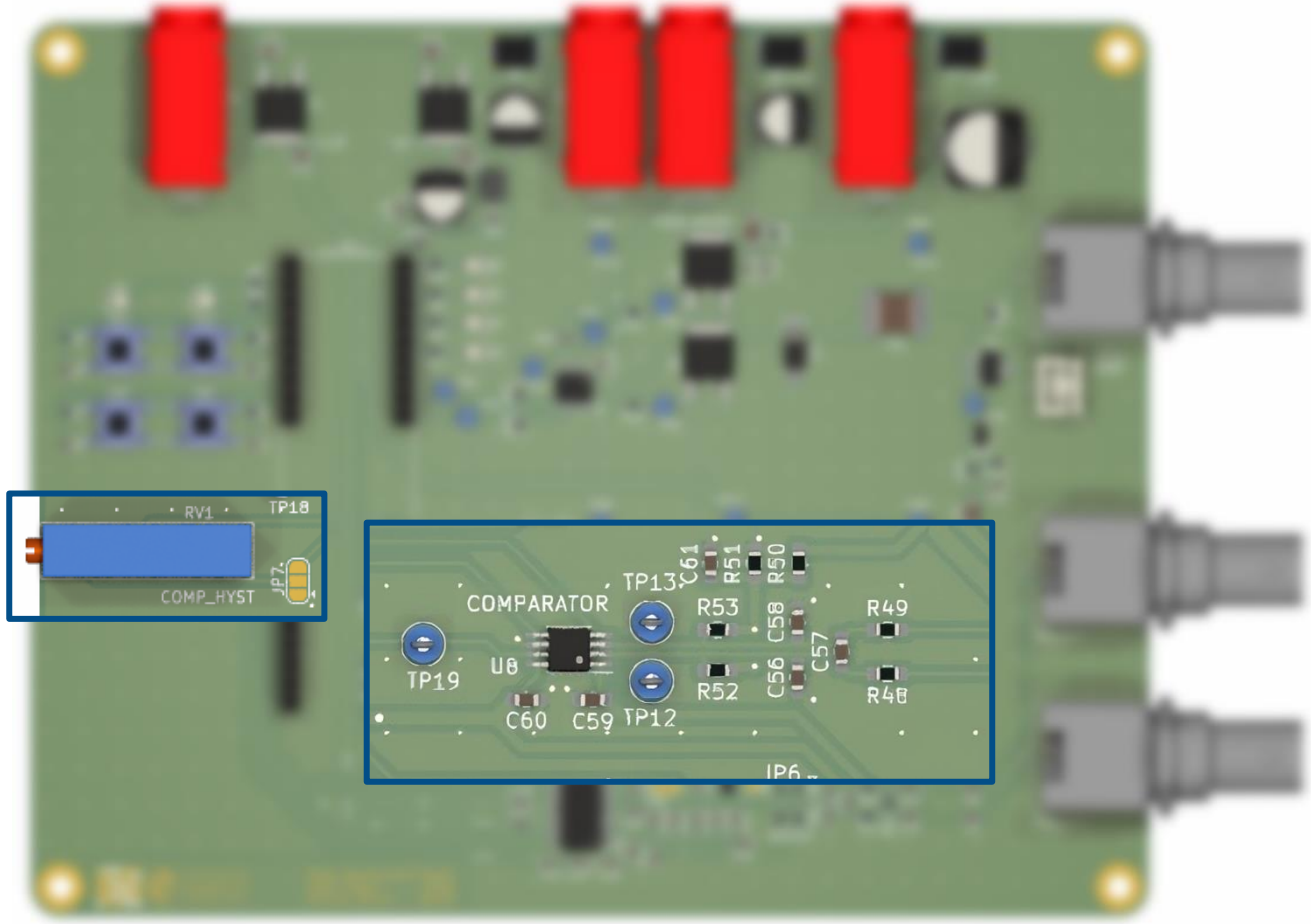
PCB DESIGN

Comparator stage:

- AC-coupled
- Band-pass filter network
- LTC6752 280MHz comparator
- External biasing
- Adjustable hysteresis



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FPGA MODULES

Main modules:

- comm_protocol
- vga_driver
- comp_driver
- adc_driver

Helper modules:

Imported modules:

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FPGA MODULES

Main modules:

- comm_protocol
- vga_driver
- comp_driver
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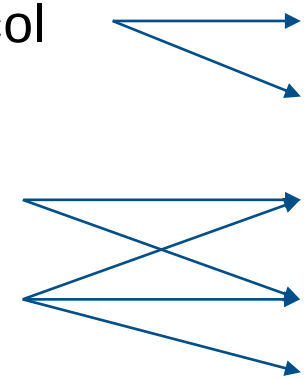

Helper modules:

- piezo_driver
- delay
- fifo_aggregate
- fifo_x2byte
- pulse_stretcher
- serial_tx_handler
- serial_rx_handler
- buttons_handler

Imported modules:

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FPGA MODULES

Main modules:

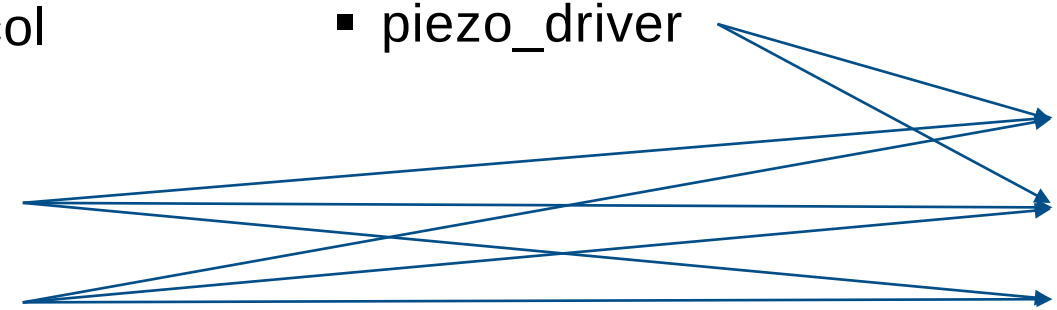
- comm_protocol
- vga_driver
- comp_driver
- adc_driver

Helper modules:

- piezo_driver
- serial_tx_handler
- serial_rx_handler

Imported modules:

- mmcme2_*
- xpm_cdc_*
- xpm_fifo_async
- uart_tx
- uart_rx



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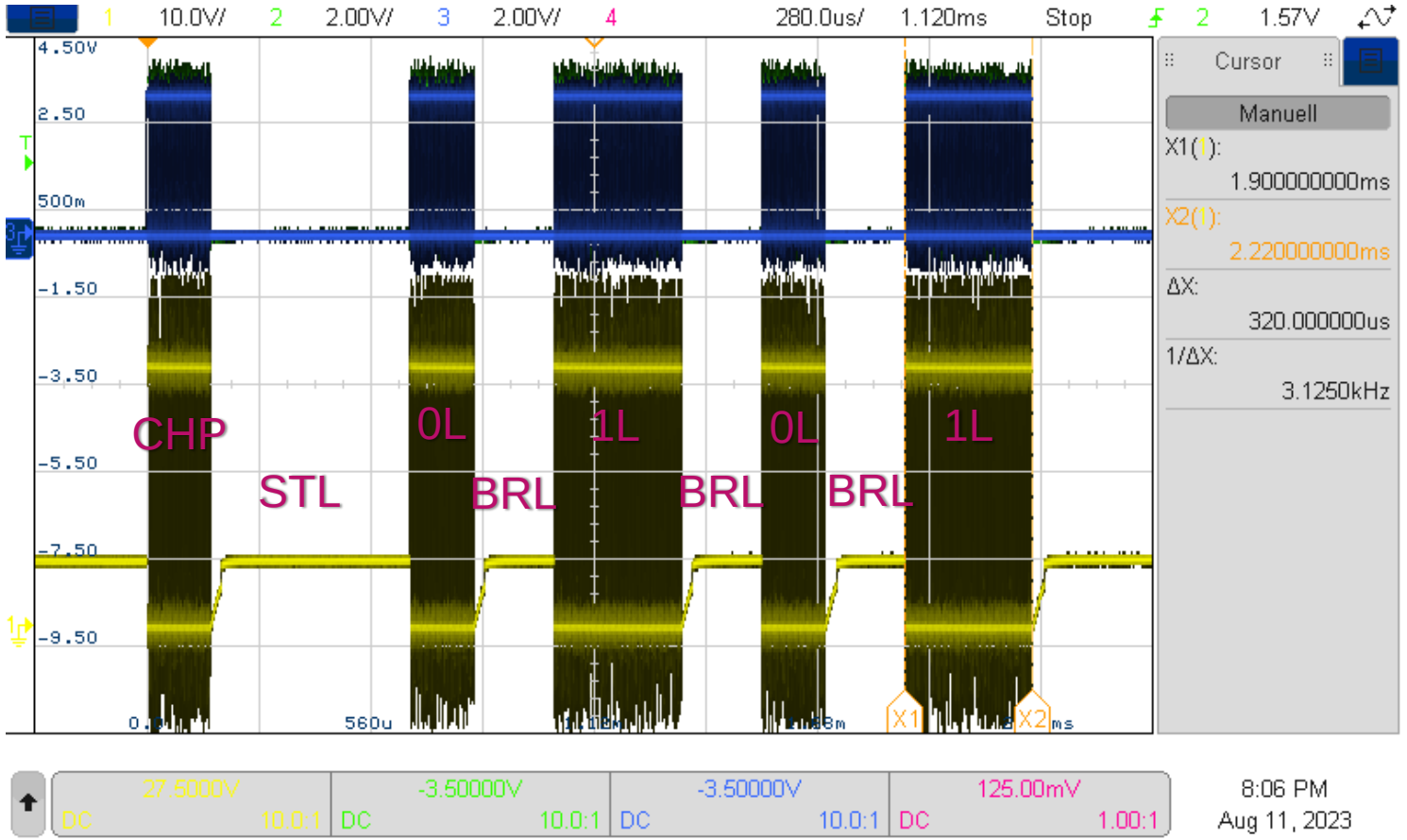
RESULTS – TRANSMISSION

Low-side and high-side output from FPGA

Half-bridge output to primary piezo



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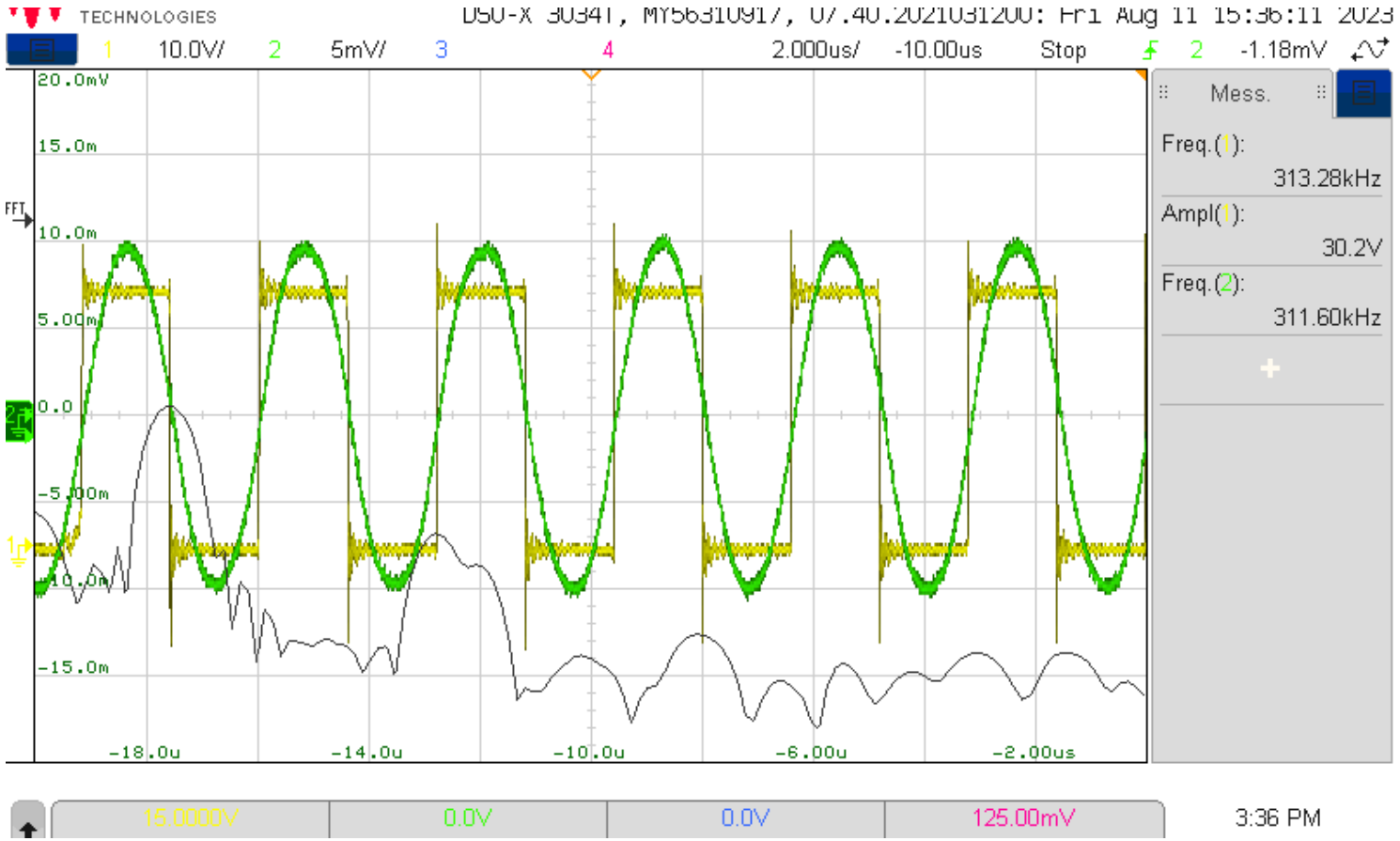
RESULTS – TRANSMISSION

Secondary piezo output

Half-bridge output to primary piezo



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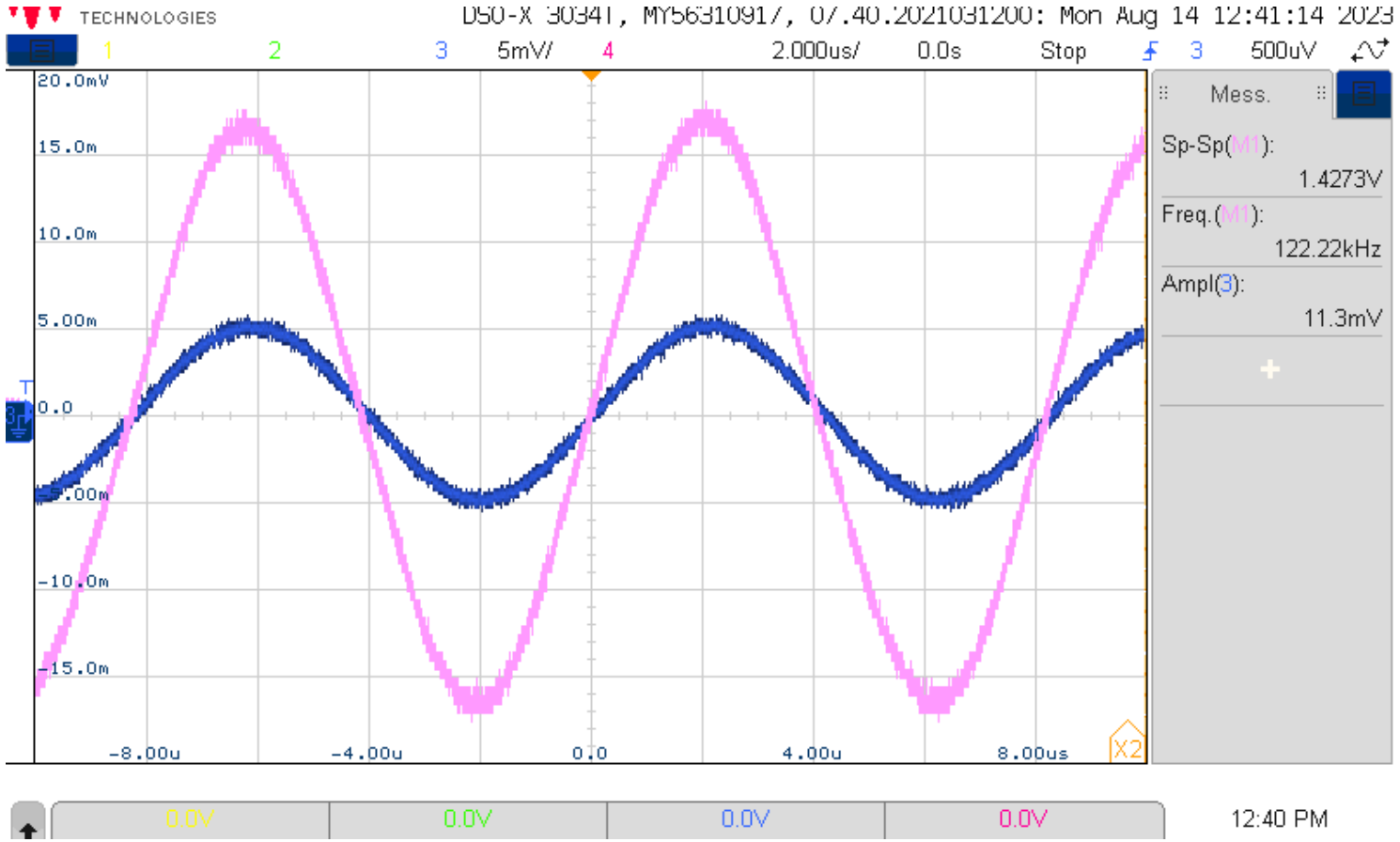
RESULTS – VGA

Amplified differential output signal

10 mV input signal



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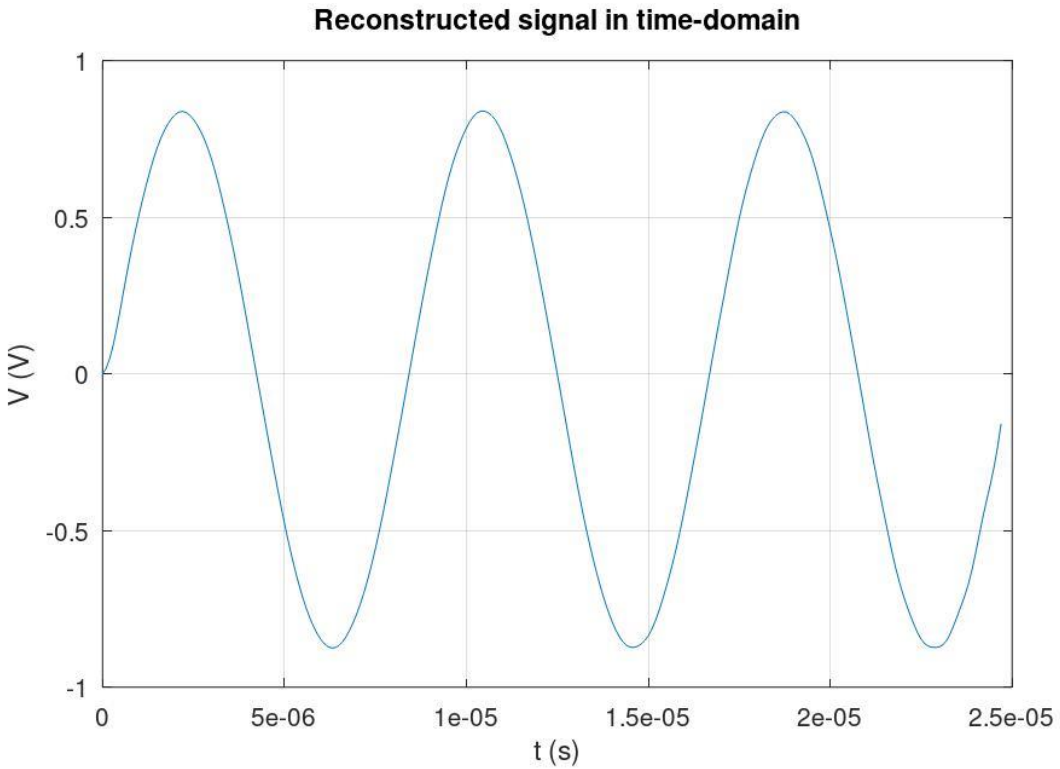
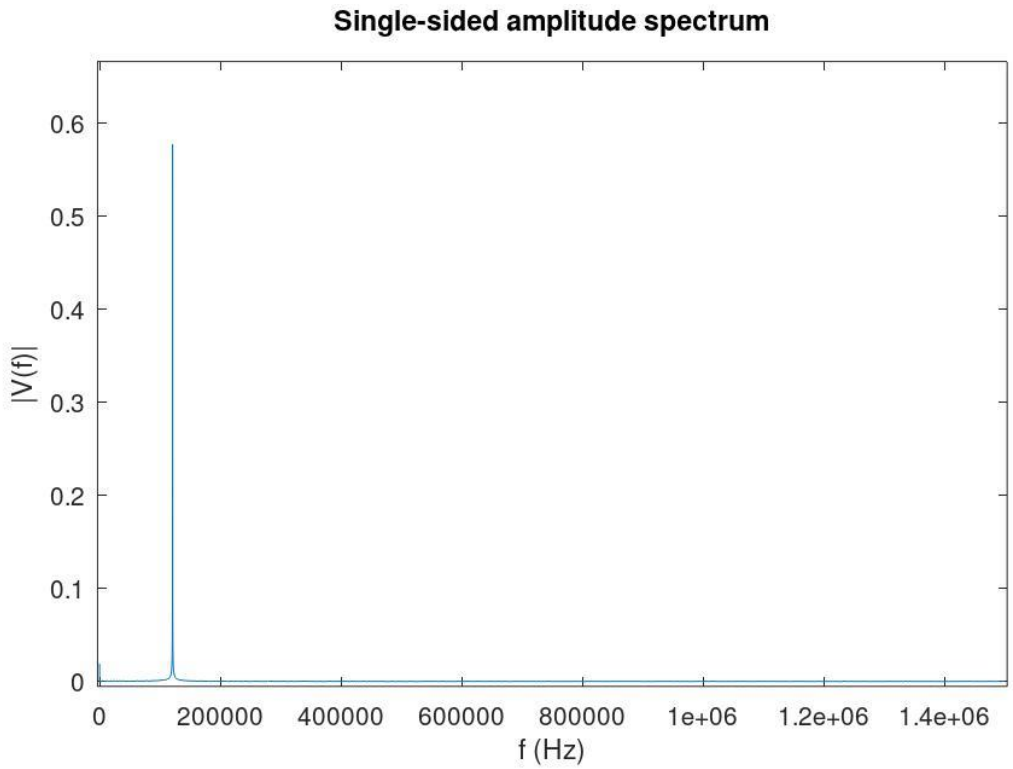
RESULTS – ADC





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CONCLUSION

- Hardware platform:
  - Drives piezo at specified loads (38 V, 100 Ω load, 2 MHz switching frequency)
  - Sampling of up to 5 MHz signals (ADC) or up to 25 MHz (comparator)
- Software platform:
  - OOK transmission scheme
  - Variable sampling frequency and bit width
- Possible improvements:
  - Increased host communication speed
  - Other transmission schemes