Guaranteeing Reaction Times for Predictable Real-Time Applications on Multicore System with Shared Resources

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In this paper, we present a static analysis that guarantees the execution times of concurrent programs that comply with Globally Asynchronous Locally Synchronous (GALS) formal model of computation (MoC) on chip multiprocessor with shared resources such as memory while using minimal resources. The interference to shared resources represent a bottleneck for timing predictability which is controlled by deploying Time Division Multiple Access (TDMA) and guarantees bounded delays. TDMA may lead to at the same time to increasing memory access latencies exacerbating the execution time of task dominated with memory access instructions on a particular processor with fair based slot allocation technique. The analytical tool statically analyses the program during compilation and finds out memory reference and non-memory reference instruction along the worst case execution path. It then computes the worst case execution time for each of the task running on a processor and calculates individual slot lengths for each processor so that all the tasks meet the deadlines which is inter arrival time between inputs. We demonstrate the applicability and computational efficiency of the presented methods by execution of benchmarks on multiprocessor based embedded system with a TDMA bus, where we will find the optimal parameter set for the TDMA bus.

In this paper, we propose an approach to worst-case execution time analysis and system scheduling for real-time applications implemented on a multiprocessor SoC architectures.

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Additional Key Words and Phrases: Wireless sensor networks, media access control, multi-channel, radio interference, time synchronization

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# INTRODUCTION

The growth in semiconductor industry has allowed us to realize more transistors and as a result, more computational power on a single larger dies. This has helped us to realize even more complex applications which were not possible to realize due to limited computational capabilities. These complex applications required more and more processing speeds which have been achieved by lowering the feature size and increasing the frequency of a uniprocessor in the past. Due to increased power consumption area and lack of cooling mechanism does not allow to exploit this feature any further for the quest of more processing power. This leads to a system where multiple processors are used to exploit the parallelism of the application by executing the different tasks or processes on different processors. The performance gain also achieved even if there is no parallelism as the task being executed on individual processor need not to be interrupted thus avoiding the context switch time. The multiprocessor system integrates two or more processing units and a sophisticated communication network into a single integrated circuit. The homogeneous multiprocessor processor systems consist of identical processors connected to a single shared memory to save resources and keep the price real-state low.

Furthermore, modern embedded systems consist of many computational units leading to GALS paradigm [[Chapiro 1985](#_ENREF_3)]which is based on a system composed of a number of synchronous modules designed in a traditional way which communicate asynchronously using handshake.

Today, many embedded systems are deployed for safety critical applications where real-time behavior is more important than computation power. Failure to meet deadlines may result in the loss of life or in large damages. For a real-time application, predictability with respect to time is of uttermost importance. Therefore, such systems must undergo a timing analysis. In general, upper bounds on the execution times, also called worst case execution times, are needed to show the satisfaction of stringent timing constraints, which are derived from the hard real-time systems controlled. A lot of research has been carried out in the area of worst case execution time analysis [[Puschner and Burns 2000](#_ENREF_16)]. However, according to the proposed techniques, each task is analyzed in isolation, as if it was running on a monoprocessor system. Consequently, it is assumed that memory access over the bus takes constant amount of time to process, since no bus conflicts can occur. In case of multiprocessor system, the processors are connected to share memory which requires arbitration. The time to gain access to shared memory may vary significantly, depending on the used bus arbitration protocol and access timings. Hence, application tasks running on different processor may influence the execution time of each other. A precondition for predictability is to use a predictable bus architecture which could take into the interference or completely eliminate it. One way to eliminate shared bus interference is to adopt time-division multiple access (TDMA) arbitration, which grants each CPU access to the bus on a fixed, statically predictable schedule and consequently, a constant bandwidth to each processor and makes it suitable for modern system-on-chip design with timing constraints. The bus schedule defines the behavior of the arbiter. It consists of sequence of slots and each slot is owned by exactly one processor with exclusive rights to access the bus during that ti9me period. With the use of TDMA arbitration scheme, the WCET of an arbitrary memory access of a processor is given by the following equation:

WCETaccess = (P-1).Ts + taccess

Where P specifies the number of processor in the system and Ts gives the width of a slot in clock cycles. taccess describes the memory access time in clock cycles and also determines the lower limit for Ts (no split transaction) so that a processor could successfully access the memory in single slot. P-1 gives the number of slots which, a processor requesting a memory access, needs to wait before its allotted slot where its request is entertained.

The above equation reveals that worst case memory access time depends on the number of processors in the systems indicating that multiprocessor system improves power consumption and performance on one hand but deployment of too many resources might also result in degradation of performance as is the case here. Thus, the bus access delay is the factor with greatest potential for overestimations during WCET analysis.

Furthermore, task running on different processor are not identical may have different amount of memory accesses. The fair TDMA schedule, where each processing element gets the same number of slots, might seem unfair to the processing element executing the task with more frequent memory accesses as compared to other processing elements with no or minimal memory accesses. The general TDMA policy may lengthen the WCET due to allocation of equal amount of time (slot) to a processor with no or minimal memory access requirements. This might result in missing deadlines. Therefore, the slots or slot length allocated to a processing element should be proportional to the number of memory accesses contained by the clock-domains executing on it, weighted TDMA schedule. The weighting of the slots is not a solution as the consecutive slots in TDMA schedule might improve average case execution time but not the worst case as P-1 factor remains the same. A perfect TDMA schedule is the one where slot allocated to a particular processing element perfectly aligns with its memory accesses. This is only possible if memory access pattern is statically analyzable. Since the memory access pattern depends on the path taken during execution which depends on the input. Unfortunately, in general the worst-case input is not known and hard to derive. The oblivious memory access pattern does not allow calculating tighter execution times. The only way to achieve the tighter worst case execution times is by providing a TDMA schedule which results in reduced wait time.

One of the obstacles when performing the timing analysis on the multiprocessor system is that the scheduling of task assumes that their worst case execution times are known. However, to calculate these worst case execution times, knowledge about the task schedule is required. We have integrated both in one frame work. The worst-case execution time analysis is performed with fair bus schedule and, if unable to meet the timing requirements, a weighted bus schedule is provided which meets the timing requirements.

The allocation of tasks to processors in a multicore processor system is an issue which needs some attention. Two questions needed to be answered: 1) what is the minimum number of processor core to be used so that system meets all timing construct while using minimum logic resource and 2) What number and combination of clock-domains should be allocated to each core in the system so that the system meets all the timing constraints. The simplest answer can be to allocate a single clock-domain to each processor node in the system. But, systemJ programs can be very large and comprise of hundreds of clock-domains and allocating a single clock-domain allocation policy will result in hundreds of processors used and it may turn out impractical to implement such a huge number of cores. This need design space exploration to come out the system implementation optimized in terms of latency and resource requirements. The parameters which need to be evaluated are the number of cores objective for design space exploration will be to meet the reaction time.

The objective of this paper is to address, at the system level, the specific issue of predictability for embedded systems implemented on current and future multiprocessor architectures.

We only model instruction caches and thus assume that data access occur via a different bus and do not interfere with the instruction access in any other way.

Assumptions

We

In this paper, we present a framework which takes a SystemJ program and analyze and calculate the worst case reaction time of each clock-domain assuming that the processor executing it has exclusive access to the memory. It than allocates the clock-domains to the processors such that the required execution times are met while using minimum number of cores. It means each core is allocated at least one clock-domian and may execute more if timing constraints are met. If required run time is too large, then all the cores can be run on a single processor. As mentioned earlier, shared resources (memory in this case) affect the execution of the clock-domains on a processor, resulting in lengthening of execution times, it recalculates the worst case reaction time of each clock-domain assuming a generic TDMA schedule. If timing guarantees are violated, the tool gives weighted TDMA schedule where each processor is allocated a number of slots in a TDMA cycle while guaranteeing the required reaction times.

**Contributions**

A contribution of this paper is

* The extension of the WCET tool for timing analysis of the SystemJ programs running on JOPPlus.
* The design space exploration of system which allocates the clock-domains to the individual processor in a clock-domain with an objective to minimize the resource usage while guaranteeing the required reaction times.
* Find out the TDMA weights for each processor so that all the clock-domains meet the GRT. It can be composed into: that makes at least one individual [better off](http://en.wikipedia.org/wiki/Utility) without making any other individual worse off is called a Pareto

# Motivational example

Let us consider four clock-domains C1, C2, C3 and C4 with worst case reaction time of WR1, WR2, WR3 and WR4 having values 20 (5I + 15M), 15 (5I+10M), 25(10I+15M) and 35 (20I + 15M) cycles, respectively. The worst case reaction time is equal to number of instructions falling in the worst case execution path assuming that each instruction takes single cycle to execute while I and M indicates non-memory referenced and memory referenced instructions, respectively. The required run time of the clock-domains should always be greater than the worst case reactions. Let RR1, RR2, RR3 and RR4 are the required run times of each individual clock-domain having values of 30, 40, 45 and 50 respectively. These clock-domains will be executed on a multiprocessor system. The framework is provided with worst case reaction time and required run times as constraints with an objective that these clock-domains are allocated to minimum number of processors. If all clock-domains are allocated on single processor with cyclic execution scheduling policy, then the reaction time of each clock-domain is 175 (=30+40+25+35) which is much higher than the required run time resulting timing violations. Therefore, they cannot be allocated to a single processor. In other extreme case, each clock-domain can be allocated to an individual processor in shared memory multiprocessor system with fair based TDMA interconnection mechanism. The introduction of fair TDMA access introduces delays as each processor has to wait for its slot before it can access the memory. Since there are four slots, each processor will wait for 3 cycles when it comes across a memory access instruction. This results in degraded reaction times of 25, 45, 70 and 80, respectively. This highlights two issues: firstly, too many logic resources (processors) are needed and secondly, the clock-domains are unable to meet the required execution times due to excessive delays introduced by the deployment of TDMA.

As it can be seen that CD 1 and CD2 can be assigned to a single processor as the WR1 + WR2 > MIN (RR1, RR2), the worst case reaction time of all clock-domains is sum of their individual worst case reaction times when executed in a cyclic executive fashion. The remaining clock-domains will be allocated to individual processor as they will be unable to satisfy conditions mentioned above. The frame tries all possible combinations of clock-domain which could allocate maximum number of clock-domains to a single processor as while meeting the required run time at the same time. As a result, the multiprocessor system consists of three processors P1, P2 and P3 with CD1 & CD2 being allocated to P1 and whereas CD2 and CD3 are allocated to P2 and P3, respectively. The reaction times for clock-domains without considering the shared resource are 35, 35, 25 and 35 in the same order for all clock-domains. Assuming shared resources connected through fair based TDMA, the worst reaction times are inflated and become 60, 60, 30 and 50. An analysis of the instructions reveals that the processor P1 needs to access the shared the resources more often than others, therefore, it should be given more time (slots here) to access the shared memory. In other words slots should be according to the memory access requirement of each processor.

The framework provides the weight of each slot so that all the time requirements are met. It comes out with a solution where base cycle has four slots with one slot allocated to P1 and one slot is allocated to each of the other clock-domains.

P1, P1, P2, P3

Since the memory access pattern is not known, having two consecutive slots in a base cycle does not improve the worst case execution time of any of the clock-domains, instead, it worsen the execution of time of CD3 and CD4 which now becomes 45 and 70. If we allocate the slots in such a way such that the distance between two consecutive slots of P1 becomes minimum, this will improve the execution time of the clock-domains running on the P1. The following slot allocation will result in a single wait cycle for P1:

P1, P2, P1, P3

Now the memory access times for all the four clock-domains become 60, 60, 70 and 80, in the order.

# Related Work

WCET analysis has been an investigation topic for already a long time, the basic driving force of this research has been, and still is, to improve the tightness of the analysis and to incorporate more and more features of modern processor architectures. However, one of the basic assumptions of this research is that WCETs are determined for each task in isolation and then, in a separate step, task scheduling analysis takes the global view of the system [[Thiele and Wilhelm 2004](#_ENREF_21)]. This approach is valid as long as the applications are implemented either on single processor systems or on very particular multiprocessor architectures in which, for example, each processor has a dedicated, private access to an exclusively private memory. The WCET analysis of multiprocessors [[Andrei et al. 2008](#_ENREF_1); [Rosen et al. 2007](#_ENREF_17)] is based on a multiprocessor system-on-chip with a shared communication bus, connecting several CPUs with two different types of memory. The approach estimates WCET and performs bus access optimization in the global context system optimization. But, it only handles synchronous tasks and is not capable of dealing with asynchronous task where start time of the tasks is not known. This makes it impossible to determine the precise time at which every single memory access takes place. [Pitter and Schoeberl (2010)] compared the predominant arbitration methods, and TDMA arbitration resulted as the most predictable method. However, in order to avoid the problem of scheduling tasks, they assume that the numbers of cores are greater than the number of tasks. This is also the conclusion that is drawn in [Wilhelm et al (2009)], where future architectures of time-critical embedded systems are discussed. Our approach not only deals with the problem of scheduling task but also finds the optimal resource usage.

# Preliminaries

SystemJ

The system-level programming language SystemJ [[Gruian et al. 2006](#_ENREF_4); [Malik et al. 2010](#_ENREF_10)] extends Java with synchronous and asynchronous concurrency and reactivity, making it suitable for designing complex embedded programs. The language allows use of full Java and discourages the use of Java concurrency (threading library). Instead, SystemJ provides its own concurrency model based on the formal Globally Asynchronous Locally Synchronous (GALS) model of computation (MoC). A SystemJ program consists of multiple asynchronous processes, called clock-domains (CD),which are described at the top design level. The clock-domains are composed together with the asynchronous parallel operator (><). Each clock-domain consists of a number of synchronous concurrent processes, called reactions, which execute in lock-step, driven by a logical clock, called tick. A synchronous program reacts to its environment in a sequence of ticks, and computations within a tick are assumed to be instantaneous, i.e., as if the processor executing them was infinitely fast. The reactions communicate within a clock-domain, as well as with the external environment (input/output) through signals, which are broadcast and present within the current tick and comply with synchronous reactive MoC [16, 41–43]. The reactions are represented as concurrent processes within a clock-domain using the synchronous parallel operator (||). Communication between reactions in different clock-domains, which are asynchronous each to the other, is carried out through the exchange of messages over channels, which are semantically the same as channels used in CSP MoC [1, 23]. Besides operations on signals and channels, SystemJ allows free use of Java data objects and statements in its reactions, and those statements are considered instantaneous in terms of logical time (i.e. they do not consume logical time or ticks). Control flow of a SystemJ program incorporates scheduling of all reactions and clock-domains, as well as communication between reactions, and communication with the external environment. The data-driven computations and transformations are performed in Java.

The system is the top level entity through which a SystemJ program sees its environment and vice versa. In the declarative part of the system entity, the interface with the environment (whichare input/output signals) and channels are declared. The clock-domains are declared inside the body of the system. The channels serve as the communication medium between the clock-domains. Multiple clock-domains, which are asynchronous processes, are also declared in thebody of this entity. Within a system, each clock-domain executes at its own tick, and any two clock-domain ticks are unrelated.

Each clock-domain consists of a number of synchronous concurrent processes called reactions. The clock-domain can be given some name or can be unnamed. The clock-domains can communicate with each other and with the environment using their own set of channels and signals, respectively. Two clock-domains synchronizing with each other using CSP style communication are called partner clock-domains. The data structures cannot be shared among the reactions and among the clock-domains. This prohibition allows communication only through the signals and channels, which is safer and easier to validate. Reactions are combined and controlled within a clock-domain using the synchronous parallel operator (||).As mentioned earlier; communication between reactions of different clock-domains is carried out through the exchange of messages over channels. They are used to synchronize the clock-domains. The channels can be of any Java type and are declared in the interface body of the system. The clock-domains are synchronized through channels using CSP style rendezvous mechanism. The idea is that two clock-domains rendezvous at a point of execution, and neither is allowed to proceed from that point until both have arrived, but they can proceed to execute other reactions of the same clock-domain if needed. The channels are point-to-point i.e., for every sending channel port there needs to be a corresponding receiving channel. The channels are unidirectional, therefore, they are always declared in pairs (input and output).Every channel has status and value buffers which are used to implement the rendezvous communication. Besides signals and channels objects, SystemJ allows free use of Java data objects in the program.

The SystemJ is amenable to verification as it is based on mathematical semantics and can be deployed in mission critical systems. Figure 1 gives an abstract representation of a SystemJ program that implements an extended version of asynchronous protocol stack [[Nadeem et al. 2013](#_ENREF_14)]. This program is readily runnable on any processor with JVM. It has three clock-domains; the first clock-domain models the packet generation from a network device, while the second and third clock-domains implement the main functionality of ***protocol stack*** [[Gruian, Roop, Salcic and Radojevic 2006](#_ENREF_4); [Lavagno and Sentovich 1999](#_ENREF_6)], which can be extended to model complete communication stack like TCP/IP. There are three synchronous parallel reactions in each protocol\_stack clock-domain: *Assemble*, *Checkhdr* and *Stack*. The *Assemble* reaction receives the bytes asynchronously on channel and assembles them into a packet that is sent synchronously through a valued signal for further processing. The packet is awaited for in reaction *Checkcrc*, a *Cyclic Redundancy Check* is carried out on it and the outcome of this test is emitted through a Boolean signal further. Note how both the data and data operations are neatly encapsulated in the *Packet*, thanks to Java object orientation, making the code more legible. The *Prochdr* reaction carries out an address match computation in parallel with checking the *crc ok* signal. If the packet is faulty, the address calculation is aborted by emitting a signal (line 52), monitored by the address matching sub-reaction. Finally, the full protocol stack is another reaction, *TheStack*, which contains just a synchronous composition of the *Assemble*, *Checkcrc*, and *Prochdr* reactions. Note that the valued signals *packet* and *crc ok* are local signals, hidden from the environment outside *TheStack*.



Fig. 1. The asynchronous protocol stack

SystemJ programs integrate both control-driven and data-driven operations which are separated at the compiler back-end. The control flow representing control-driven operations is named Concurrency and Reactivity Control Flow (CRCF). Besides control flow of the reactions, CRCF also includes scheduling of all reactions and clock-domains, communication between reactions and clock-domains, and communication with the environment. On the other hand, the control flow of data-driven operations is called Java Control Flow (JCF), since all data computations of SystemJ programs are compiled to Java bytecodes.

Time-Analyzable Chip Multicore Processor

Then these control flows can be supported in the execution platform by using the extended execution unit. This new execution unit has single instruction decoding unit and performs very efficient switching between CRCF and JCF when necessary. At the same time the compiler did not require any modifications. Thus, all SystemJ and JOP tools, without practically any modification, are made ready for the new processor.

The multicore platform used in this research is called GALS-CMP which implements the symmetric shared-memory multiprocessor model [[Hennessy and Patterson 2003](#_ENREF_5)]. The GALS-CMP follows the methodology adopted by the time predictable multiprocessor system JopCMP [[Pitter and Schoeberl 2007](#_ENREF_15)]. Several JOP-plus [[Nadeem et al. 2012](#_ENREF_12)] cores, an extension of JOP [[Schoeberl 2005](#_ENREF_18); [Schoeberl 2008](#_ENREF_20)], provides the basis of the homogeneous CMP as depicted in Figure ccc. JOP-plus provides a seamless integration of both control and data execution modes in one processor unlike TP-JOP [[Nadeem et al. 2011](#_ENREF_11)]which uses two different processors thus consuming too many logic resources. The JOP-plus supports two separate components of the control flow in SystemJ programs, Concurrency and Reactive Control Flow (CRCF) and Java Control Flow (JCF), by extending the instruction set of the original JOP while using single execution unit. JCF is dealt in conventional was as the JOP while CRCF is stored in a separate memory. The control execution is capable of invoking the data computations in Java, which then returns to the control directly. Shared memory is used to store Java data computations (JCF) made of a collection of Java methods that are loaded upon call from the control code into local method caches of individual cores before they are executed. Also, shared memory is used to store the JVM run time data areas. The JOP features a stack cache for the private data of each thread. Additionally, a kind of instruction cache (called method cache) limits the memory access frequency and increases the processing power. JOP-plus is also a time-predictable processor. One of the highlighting features of JOP-Plus is that it is designed in a way so that it can use all SystemJ and JOP tools without practically any modification.

The depicted GALS-CMP architecture shows a synchronization unit which has the responsibility to coordinate access to the shared objects by a mutual exclusion mechanism. All cores are connected to each other and to the memory via simple SoC interconnect(SimpCon) [[Schoeberl 2007](#_ENREF_19)] which provides point-to-point interconnections between components. All cores communicate with each other through the shared memory and an arbiter is used when multiple masters try to access the same slave.



Fig. ccc. GALS-CMP system.

# Methodology

Figure ddd gives an overview of our framework. SystemJ compiler front end compiles the GALS program described in SystemJ and produces AGRC in step 1. This together with abstract details of processor is fed to TACO framework in step 2 which calculates the WCRT of each clock-domain in isolation as if running on a dedicated processor. The framework analyses for worst case execution path and finds out all instructions falling in this path by separating them into memory referenced (M) and non-memory reference (I) instruction. This information together with the execution platform details is used to calculate the worst case reaction time. It then generates a Task Graph (TG) where each clock-domain is represented as a task annotated with its WCRT. The details of TACO framework are provided in Section 5.2. This TG together with AG and timing information is fed to design space exploration tool in step 3 with an objective to schedule all the clock-domains on minimum number of processor while meeting all the timing constraints. These objective functions and constraints are also formulated using ILP. Any ILP solver (e.g. Gurobi) can be used for deriving the whole program’s schedule whose details are provided in Section 7.The result of step 3 is multicore system connected to a shared memory via bus. For shared bus, we assume a TDMA-based round robin arbitration policy, where a fixed length bus slot is assigned to each core

The WCRT of all the clock-domains are recomputed for multicore architecture at step 4 accounting for allocation and delays due to TDMA. In case, time constraints are violated which are due to memory access, a weighted schedule for TDMA is computed at step 5 thus providing more bandwidth to processor excessive memory reference instructions so that it is able to meet the timing requirements. The details are provided in Section



Fig. ccc. GALS-CMP system.

## Memory Access Pattern

The SystemJ compiler compiles the program into CRCF instructions and JCF instructions which are executed on JOPPlus, an extension of JOP. JOP translates most of the byte-codes to its native microcode instructions. Each byte-code is composed of a microcode instruction or a series of microcode instructions. Some byte-codes are actually implemented in hardware. A couple of byte-codes are implemented in Java. According to the JVM specification [[Lindholm and Yellin 1999](#_ENREF_8)], the heap and the method area are shared data areas, whereas the stack is a private data area for each thread. In JOP, the heap and the method area are located in the main memory. Consequently, all byte-codes that work on these areas have to be carefully examined. Some byte-codes access the memory several times, some only once. Hence, it makes sense to have a closer look at the different instructions.

Table II summarizes the bytecodes that access the main memory. Most memory access patterns of the bytecodes can be statically analysed; i.e. bytecodes that access the heap and those of type *const*. The pattern is only dependent on the memory access time. If the memory access time is known, the memory access pattern of the bytecodes can be analyzed regardless of the source code of the program. An example of such a bytecode is *ldc*, which pushes a single word constant onto the stack. Therefore, only one memory access to the method area is needed. JOP translates this bytecode into a series of microcodes. If the memory access time is known, the memory access pattern can be specified using JOP’s bytecode implementation. Another example is *iaload*, which is implemented in hardware. For the analysis of the memory access pattern, we determine the VHDL implementation in combination with ModelSim simulations.

The memory access patterns of the bytecodes of type call and return need a dynamic analysis and are more difficult to attain. Each JOP is equipped with an instruction cache that caches complete Java methods [14]. Consequently, the memory access patterns of these bytecodes vary, depending on the history of the execution. If the method is already in the cache, no additional memory accesses are needed to load the method into the cache. If a cache miss occurs, JOP will have to load the whole method into the cache.

The bytecodes data*call* and *returnresult* have different behaviour as compared to return and call. The methodcall bytecode directly invokes a method and always result in cache miss. Similarly, *returnresult* from a Java method to CRCF will not return to cache loading instead simply writes to CRCF memory and return to CRCF instruction execution. Depending on a cache hit or a cache miss and the length of the method that has to be loaded, the access pattern is created for each individual occurrence of the bytecode in the source code and integrated in the generation of the patterns into the WCET analysis tool where the cache information is available.

Table II. Bytecodes accessing the shared memory

|  |  |  |
| --- | --- | --- |
| **Type** | **Bytecode** | **Memory Area** |
| const | ldc, ldc\_w, ldc2\_w | Method Area |
| get | getfield, getstatic | Heap |
| put | putfield, putstatic | Heap |
| array | aaload, aastore, baload, bastore, caload, castore, daload, dastore, faload, fastore, iaload, iastore, laload, lastore, saload, sastore, arraylength | Heap |
| call | invokeinterface, invokespecial, invokestatic, invokevirtual, datacall | Method Area |
| return | areturn, dreturn, freturn, ireturn, lreturn, return, returncrcf | Method Area |
| new | anewarray, multianewarray, new, newarray | Heap |
| switch | lookupswitch, tableswitch | Method Area |
| cast | checkcast, instanceof | Heap |

## WCET Analysis

We use TACO [[Zhenmin et al. 2014](#_ENREF_22)], static analysis framework, for tight WCRT analysis and code optimization for each clock-domain of SystemJ programs. As shown in Fig [TODO] in Section [TODO], the TACO framework is invoked from Steps [TODO] to [TODO] in the complete flow of our approach. The source code of SystemJ program is firstly compiled into *Asynchronous GRaph Code* (AGRC) intermediate representation using the front-end of SystemJ compiler presented in [[Malik et al. 2011](#_ENREF_9)] (step 1). The AGRC extends the *GRaph Code* (GRC) with asynchrony by composing separated GRCs, one for every clock-domain in the program, using afork and ajoin nodes. The AGRC representation at this step does not contain any timing information and is then sent to the back-end of SystemJ compiler for target code generation. The target code generated by SystemJ compiler for JOP-Plus is based on the standard Java Virtual Machine (JVM) instruction set for JCF and a customized instruction set for CRCF (step 2) [[Nadeem et al. 2012](#_ENREF_13)]. The produced codes are in the format of Java byte codes. During target code generation in step 2, the tracking information is also produced; indicating the original AGRC node from which a segment of target code is generated.Both CRCF assembly code and JCF Java code are analyzed by our customized WCET analyzer to calculate WCET information for each AGRC node (step 3). We modify the WCET Analyzer used in TACO framework [[Li et al. 2014](#_ENREF_7)] to accommodate JOP-Plus execution platform. We first extend the JOP WCET analysis tool, called *JOP WCET Analyzer* (WCA), to be able to analyze the byte code generated based on the newly added instruction set to implement CRCF. We then analyze the Java byte codes for CRCF and JCF separately using extended JOP WCA to attain node-level WCET information. When analyzing the JCF code for each Java data computation, we separately calculate the worst-case execution time for only memory accesses (WCMT) and instruction execution time without memory access (WCIT). The original AGRC is then back-annotated with the node-level WCET information acquired from step 3 to obtain *Timed Asynchronous GRaph Code* (TAGRC). We annotate both WCMT and WCIT for each node in the AGRC. Note here, the WCMT for any control node representing CRCF is always 0 since no shared memory access occur during CRCF execution. In order to compartmentalize our WCRT analysis to each synchronous clock-domain, TAGRC is partitioned into a set of *Timed GRaph Codes* (TGRCs), one for every clock-domain. After obtaining TGRCs, model checking based tight WCRT analysis is carried out in steps 4-6. In step 4, each TGRC obtained from step 3 is translated to *Timed Automaton* (TA). Instead of using real-valued clocks, we employ a single bounded integer to capture the total time cost of a complete transition from the beginning to the end of a logic tick.The UPPAAL model checker [[Behrmann et al. 2004](#_ENREF_2)] is used in TACO framework as it offers efficient algorithms for both TA and automata with integer operations, while offering an excellent graphical user interface. All the timed automata produced in TACO framework are in the format of UPPAAL model. During the translation from TGRC to TA we preserve the following information in the UPPAAL model: (1) the state encoding and decoding that capture tick transition semantics and (2) internal and output signal emission and testing. The preserved information essentially models the execution flow of the SystemJ program. After the UPPAAL model is produced, tight WCRT result can be obtained by using the model checker which will automatically identify the scenarios where conventional WCRT estimation techniques like Max-Plus algebra would produce large over-estimates.



Fig. 5. Overview of TACO framework

 

(a) (b)

Fig. 7. Translation from TGRC to UPPAAL Model of TA

## Translation from Timed GRC to UPPAAL Model

This sub-section describes the translation from TGRC to UPPAAL model (UM) of TA, which is illustrated in Fig. 7. The graph code shown in Fig. 7(a) is the TGRC for the Asproto example introduced in Section [TODO]. The corresponding UPPAAL model translated from the TGRC is shown in Fig. 7(b). The first step in the translation is to perform a one-to-one mapping for each node in the TGRC to a location in the UM. For example, afork node AF0 in the TGRC is mapped to the initial location AF0 in UM. Similarly switch node S1 is mapped to a location S1, and so on. Next, we map each control flow edge in the TGRC to a transition between two locations in the UM. The conditional branching is modeled by annotating the transitions with additional guards. For instance, the transition from location S1 to E3 in Fig. 7(b) has the expression S633==636 as its guard to capture the tick transition semantics based on state encoding and decoding of switch node S1 in Fig. 7(a).

The signal emission and state encoding process are captured by the assignments on the transition. In Fig. 7(b), assignments on transitions from E3, E7 and E8 model three distinct state encoding. Three bounded integers, i.e. wcrt, wcmt and wcit, are used to count the execution time for only memory access, the execution time without any memory access, and the total execution time for both types of execution, respectively. The execution time is counted within a single global tick and reset to zero upon completion of one tick (during transition AJ5 to AF0). Therefore, every transition in the UM is annotated with an assignment that increases the value of integers wcrt, wcmt and wcit by the corresponding WCET values of the target location. Due to the semantics of AGRC nodes related with control flow, modifications should be done to the UM to correctly model the execution flow. Because the parallelism of the branches forked out by a fork node is compiled away so that each branch is executed one after another. Thus, the join node should have a transition back to its corresponding fork node to model the semantics of fork and join node. Furthermore, since a tick starts at afork node and finishes at ajoin node, there should be a transition from ajoin node back to afork node to model the repetitive execution of ticks. The bounded integer wcrt should also be cleared to zero during the transition from ajoin node to afork node (from AJ5 to AF0), and at the same time all the signal statues and values are updated.

We model the tight WCRT analysis problem as verifying a CTL property in UPPAAL model checker. The tight WCRT, named WCRTtight, is the objective of WCRT analysis. WCRT-tight lies in the bounded range denoted by [WCRTlb, WCRTub]. WCRTub is a safe upper-bound of WCRT obtained by applying Max-Plus algebra to the TGRC, which is essentially summing up the maximum tick execution time of every reaction in the clock-domain. Similarly, we calculate a lower-bound of WCRT, termed WCRTlb, by summing up the minimum tick execution time of every reaction in the clock-domain. After translating TGRC to UM, we check the validity of a WCRT estimate of the clock-domain, termed WCRTest, by verifying a CTL property upon the UM using UPPAAL model checker. The CTL property is written as A[](wcrt ≤ WCRTest), meaning that the value of integer wcrt is less or equal to the WCRTest for every path starting from the initial location. In order to minimize the number of queries, we use standard binary search algorithm to find WCRTtight.

# milp formulations for weighted tdma

In this section, we first state the problem formally and then present the MILP constraint formulation for finding the optimal weighted TDMA solution in terms of resource usage while satisfying timing constraints for every clock-domain considering resource binding. In Section 4.1 we…, Section 4.2 presents the optimal constraint formulation (MILP). In Section 4.3 we ….

## Problem definition

The problem that we address consists of binding clock-domains to allocable JOP-Plus cores and obtaining a weighted TDMA scheme such that the minimum hardware resource usage is achieved and the timeliness of the system is guaranteed. Formally, the problem can be stated as follows.

Given:

* A GALS system described by a SystemJ program consisting of a set of asynchronous clock-domains , where denotes a clock-domain that is comprised of parallel reactions running synchronously in its own lockstep.
* An execution platform named GALS-CMP with TDMA based shared memory architecture. The GALS-CMP multi-core architecture is abstracted as a set of JOP-Plus cores , where represents a JOP-Plus core on which single or multiple asynchronous clock-domains are running.
* A TDMA bus access schedule specified as a set of time slot allocation schemes , where each time slot allocation scheme is applied to a unique JOP-Plus core. The representation of time slot allocation scheme is further discussed in Section TODO.
* A resource binding function associating clock-domains of the SystemJ program with JOP-Plus cores of GALS-CMP platform. Each JOP-Plus core is capable of executing any number of clock-domains.
* A set *Worst-Case Execution Time* (WCET) profiles, , for every clock-domain of the SystemJ program, where denotes the WCET profile for a single clock-domain. Each is characterized by a tuple , where represent the Worst-Case Memory Access Time (WCMAT) and denotes the Worst-Case Instruction Execution Time (WCIET) that does not involve memory accessing.
* A set of timing requirements, , for every clock-domain of the SystemJ program, where refers to the timing constraint for . Since every clock-domain is a unique synchronous hard real-time reactive system and the execution of a clock-domain is based on a logical and discrete clock event named *tick*, the timing requirements for is essentially the upper bound of the execution time between any two consecutive ticks, namely *Worst-Case Reaction Time* (WCRT) [TODO]. In other words, the WCRT for should be less or equal to its timing requirement, i.e. .

The objective is to find an optimal resource binding allocating clock-domains to the available JOP-Plus cores as well as an optimal TDMA bus access schedule for every JOP-Plus core used, such that all the timing requirements for every clock-domain are satisfied and the hardware resource usage in terms of the number of the JOP-Plus cores is minimized. Each feasible solution in the design space formed by varied resource binding and TDMA bus access schedule corresponds to a unique real-time characteristic of the system described by SystemJ program, in terms of WCRT estimates for every clock-domain. In this article we employ MILP method to explore the design space efficiently for finding the optimal solution in the matter of resource usage while meeting all the timing requirements. The MILP formulation the discussion about TDMA bus access schedule is given in Section TODO.

## TDMA bus time slot allocation scheme and access scheduling

In this section we discuss the time slot allocation scheme for TDMA based shared memory architecture used in GALS-CMP execution platform. We first give the definition for TDMA time slot allocation scheme a schedulability analysis for TDMA bus access.

As specified in Section TODO, the TDMA bus access schedule is represented as a set of time slot allocation schemes , where is the time slot allocation scheme applied to a unique JOP-Plus core . The execution time spent for to complete a single memory access (either read or write) is determine by TDMA bus access schedule.

**Property 3.1.** For any JOP-Plus core of GALS-CMP execution platform, the worst-case execution time for any single memory access (either read or write), denoted as , is bounded by the longest time interval between two consecutive memory access time slots plus the actual access time.

Due to the fact that is irrelevant to the length of TDMA time slots that are assigned to contiguous memory accesses, in our approach memory access time slots assigned to any JOP-Plus core are not contiguous, in order to simplify TDMA bus scheduling and facilitate schedulability analysis.

Let be a TDMA bus schedule for all the JOP-Plus cores sharing the bus. can be described by the complete set of time slot allocation schemes , where an allocation scheme for JOP-Plus core can be represented as its worst-case execution time for any single memory access, therefore TDMA bus schedule can be formulated as .

We name to be *unit memory access time* (UMAT) for core

Dynamic TDMA schedule, Static schedule

**Theorem 3.2.**

**Property 3.2.** The timing requirement for any JOP-Plus core of GALS-CMP execution platform, denoted as , is the minimum timing requirement of all the clock-domains mapped onto core .

## The MILP formulation for optimal solution

In this section, we present the MILP formulation that gives an optimum solution for the problem defined in Section TODO. We first discuss the TDMA bus schedule scheme for the

In the following description

Table 1 gives the nomenclature of various variables utilized in the formulation and acts as a quick reference for the reader.

Referring to Figure 1,

Integer linear programming (ILP) provides a method to achieve the optimal solution of a problem in which all of its constraints can be formulated as linear constraints of integer variables. Mixed-integer linear programming (MILP) is an extension of ILP for capturing problems with both discrete decisions and continuous variables. MILP provides a systematic approach to describe the complex interaction among resource binding, TMDA bus access scheduling, timing analysis and real-time property verification. Note here the resource binding and the TMDA bus access schedule jointly affects the worst-case execution time for each clock-domain.

*1.3.1 Constants*

Firstly we define the following constants that are derived from the problem definition:

* *Number of the clock-domains* : Let be the number of clock-domains comprising the GALS system described by a SystemJ program.
* *Number of the JOP-Plus cores* : Let be the number of JOP-Plus cores within the GALS-CMP multi-core execution platform.
* *Number of the unit memory access time (UMAT) candidate groups* : Let be the number of UMAT Candidate Groups comprised of sets of UMAT candidates.
* *Number of the unit memory access time (UMAT) candidates*: Let be the number of UMAT candidates forming a UMAT Candidate Group. For the sake of simplicity we assume that all UMAT candidate groups have the same number of UMAT candidates.
* *WCET profiles for every clock-domain* : Let be the set of WCET profiles, where is characterized by a tuple and denotes the WCET profile for clock-domain .
* *Timing requirements* : Let be the set of timing requirements for the SystemJ program, where refers to the WCRT constraint for .
* *Group of UMAT candidate*: TODO TODO Let

*1.3.2 Variables*

In this section, we define the independent and the dependent variables that are used in the formulation.

We define the following base (independent) variables:

* *Binding decision variable matrix* : We define a binary variable such that and ,
* *Unit memory access time (UMAT) Candidate Group decision variable* : We define a binary variable such that ,
* *Unit memory access time (UMAT) decision variable matrix* : We define a binary variable such that , and ,

We define the following derived variables:

* *Core utilization decision variable* : We define a binary variable such that ,
* *Worst-case memory access time variable*: We define an integer variable indicating the total worst-case memory access time for core after resource binding such that , is the sum of the worst-case memory access time (WCMAT) for all the clock-domains mapped onto core . Note here is calculated without considering the TDMA bus sharing.
* *Worst-case instruction execution time variable*: We define an integer variable indicating the total worst-case instruction execution time for core after resource binding such that , is the sum of the worst-case instruction execution time (WCIET) for all the clock-domains mapped onto core
* *Timing Requirement variable*: We define an integer variable indicating the timing requirement for core after resource binding such that , is the minimum timing requirement of all the clock-domains mapped onto core , as specified in Property TODO.

*1.3.3 Objective function*

The objective of the proposed MILP formulation is to minimize the hardware resource usage in terms of the number of the JOP-Plus cores, while satisfying the timing requirements for all the clock-domains mapped onto a set of JOP-Plus cores. The objective function can be stated as follows:

*1.3.4 Constraints*

In this section we elaborate the constraints to which the objective function is subject.

* *Resource binding constraint* : A clock-domain should be mapped onto only one JOP-Plus core. Therefore, for each , i.e.

(1)

* *Core utilization constraint* : If no clock-domain is mapped to core the core utilization decision variable for core should be zero, otherwise should be one. Therefore, for each , i.e.

(1)

For each and

(1)

* *Unit memory access time (UMAT) candidate group selection constraint*: In order to enable schedulable TDMA bus access, only one UMAT candidate group can be selected, as elaborated in Section TODO. Thus,

(1)

* *Unit memory access time (UMAT) candidate constraint*: If the unit memory access time (UMAT) candidate group is not selected, the corresponding UMAT decision variable should be zero. For each and

(1)

If core is utilized, i.e. at least one clock-domain is mapped onto core , only one UMAT value should be chosen from a UMAT candidate group. Therefore, For each ,

(1)

(1)

If core is not utilized, i.e. no clock-domain is mapped onto core , all *UMAT* candidate decision variable should be zero. Therefore, For each and

* *TDMA bus access schedulability constraint*: According to the schedulability analysis in Section TODO, the sum of reciprocal of UMAT should be less than one.

(1)

* *Worst-case memory access time variable constraint*: According to the definition of worst-case memory access time variable*,* For each ,

(1)

* *Worst-case instruction execution time variable constraint*: According to the definition of worst-case instruction executiontime variable*,* For each ,

(1)

* *Timing Requirement variable constraint*: According to the definition of timing requirement variable*,* For each ,

(1)

* *Real-time property constraint*: The timing requirement for each clock-domain should be obeyed after resource binding. Considering TDMA bus sharing for memory access, the worst-case memory access time for core should be multiplied by its unit memory access time (UMAT).Therefore, for each ,

(1)

Efficient formulation of the problem with MILP is not a trivial task.

The objective function of the proposed MILP formulation is to maximize the response time of a certain task while obeying all the constraints. The key variables in the formulation are the schedule times and execution times of all subtasks.

Consequently, the separate analysis of three factors does not guarantee the worst-case coverage. We need to consider all the factors in a single analysis framework. In this regard, we propose to use the MILP method because the complex interaction of the parameters, which are related to scheduling and contention modeling, can be expressed systematically in well-structured linear formulations. A state-of-the-art MILP solver facilitates the efficient computation of those formulations on the basis of sophisticated algorithms such as branch-and-bound, cutting-plane method, and so on [25].

Since the MILP solver basically explores the whole design space to find out an optimal solution, the time complexity is the critical problem for practical use. For the faster evaluation, we have to prune out nonsense solutions by adding problem specific constraints to MILP.

Although the time complexity of an MILP solver is inherently exponential, we observe that how to formulate the design constraints greatly affects the execution time of an ILP solver by orders of magnitude in time-complexity.

## Problem Formulation

# PERFORMANCE EVALUATION

First, we derive operating points for each of the benchmark’s five applications (consumer, auto, office, network, telecom) by performingdesign space exploration using an optimization frameworkwith the objectives of minimizing resource usage andpower consumption, and maximizing speedup (compared tothe operating point with highest latency).

most cases.

# CONCLUSIONS

In this article, ss design.

# TYPICAL REFERENCES IN NEW ACM REFERENCE FORMAT

thesis: [Anisi 2003], an online document / world wide web resource [Thornburg 2001], [Ablamowicz and Fauser 2007], [Poker-Edge.Com 2006], a video game (Case 1) [Obama 2008] and (Case 2) [Novak 2003] and [Lee 2005] and (Case 3) a patent Scientist 2009], work accepted for publication [Rous 2008], ‘YYYYb’-test for prolific author [Saeedi et al. 2010a] and [Saeedi et al. 2010b]. Other cites might contain ‘duplicate’ DOI and URLs (some SIAM articles) [Kirschmer and Voight 2010]. Boris / Barbara Beeton: multi-volume works as books [Hörmander 1985b] and [Hörmander 1985a].

APPENDIX

In this appendix, we measure the channel switching time of Micaz [CROSSBOW 2008] sensor devices. In our experiments, one mote alternatingly switches between Channels 11 and 12. Every time after the node switches to a channel, it sends out a packet immediately and then changes to a new channel as soon as the transmission is finished. e measure the number of packets the test mote can send in 10 seconds, denoted as 1. In contrast, we also measure the same value of the test mote without switching channels, denoted as N2. We calculate the channel-switching time s as



By repeating the experiments 100 times, we get the average channel-switching time of icaz motes: 24.3 *μ*s.

ELECTRONIC APPENDIX

The electronic appendix for this article can be accessed in the ACM Digital Library.

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