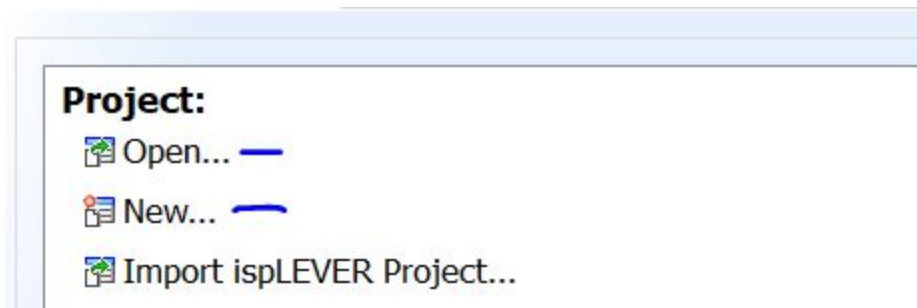
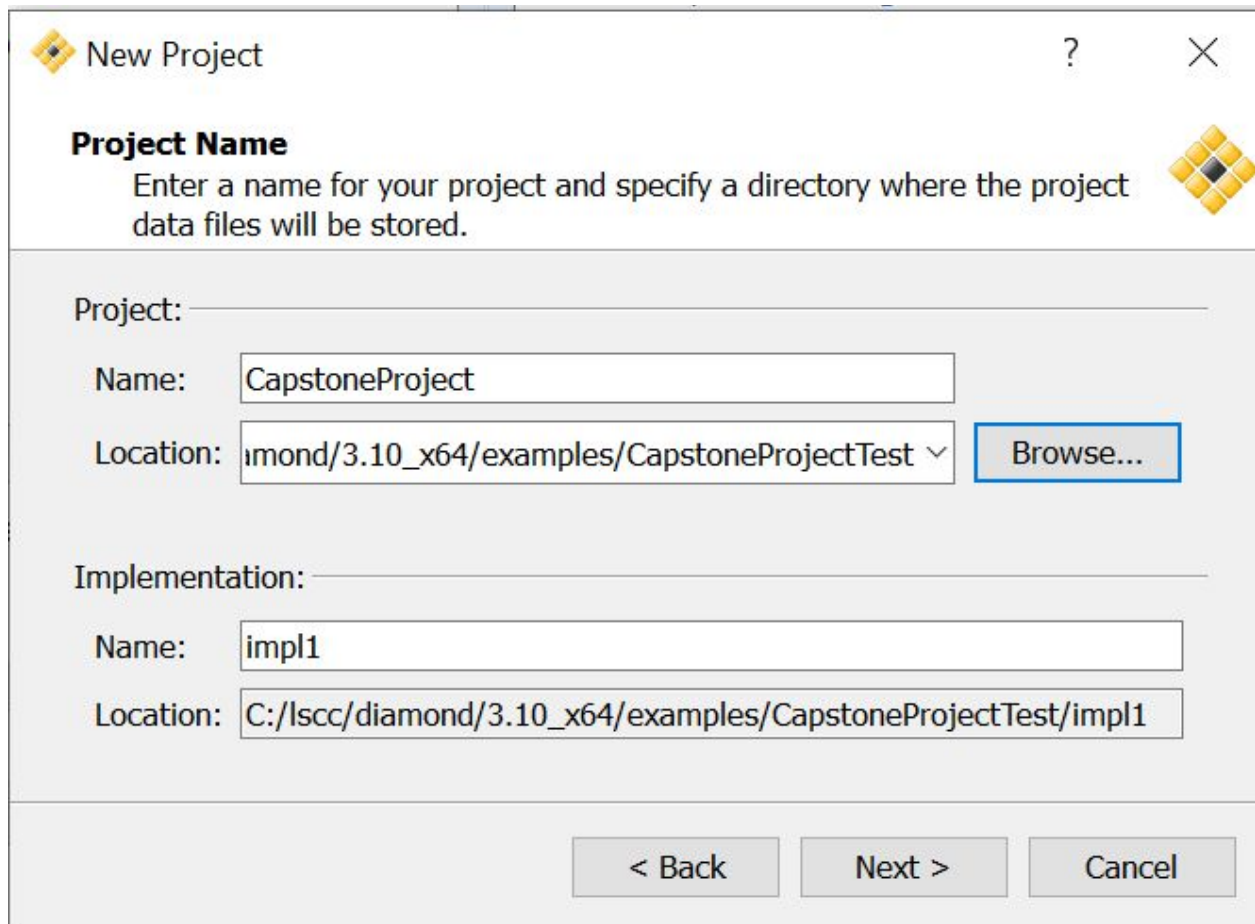


This is a guide to using the verilog code on Github with the Lattice IDE. Make sure to also have the other two .v files which contain the division module and DC PWM module.

Open or create a new project



If you open new, choose a new location for your project. Make sure it's different from previous implementations.

A screenshot of the 'New Project' dialog box in the Lattice IDE. The dialog has a title bar with the Lattice logo, 'New Project', and window controls. The main area is divided into sections. The 'Project Name' section has a description: 'Enter a name for your project and specify a directory where the project data files will be stored.' Below this, there are fields for 'Project:' (empty), 'Name:' (containing 'CapstoneProject'), and 'Location:' (containing 'iamond/3.10_x64/examples/CapstoneProjectTest' with a dropdown arrow). A 'Browse...' button is next to the location field. The 'Implementation:' section has fields for 'Name:' (containing 'impl1') and 'Location:' (containing 'C:/lsc/diamond/3.10_x64/examples/CapstoneProjectTest/impl1'). At the bottom, there are three buttons: '< Back', 'Next >', and 'Cancel'.

Then add your source files, these are the verilog files that you can add on if you downloaded them from GitHub, or from other example projects like the starter blink project.

Add Source

Add HDL, EDIF netlist, LPF constraints, or other files.



Source files:

Add Source... Remove Source

☒ Copy source to implementation directory

< Back Next > Cancel

The next page will ask you to input device information, the picture below shows the settings we needed for our project. The blue lines point to where I needed to change from original settings,

so make sure those are right at least.

Device Selector

Select Device:

Family:

- LatticeECP
- LatticeECP2
- LatticeXP
- LatticeXP2
- MachXO
- MachXO2
- MachXO3L
- MachXO3LF**
- Platform Manager

Device:

- LCMXO3LF-640E
- LCMXO3LF-1300C
- LCMXO3LF-1300E
- LCMXO3LF-2100C
- LCMXO3LF-2100E
- LCMXO3LF-4300C
- LCMXO3LF-4300E
- LCMXO3LF-6900C**

Performance grade:(_)

6

Package type:

CABGA256

Operating conditions:

Industrial

Part Names:

LCMXO3LF-6900C-6BG256I

Select ASC Device:

Part Names	Numbers
L-ASC10-1SG48I	0

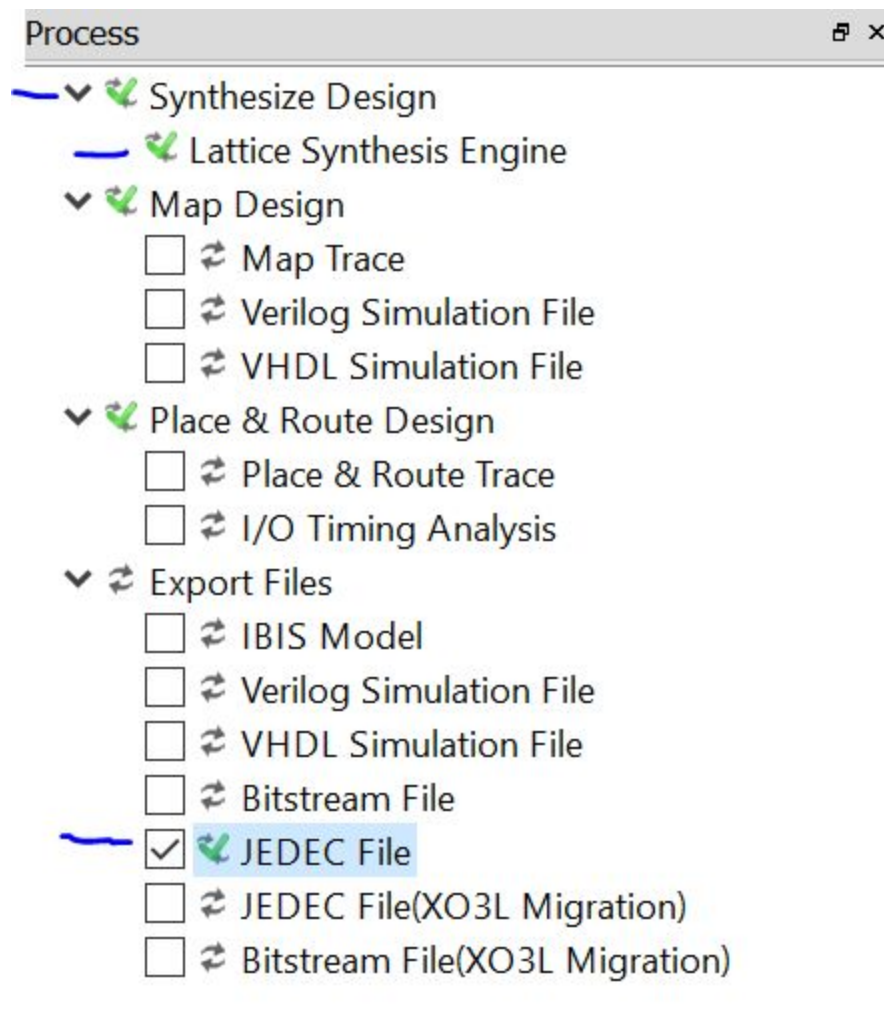
[Online Data Sheet for Device](#)

Device Information:

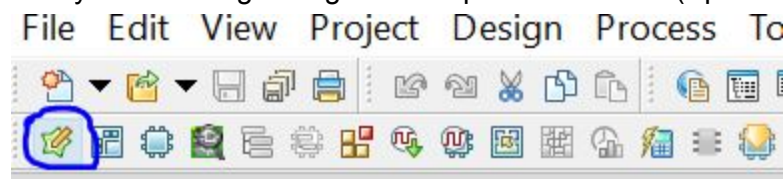
Voltage:	2.5V/3.3V
LUT:	6864
Registers:	6864
EBR Bits:	234K
EBR Blocks:	26
Dist RAM:	54912
DSP:	-
PLL:	2
DLL:	0
PCS:	-
APIO:	-
PIO Cells:	336
PIO Pins:	207
Max Programmable IOs:	206
VMON Pins:	0
IMON Pins:	0
TMON Pins:	0
Trim/Mar Pins:	0
HVOUT Pins:	0
GPIO:	0

That should be the last window. Next the files to use should be opened. So far I use the ProjectCodeVX.v , PWM_Signal_DC.v , ClockDivisionforPWM.v

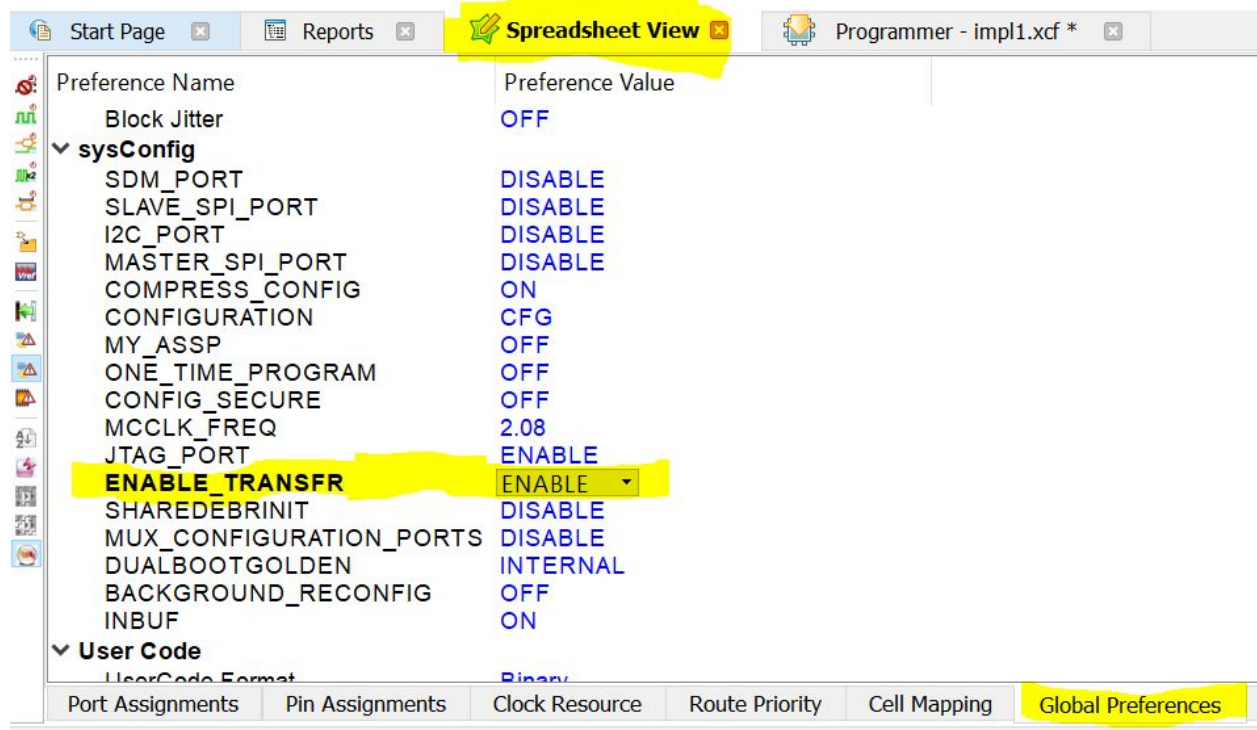
After making sure you have these under your files. Click process.



Now you can assign things in the Spreadsheet tab. (Spreadsheet is icon circled below)



After this, it should open a **Spreadsheet View** tab. The highlighted text below shows that you need to change enable transfer to TRUE.



Now you can change the pin assignments, its one of tabs along the bottom. Shown below.

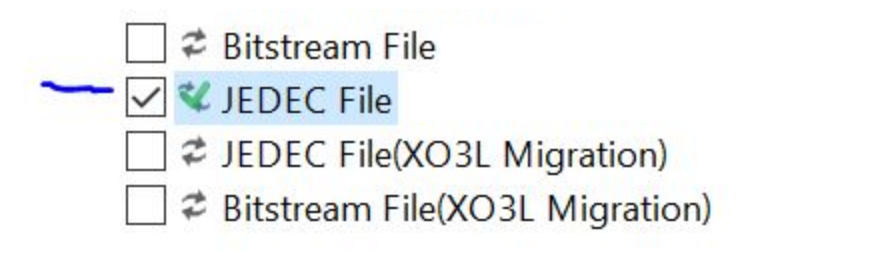
Pin	Pad Name	Dual Function	Polarity	BANK	VCC	IO TYPE	Signal Name	Signal Type
1	Bank0	N/A	N/A	N/A	N/A	N/A	N/A	N/A
1.1	A3	FIO:PT12A	P	Auto				
1.2	A4	FIO:PT10A	P	Auto				
1.3	A5	FIO:PT11A	L_GPLLT_MFGOUT1	P	Auto			
1.4	A6	FIO:PT14D	TDI/MD7	N	N/A	N/A	N/A	N/A
1.5	A7	FIO:PT17C	TCK/TEST_CLK	P	N/A	N/A	N/A	N/A
1.6	A8	FIO:PT18B	PCLKC0_1	N	Auto	(LVCMOS25)	(clk_x1)	(Clock)
1.7	A9	FIO:PT22C	SCL/IO2/MD2/ATB_SENSE/PCLKT0_0	P	Auto	(LVCMOS25)	(LED[6])	(Output)
1.8	A10	FIO:PT25B		N	Auto			
1.9	A11	FIO:PT28A		P	Auto			
1.10	A12	FIO:PT33B		N	Auto			
1.11	A13	FIO:PT36C	INITN	P	Auto			

Port Assignments | **Pin Assignments** | Clock Resource | Route Priority | Cell Mapping | Global Preferences | Timing Preferences | Group | Misc

Click on the signal name to correct pad name.

Now we need to click process again to make sure the spreadsheet view changes are added to the jedec file.

Click on the process icon again. Before you do, you'll notice the check mark isn't there anymore. This indicates changes has been made.



Lastly, make sure to check that the voltages are set to default in Port Assignments. I've never really had issues with it, but our Lattice Sponsor warned me about making sure the voltages are set to the default. Image below shows the highlighted area.

Start Page Reports Spreadsheet View Programmer - impl1.xcf *

	Name	Group Bv	Pin	BANK	BANK VCC	VRFF	IO TYPE
1	All Ports	N/A	N/A	N/A	N/A	N/A	
1.1	Input	N/A	N/A	N/A	N/A	N/A	
1.1.1	Clock	N/A	N/A	N/A	N/A	N/A	
1.1.1.1	DIPSW[0]	N/A	(E6)	(0)	N/A	N/A	LVC MOS25(LVC MOS25)
1.1.1.2	DIPSW[1]	N/A	(F7)	(0)	N/A	N/A	LVC MOS25(LVC MOS25)
1.1.1.3	DIPSW[2]	N/A	(E9)	(0)	N/A	N/A	LVC MOS25(LVC MOS25)
1.1.1.4	DIPSW[3]	N/A	(D9)	(0)	N/A	N/A	LVC MOS25(LVC MOS25)
1.1.1.5	clk_x1	N/A	(A8)	(0)	N/A	N/A	LVC MOS25(LVC MOS25)
1.1.2	IO_A4	N/A	(E8)	(0)	N/A	N/A	LVC MOS25(LVC MOS25)
1.1.3	rstn	N/A	(B1)	(5)	N/A	N/A	LVC MOS25(LVC MOS25)
1.2	Output	N/A	N/A	N/A	N/A	N/A	

Port Assignments Pin Assignments Clock Resource Route Priority Cell Mapping Global Preferences

Now we're ready to program. Click on the programmer. Icon is circled below.



This opens up the programmer. You might get a window asking you to create an implementation. It should have already been created when creating a new project. If it still comes up, just create it then and make sure it's under the same folder that was created for the

project.

Implementation: _____

Name:

Location:

Above shows an example of the file location made.

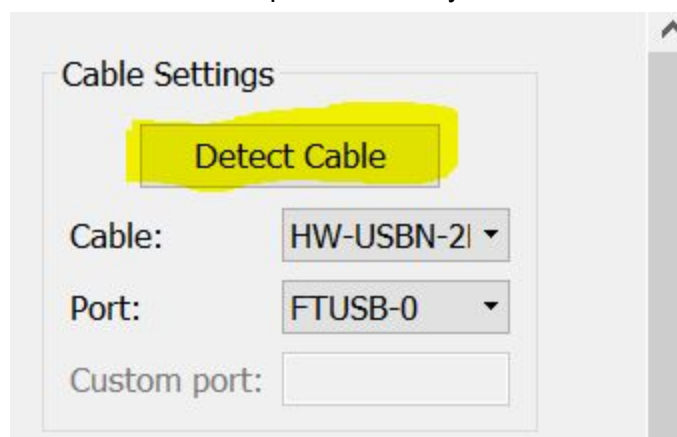
Now we need to make sure the programmer will program the right board. The image below highlights



Enable	Status	Device Vendor	Device Family	Device	Device Full Name	Desc	Operation	File Name
1	<input checked="" type="checkbox"/>	Lattice	MachXO3LF	LCMXO3LF-6900C	LCMXO3LF-6900C		FLASH Erase,Program,Verify	...st/impl1/CapstoneProjectTest_impl1.jed

The highlighted sections are essential to keep. You can technically change Operation to do different things to the FPGA. And changing File Name allows you to choose another implementation for example.

After those are set up. Make sure you can detect the cable.



Cable Settings

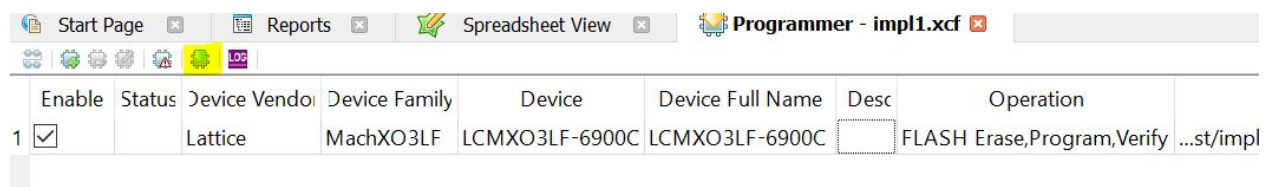
Detect Cable

Cable:

Port:

Custom port:

Should detect USB-0.



Enable	Status	Device Vendor	Device Family	Device	Device Full Name	Desc	Operation	
1	<input checked="" type="checkbox"/>	Lattice	MachXO3LF	LCMXO3LF-6900C	LCMXO3LF-6900C		FLASH Erase,Program,Verify	...st/impl

Highlighted button is the one to press for programming the board.
If the programming was successful, the output should be like below.

