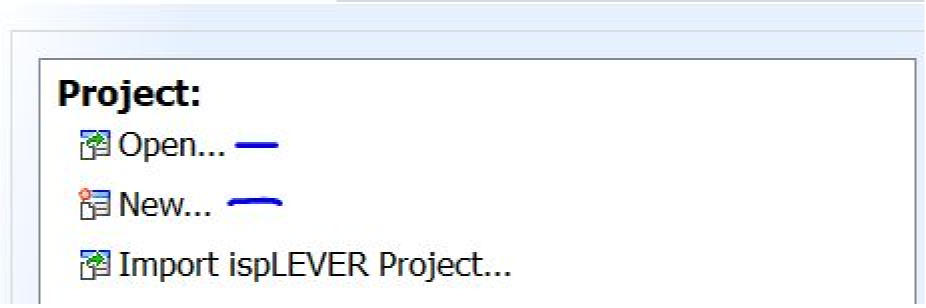
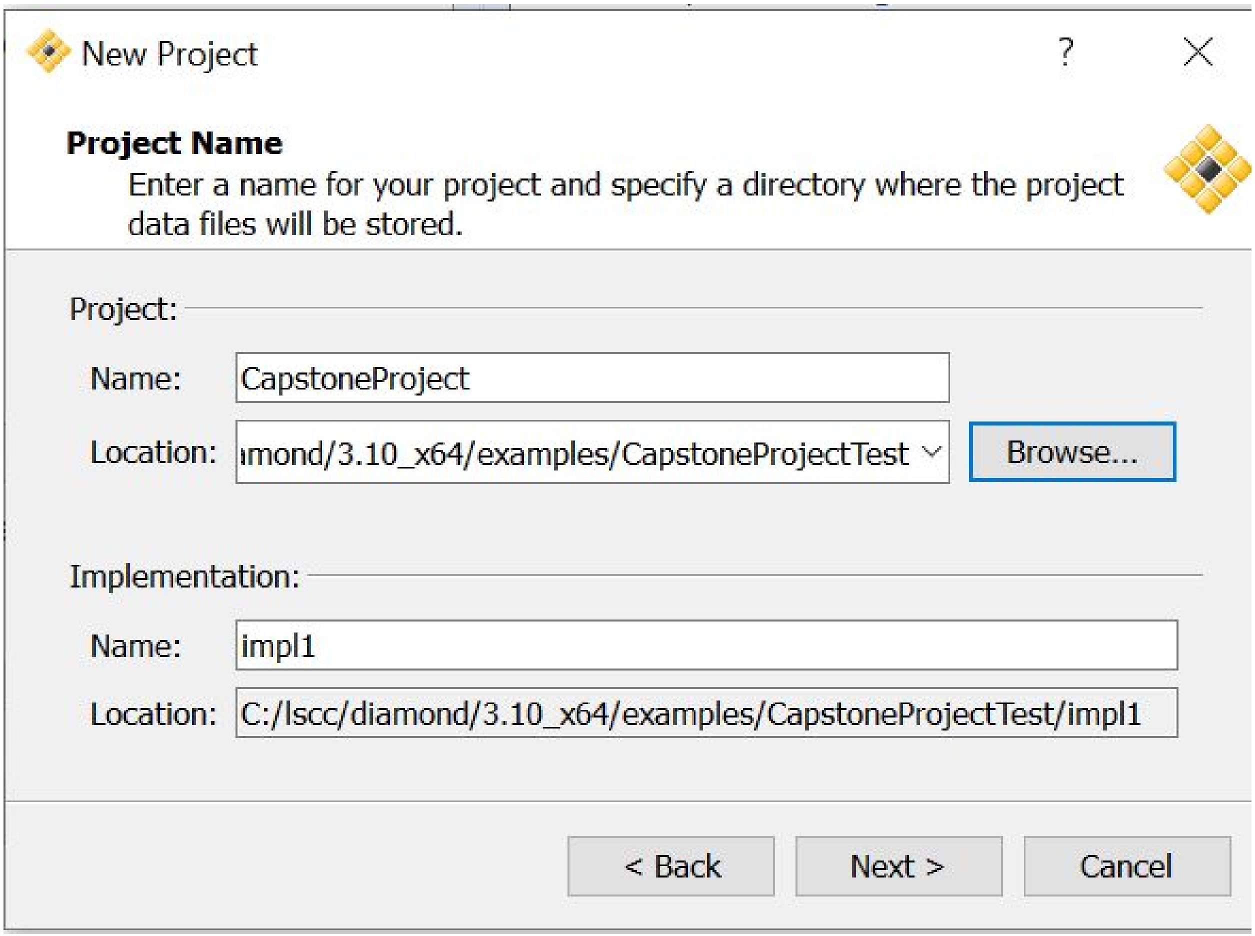
This is a guide to using the verilog code on Github with the Lattice IDE. Make sure to also have the other two .v files (heartbeat.v and kitcar.v) from the latticesemiconductor site. It's the simple blink project.
(https://www.latticesemi.com/en/Products/DevelopmentBoardsAndKits/MachXO3LFStarterKit)
Click on **MachXO3 Starter Kit User's Guide.** Go to page 6. Look at **Download Demo Designs** section.
Open or create a new project



If you open new, choose a new location for your project. Make sure it's different from previous implementations.

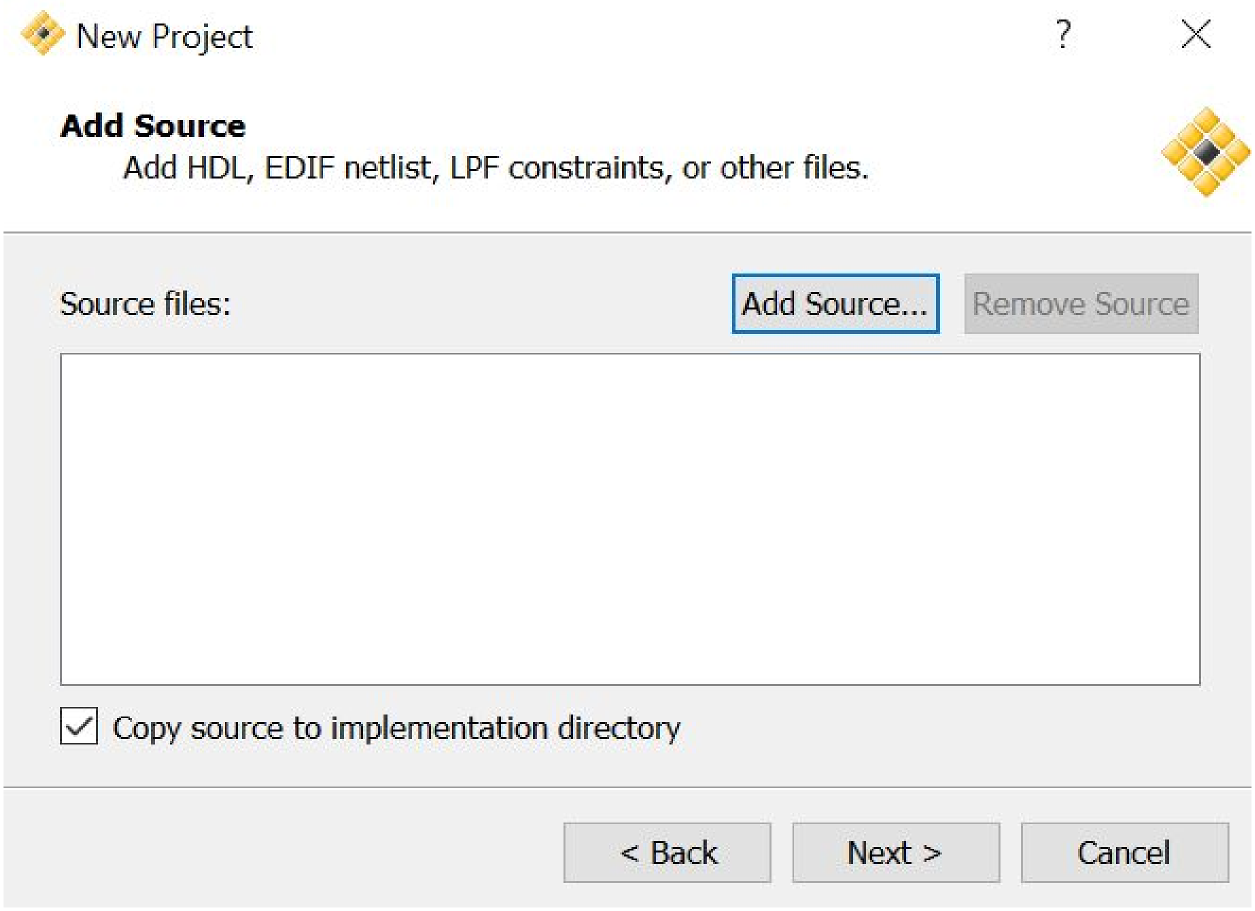


Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project:
Name: CapstoneProject
Location: ımond/3.10_x64/examples/CapstoneProjectTest

Implementation:
Name: impl1
Location: C:/lscc/diamond/3.10_x64/examples/CapstoneProjectTest/impl1

Then add your source files, these are the verilog files that you can add on if you downloaded them from GitHub, or from other example projects like the starter blink project.



New Project

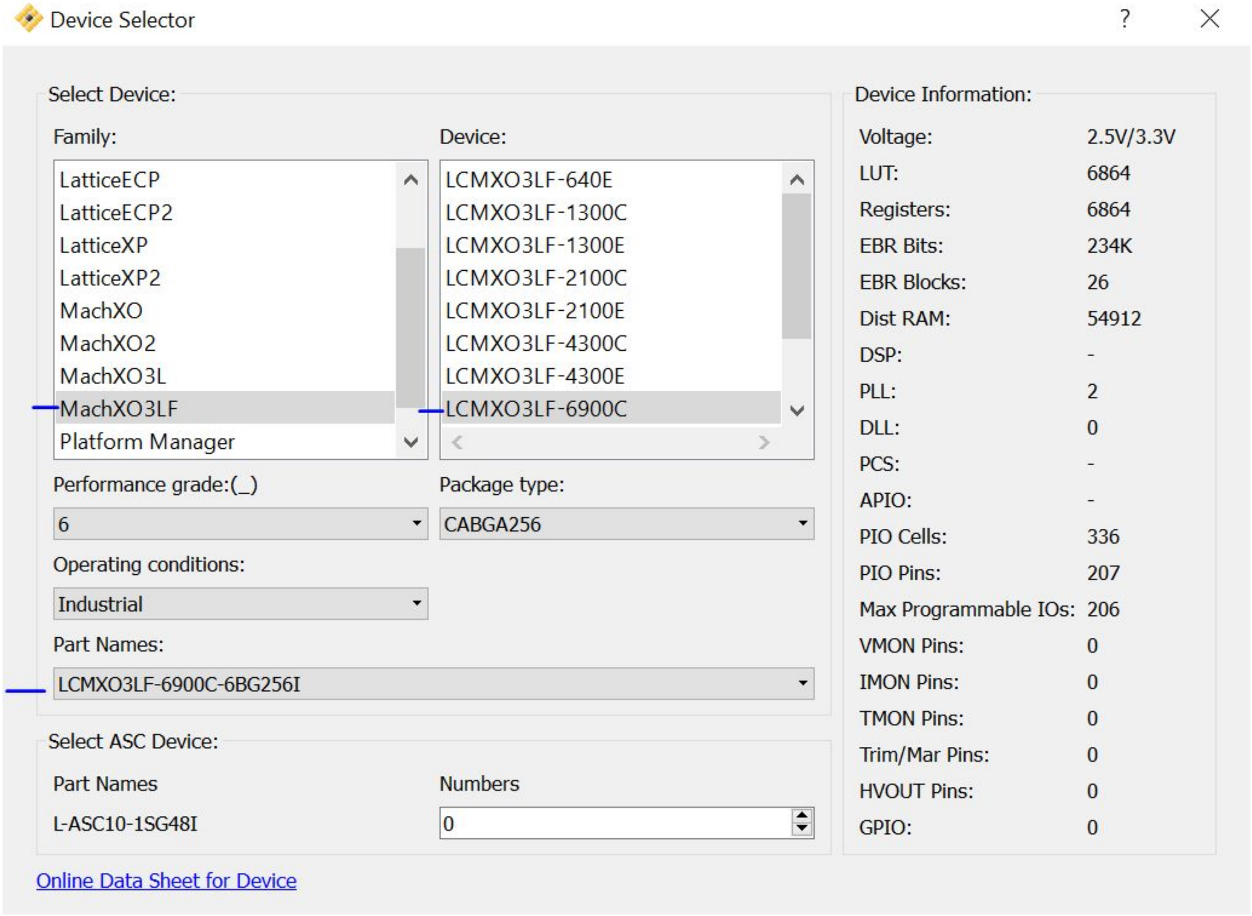
Add Source

Add HDL, EDIF netlist, LPF constraints, or other files.

Source files:

☑ Copy source to implementation directory

The next page will ask you to input device information, the picture below shows the settings we needed for our project. The blue lines point to where I needed to change from original settings, so make sure those are right at least.



Family: MachXO3LF

Device: LCMXO3LF-6900C

Performance grade:(_): 6

Package type: CABGA256

Operating conditions: Industrial

Part Names: LCMXO3LF-6900C-6BG256I

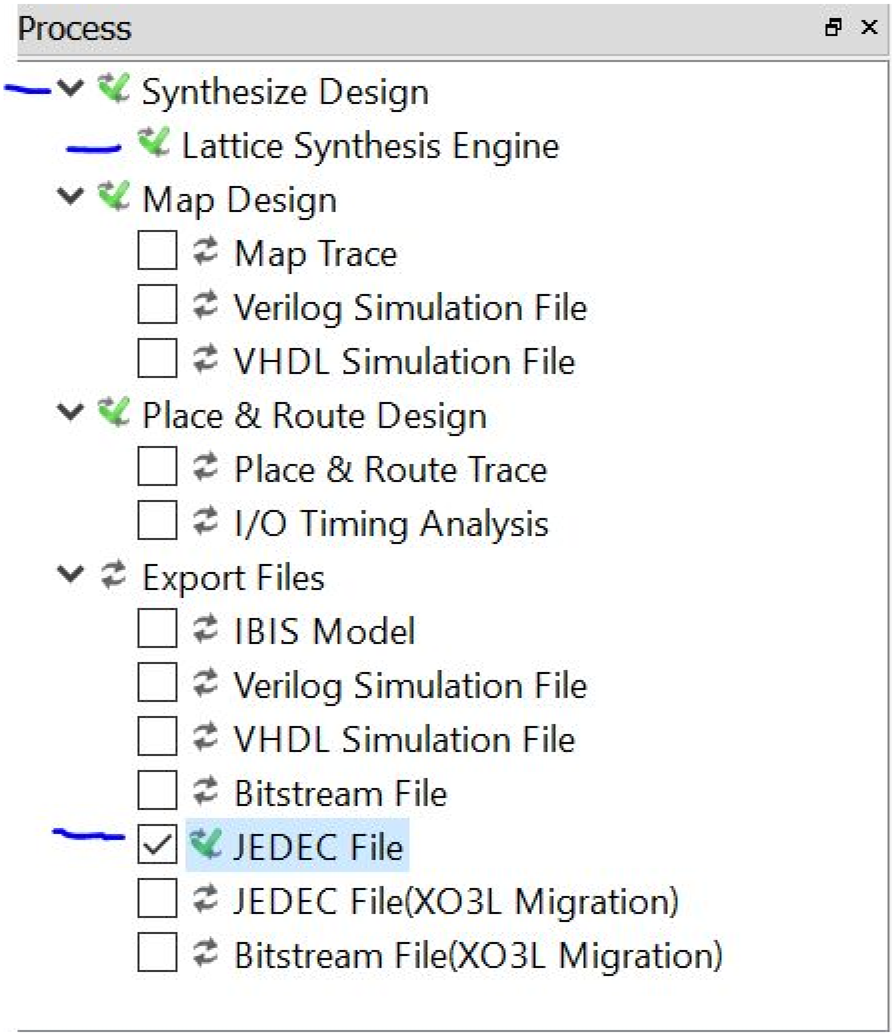
Part Names	Numbers
L-ASC10-1SG48I	0

Device Information:

Voltage:	2.5V/3.3V
LUT:	6864
Registers:	6864
EBR Bits:	234K
EBR Blocks:	26
Dist RAM:	54912
DSP:	-
PLL:	2
DLL:	0
PCS:	-
APIO:	-
PIO Cells:	336
PIO Pins:	207
Max Programmable IOs:	206
VMON Pins:	0
IMON Pins:	0
TMON Pins:	0
Trim/Mar Pins:	0
HVOUT Pins:	0
GPIO:	0

That should be the last window. Next the files to use should be opened. So far I use the ProjectCodeVX.v , heartbeat.v, and kitcar.v

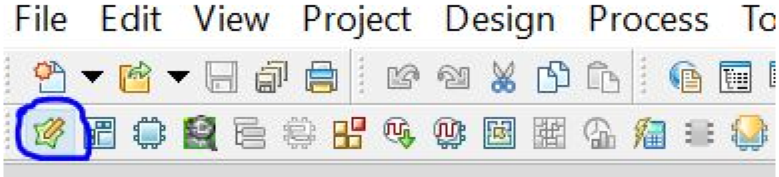
After making sure you have these under your files. Click process.



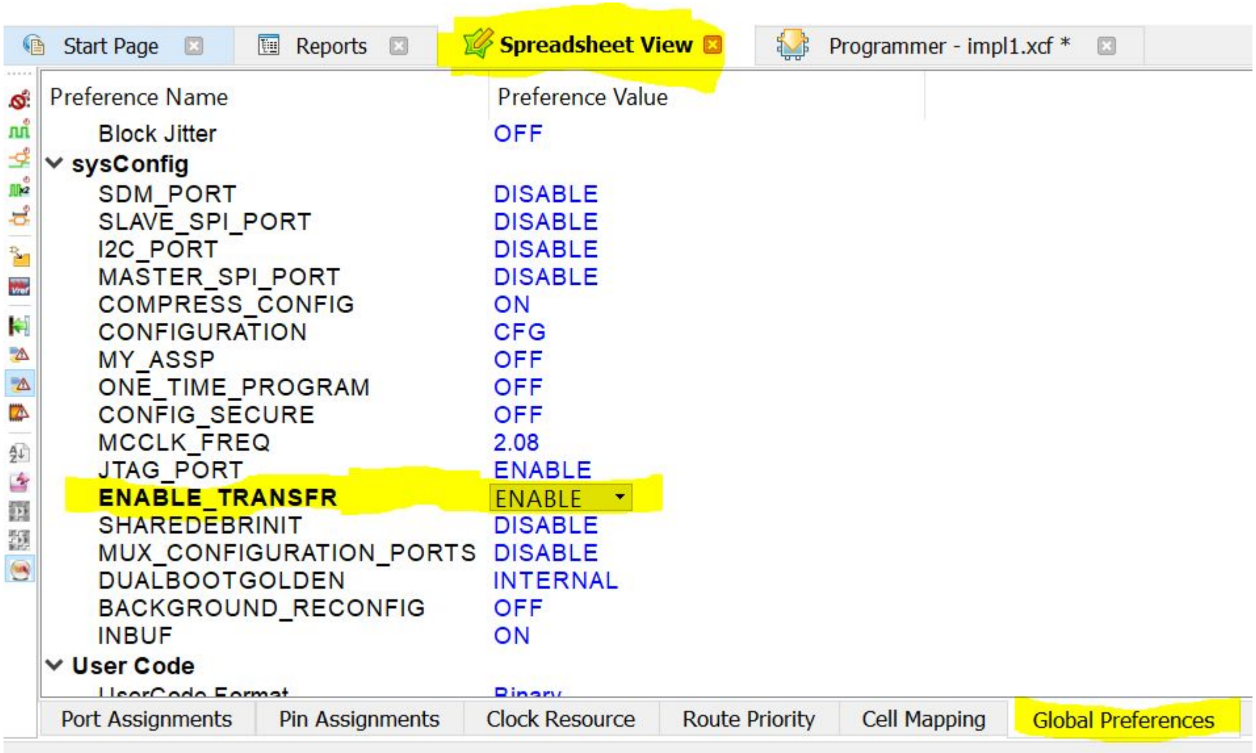
Process

- ✓ Synthesize Design
  - ✓ Lattice Synthesis Engine
- ✓ Map Design
  - □ Map Trace
  - □ Verilog Simulation File
  - □ VHDL Simulation File
- ✓ Place & Route Design
  - □ Place & Route Trace
  - □ I/O Timing Analysis
- Export Files
  - □ IBIS Model
  - □ Verilog Simulation File
  - □ VHDL Simulation File
  - □ Bitstream File
  - ☑ JEDEC File
  - □ JEDEC File(XO3L Migration)
  - □ Bitstream File(XO3L Migration)

Now you can assign things in the Spreadsheet tab. (Spreadsheet is icon circled below)

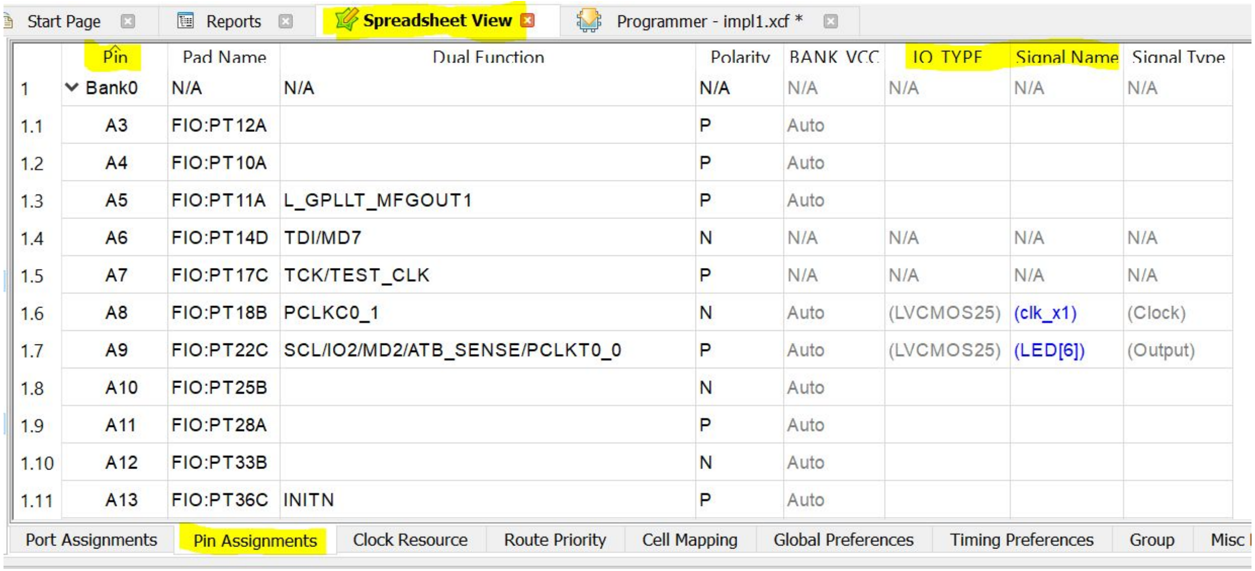


After this, it should open a **Spreadsheet View** tab.The highlighted text below shows that you need to change enable transfer to TRUE.



Preference Name	Preference Value
Block Jitter	OFF
sysConfig	
SDM_PORT	DISABLE
SLAVE_SPI_PORT	DISABLE
I2C_PORT	DISABLE
MASTER_SPI_PORT	DISABLE
COMPRESS_CONFIG	ON
CONFIGURATION	CFG
MY_ASSP	OFF
ONE_TIME_PROGRAM	OFF
CONFIG_SECURE	OFF
MCCLK_FREQ	2.08
JTAG_PORT	ENABLE
ENABLE_TRANSFR	ENABLE
SHAREDEBRINIT	DISABLE
MUX_CONFIGURATION_PORTS	DISABLE
DUALBOOTGOLDEN	INTERNAL
BACKGROUND_RECONFIG	OFF
INBUF	ON
User Code	
UserCode Format	Binary

Now you can change the pin assignments, its one of tabs along the bottom. Shown below.

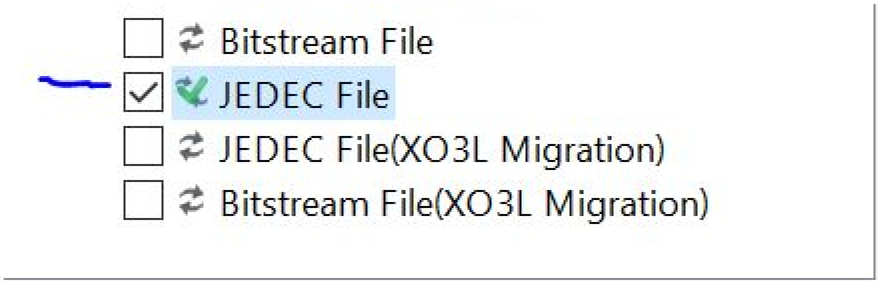


	Pin	Pad Name	Dual Function	Polarity	BANK VCC	IO TYPE	Signal Name	Signal Type
1	Bank0	N/A	N/A	N/A	N/A	N/A	N/A	N/A
1.1	A3	FIO:PT12A		P	Auto			
1.2	A4	FIO:PT10A		P	Auto			
1.3	A5	FIO:PT11A	L_GPLLT_MFGOUT1	P	Auto			
1.4	A6	FIO:PT14D	TDI/MD7	N	N/A	N/A	N/A	N/A
1.5	A7	FIO:PT17C	TCK/TEST_CLK	P	N/A	N/A	N/A	N/A
1.6	A8	FIO:PT18B	PCLKC0_1	N	Auto	(LVCMOS25)	(clk_x1)	(Clock)
1.7	A9	FIO:PT22C	SCL/IO2/MD2/ATB_SENSE/PCLKT0_0	P	Auto	(LVCMOS25)	(LED[6])	(Output)
1.8	A10	FIO:PT25B		N	Auto			
1.9	A11	FIO:PT28A		P	Auto			
1.10	A12	FIO:PT33B		N	Auto			
1.11	A13	FIO:PT36C	INITN	P	Auto			

Click on the signal name to correct pad name. Professor Greenwood says there's a script to do this faster. I haven't looked into it yet.

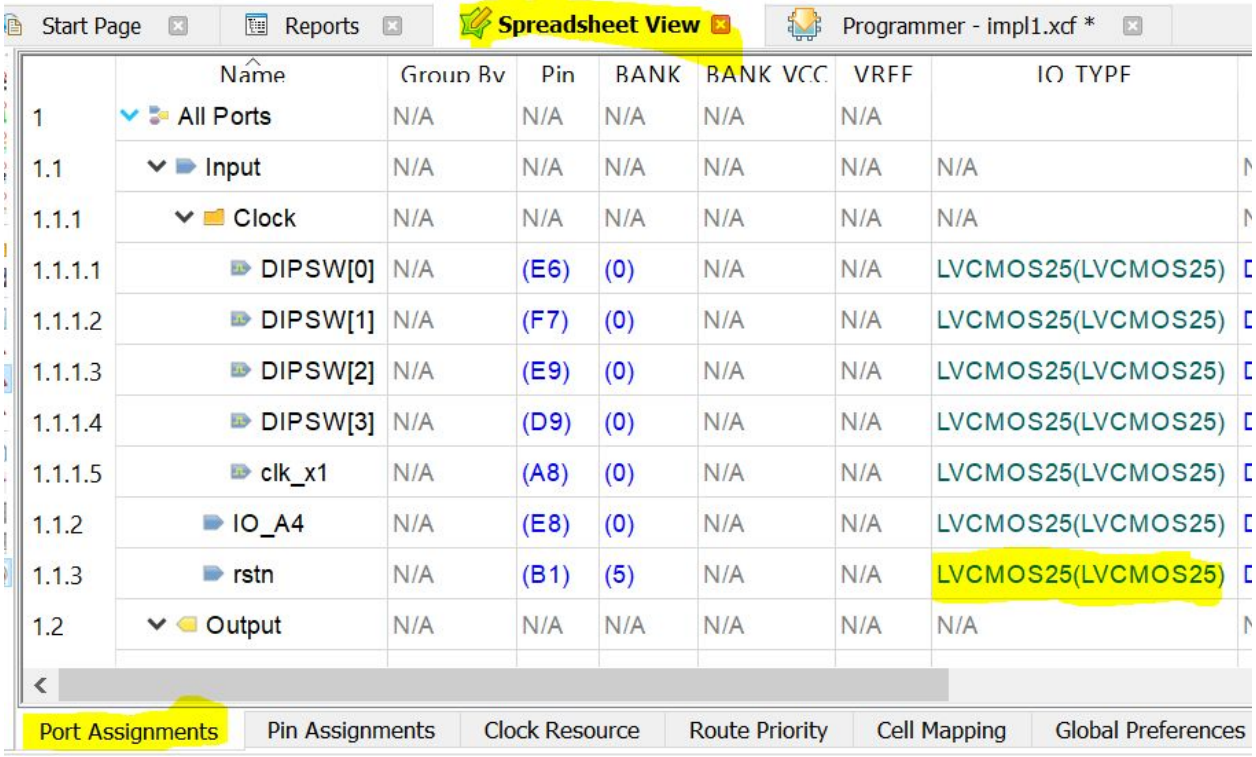
Now we need to click process again to make sure the spreadsheet view changes are added to the jedec file.

Click on the process icon again. Before you do, you'll notice the check mark isn't there anymore. This indicates changes has been made.



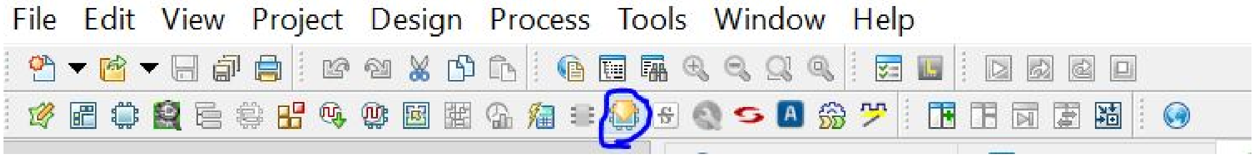
□ Bitstream File
☑ JEDEC File
□ JEDEC File(XO3L Migration)
□ Bitstream File(XO3L Migration)

Lastly, make sure to check that the voltages are set to default in Port Assignments. I've never really had issues with it, but Rahul warned me about making sure the voltages are set to the default. Image below shows the highlighted area.

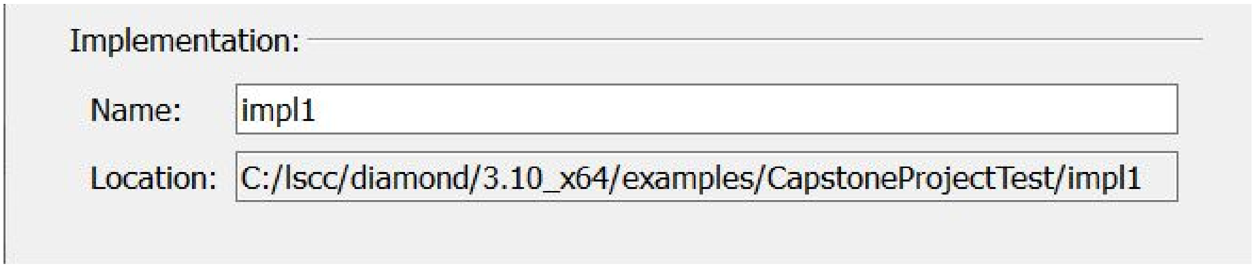


	Name	Group By	Pin	BANK	BANK VCC	VREF	IO TYPE	
1	All Ports	N/A	N/A	N/A	N/A	N/A		
1.1	Input	N/A	N/A	N/A	N/A	N/A	N/A	N
1.1.1	Clock	N/A	N/A	N/A	N/A	N/A	N/A	N
1.1.1.1	DIPSW[0]	N/A	(E6)	(0)	N/A	N/A	LVCMOS25(LVCMOS25)	D
1.1.1.2	DIPSW[1]	N/A	(F7)	(0)	N/A	N/A	LVCMOS25(LVCMOS25)	D
1.1.1.3	DIPSW[2]	N/A	(E9)	(0)	N/A	N/A	LVCMOS25(LVCMOS25)	D
1.1.1.4	DIPSW[3]	N/A	(D9)	(0)	N/A	N/A	LVCMOS25(LVCMOS25)	D
1.1.1.5	clk_x1	N/A	(A8)	(0)	N/A	N/A	LVCMOS25(LVCMOS25)	D
1.1.2	IO_A4	N/A	(E8)	(0)	N/A	N/A	LVCMOS25(LVCMOS25)	D
1.1.3	rstn	N/A	(B1)	(5)	N/A	N/A	LVCMOS25(LVCMOS25)	D
1.2	Output	N/A	N/A	N/A	N/A	N/A	N/A	N

Now we're ready to program. Click on the programmer. Icon is circled below.



This opens up the programmer. You might get a window asking you to create an implementation. It should have already been created when creating a new project. If it still comes up, just create it then and make sure it's under the same folder that was created for the project.



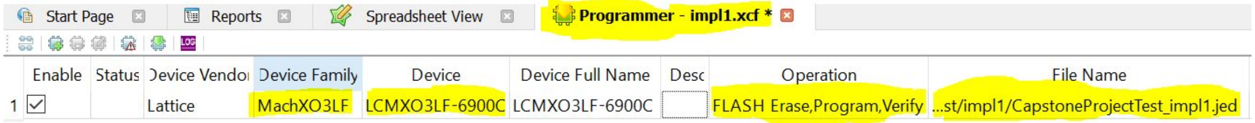
Implementation:

Name: impl1

Location: C:/lscc/diamond/3.10_x64/examples/CapstoneProjectTest/impl1

In my case, above shows an example of the file location I mean.

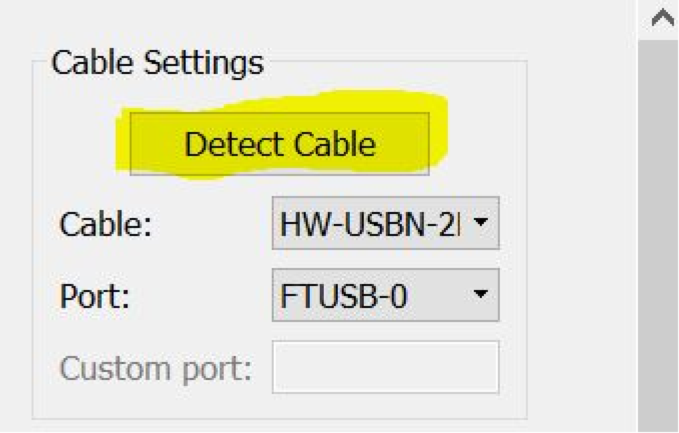
Now we need to make sure the programmer will program the right board. The image below highlights



	Enable	Status	Device Vendoi	Device Family	Device	Device Full Name	Desc	Operation	File Name
1	☑		Lattice	MachXO3LF	LCMXO3LF-6900C	LCMXO3LF-6900C		FLASH Erase,Program,Verify	...st/impl1/CapstoneProjectTest_impl1.jed

The highlighted sections are essential to keep. You can technically change Operation to do different things to the FPGA. And changing File Name allows you to choose another implementation for example. Or a bitstream. But we're not using bitstreams.

After those are set up. Make sure you can detect the cable.



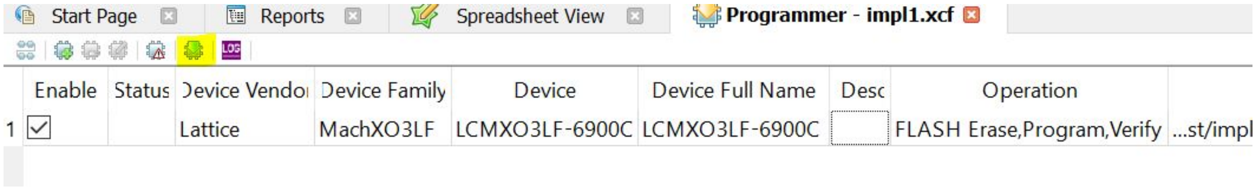
Cable: HW-USBN-2I

Port: FTUSB-0

Custom port:

Should detect USB-0.

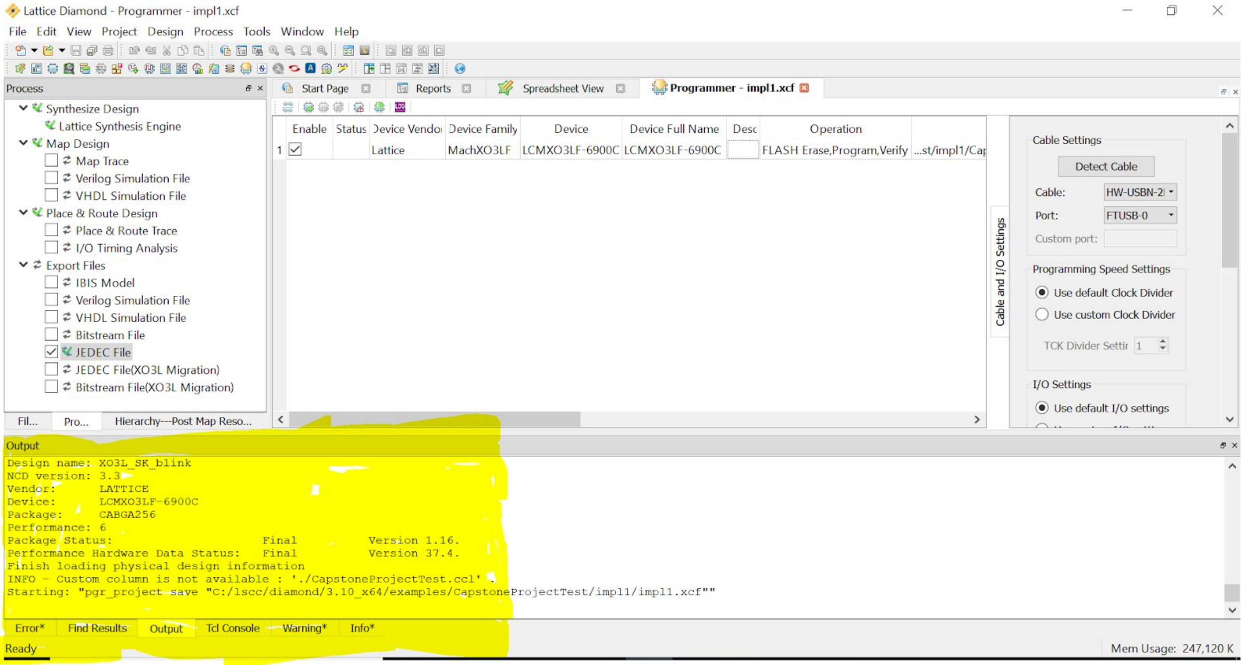
Last thing to do is to program the board. Cross your fingers here. Absolutely make sure to have the Lattice Cable connected to the USB Hub and avoid unplugging/plugging the board to the USB hub. The only thing that should be disconnected is the USB hub from your laptop if necessary. Avoid at all costs unplugging the cable from your laptop while programming the board. Make sure to not reprogram the board too often. (~5mins?) We still don't know why the boards are dying yet, so it’s just a precaution.



	Enable	Status	Device Vendo	Device Family	Device	Device Full Name	Desc	Operation	
1	☑		Lattice	MachXO3LF	LCMXO3LF-6900C	LCMXO3LF-6900C		FLASH Erase,Program,Verify	...st/impl

Highlighted button is the one to press for programming the board.

If the programming was successful, the output should be like below.



	Enable	Status	Device Vendo	Device Family	Device	Device Full Name	Desc	Operation	
1	☑		Lattice	MachXO3LF	LCMXO3LF-6900C	LCMXO3LF-6900C		FLASH Erase,Program,Verify	...st/impl1/Ca

Cable Settings

Cable: HW-USBN-2

Port: FTUSB-0

Custom port:

Programming Speed Settings

● Use default Clock Divider

○ Use custom Clock Divider

TCK Divider Settir 1

I/O Settings

● Use default I/O settings

Output

```
Design name: XO3L_SK_blink
NCD version: 3.3
Vendor:      LATTICE
Device:      LCMXO3LF-6900C
Package:     CABGA256
Performance: 6
Package Status:                     Final          Version 1.16.
Performance Hardware Data Status:   Final          Version 37.4.
Finish loading physical design information
INFO - Custom column is not available : './CapstoneProjectTest.ccl' .
Starting: "pgr_project save "C:/lscc/diamond/3.10_x64/examples/CapstoneProjectTest/impl1/impl1.xcf""
```

Ready

Mem Usage: 247,120 K