

# INTRODUCTION AND LOGISTICS

Mahdi Nazm Bojnordi

Assistant Professor

School of Computing

University of Utah

# Overview

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- This lecture
  - Instructor
  - Teaching assistants
  - Course resources and requirements
  - Academic integrity
  - Computer architecture
  - Trends and challenges

# Instructor

- Mahdi Nazm Bojnordi
  - ▣ Assistant Professor of School of Computing
  - ▣ PhD degree in Electrical Engineering
  - ▣ Personal webpage: <http://www.cs.utah.edu/~bojnordi/>
- Research in Computer Architecture
  - ▣ Novel Memory Technologies
  - ▣ Energy-Efficient Hardware Accelerators
  - ▣ Research Lab. (MEB 3383)
    - Open positions are available!
- Office Hours (MEB 3418)
  - ▣ Please email me for an appointment
- Class webpage: <http://www.cs.utah.edu/~bojnordi/classes/6810/f18/>

# Webpage

## □ Please visit online

### CS/ECE 6810: Computer Architecture

#### Course Information

- ☛ Time: Mon/Wed 11:50AM - 01:10PM
- ☛ Location: CSC 205
- ☛ Instructor: Mahdi Nazm Bojnordi, email: lastname@cs.utah.edu, office hours: email me for appointment, MEB 3418
- ☛ Teaching Assistants: Payman Behnam, email: paymanbehnam@gmail.com, office hours: Tue 12:00 - 02:00PM, MEB 3115 (TA Lab.); Krunal Jain, email: krunal@cs.utah.edu, office hours: Thu 11:30AM - 01:30PM, MEB 3115 (TA Lab.)
- ☛ Pre-Requisite: CS 3810 or equivalent
- ☛ Textbook: Computer Architecture A Quantitative Approach - 5th Edition, John Hennessy and David Patterson
- ☛ Canvas is the main venue for class announcements, homework assignments, and discussions.

#### Important Policies

Please refer to the [College of Engineering Guidelines](#) for disabilities, add, drop, appeals, etc. Notice that we have zero tolerance for cheating; as a result, please read the [Policy Statement on Academic Misconduct](#), carefully. Also, you should be aware of the [SoC Policies and Guidelines](#).

Class rosters are provided to the instructor with the student's legal name as well as "Preferred first name" (if previously entered by you in the Student Profile section of your CIS account). While CIS refers to this as merely a preference, I will honor you by referring to you with the name and pronoun that feels best for you in class, on papers, exams, group projects, etc. Please advise me of any name or pronoun changes (and please update CIS) so I can help create a learning environment in which you, your name, and your pronoun will be respected.

#### Grading

The following items will be considered for evaluating the performance of students.

	Fraction	Notes
Homework Assignments	30%	as scheduled below
Midterm Exam	30%	11:50AM - 01:00PM, Mon., October 15th
Final Exam	40%	10:30AM - 12:30PM, Thu., December 13th

#### Homework Assignments

Homework assignments will be released on Canvas; all submissions must be made through Canvas. Only those submissions made before midnight will be accepted. Any late submission will be considered as no submission.

	Release Date	Submission Deadline
Homework 1	Sep. 05th	Sep. 12th
Homework 2	Sep. 26st	Oct. 03rd
Homework 3	Oct. 31st	Nov. 07th
Homework 4	Nov. 28th	Dec. 05th

#### Class Schedule (subject to change)

The following is a tentative class schedule that may be updated on a week-by-week basis during the course semester.

# Teaching Assistants

□ Payman Behnam

■ Email: [paymanbehnam@gmail.com](mailto:paymanbehnam@gmail.com)

■ Office Hours: TBD

■ MEB 3115 (TA Lab.)



□ Krunal Jain

■ Email: [krunal@cs.utah.edu](mailto:krunal@cs.utah.edu)

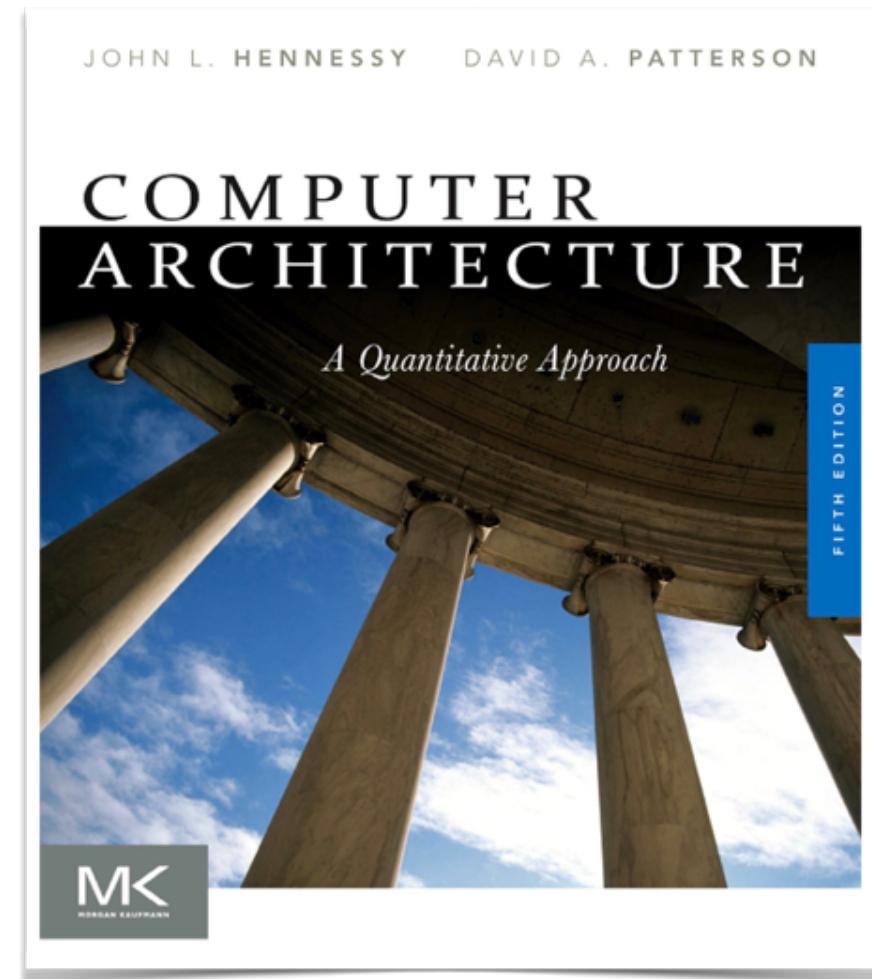
■ Office Hours: TBD

■ MEB 3115 (TA Lab.)



# Resources and Requirements

- Textbook: Computer Architecture A Quantitative Approach - 5th Edition, John Hennessy and David Patterson
- Pre-requisite: CS/ECE 3810 or equivalent



# Course Expectation

- We use Canvas for homework submissions, grades, and homework announcements.
- Grading

	Fraction	Notes
Assignments	30%	homework assignments
Midterm Exam	30%	Monday, October 15th
Final Exam	40%	Thursday, December 13th
Class Participation	--%	Questions and answers in class

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# Academic Integrity

- Do NOT cheat!!
  - ▣ Please read the Policy Statement on Academic Misconduct, carefully.
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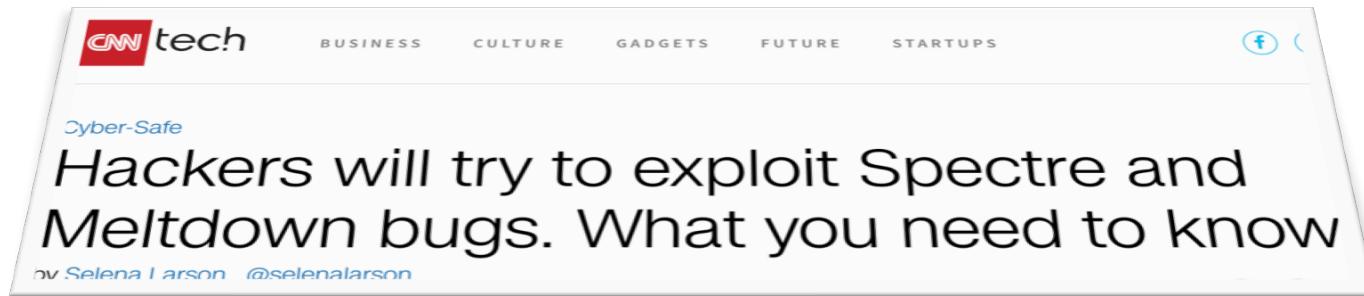
# Why CS/ECE 6810?

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- Need another qualifier/graduation requirement?
- You plan to become a Computer Architect?
- Understand what is inside a modern processor?
- Want to use the knowledge from this course in your own field of study?
- Understand the technology trends and recent developments for future computing?
- ...

# Why CS/ECE 6810?

- Better understanding of today's computing problems
- Security flaw: Spectre and Meltdown



- How to fix?

**Warning: Microsoft's Meltdown and Spectre patch is bricking some AMD PCs**



By [Mark Wycislik-Wilson](#)

| Published 6 hours ago

| [Follow @MarkWilsonWords](#)

# Estimated Class Schedule

- Processor Core
  - ▣ Introduction and Performance Metrics
  - ▣ Instruction Set Architecture and Pipelining
  - ▣ Instruction-Level Parallelism
  - ▣ Compiler Optimization
  - ▣ Dynamic Instruction Scheduling
- Memory System
  - ▣ Cache Architecture
  - ▣ Virtual Memory
  - ▣ Main Memory and DRAM
  - ▣ Data Parallel Processors

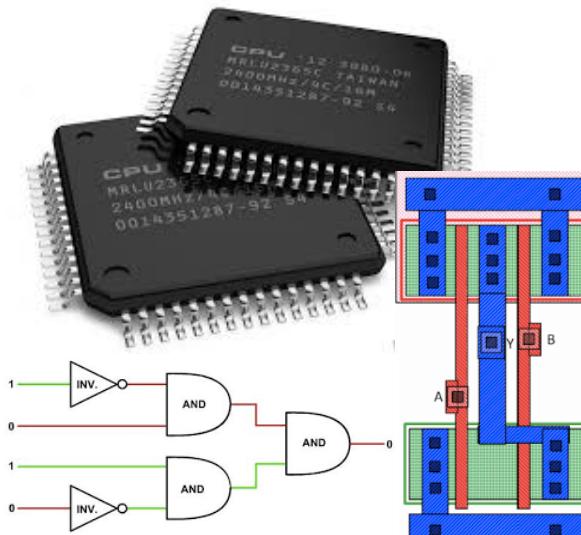
# What is Computer Architecture?

- Computer systems are everywhere ...



# What is Computer Architecture?

- What is inside modern processors ...



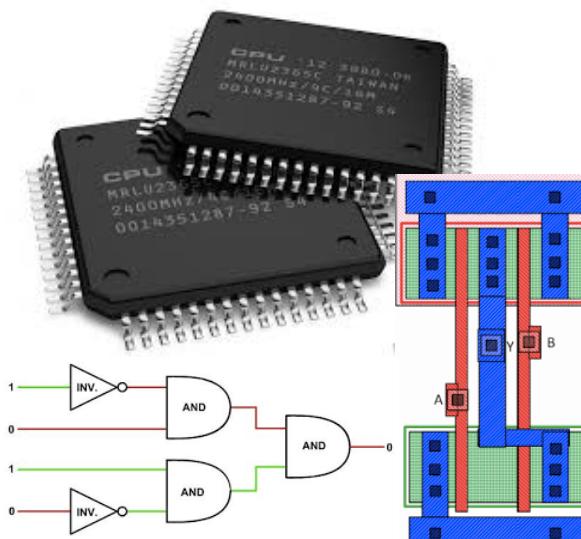
VLSI Circuits  
Hardware Implementation



Software Applications  
OS and Compiler

# What is Computer Architecture?

- Computer architecture is the glue between software and VLSI implementation



VLSI Circuits  
Hardware Implementation

ISA,  
μarchitecture  
, system  
Architecture



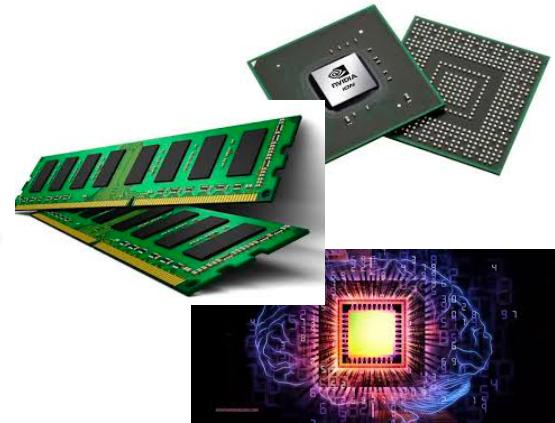
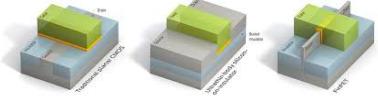
Software Applications  
OS and Compiler

# What is Computer Architecture?

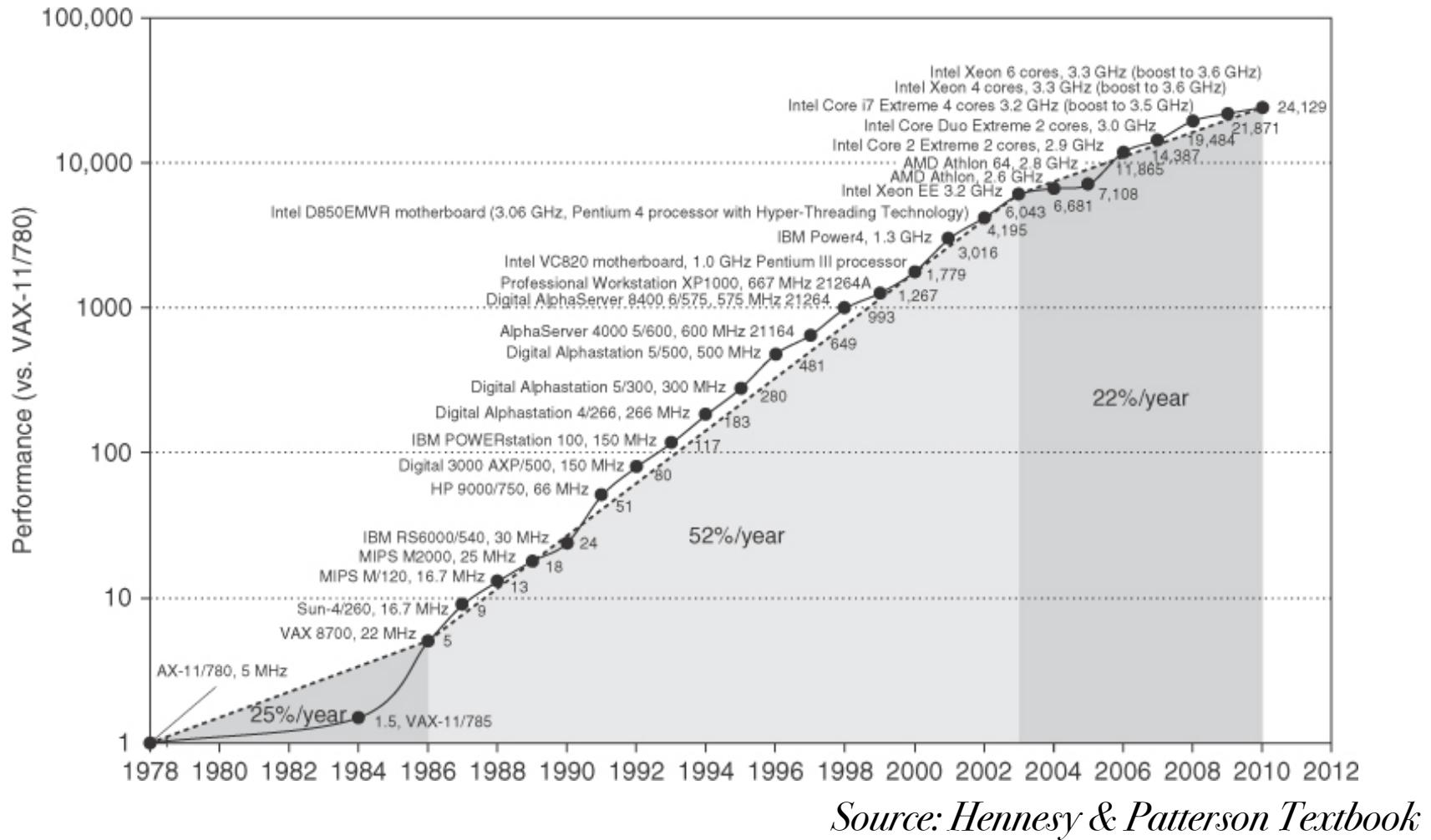
## □ Architects



## □ Computer Architects



# Growth in Processor Performance



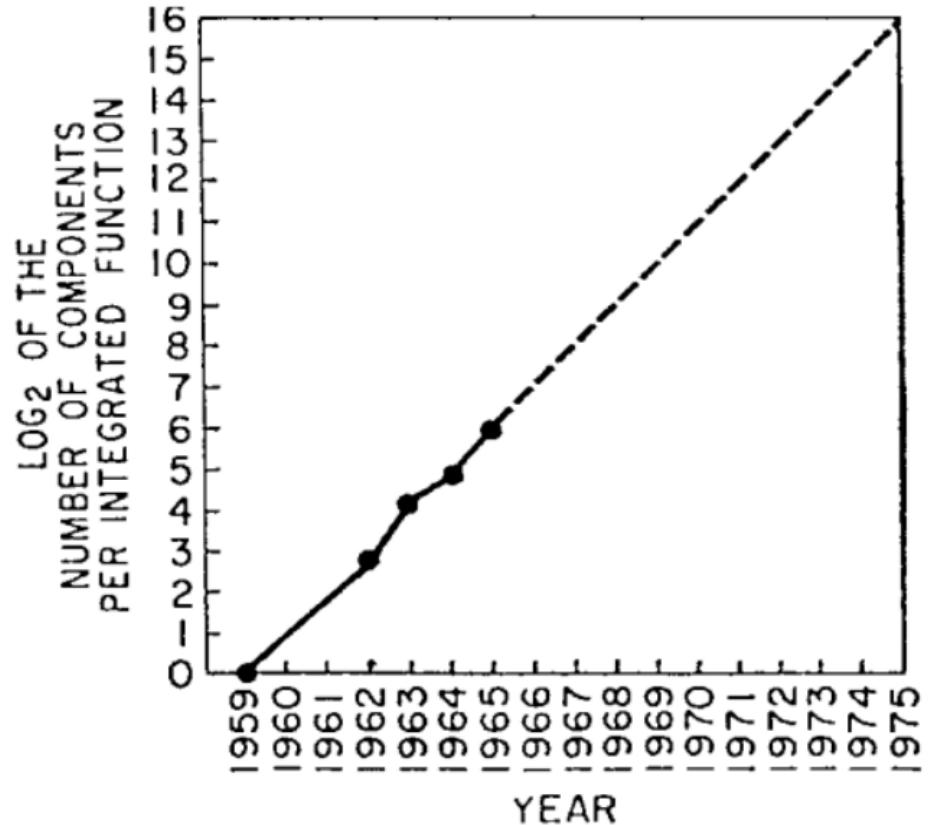
# Growth in Processor Performance

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- Main sources of the performance improvement
  - ▣ Enhanced underlying technology (semiconductor)
    - Faster and smaller transistors (Moore's Law)
  - ▣ Improvements in computer architecture
    - How to better utilize the additional resources to gain more power savings, functionalities, and processing speed.

# Moore's Law

- Moore's Law (1965)
  - Transistor count doubles every year
- Moore's Law (1975)
  - Transistor count doubles every two years



*Source: G.E. Moore, "Cramming more components onto integrated circuits," 1965*

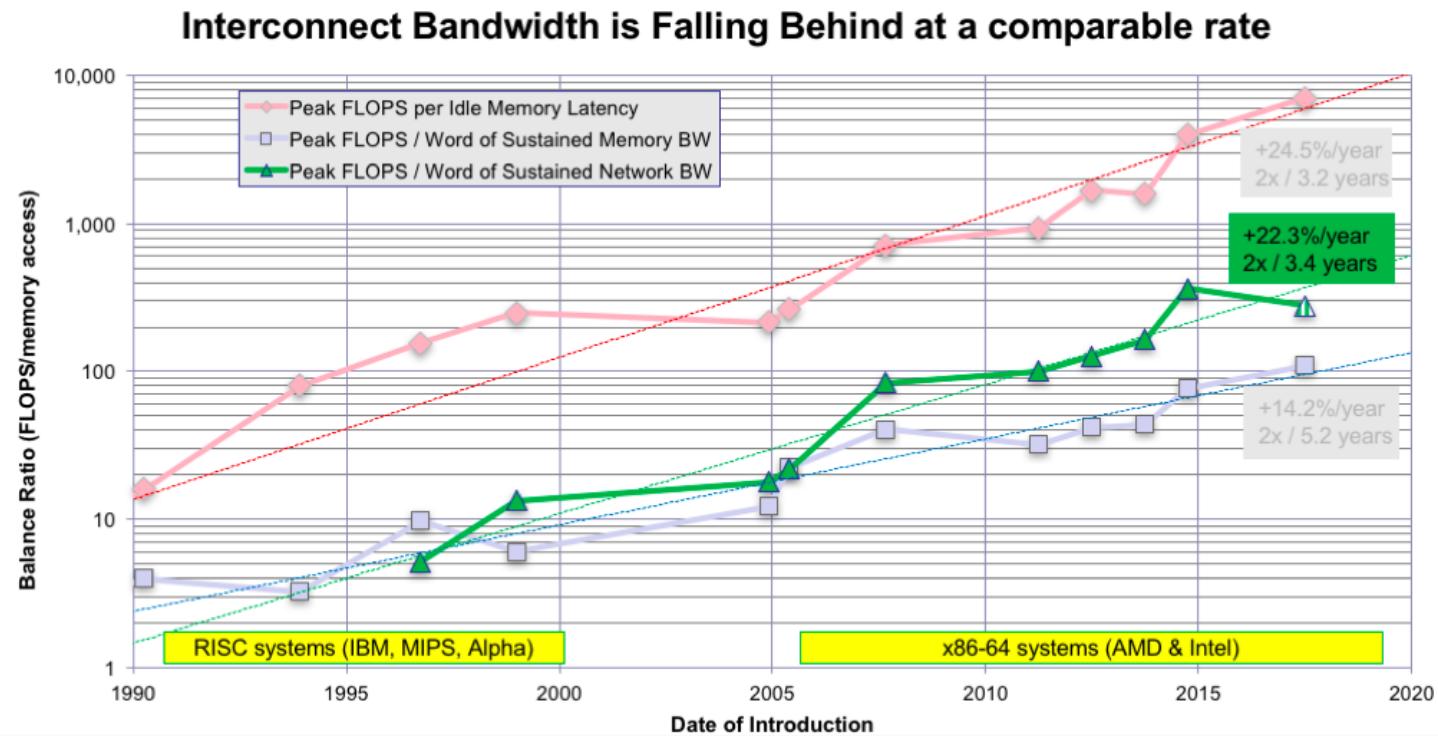
# What are New Challenges?

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- Resources (transistors) on a processor chip?
  - ▣ Not really, billions of transistors on a single chip.
- Can we use all of the transistors?
  - ▣ Due to **energy-efficiency** limitations, only a fraction of the transistor can be turned on at the same time!
- Who is affected?
  - ▣ Server computers by the peak power
  - ▣ Mobile and wearables due to energy-efficiency

# What are New Challenges?

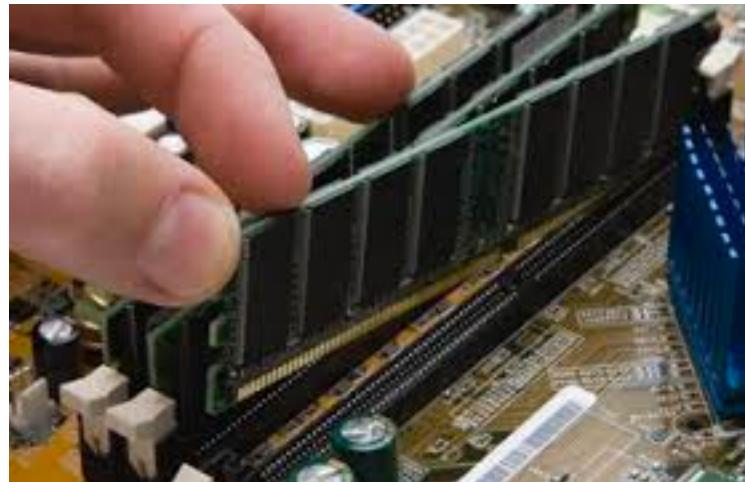
- Bandwidth optimization becomes a primary goal for memory design (**Bandwidth Wall!**)



# What are New Challenges?

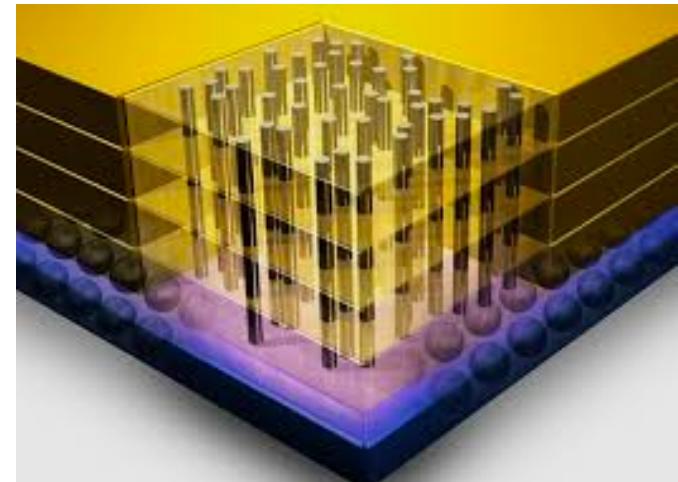
- Can in-package memory solve the problem?

**Off-chip Memory**



Lower Bandwidth  
Lower Costs

**3D Stacked Memory**



Higher Bandwidth  
Higher Costs

# What are New Challenges?

- Protecting data against side channel attacks is a serious need
- Performance in the past 40 years increased
  - ▣ hardware speculation to exploit more **instruction level parallelism**
  - ▣ shared memories to facilitate **thread-level parallelism**
- What about security?
  - ▣ <https://meltdownattack.com/>

