Homework Assignment

CS/ECE 7810: Advanced Computer Architecture

Due date: March 8, 2017

1. **(20 points) Way prediction [1].** Using examples, explain how way prediction and selective direct-mapping work. What are the differences between the two techniques?

2. **(20 points) Gated Vdd [2].** Explain the stacking effect in CMOS circuits. How does it impact the leakage power?

3. **(20 points) Smart refresh [3].** Explain the problem of updating down-counters in the smart refresh technique. How is the problem addressed in the smart refresh technique?

4. **(20 points) Time based data transfer [4].** Explain how a cache block is affected by errors in the DESC interface. How the problem is addressed in the paper?

5. **(20 points) DRAM address mapping [5].** Using an example, explain why the mapping function of a memory interleaving scheme must satisfy the one-to-one property. How is this property guaranteed in the permutation-based page interleaving scheme?

References

[1] Powell et al, "Reducing Set-Associative Cache Energy via Way-Prediction and Selective Direct-Mapping," MICRO, 2001

[2] Powell et al, "Gated-Vdd: A Circuit Technique to Reduce Leakage in Deep-Submicron Cache Memories," ISLPED, 2000

[3] Ghosh et al "Smart Refresh: An Enhanced Memory Controller Design for Reducing Energy in Conventional and 3D Die-Stacked DRAMs," MICRO, 2007

[4] Bojnordi et al, "DESC: Energy-Efficient Data Exchange using Synchronized Counters," MICRO, 2013

[5] Zhang et al, "A Permutation-based Page Interleaving Scheme to Reduce Row-buffer Conflicts and Exploit Data Locality," MICRO, 2000