INTERCONNECTION NETWORKS

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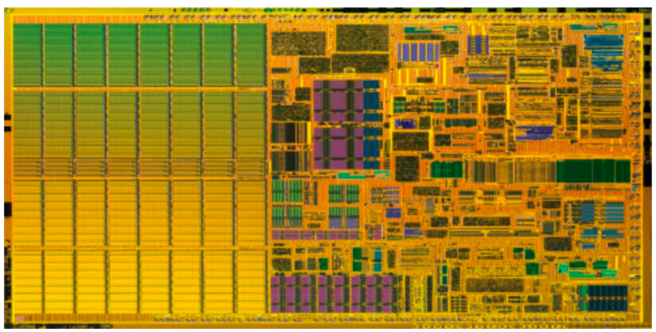
CS/ECE 7810: Advanced Computer Architecture

Overview

- Upcoming deadline
  - Feb.1st: project group formation
  - Only two groups have sent me emails!
- This lecture
  - Basics of the interconnection networks
  - Network topologies
  - Flow control

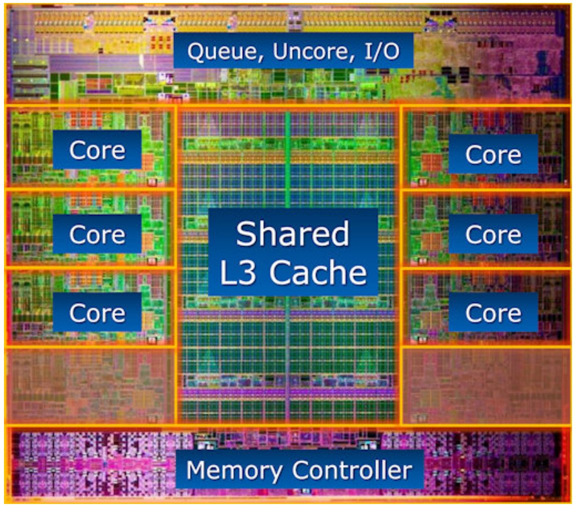
Where Interconnects Are Used?

- About 60% of the dynamic power in modern microprocessors is dissipated in on-chip interconnects



- **Analysis subject: Processor, 0.13 [μm]**
- **77 million transistors, die size of 88 [mm^2]**
- **Data sources (AF, Capacitance, Length)**
- **Excluded: L2 cache, global clock, analog units**

[Magen'04]



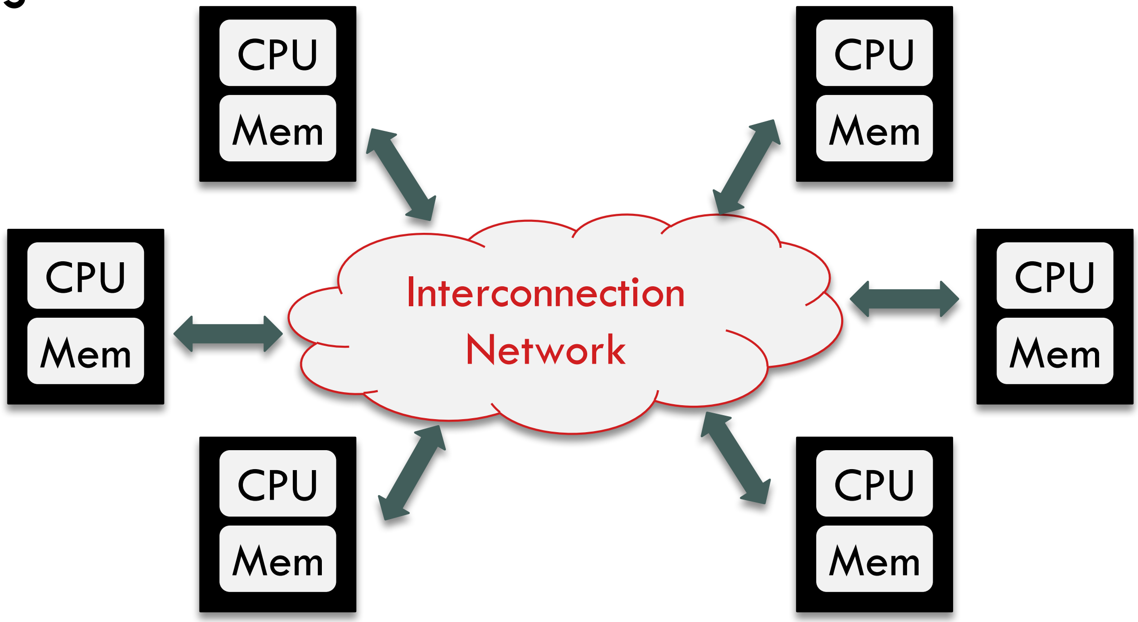
- **Six processor cores**
- **8MB Last level cache**

[Intel Core i7]

Interconnection Networks

- Goal: transfer maximum amount of information with the minimum time and power

- Connects processors, memories, caches, and I/O devices



Types of Interconnection Networks

- Four domains based on number and proximity of devices
  - On-chip networks (OCN or NOC)
    - Microarchitectural elements: cores, caches, reg. files, etc.
  - System/storage area networks (SAN)
    - Computer subsystems: storage, processor, IO device, etc.
  - Local area networks (LAN)
    - Autonomous computer systems: desktop computers etc.
  - Wide area networks (WAN)
    - Interconnected computers distributed across the globe

Basics of Interconnection Networks

- Network topology
  - How to wire switches and nodes in the network
- Routing algorithm
  - How to transfer a message from source to destination
- Flow control
  - How to control the flow messages within the network

Network Topology

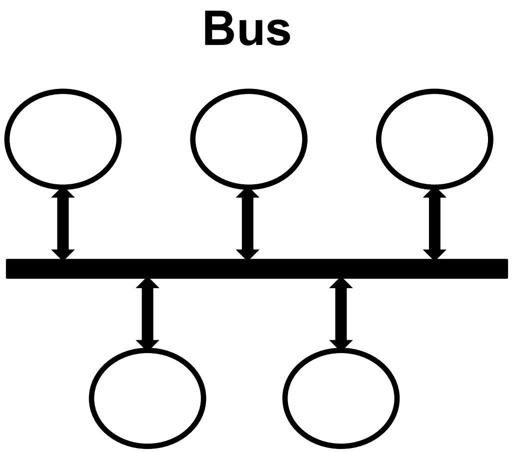
Network Topologies

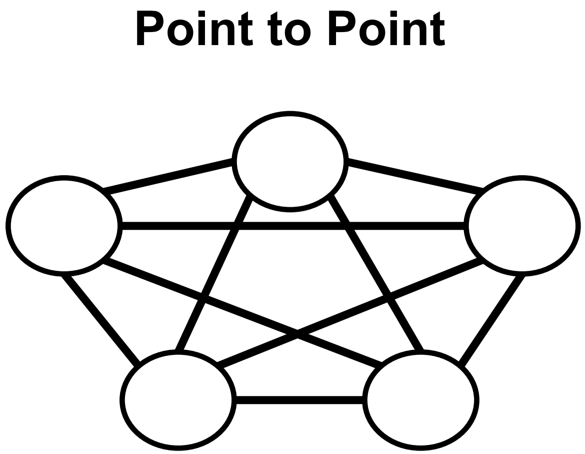
- Regular vs. irregular graphs
  - Examples of regular networks are mesh and ring

- Distances in the network
  - Routing distance: number of links/hops along a route
  - Network diameter: maximum number of hops per route
  - Average distance: average number of links/hops across all valid routes

Example Topologies

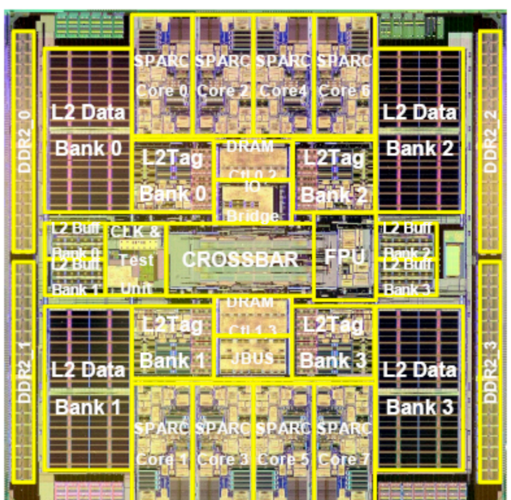
- Bus
  - Simple structure; efficient for small number of nodes
  - Not scalable; highly contended
  - Used in many processors



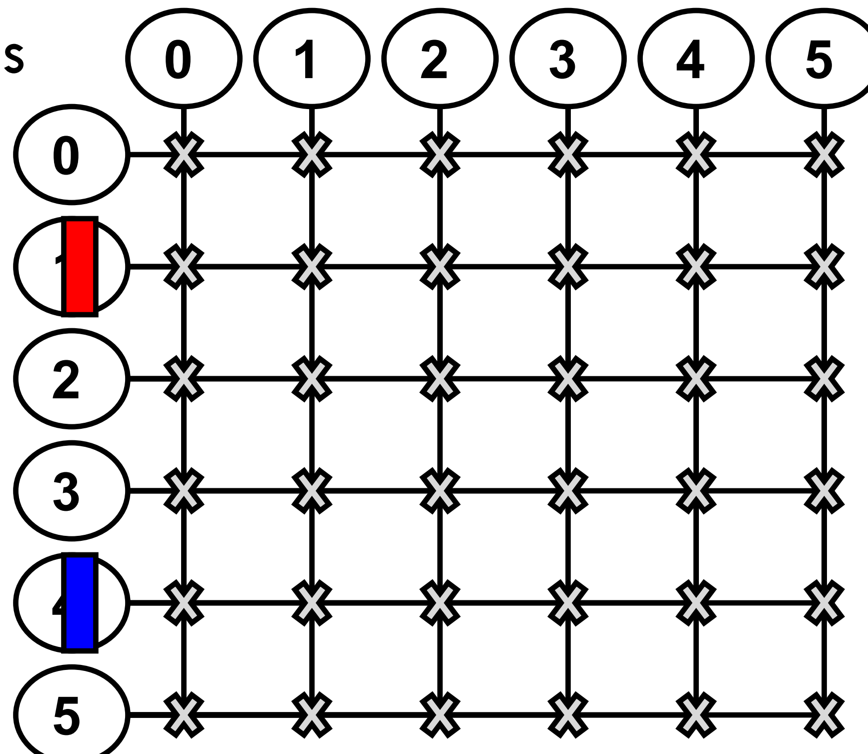


Example Topologies

- Crossbar
  - Complex arbitration
  - High throughput and fast
  - Requires a lot of resources
  - Used in Sun Niagara I/II

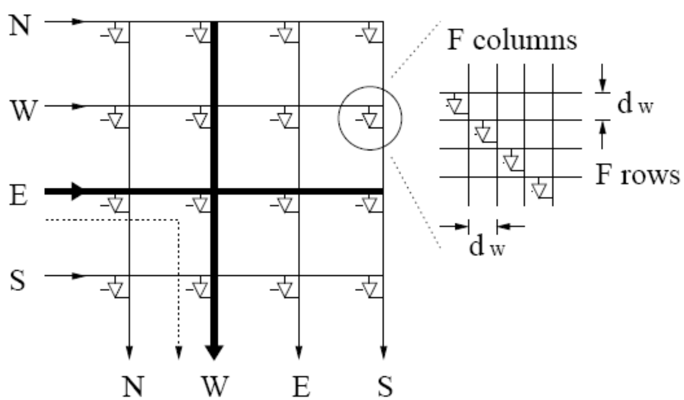


[UltraSPARC T1]

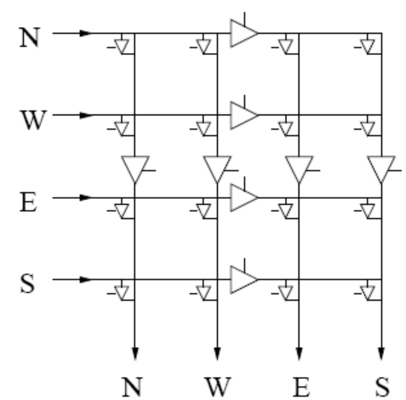


Example Topologies

- Segmented crossbar
  - Reduce switching capacitance (~15-30%)
  - Need a few additional signals to control tri-states



(a) A 4×4 matrix crossbar.



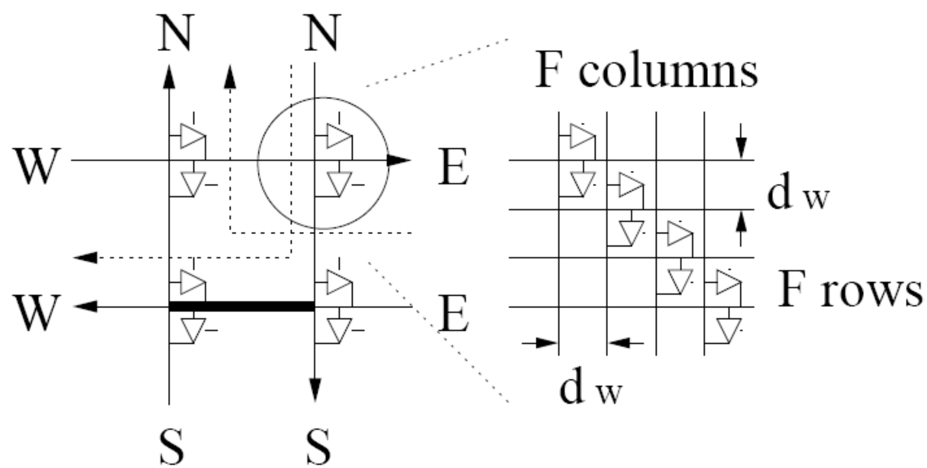
(b) A 4×4 segmented cross-bar with 2 segments per line.

[Wang'03]

Example Topologies

- Goal: optimize for the common case
  - Straight-through traffic does not go thru tristate buffers
- Some combinations of turns are not allowed
  - Why?

Read the paper for details.

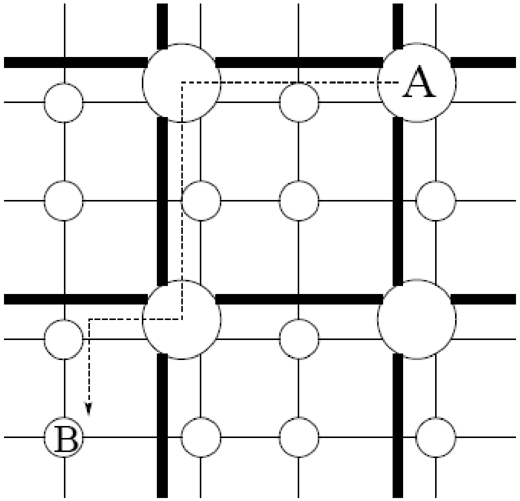


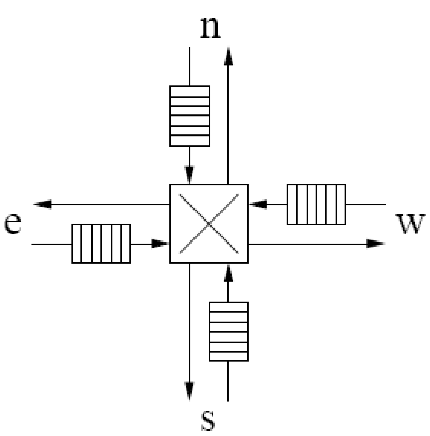
(a) A 4×4 cut-through crossbar.

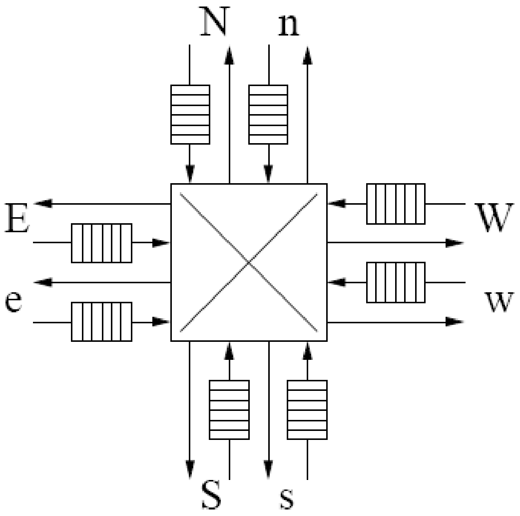
[Wang'03]

Example Topologies

- Express channels to reduce number of hops
  - like taking the freeway



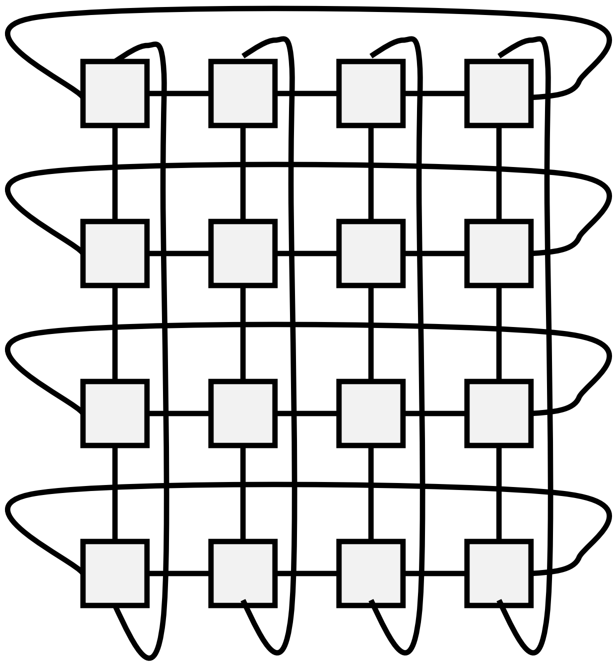




[Wang'03]

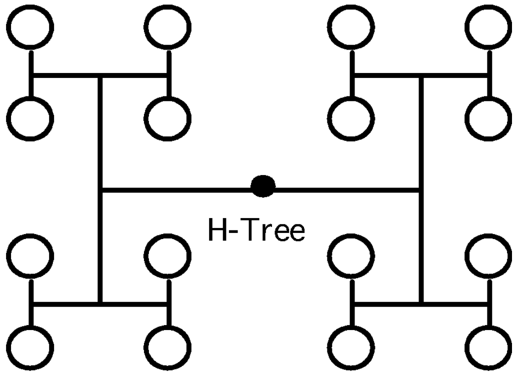
Example Topologies

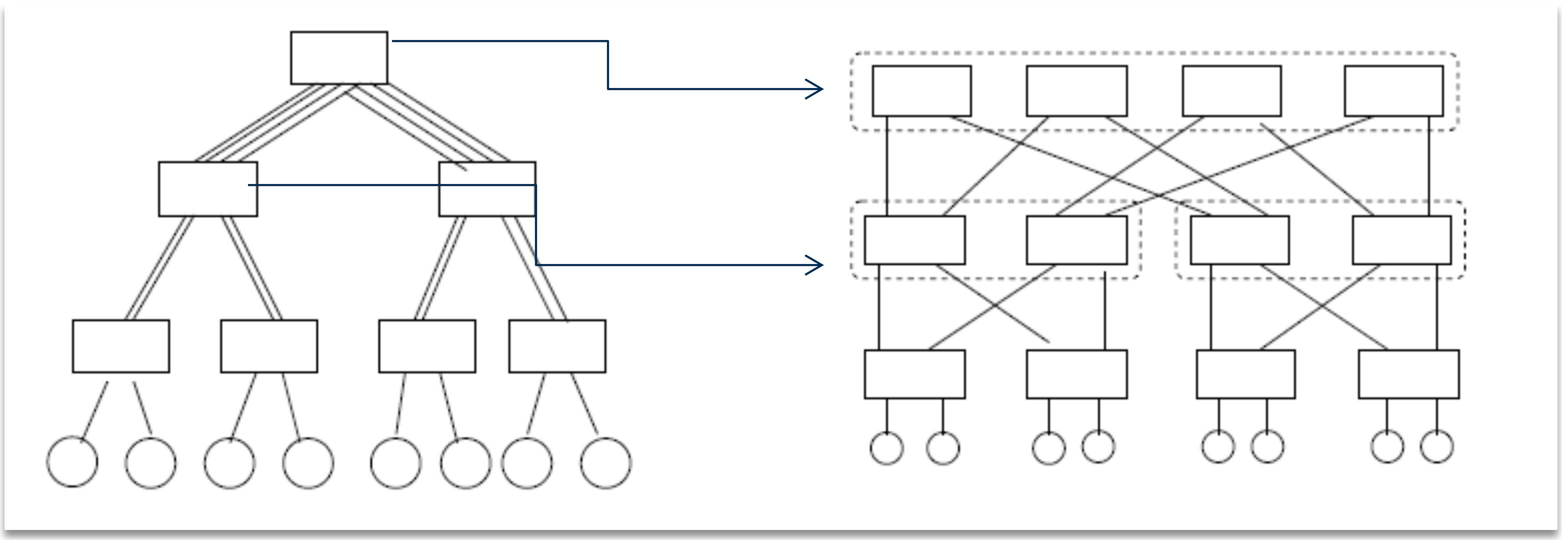
- Ring
  - Cheap; long latency
  - IBM Cell
- Mesh
  - Path diversity, efficient
  - Tilera 100-core
- Torus
  - More path diversity
  - Expensive and complex



Example Topologies

- Tree
  - Simple and low cost
  - Easy to layout
  - Efficiently handles local traffic
  - Towards root, links are heavily contended





Example Topologies

- Omega network
  - Single path from source to destination
  - Does not support all possible permutations
  - Proposed to replace costly crossbars as processor-memory interconnect

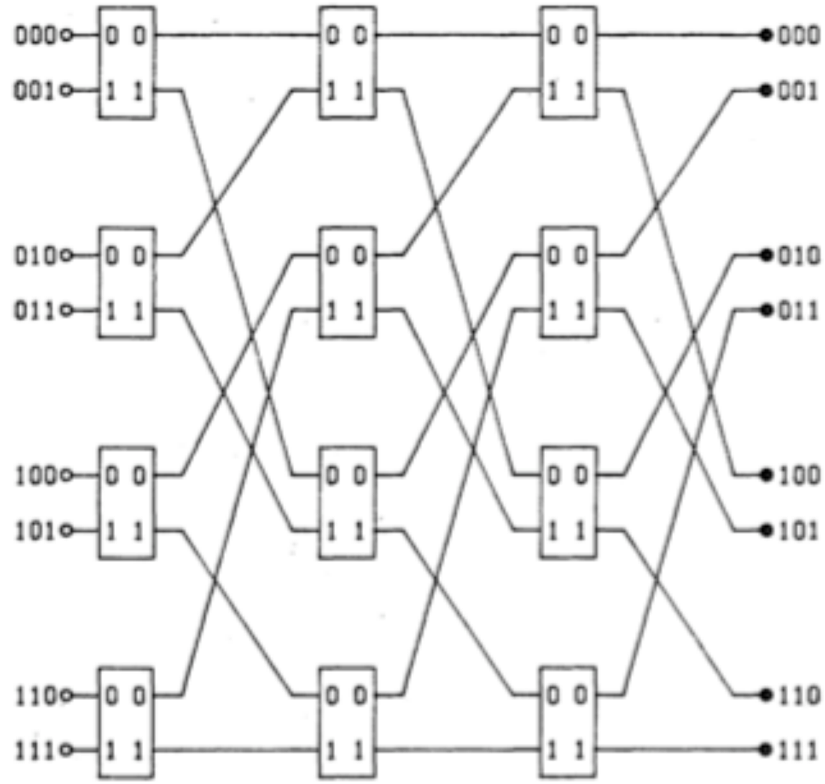


Fig. 2. Omega-network ($N = 8$).

[Gottlieb'82]

Flow Control

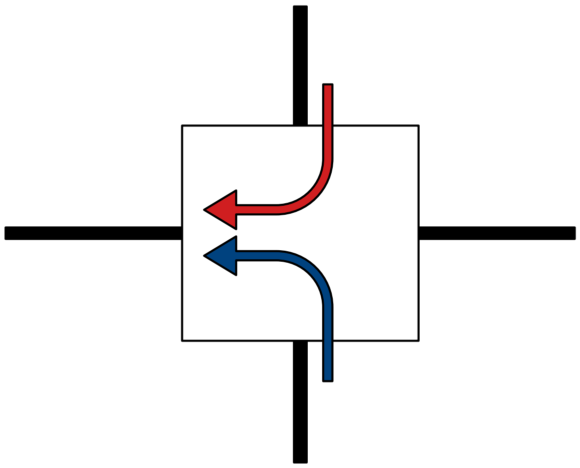
Sending Data in Network

- Circuit switching
  - Establish full path; then send data
  - Everyone else using the same link has to wait
  - Setup overheads
- Packet switching
  - Route individual packets (via different paths)
  - More flexible than CS
  - May be slower than CS

Handling Contention

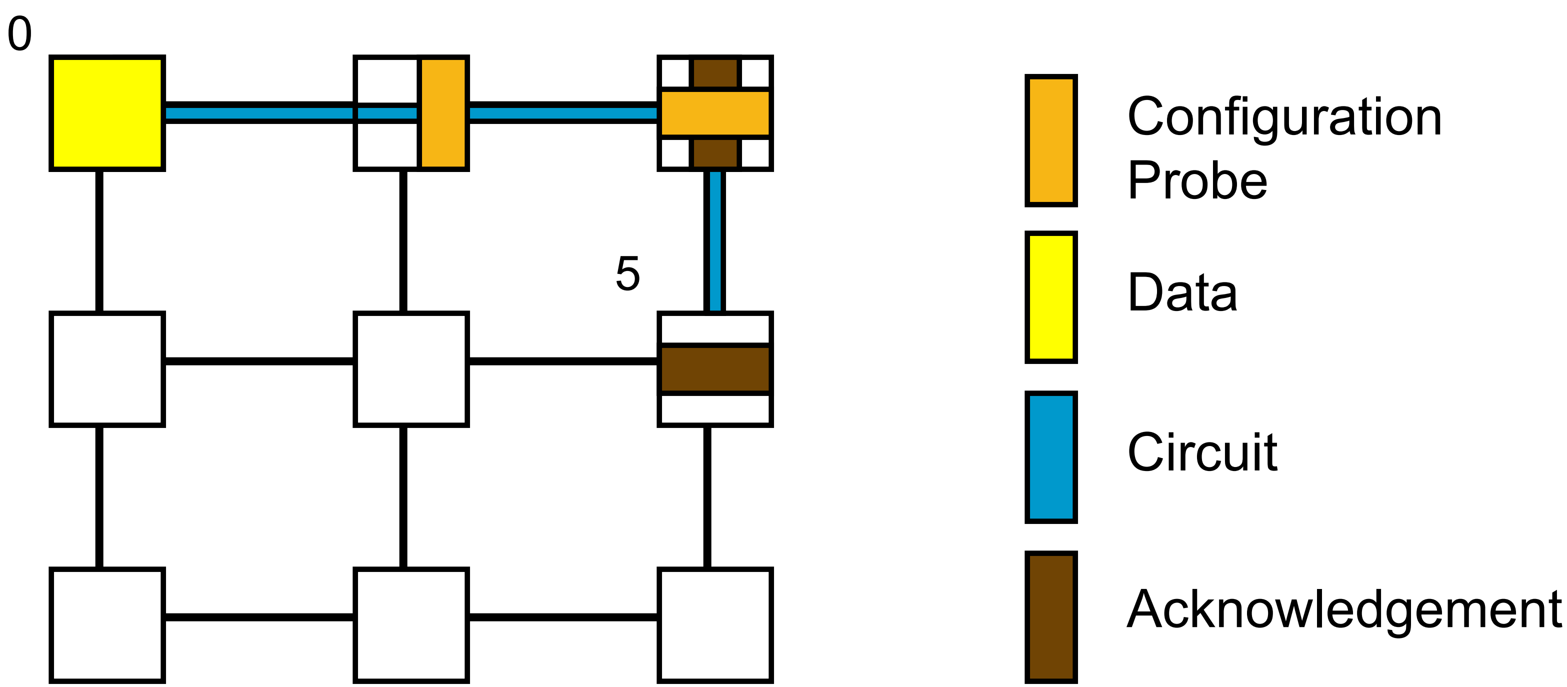
- Problem
  - Two packets want to use the same link at the same time

- Possible solutions
  - Drop one
  - Misroute one (deflection)
  - Buffer one



Circuit Switching Example

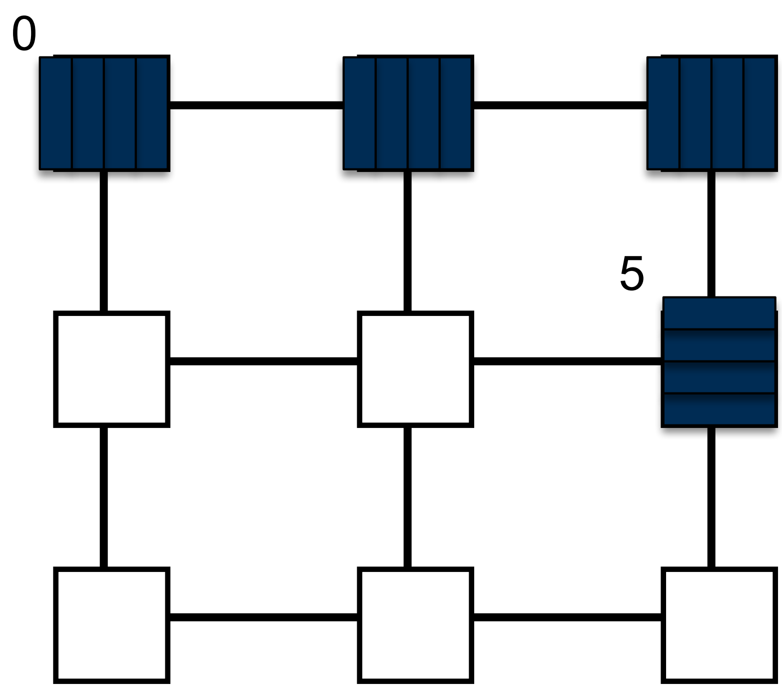
- Significant latency overhead prior to data transfer
- Other requests forced to wait for resources



[Lipasti]

Store and Forward Example

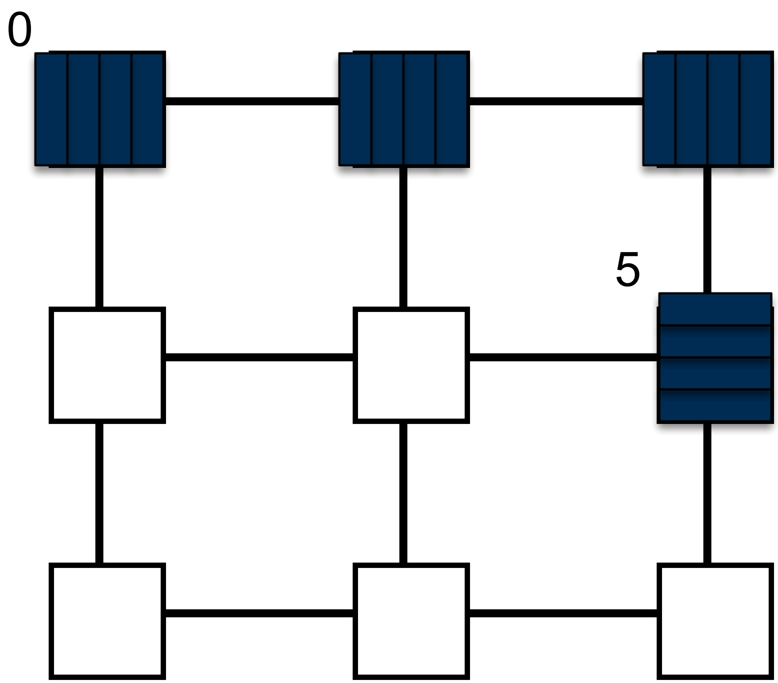
- High per-hop latency
- Larger buffering required



[Lipasti]

Virtual Cut Through Example

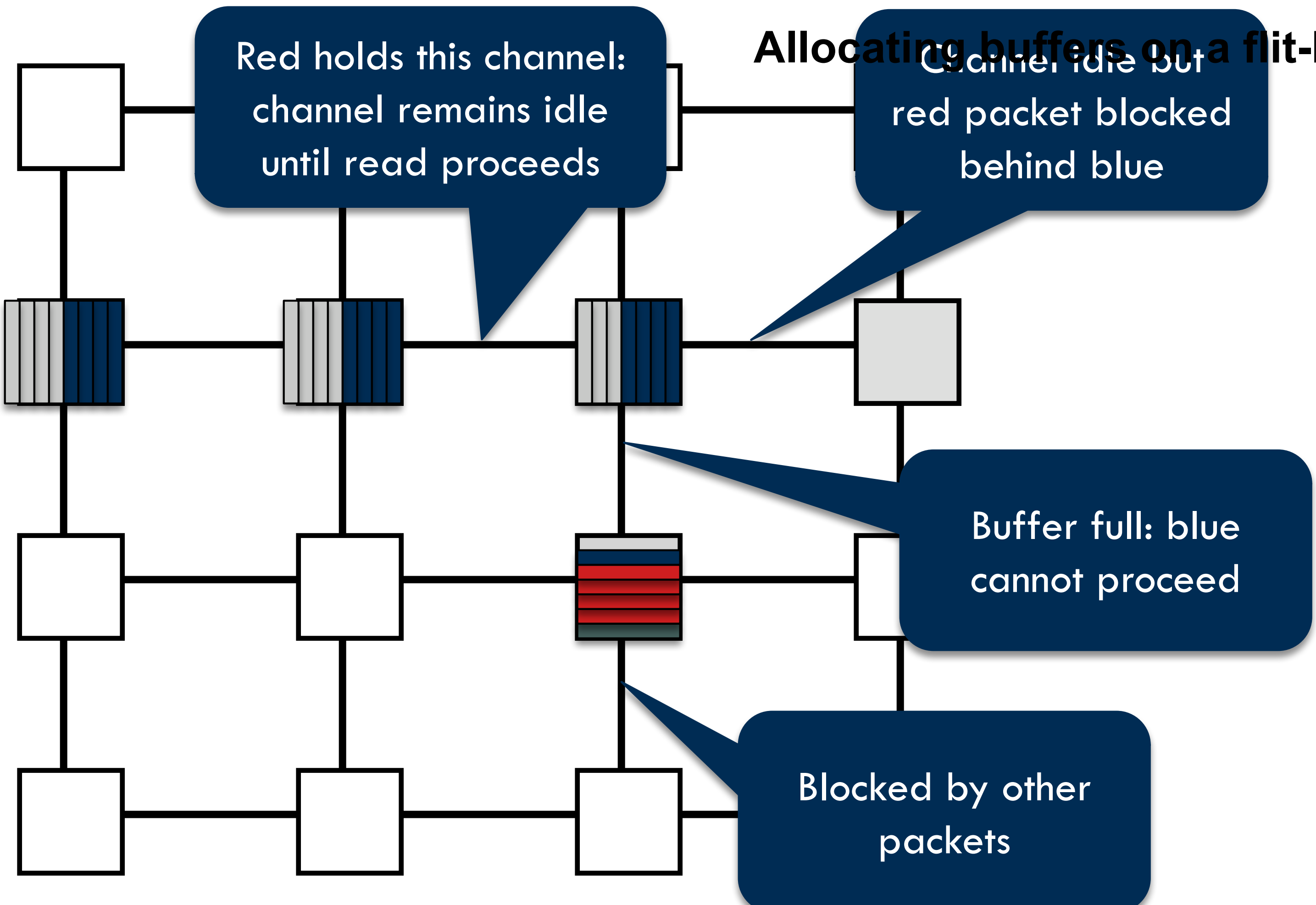
- Lower per-hop latency
- Larger buffering required



[Lipasti]

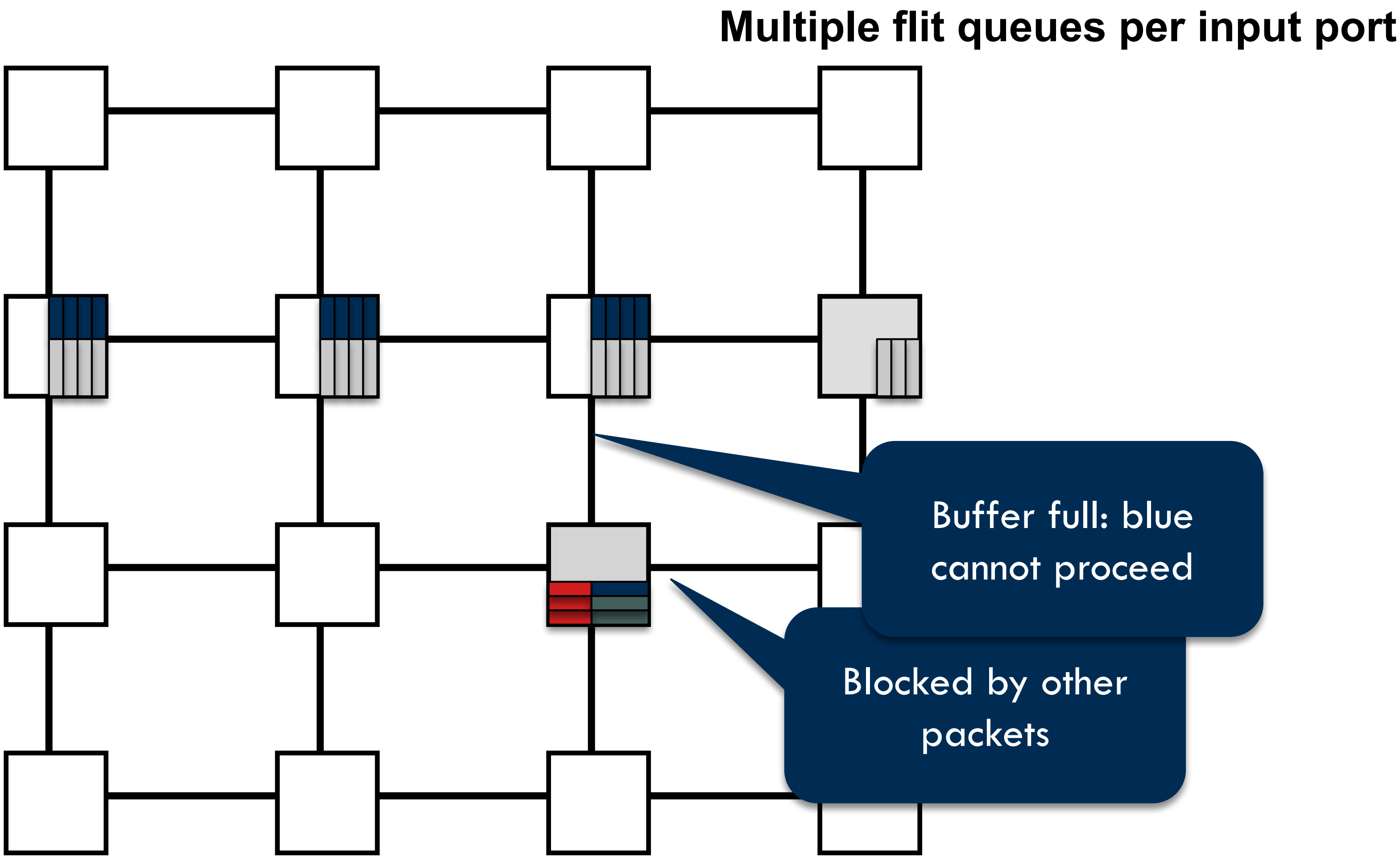
Wormhole Example

Allocating buffers on a flit-basis



[Lipasti]

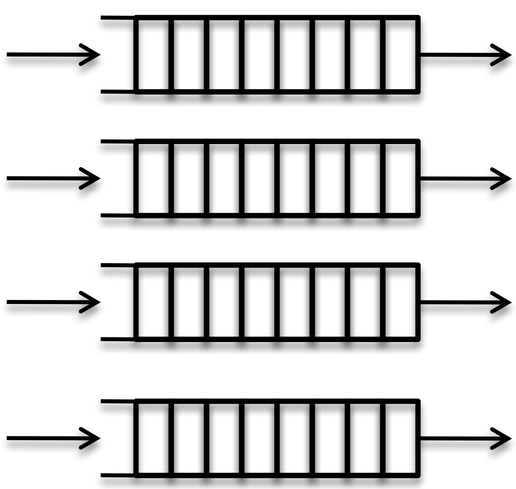
Virtual Channel Example

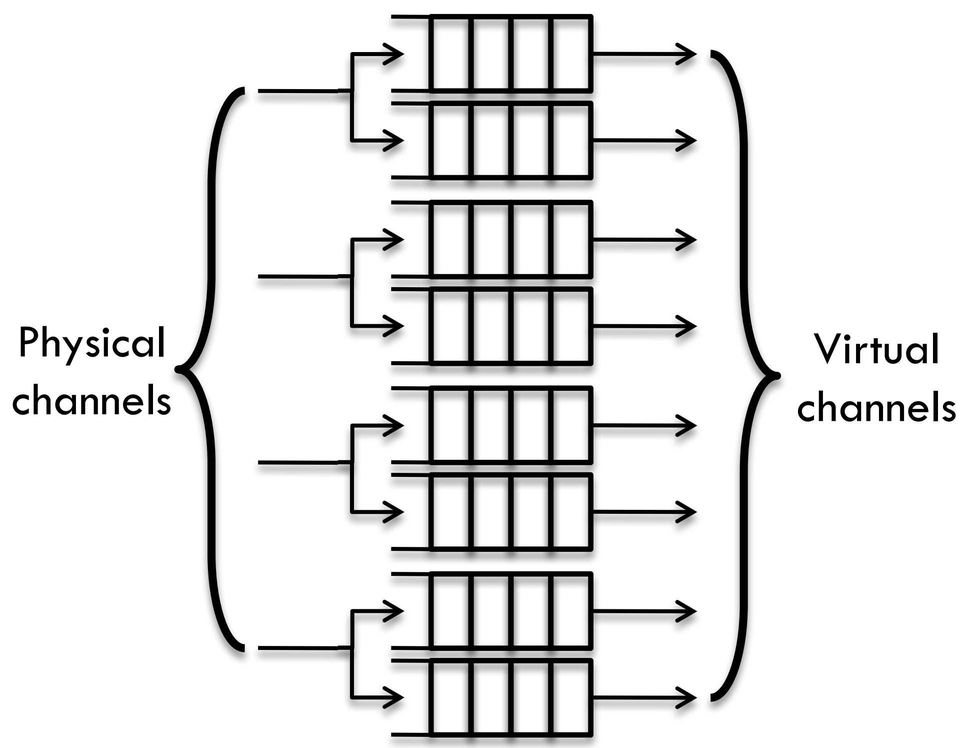


[Lipasti]

Virtual Channel Buffers

- Single buffer per input
- Multiple fixed length queues per physical channel





[Lipasti]