PIPELINE HAZARDS

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Overview

- □ This lecture
 - Pipeline Hazards
 - Structural
 - Data
 - Control

Pipeline Hazards

- Structural hazards: multiple instructions compete for the same resource
- Data hazards: a dependent instruction cannot proceed because it needs a value that hasn't been produced
- Control hazards: the next instruction cannot be fetched because the outcome of an earlier branch is unknown

□ Sample C++ code

```
for (i=100; i != 0; i--) {
    sum = sum + i;
}
total = total + sum;
```

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```
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    sum = sum + i;
}
total = total + sum;
```

```
addi $1, $0, 100

beq $0, $1, next

add $2, $2, $1

addi $1, $1, -1

J for
```

add \$3, \$3, \$2

next:

What are possible target instructions?

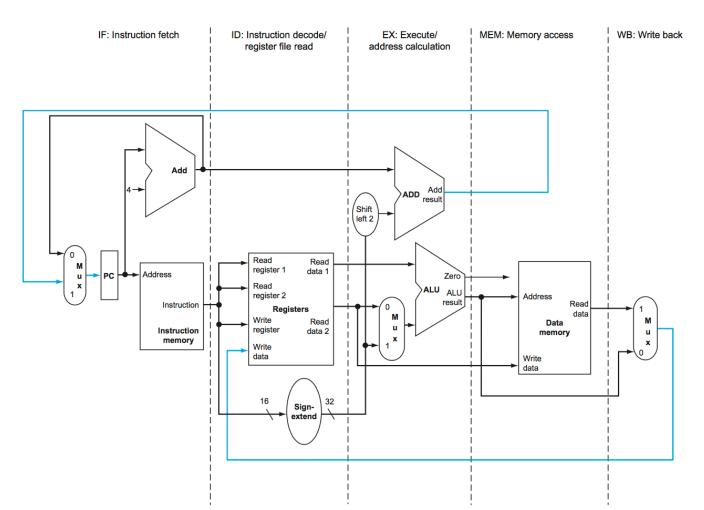
add \$3, \$3, \$2

next:

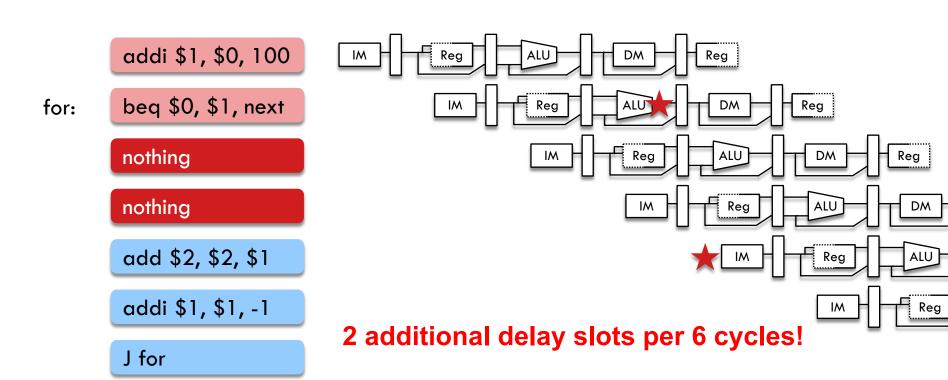
□ Sample C++ code for (i=100; i!= 0; i--) { sum = sum + i;total = total + sum;addi \$1, \$0, 100 beq \$0, \$1, next Reg Reg ALU add \$2, \$2, \$1 Reg addi \$1, \$1, -1 J for Reg ALU

What happens inside the pipeline?

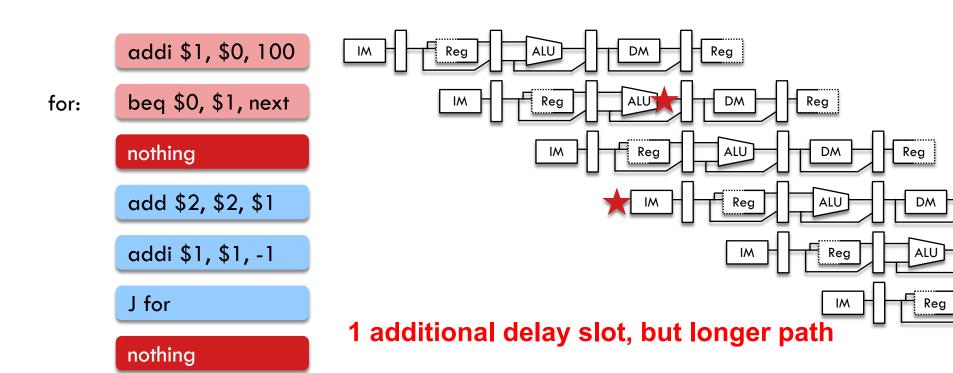
□ The outcome of the branch



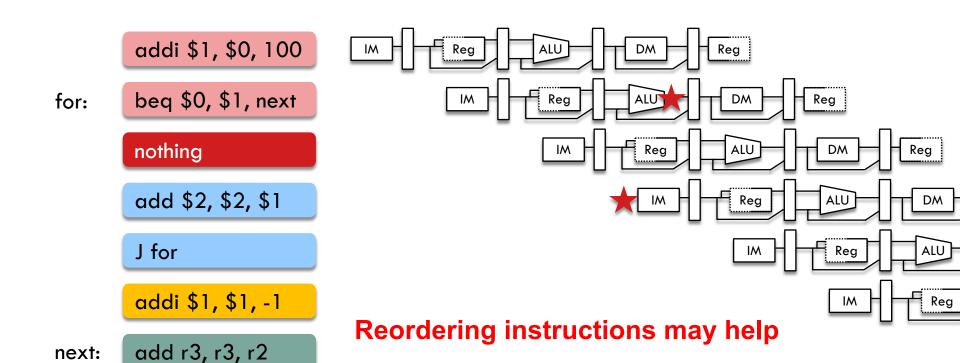
- 1. introducing stall cycles and delay slots
 - How many cycles/slots?
 - One branch per every six instructions on average!!



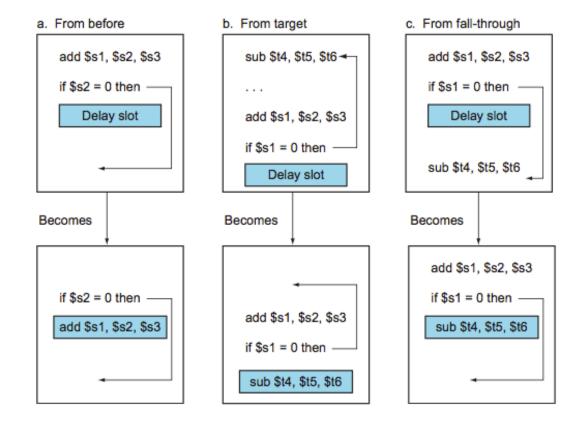
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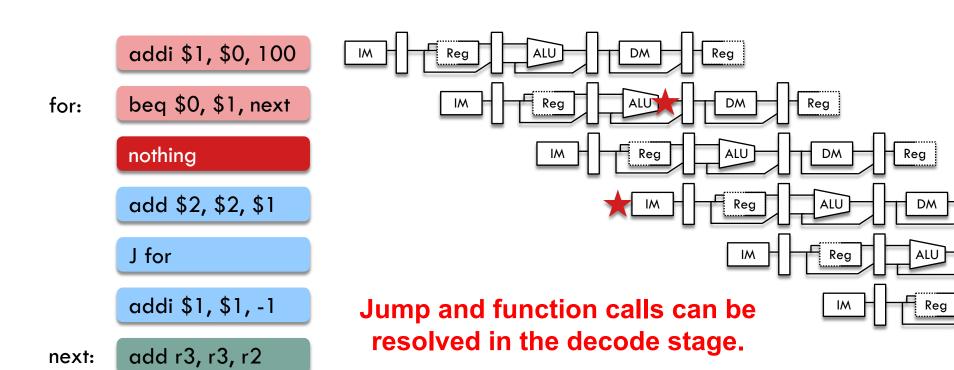
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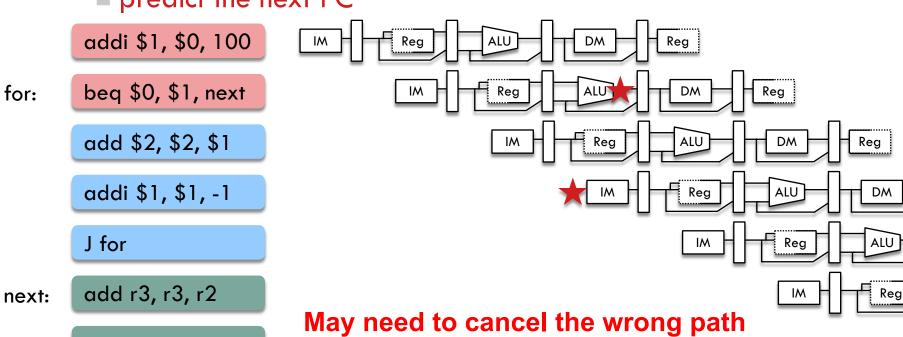
- Strategies for filling up the branch delay slot
 - (a) is the best choice; what about (b) and (c)?



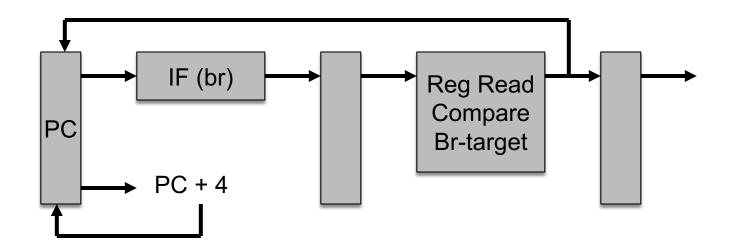
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 - How many cycles/slots?
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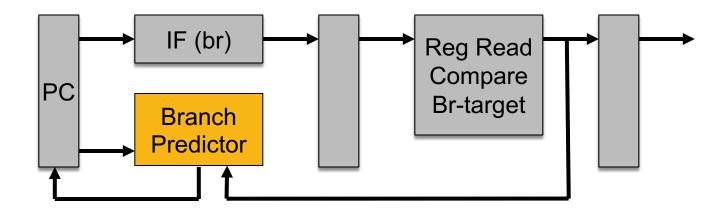
- 1. introducing stall cycles and delay slots
- 2. predict the branch outcome
 - simply assume the branch is taken or not taken
 - predict the next PC



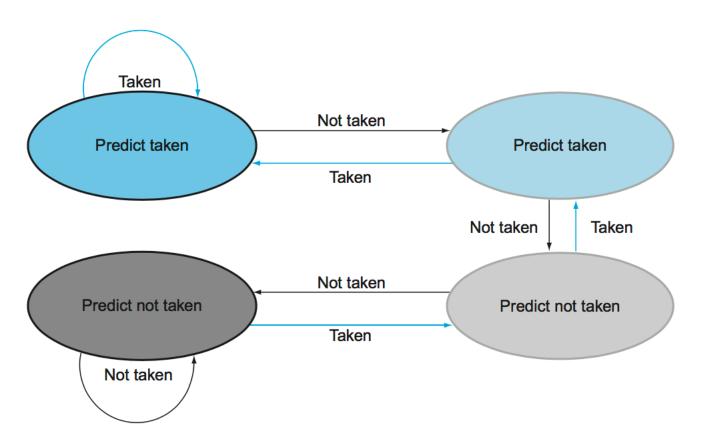
□ Pipeline without branch predictor



□ Pipeline with branch predictor



□ The 2-bit branch predictor



Summary of the Pipeline

