PIPELINE HAZARDS

Mahdi Nazm Bojnordi

Assistant Professor

School of Computing

University of Utah

THE UNIVERSITY OF UTAH

Overview

- Notes
  - Homework 8 is due tonight
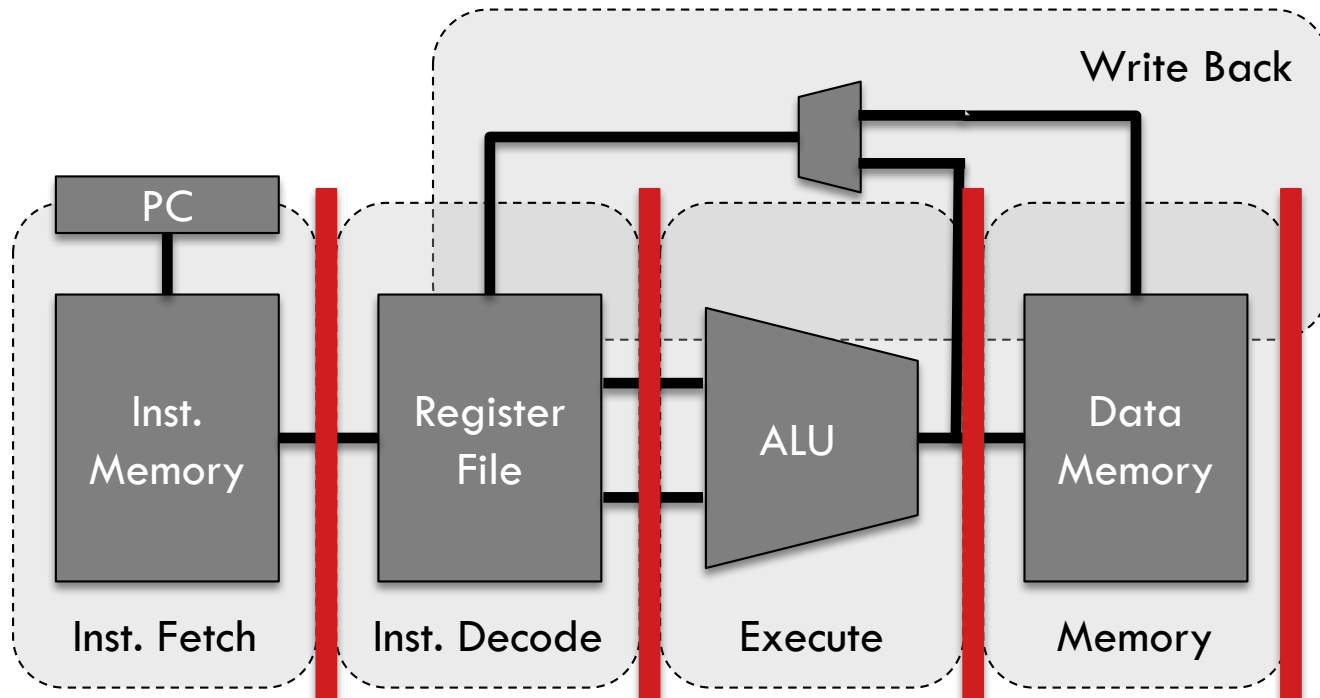   - Verify your submitted file before midnight

- This lecture
  - Pipeline Hazards
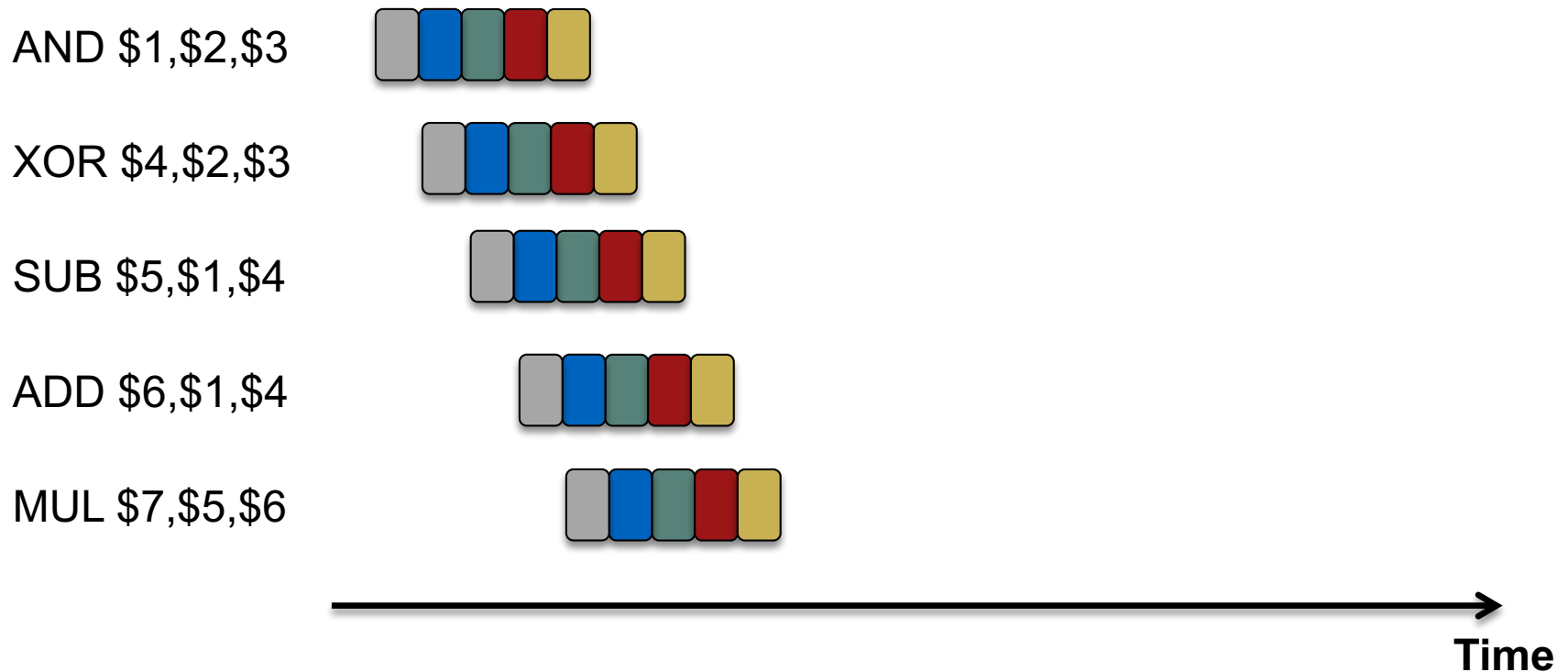   - Structural
    - Data
    - Control

Pipelined Architecture

☐ Five stage pipeline

◘ Critical path determines the cycle time
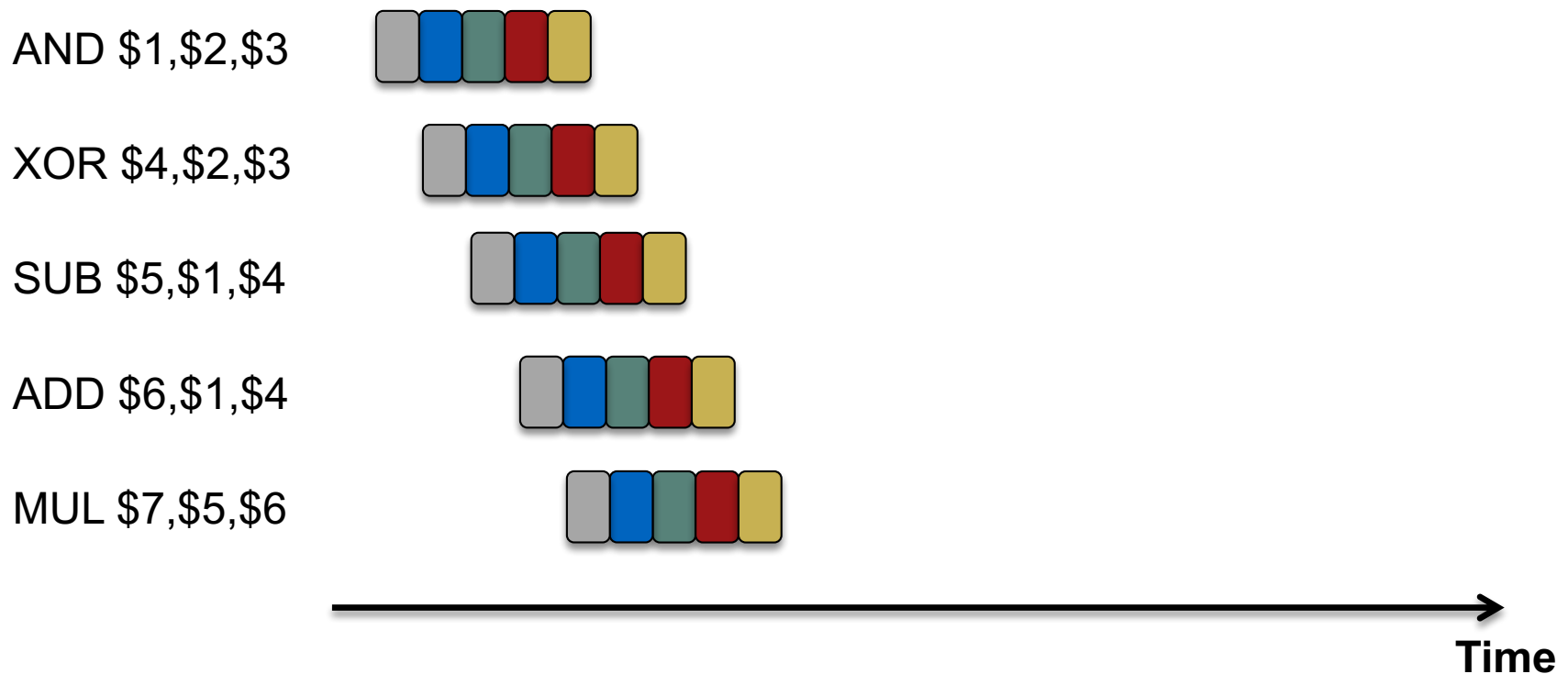
Pipelined Architecture

- Example program
  - CT=1.5ns; CPU Time = ?

AND $1,$2,$3

XOR $4,$2,$3

SUB $5,$1,$4

ADD $6,$1,$4

MUL $7,$5,$6

Time

Pipelined Architecture

- Example program
  - CT=1.5ns; CPU Time = 9 x 1.5ns = 13.5ns

AND $1,$2,$3

XOR $4,$2,$3

SUB $5,$1,$4
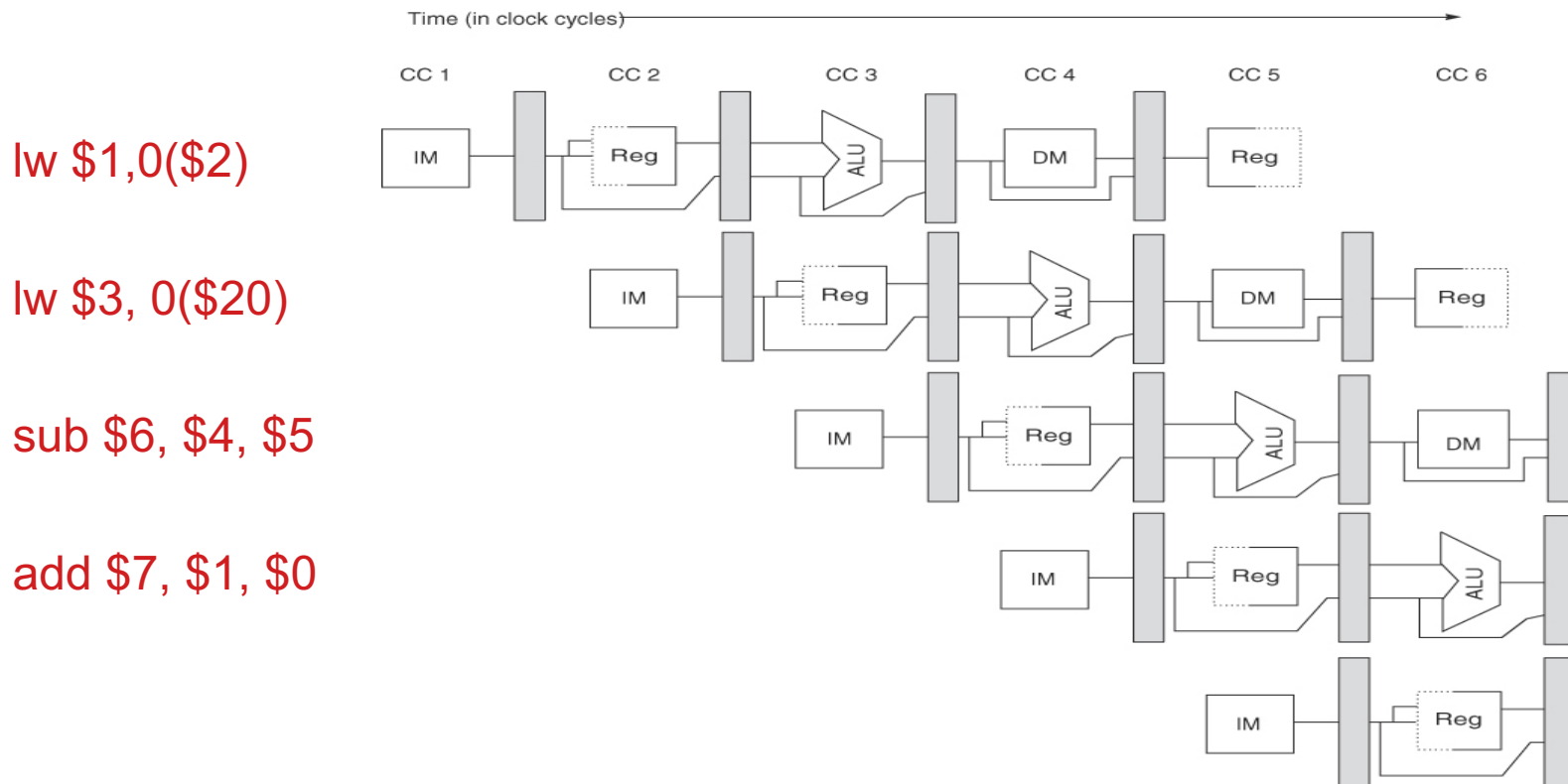
ADD $6,$1,$4

MUL $7,$5,$6

Time

Pipeline Hazards

- **Structural hazards**: multiple instructions compete for the same resource

- **Data hazards**: a dependent instruction cannot proceed because it needs a value that hasn't been produced

- **Control hazards**: the next instruction cannot be fetched because the outcome of an earlier branch is unknown
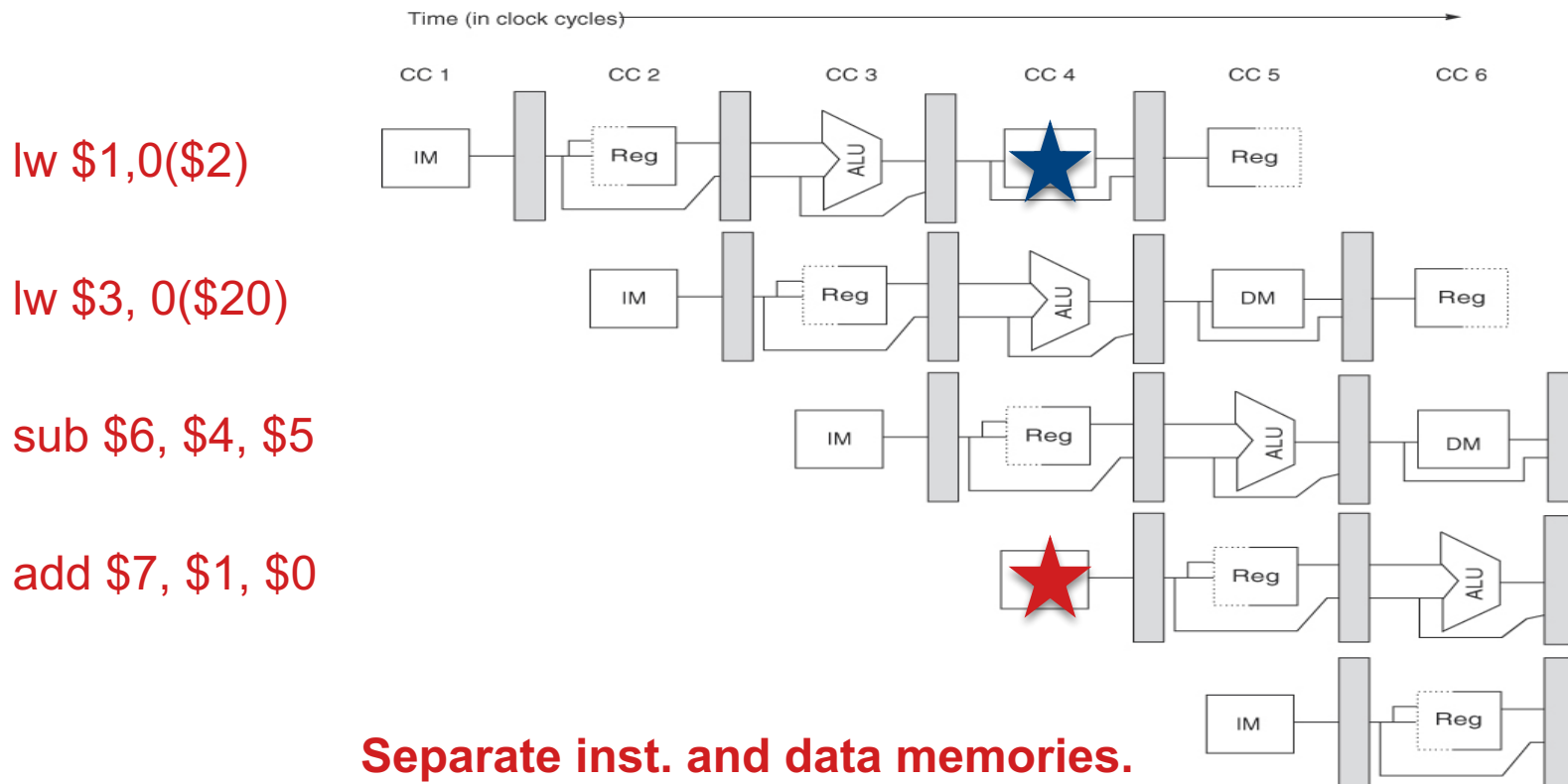
Structural Hazards

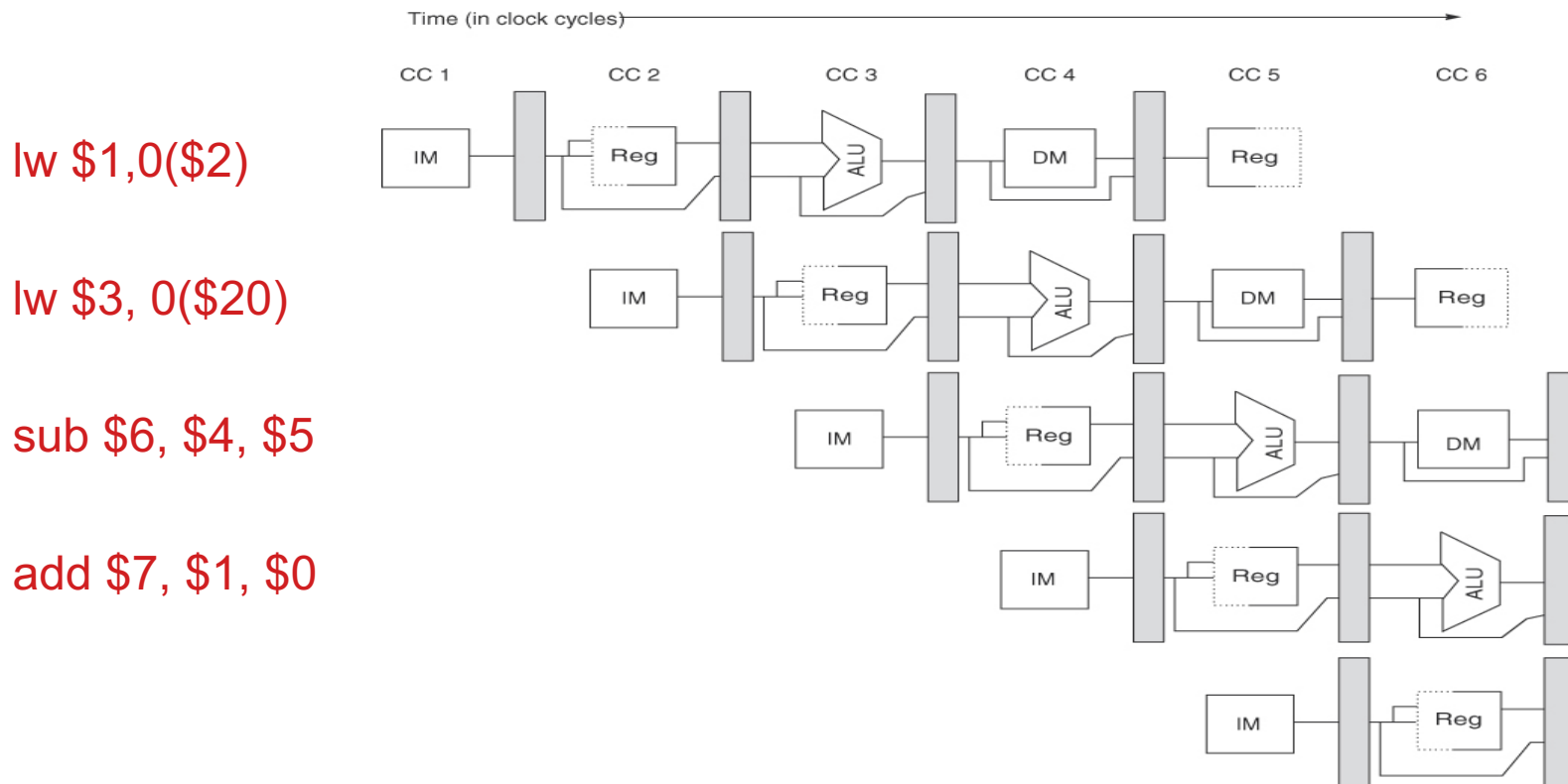□ 1. Unified memory for instruction and data

lw $1,0($2)

lw $3, 0($20)

sub $6, $4, $5

add $7, $1, $0

Structural Hazards

☐ 1. Unified memory for instruction and data

Time (in clock cycles)

| CC 1 | CC 2 | CC 3 | CC 4 | CC 5 | CC 6 |

lw $1,0($2)

lw $3, 0($20)

sub $6, $4, $5

add $7, $1, $0

Separate inst. and data memories.

Structural Hazards

- 1. Unified memory for instruction and data
- 2. Register file with shared read/write access ports

lw $1,0($2)

lw $3, 0($20)

sub $6, $4, $5

add $7, $1, $0

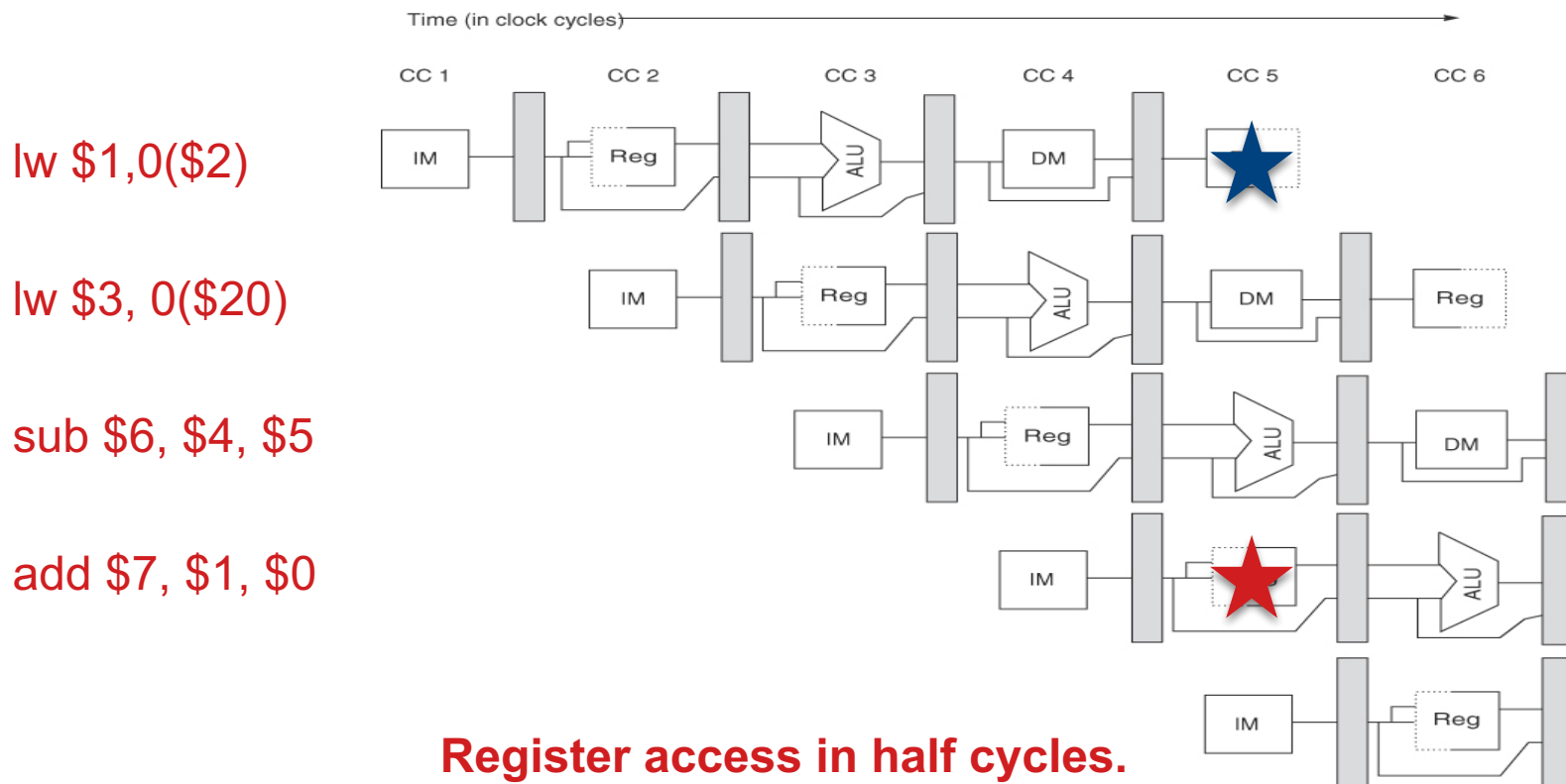# Structural Hazards

□ 1. Unified memory for instruction and data

□ 2. Register file with shared read/write access ports

lw $1,0($2)

lw $3, 0($20)

sub $6, $4, $5

add $7, $1, $0

Register access in half cycles.

Data Hazards

□ Solution: register read and write in half cycles