CPU ORGANIZATION

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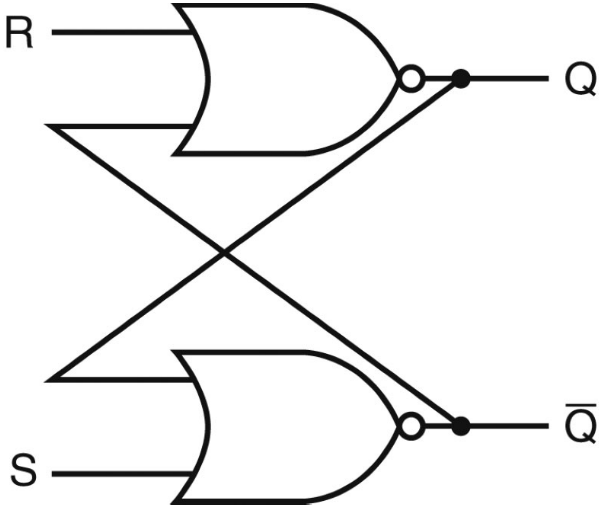
Overview

- Notes
  - Homework 7 is due tonight
    - Verify your submitted file before midnight
- This lecture
  - Finite state machine
  - Central processing unit

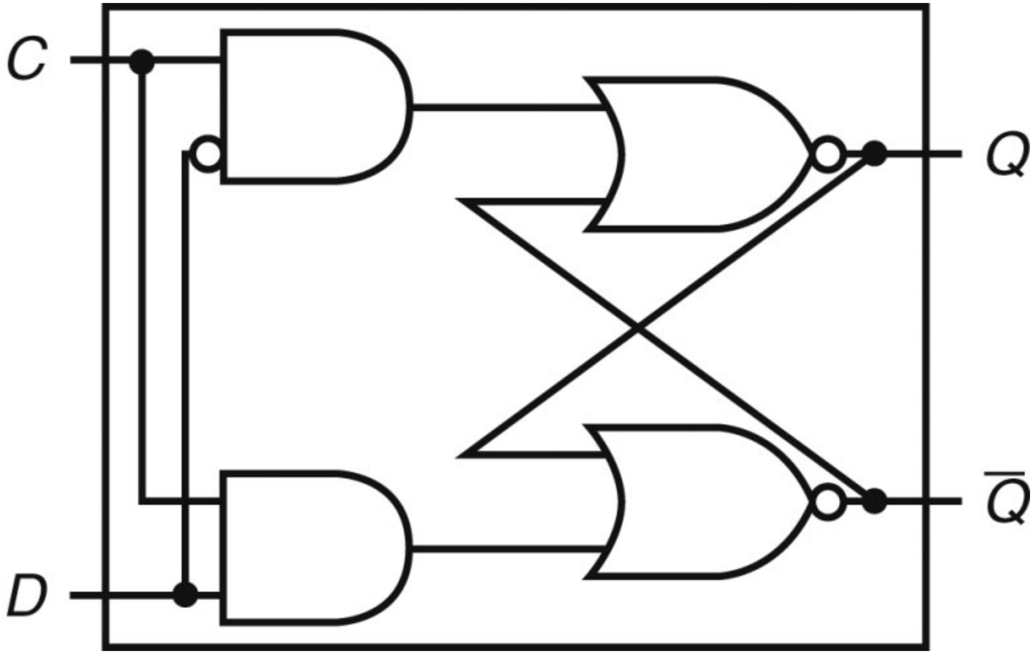
Recall: Design of an S-R Latch

- An S-R latch: set-reset latch
  - When Set is high, a 1 is stored
  - When Reset is high, a 0 is stored
  - When both are low, the previous state is preserved (hence, known as a storage or memory element)
  - Both are high – this set of inputs is not allowed



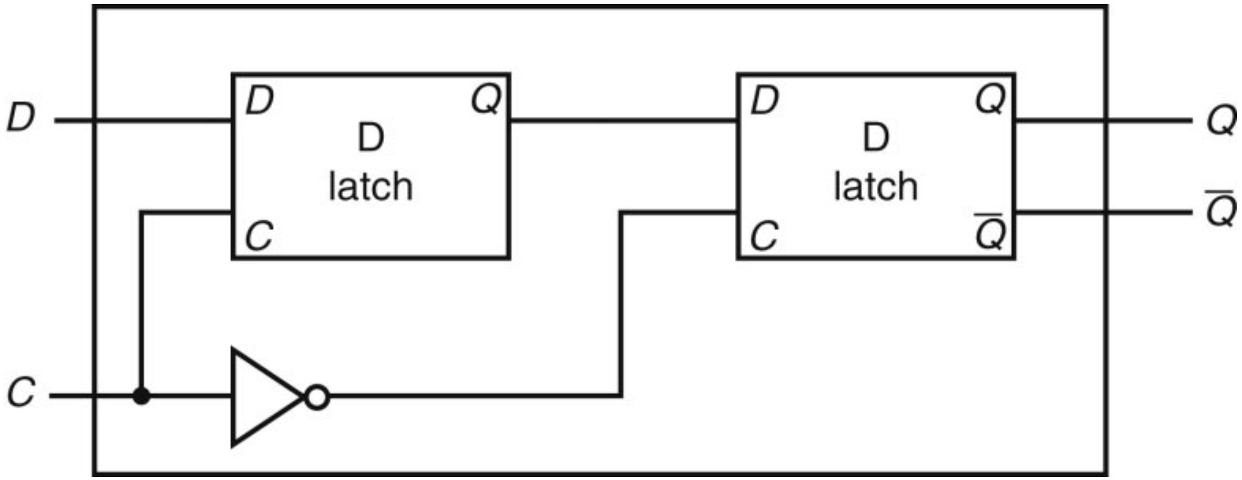
Design of a D Latch

- The value of the input D signal (data) is stored only when the clock is high – the previous state is preserved when the clock is low



Design of a D Flip Flop

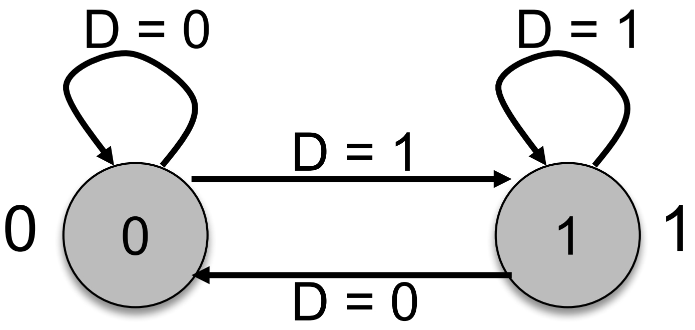
- Latch vs. Flip Flop
  - Latch: outputs can change any time the clock is high (asserted)
  - Flip flop: outputs can change only on a clock edge
    - Technically, two D latches in series



State Diagram

- Each state is shown with a circle, labeled with the state value
  - the contents of the circle are the outputs

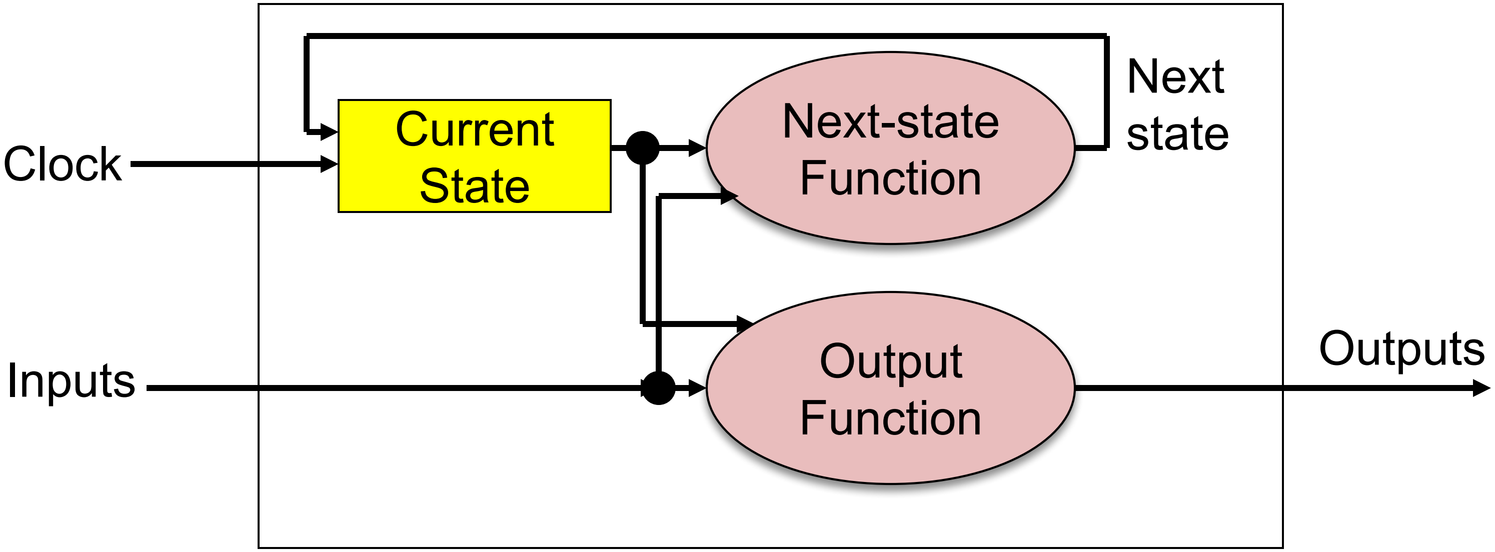
- An arc represents a transition to a different state, with the inputs indicated on the label



What is this state diagram for?

Finite State Machine

- A sequential circuit is described by a finite state diagram.
  - We use variation of a truth table for inputs and outputs
  - Note that state is updated only on a clock edge



Example: Counters

- Counters are an important class of finite state machines

- Design: a circuit that stores a 3-bit number and increments the value on every clock edge.
  - It starts again from 0 when reaching the largest value.
  - Draw the state diagram; how many states and inputs?

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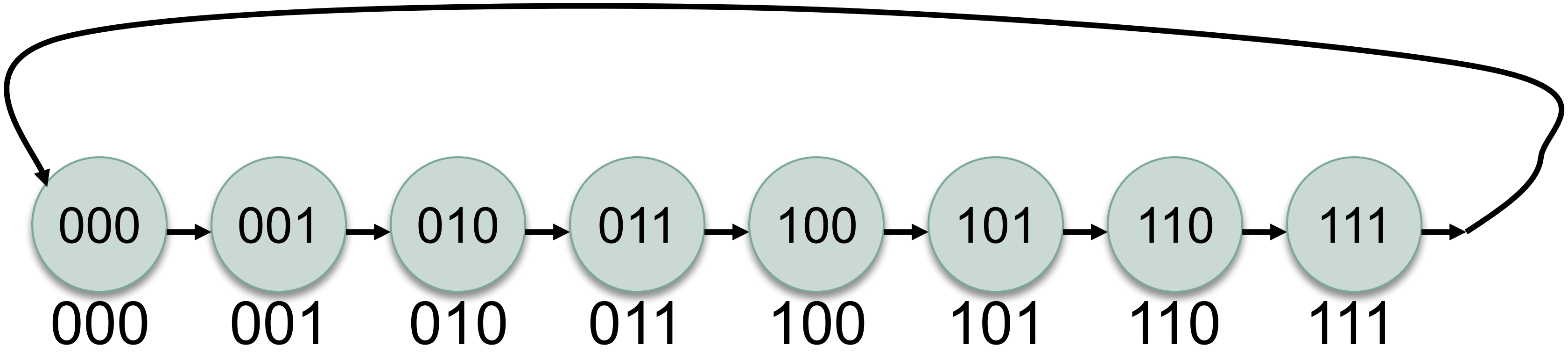

Example: Traffic Control Light

- A traffic light with only green and red; either the North-South road has green or the East-West road has green (both can't be red).

- Design: there are detectors on the roads to indicate if a car is on the road; the lights are updated every 30 seconds; a light need change only if a car is waiting on the other road
  - How many inputs, outputs, and states?

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State Transition Table:

CurrState	InputEW	InputNS	NextState=Output
N	0	0	N
N	0	1	N
N	1	0	E
N	1	1	E
E	0	0	E
E	0	1	N
E	1	0	E
E	1	1	N

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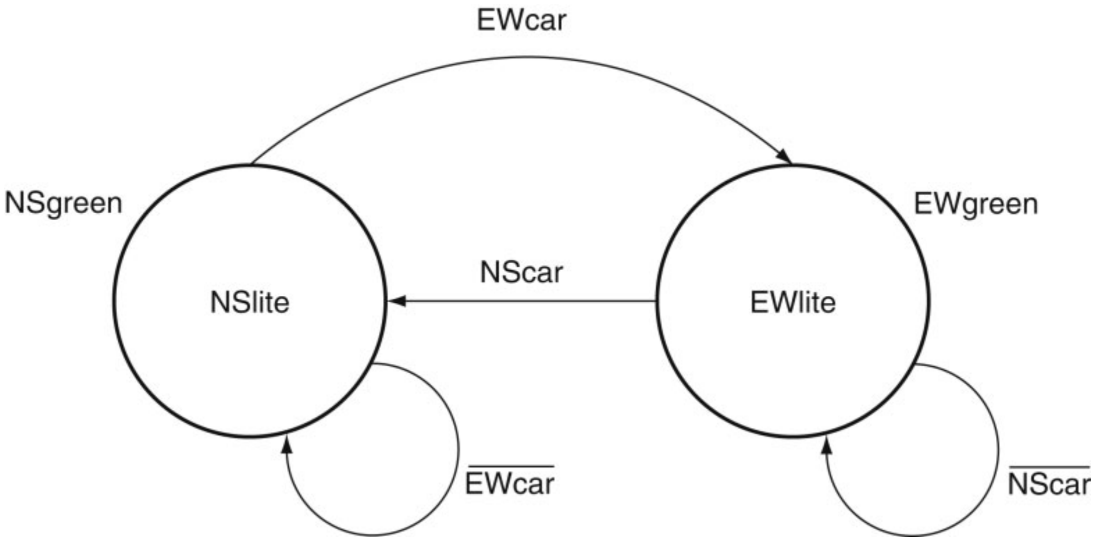
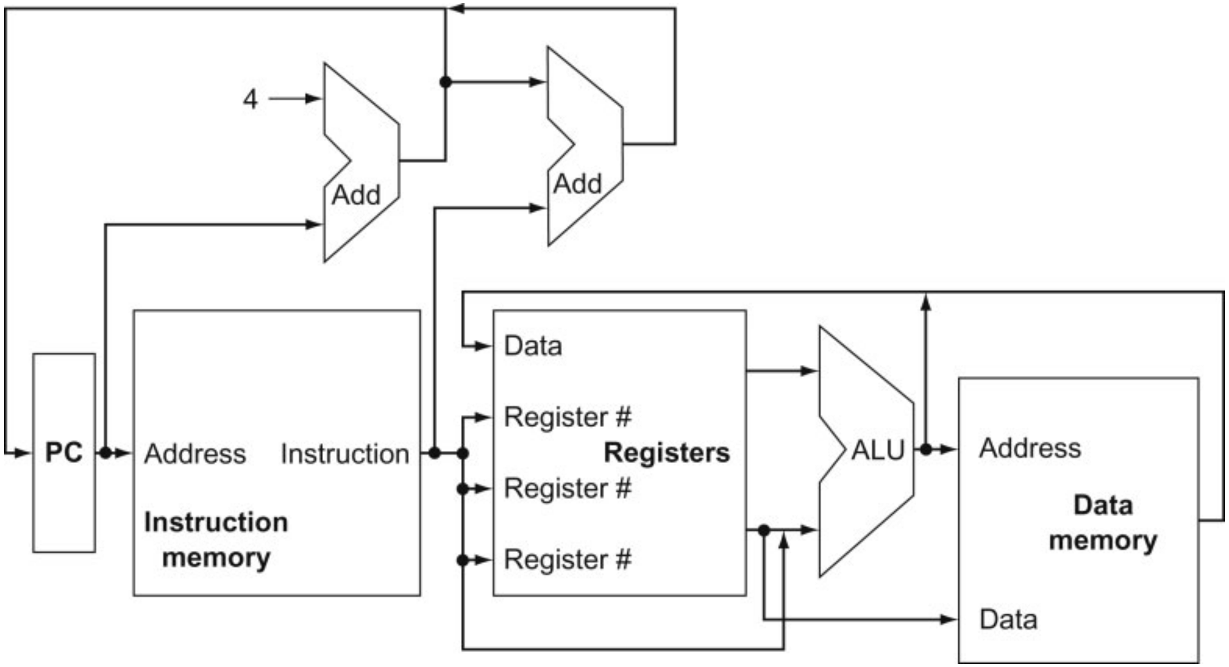


A Simple Processor

- What do we need for a basic MIPS processor?
  - basic math (add, sub, and, or, slt)
  - memory access (lw and sw)
  - branch and jump instructions (beq and j)
- Main components
  - Memory
    - Data and instructions
  - Register, ALU, and control logic
  - Common operations
    - Fetch unit
    - Register read

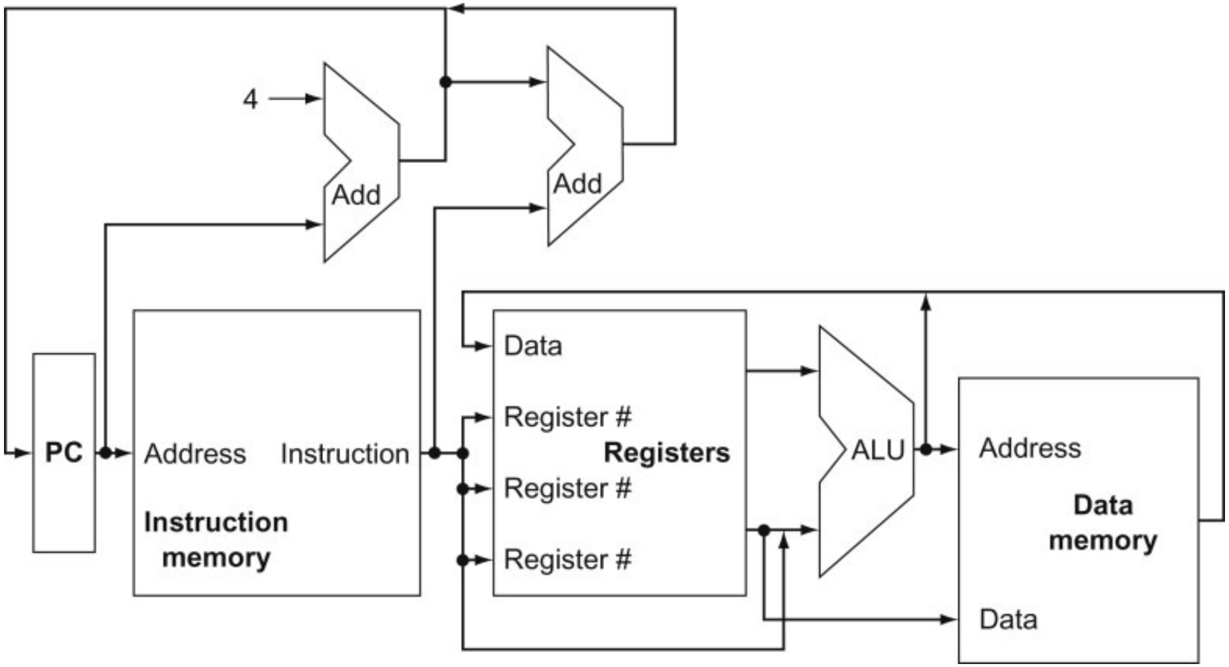
Overview of the Processor

- □ What is the role of the Add units?
- □ Explain the inputs to the data memory unit
- □ Explain the inputs to the ALU
- □ Explain the inputs to the register unit



Clocking the Processor

- Which of the units need a clock?
- What is being saved (latched) on the rising edge of the clock?
- Keep in mind that the latched value remains there for an entire cycle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Add
Add
PC
Address
Instruction
Instruction memory
Data
Register #
Registers
Register #
Register #
ALU
Address
Data memory
Data