CPU ORGANIZATION

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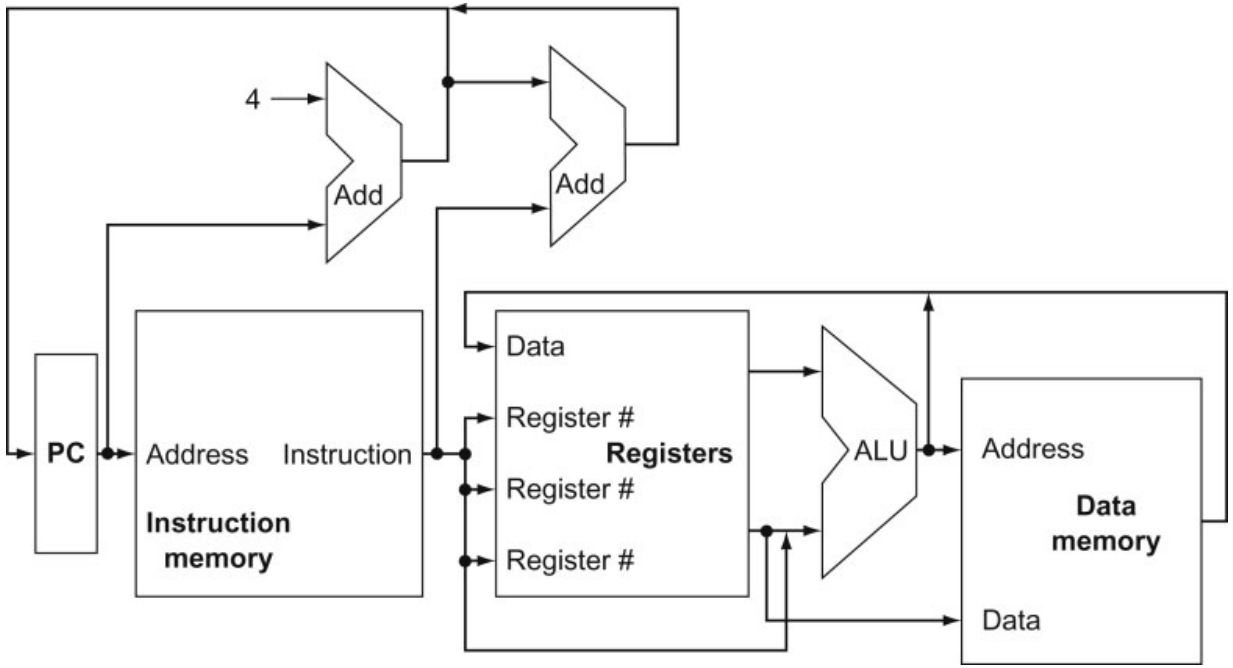
Overview

- Notes
  - Homework 8 is due Thursday (Mar. 28th)
    - Verify your submitted file before midnight
- This lecture
  - Single Cycle Processor
  - Multi-Cycle/Pipelined Processor

Recall: Clocking the Processor

- Fetch unit is involved in processing all instructions
  - Program counter (PC) and instruction memory
- Which of the units need a clock?
- What is being saved (latched) on the rising edge of the clock?
- The latched value remains there for an entire cycle

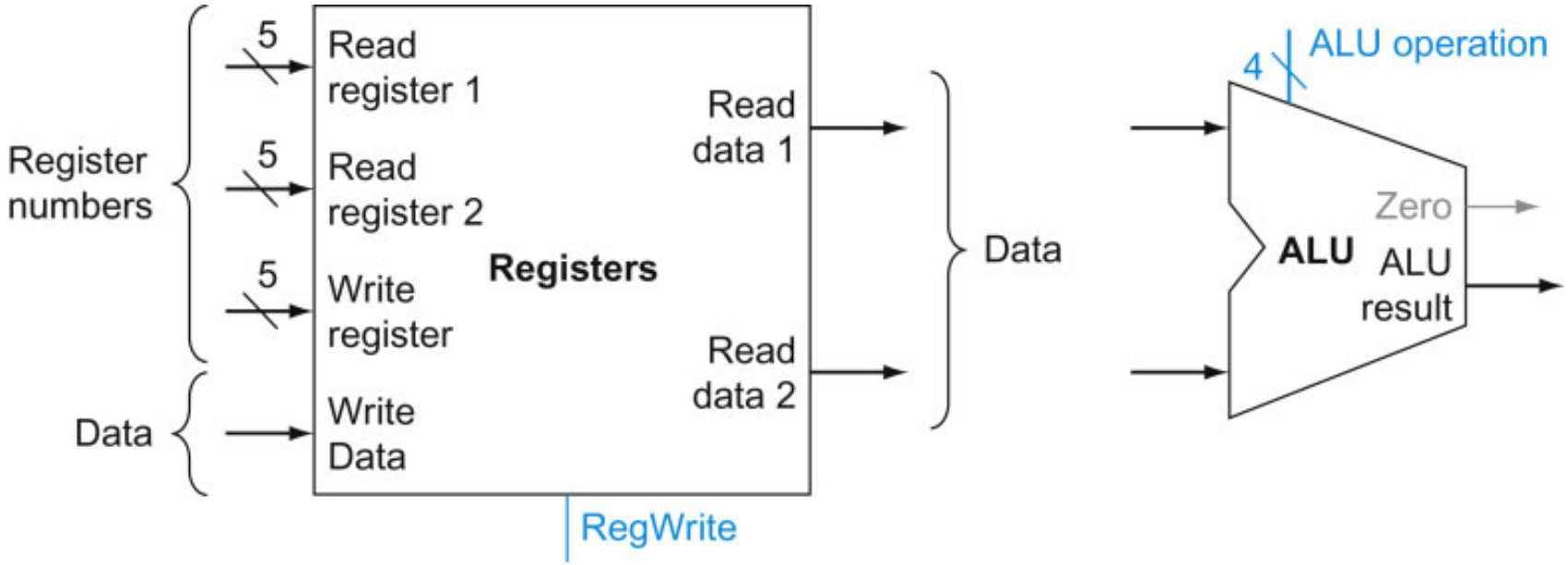


R-type Instructions

- Instructions of the form

  - Example: add $t1, $t2, $t3

- Registers and ALU



I-type Instructions

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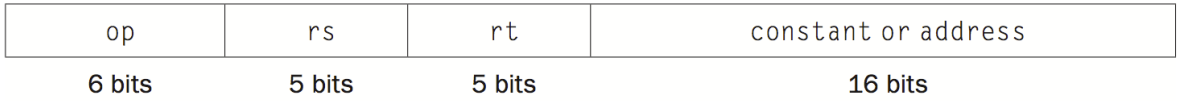
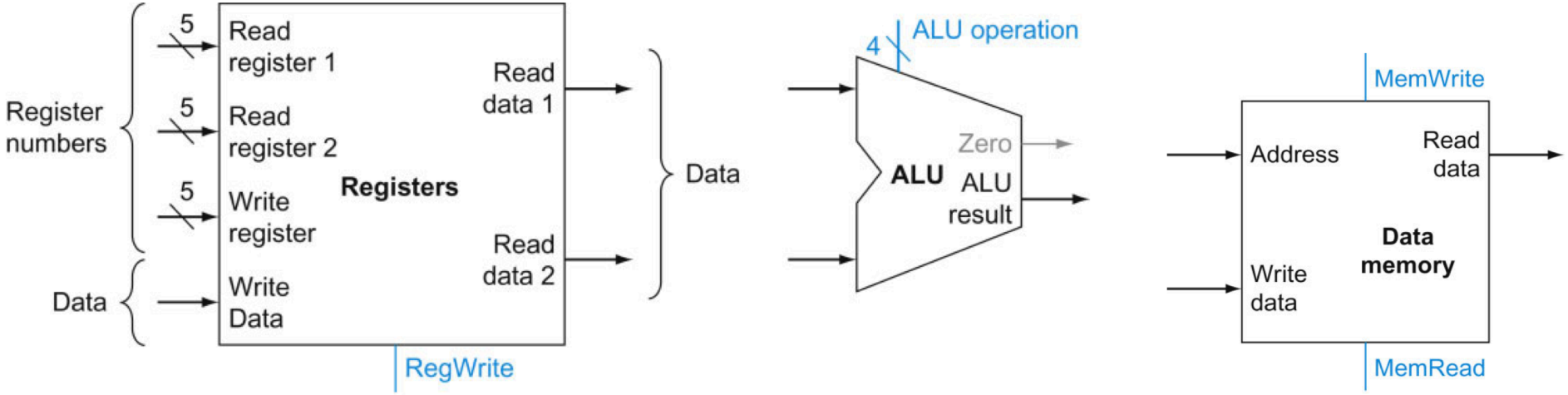


  - Examples: lw $t1, 8($t2) and sw $t1, 8($t2)
- Registers, ALU, and data memory
  - Where is the constant operand



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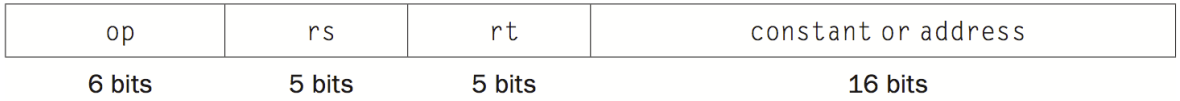

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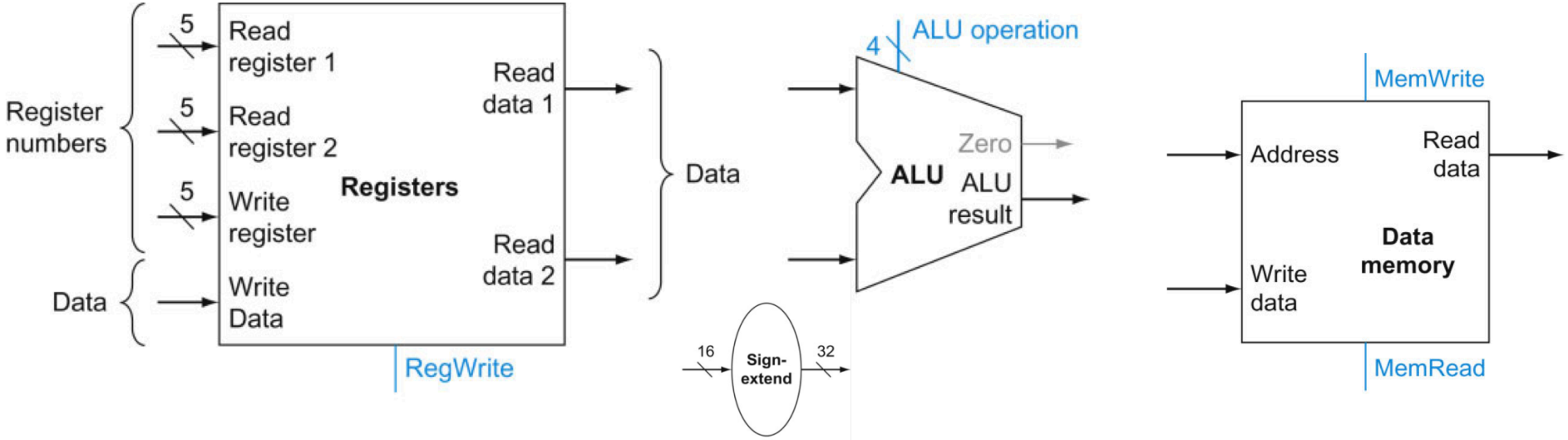
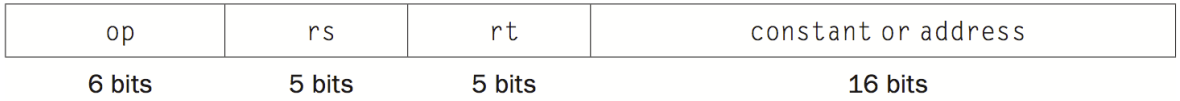
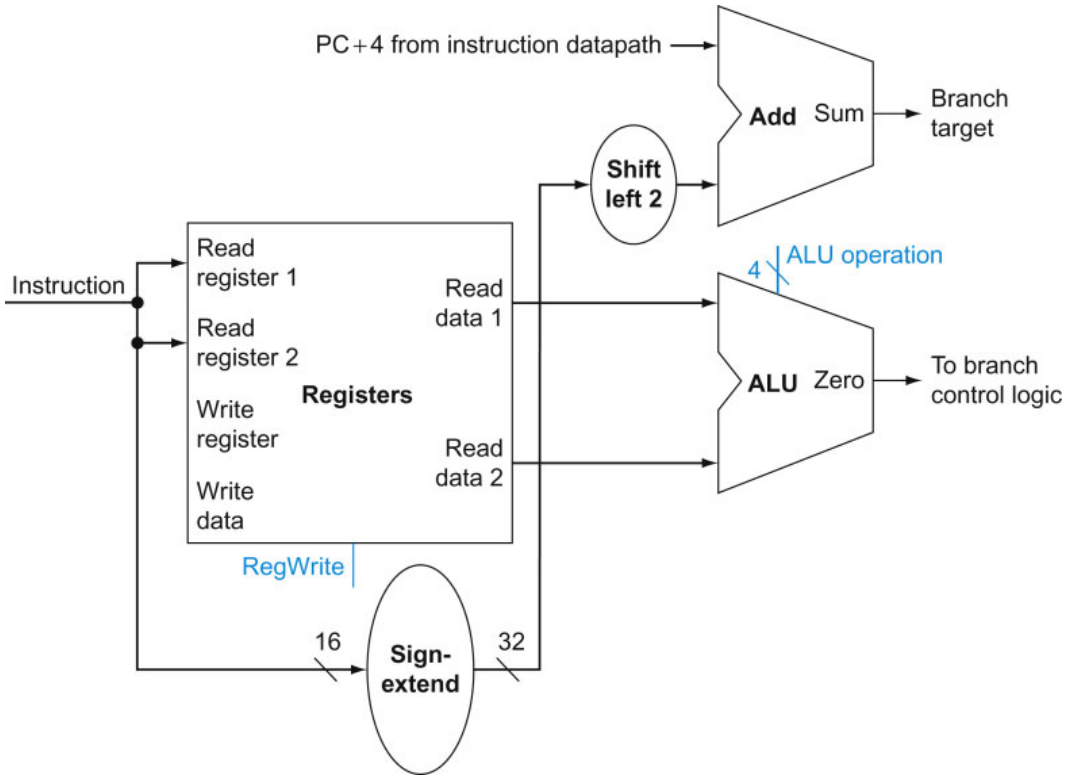


J-type Instructions

- Instructions of the form

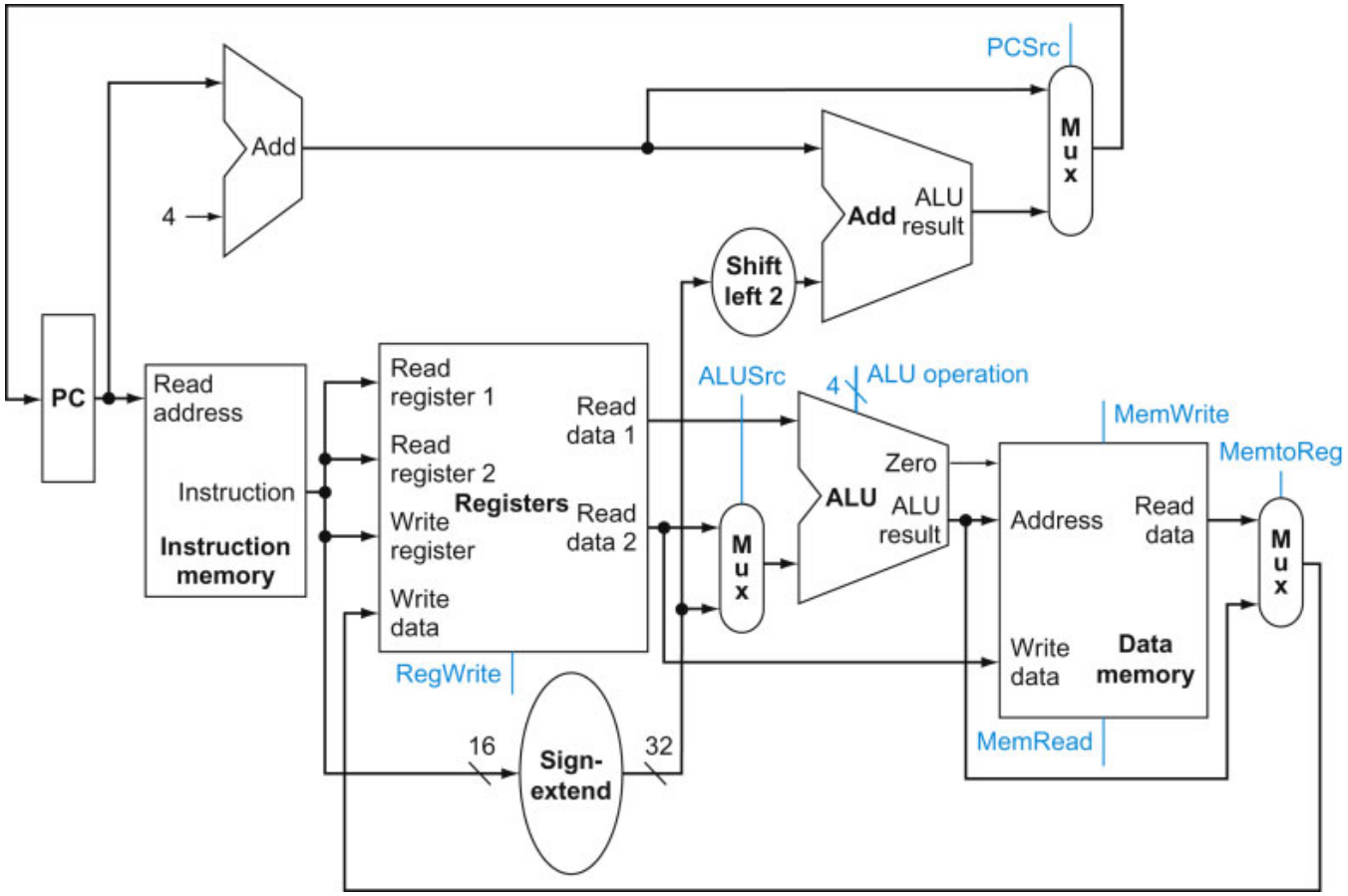


  - Example: beq $t1, $t2, offset



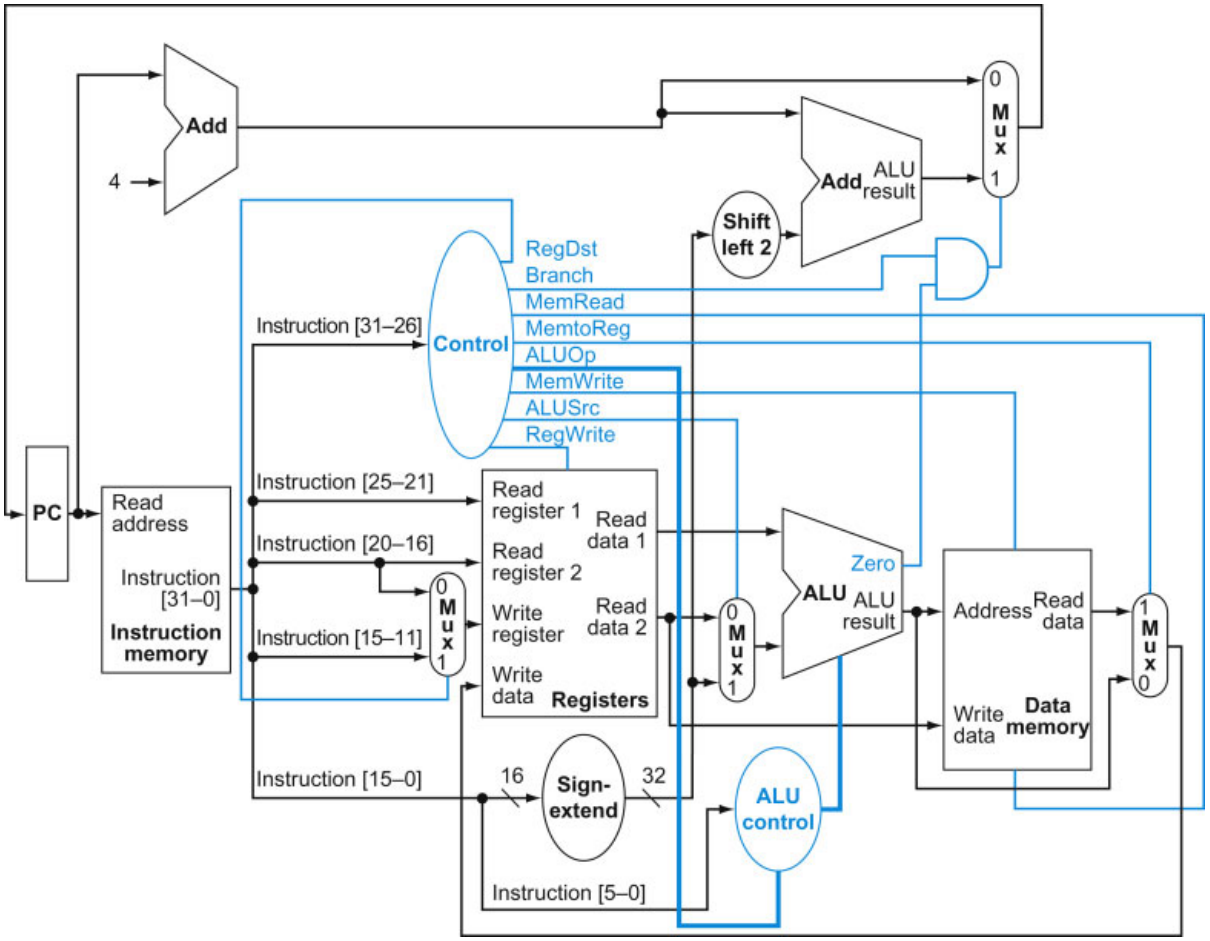
The Processor Datapath

- Control signals are generated per instruction



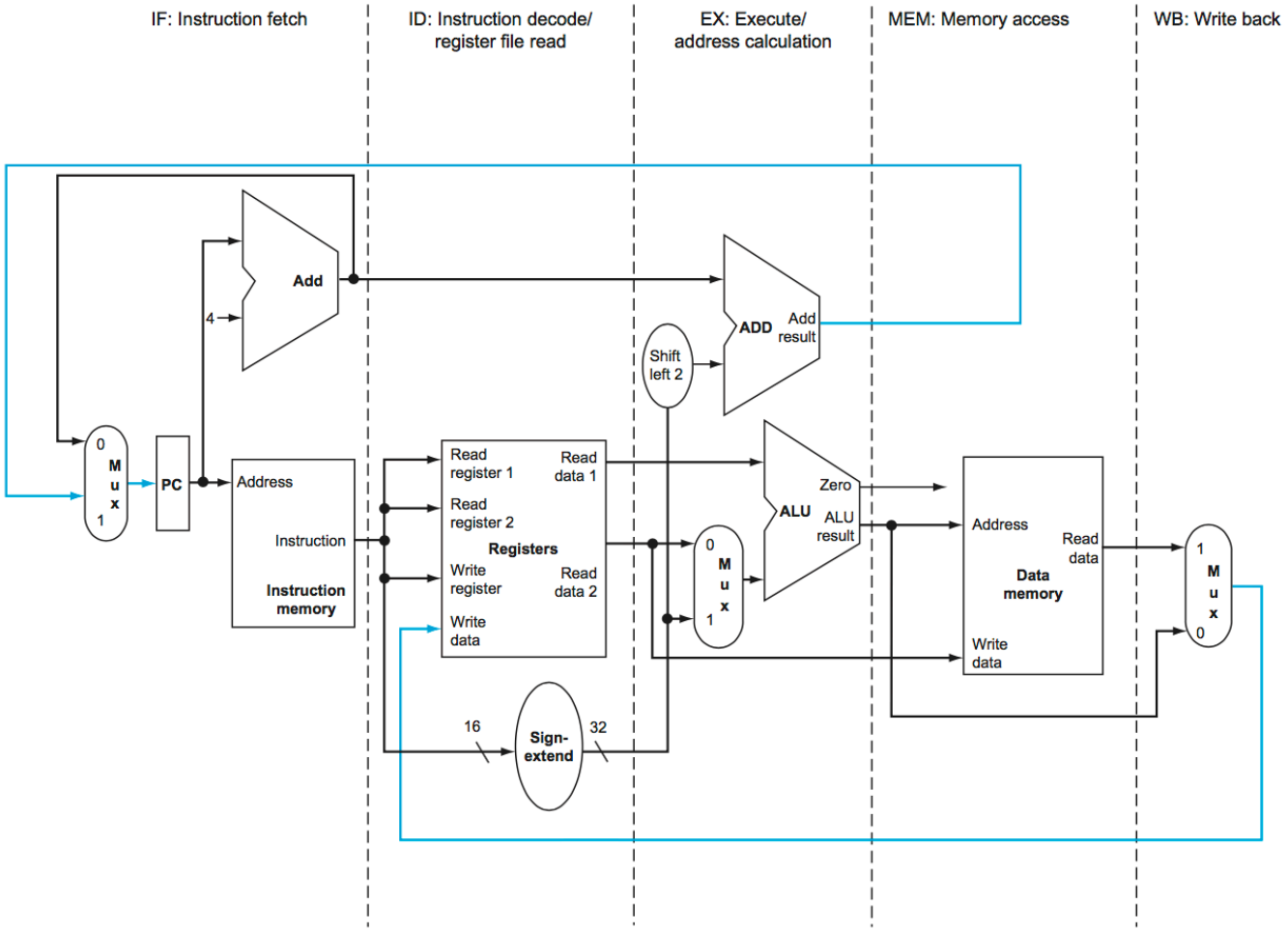
The Single Cycle MIPS Processor

- A new PC is locked at the beginning of each cycle



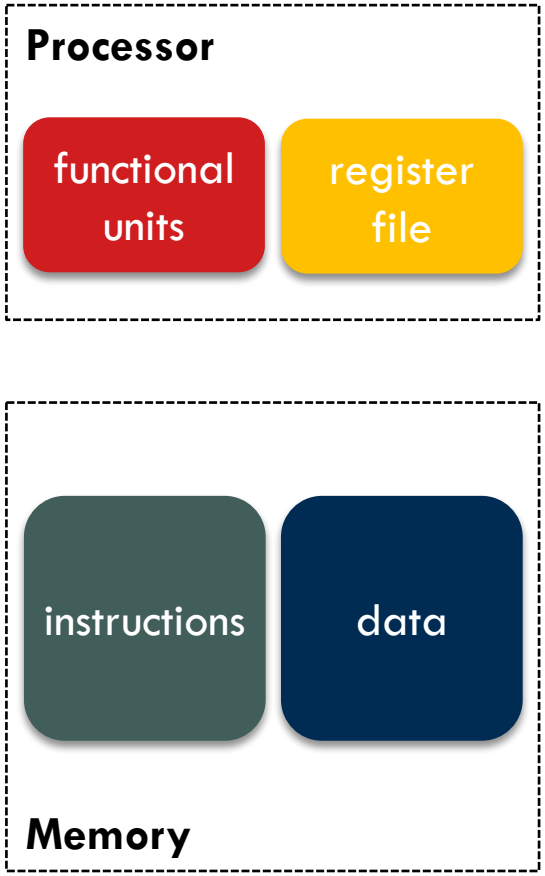
Processing Instructions

- A sequence of processing tasks per instruction



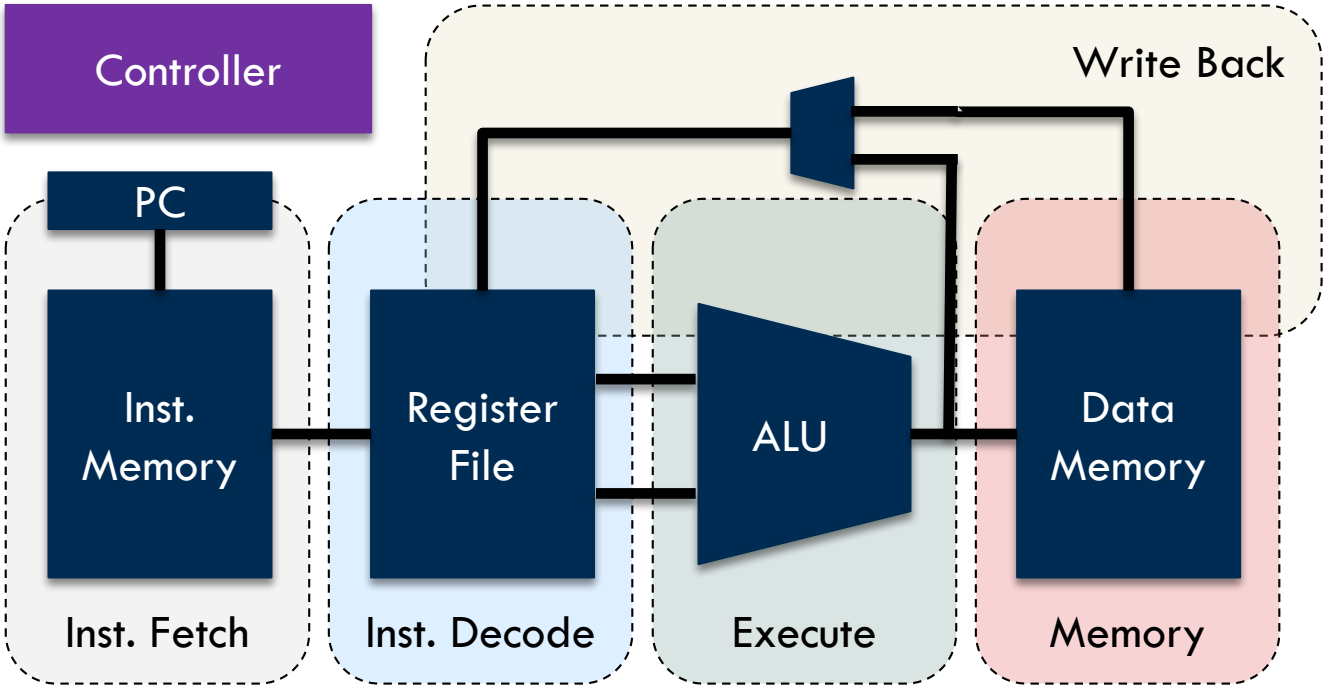
Processing Instructions

- Every RISC instruction may require multiple processing steps
  - Instruction Fetch (IF)
  - Instruction Decode (ID)
  - Register Read (RR)
    - All instructions?
  - Execute Instructions (EXE)
  - Memory Access (MEM)
    - All instructions?
  - Register Write Back (WB)



Single-cycle MIPS Architecture

- Example: simple MIPS architecture
  - Critical path includes all of the processing steps

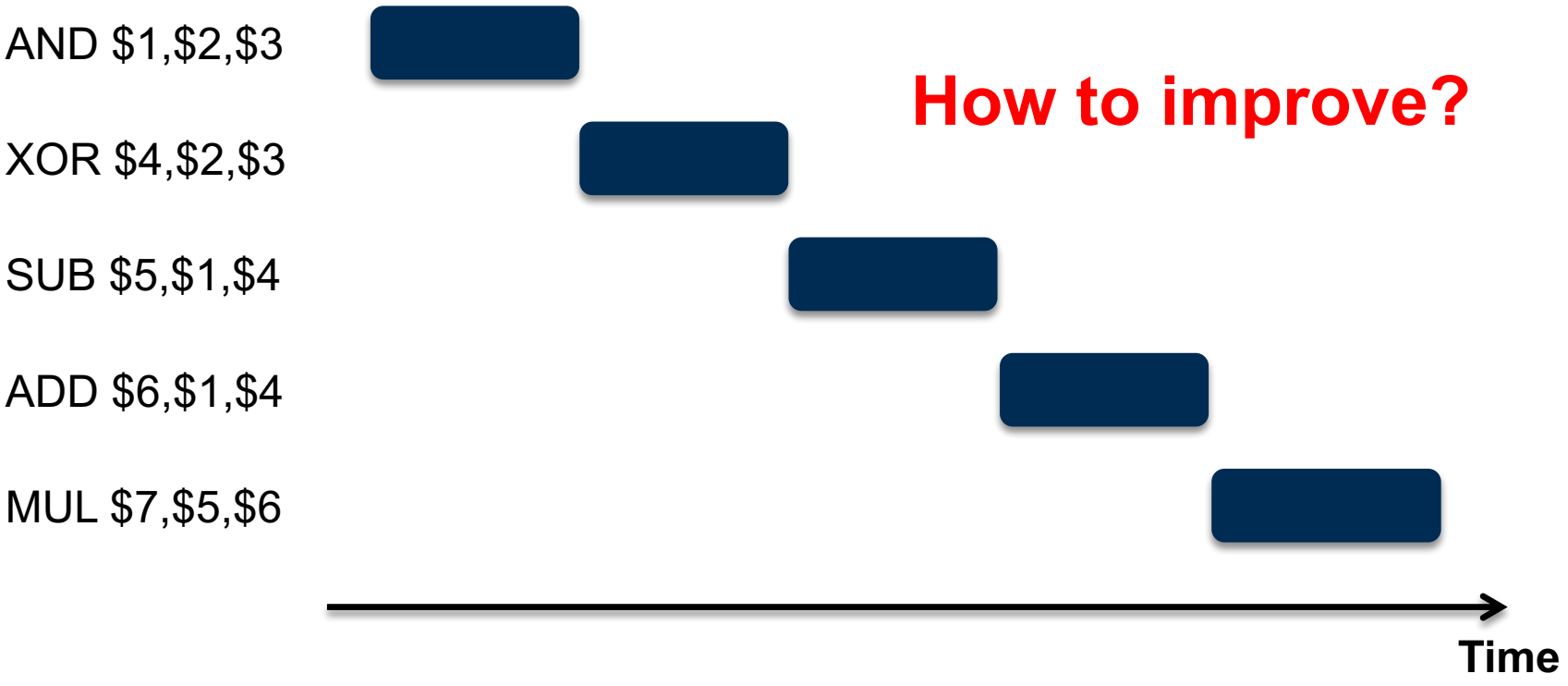


Single-cycle RISC Architecture

- Example program
  - CT=6ns; CPU Time = ?

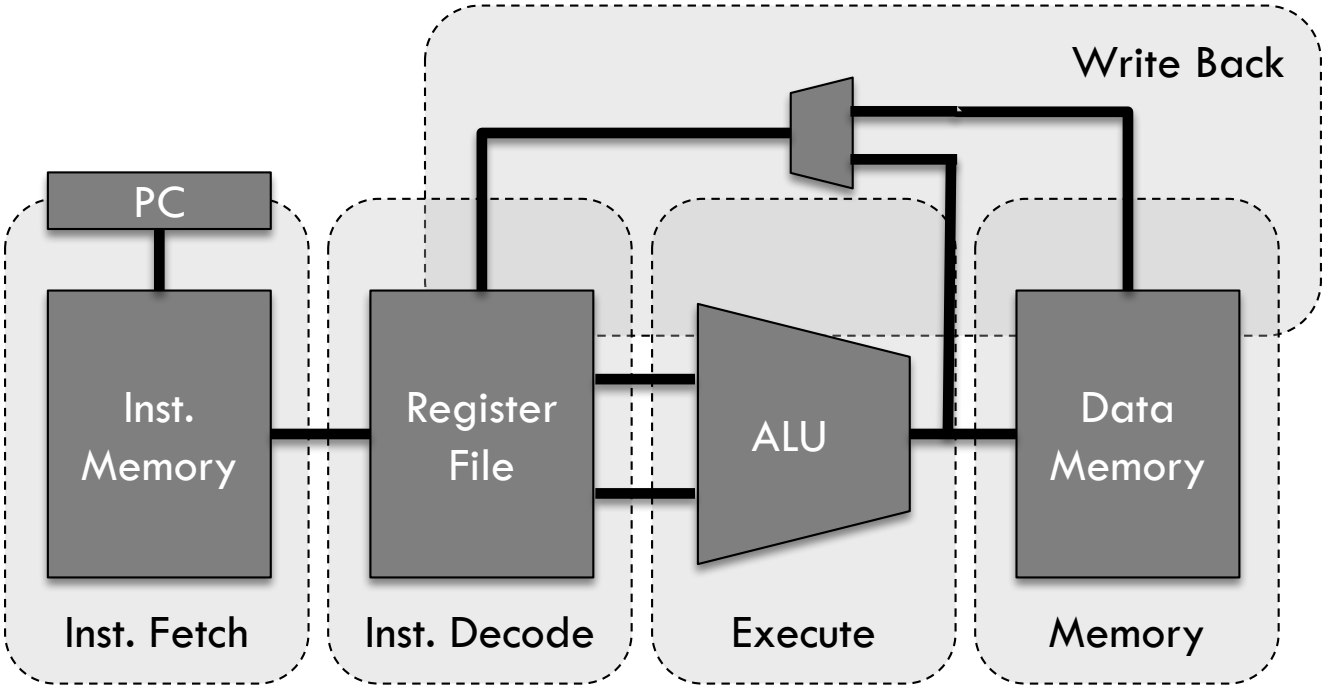
Single-cycle RISC Architecture

- Example program
  - CT=6ns; CPU Time = 5 x 6ns = 30ns



Reusing Idle Resources

- Each processing step finishes in a fraction of a cycle
  - Idle resources can be reused for processing next instructions



Pipelined Architecture

- Five stage pipeline
  - Critical path determines the cycle time