

# MAIN MEMORY SYSTEM

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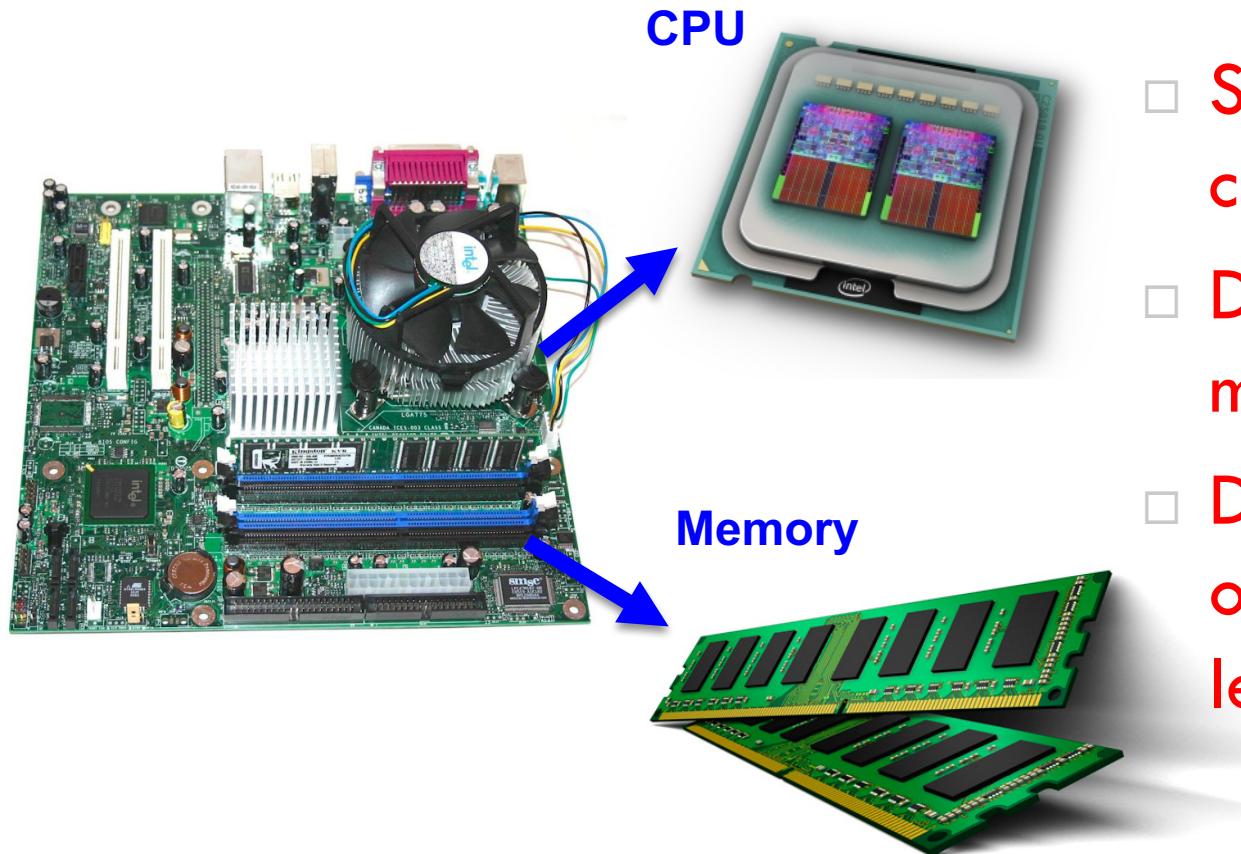
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# Overview

- Announcement
  - ▣ Homework 6 is due tonight 😊
  - ▣ Homework 7 will be released next week
- This and the following lectures
  - ▣ Dynamic random access memory (DRAM)
  - ▣ DRAM operations
  - ▣ Memory scheduling basics
  - ▣ Emerging memory technologies

# Computer System Overview

- DRAM technology is commonly used for main memory



- SRAM is used for caches
- DRAM is used for main memory
- DRAM is accessed on a TLB or last level cache miss

# Static vs. Dynamic RAM

## Static RAM (SRAM)

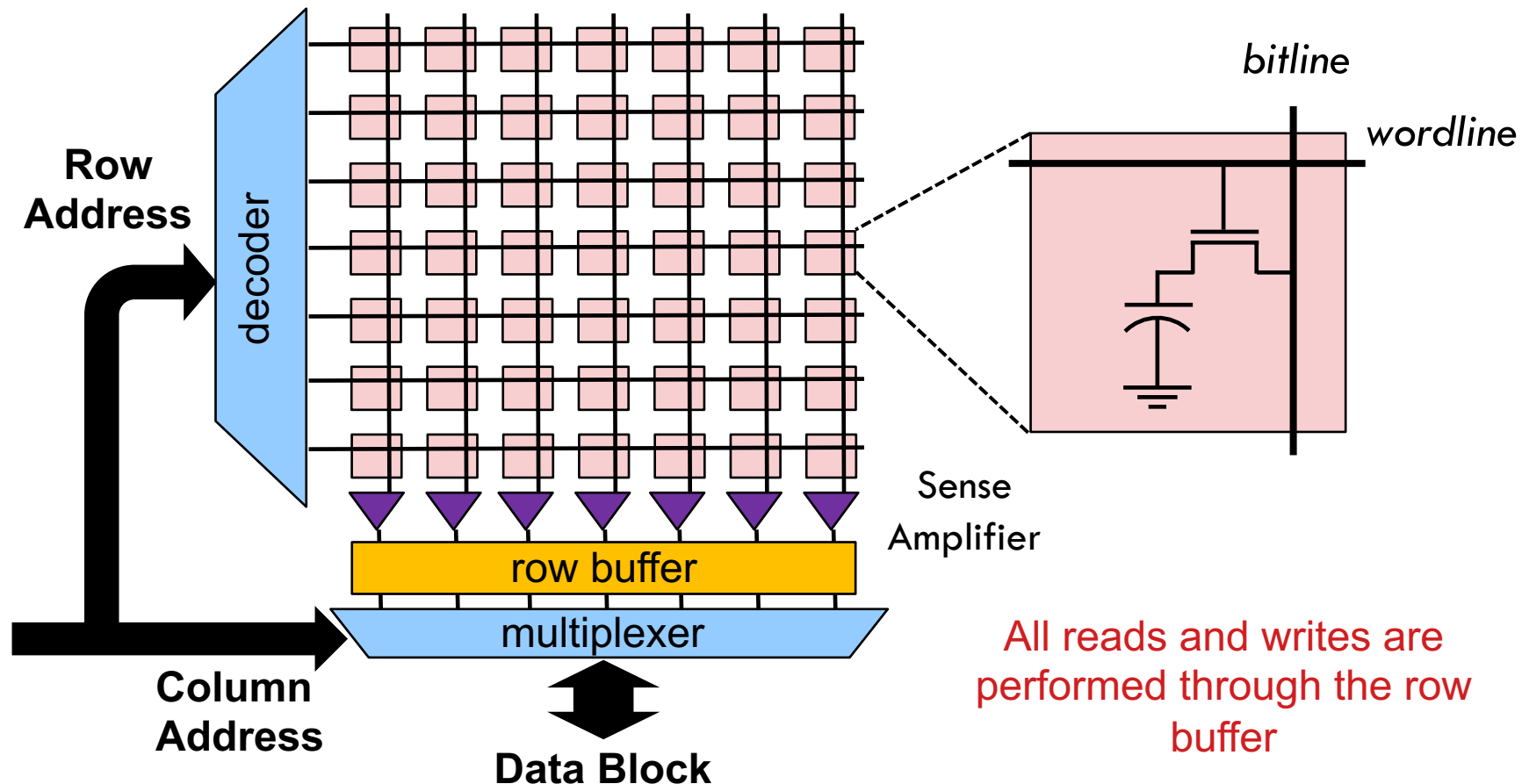
- Fast and leaky
  - ▣ 6 transistors per bit
  - ▣ Normal CMOS Tech.
- Static volatile
  - ▣ Retain data as long as powered on

## Dynamic RAM (DRAM)

- Dense and slow
  - ▣ 1 transistor per bit
  - ▣ Special DRAM process
- Dynamic volatile
  - ▣ Periodic refreshing is required to retain data

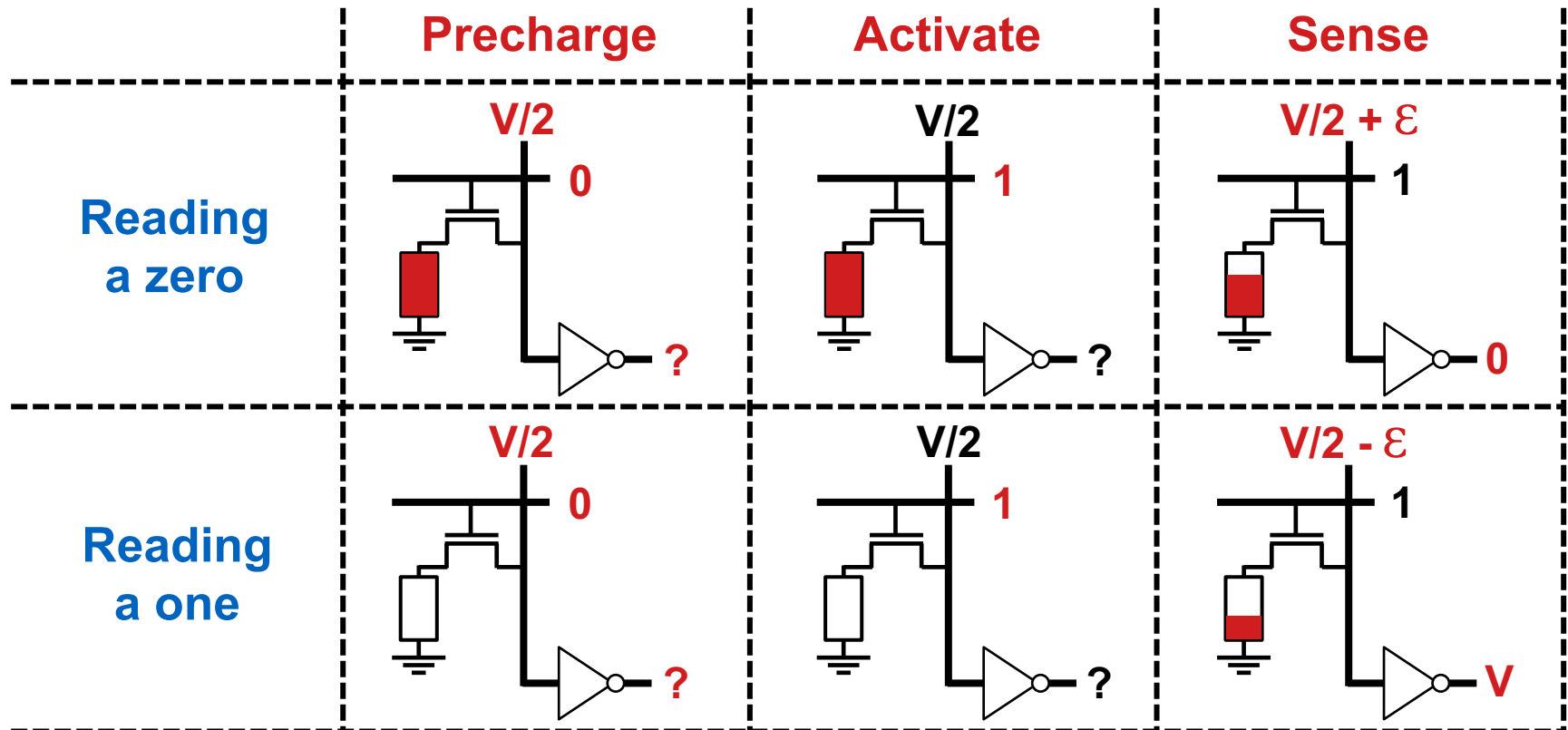
# DRAM Organization

- DRAM array is organized as *rows* × *columns*



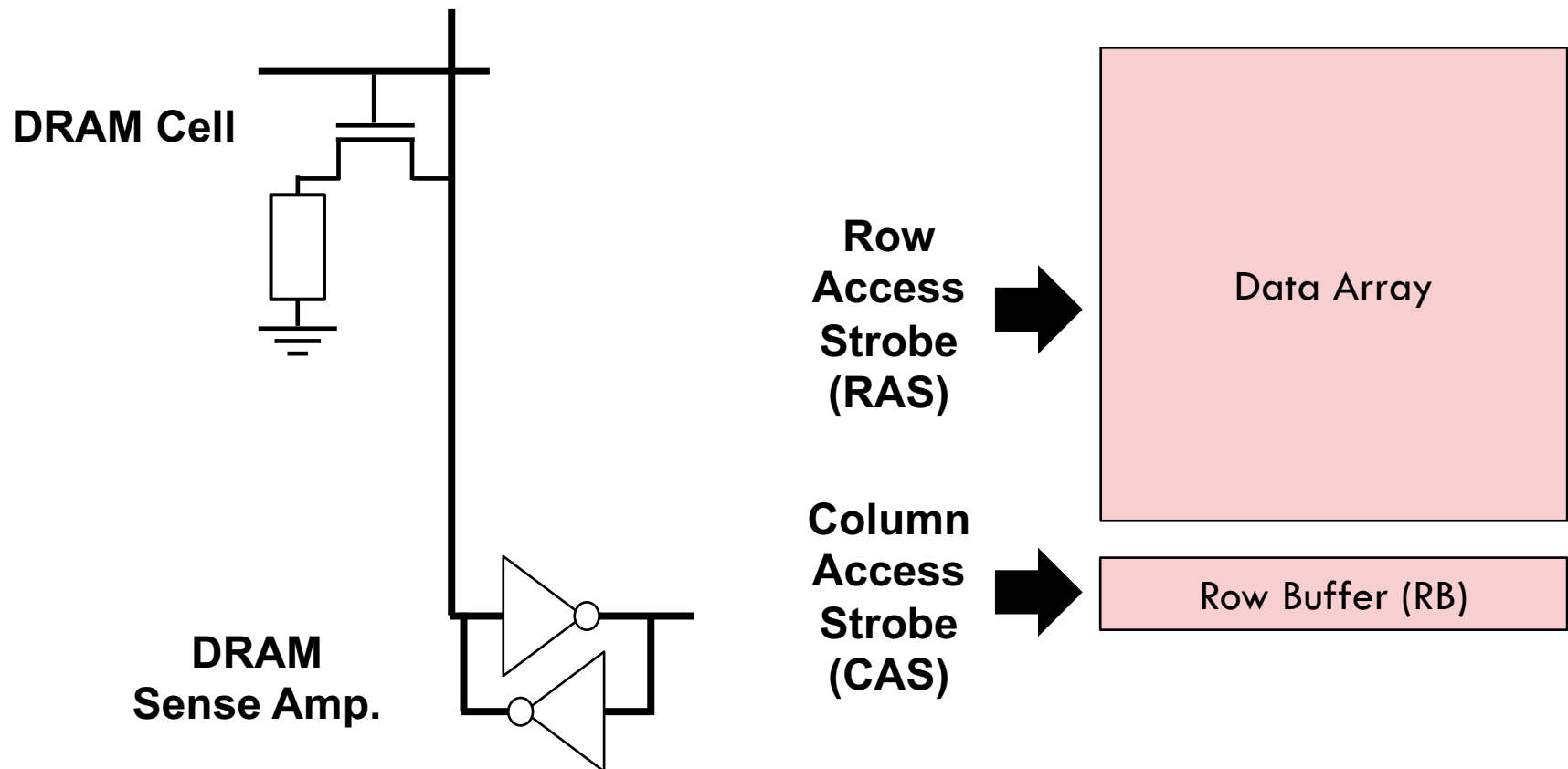
# Reading DRAM Cell

- DRAM read is destructive
  - ▣ After a read, contents of cells are destroyed



# DRAM Row Buffer

- All reads and writes are performed through RB



# DRAM Row Buffer

- Row buffer holds a single row of the array
  - ▣ A typical DRAM row (page) size is 8KB
- The entire row is moved to row buffer; but only a block is accessed each time
- Row buffer access possibilities
  - ▣ **Row buffer hit:** no need for a precharge or activate
    - ~20ns only for moving data between pins and RB
  - ▣ **Row buffer miss:** activate (and precharge) are needed
    - ~40ns for an empty row
    - ~60ns for on a row conflict



# DRAM Refresh

- Charge based memory cells may gradually lose their states due to current leakage
- DRAM requires the cells' contents to be read and written periodically
  - ▣ **Burst refresh:** refresh all of the cells each time
    - Simple control mechanism
  - ▣ **Distributed refresh:** a group of cells are refreshed
    - Avoid blocking memory for a long time

