

EMERGING MEMORY SYSTEMS

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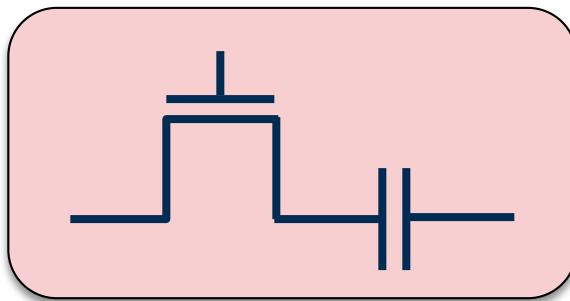
University of Utah

Overview

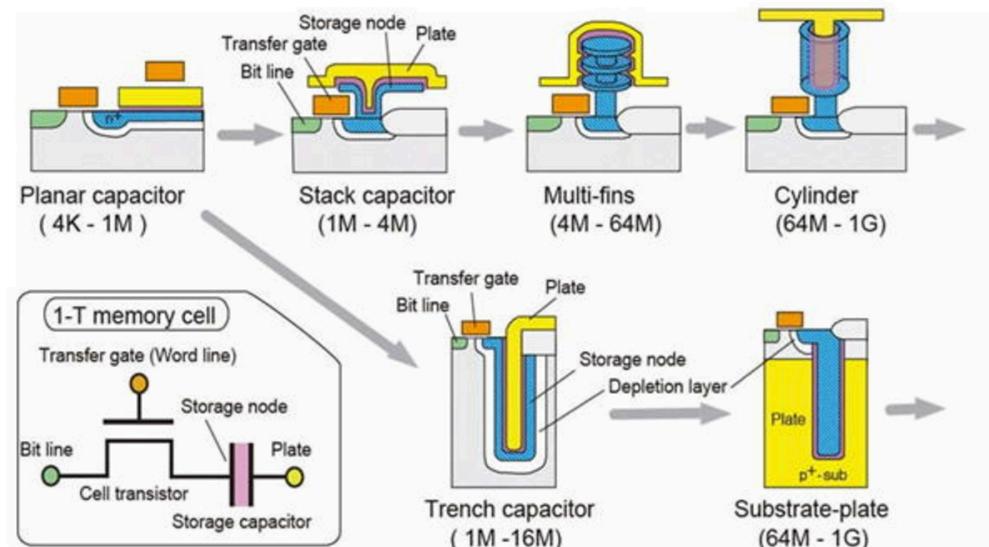
- Upcoming deadline
 - ▣ **March 8th: homework assignment is due**
- This lecture
 - ▣ DRAM technology scaling issues
 - ▣ Charge vs. phase based memory
 - ▣ Phase change memory

DRAM Cell Structure

- One-transistor, one-capacitor
 - ▣ Realizing the capacitor is challenging



- 1T-1C DRAM
- Charge based sensing
- Volatile

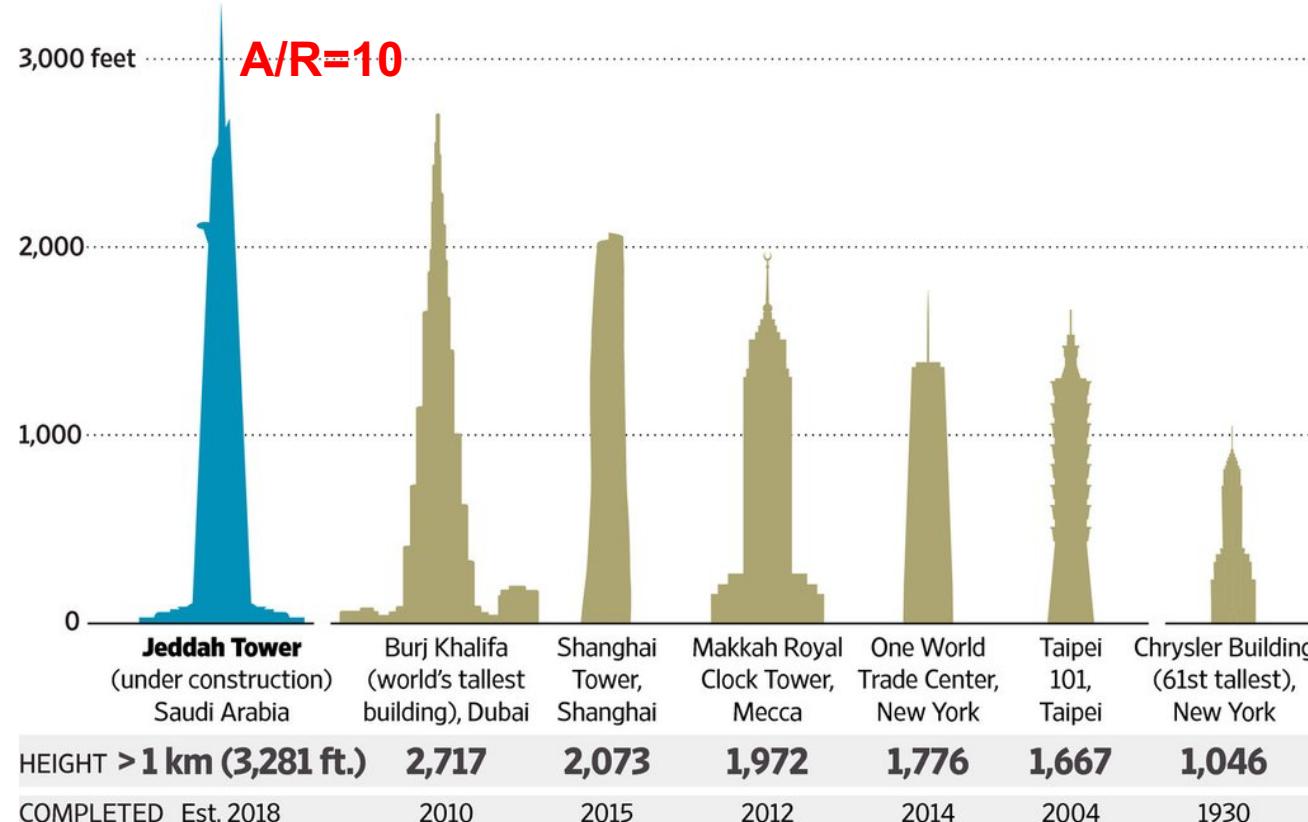


Memory Scaling in Jeopardy

Scaling of semiconductor memories greatly challenged beyond 20nm

The World's Tallest Buildings

A skyscraper being built in Jeddah aims for a record-breaking height that's expected to exceed 3,281 feet.



Note: Includes antennas Source: The Council on Tall Buildings and Urban Habitat

THE WALL STREET JOURNAL.

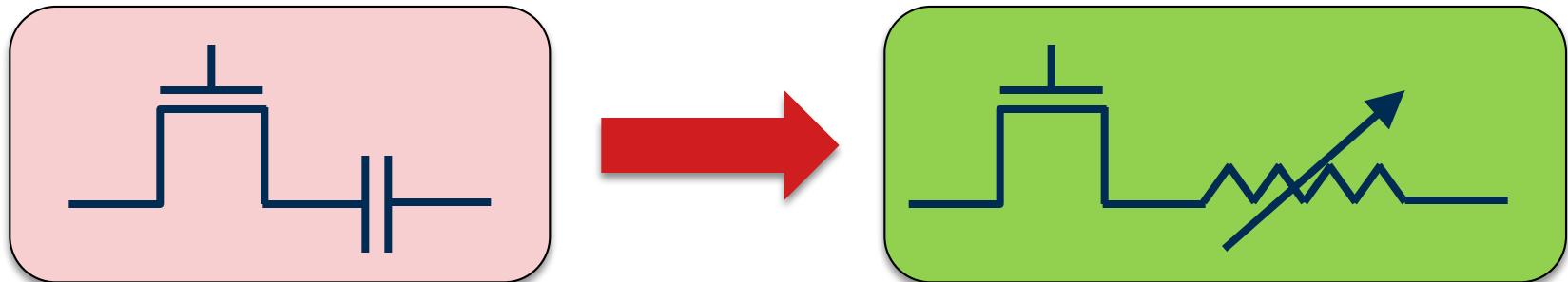
Addressing DRAM Issues

- Overcome DRAM shortcomings with
 - ▣ System-DRAM co-design
 - ▣ Novel DRAM architectures, interface, functions
 - ▣ Better waste management (efficient utilization)

- Key issues to tackle
 - ▣ Reduce refresh energy
 - ▣ Improve bandwidth and latency
 - ▣ Reduce waste
 - ▣ Enable reliability at low cost

Alternative to DRAM

- Key concept: replace DRAM cell capacitor with a programmable resistor



- 1T-1C DRAM
- Charge based sensing
- Volatile
- 1T-1R STT-MRAM, PCM, RRAM
- Resistance based sensing
- Non-volatile

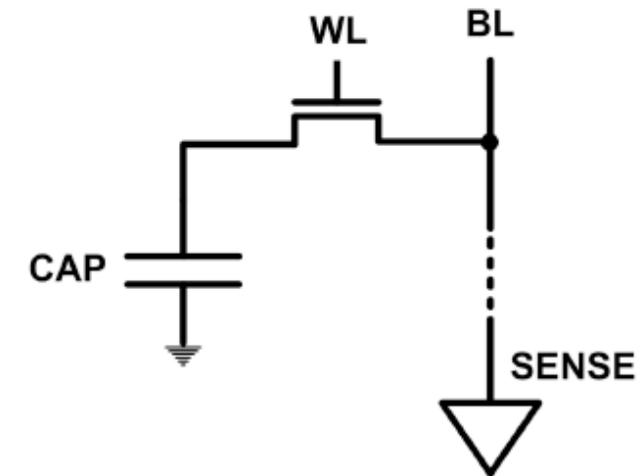
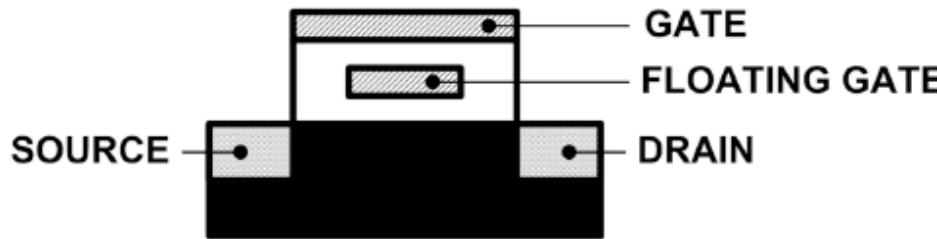
Charge vs. Phase

- Charge Memory (e.g., DRAM, Flash)
 - ▣ Write data by capturing charge Q
 - ▣ Read data by detecting voltage V

- Resistive Memory (e.g., PCM, STT-MRAM, memristors)
 - ▣ Write data by pulsing current dQ/dt
 - ▣ Read data by detecting resistance R

Limits of Charge Based Memory

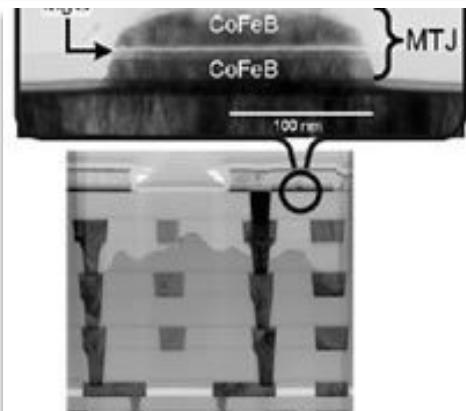
- Difficult charge placement and control
 - ▣ Flash: floating gate charge
 - ▣ DRAM: capacitor charge, transistor leakage
- Reliable sensing becomes difficult as charge storage unit size reduces



[slide ref: Mutlu]

Leading Contenders

STT-MRAM



[Halupka, et al. ISSCC'10]

- Limited to single-level cell
- 3D un-stackable
- + High endurance ($\sim 10^{15}$)
- + $\sim 4\text{ns}$ switching time
- + $\sim 50\mu\text{W}$ switching power

PCM-RAM

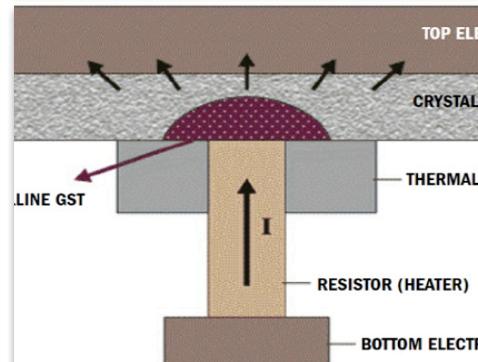
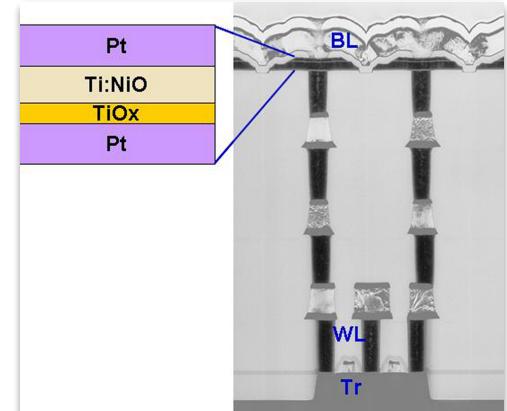


Figure 1. Typical PCM device structure.

[Pronin. EETime'13]

- + Multi-level cell capable
- + 4F^2 3D-stackable cell
- Endurance: $\sim 10^9$ writes
- $\sim 100\text{ns}$ switching time
- $\sim 300\mu\text{W}$ switching power

R-RAM

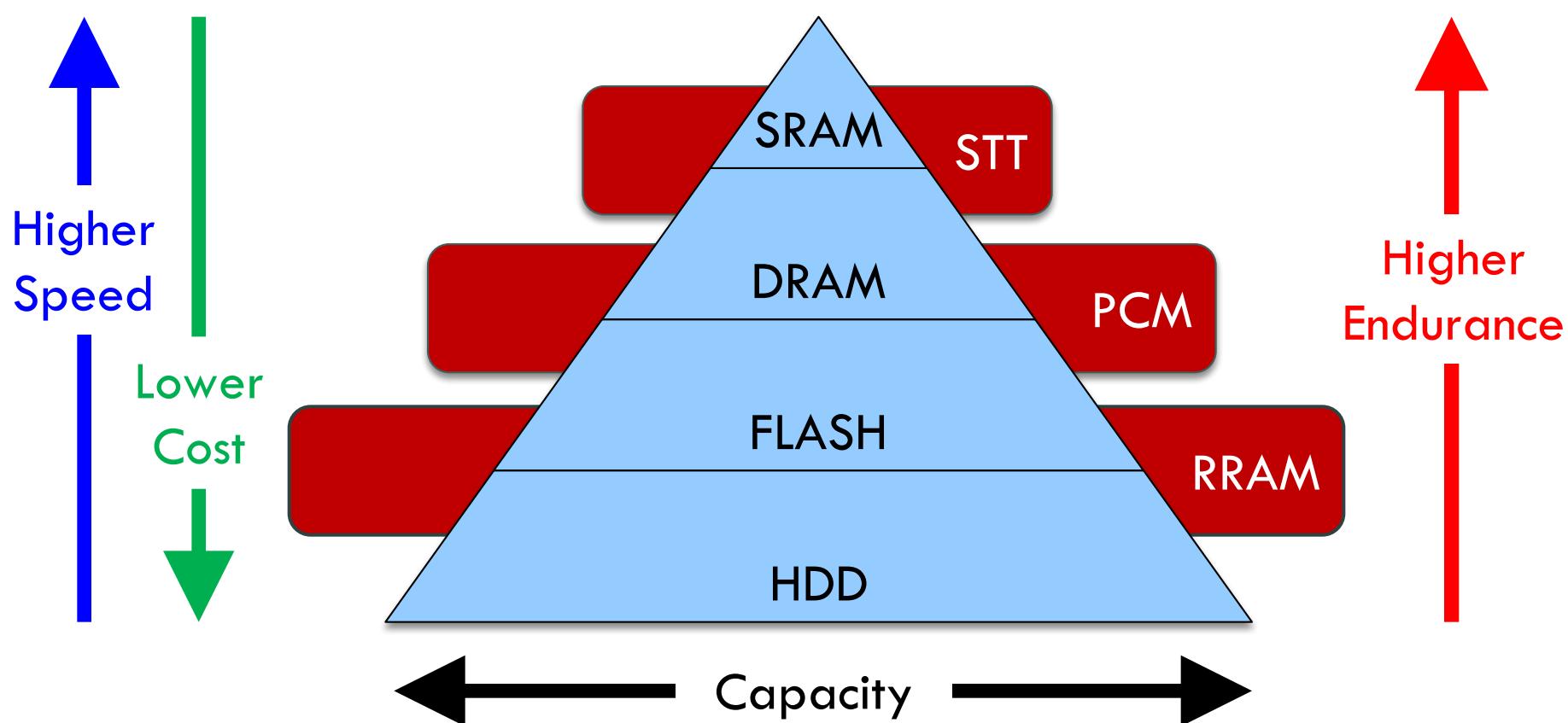


[Henderson. InfoTracks'11]

- + Multi-level cell capable
- + 4F^2 3D-stackable cell
- Endurance: $10^6 \sim 10^{12}$ writes
- + $\sim 5\text{ns}$ switching time
- + $\sim 50\mu\text{W}$ switching power

[ITRS'13]

Positioning of New Memories

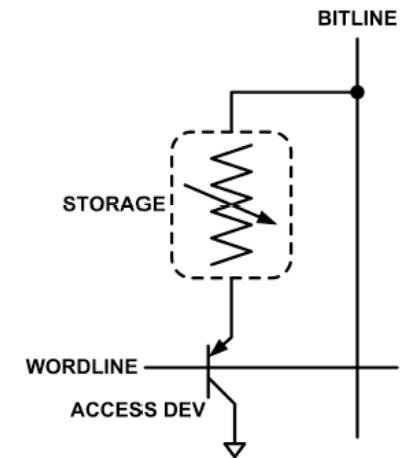
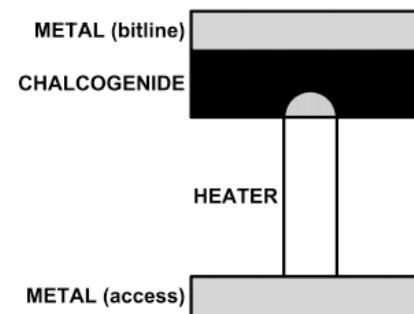
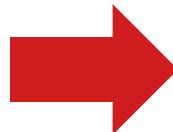


Phase Change Memory

- Phase change material (chalcogenide glass) exists in two states:
 - **Amorphous**: Low optical reflexivity, high electrical resistivity
 - **Crystalline**: High optical reflexivity, low electrical resistivity



Amorphous chalcogenide materials



Phase Change Memory

- Write: change phase via current injection
 - ▣ SET: sustained current to heat cell above T_{cryst}
 - ▣ RESET: cell heated above T_{melt} and quenched
- Read: detect phase via material resistance
 - ▣ amorphous/crystalline

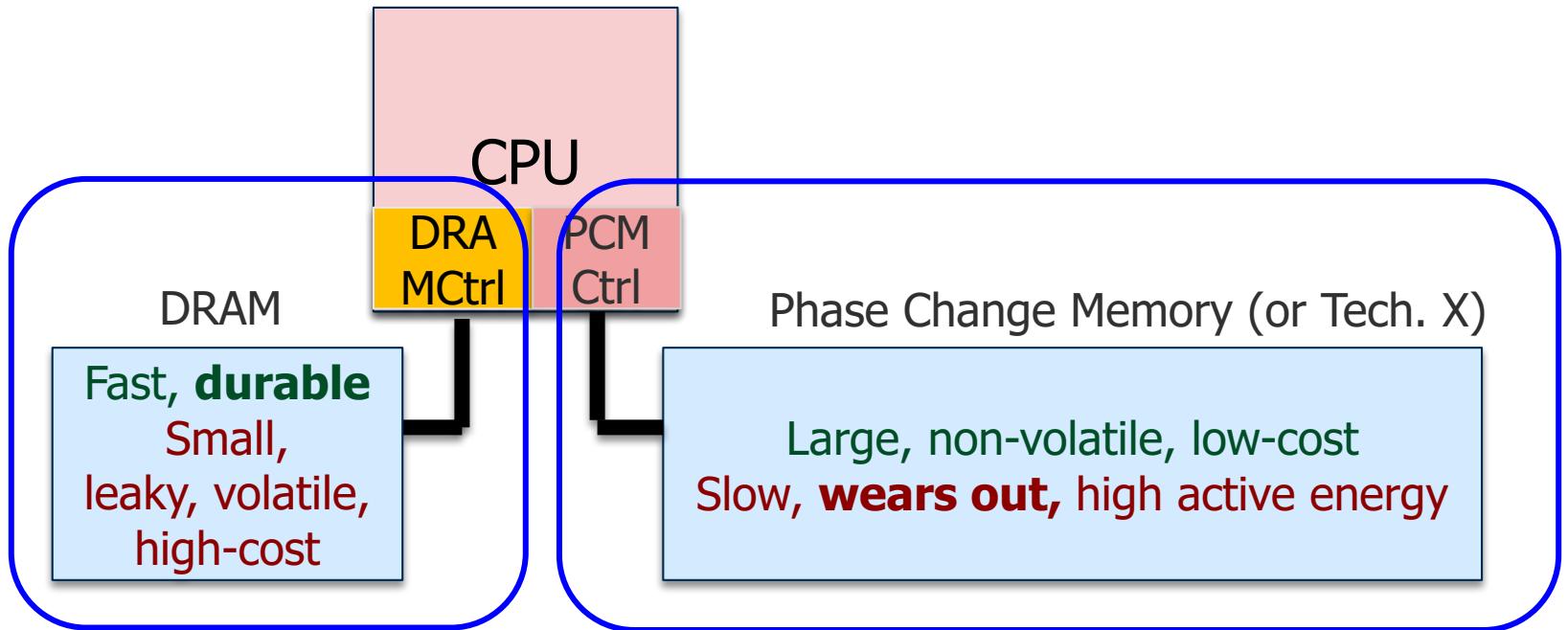


[slide ref: Mutlu]

PCM in Memory Systems

- Some emerging resistive memory technologies seem more scalable than DRAM (and they are non-volatile)
 - ▣ Example: Phase Change Memory
 - ▣ Expected to scale to 9nm (2022 [ITRS])
 - ▣ Expected to be denser than DRAM: can store multiple bits/cell
- But, emerging technologies have shortcomings as well
- Can they be enabled to replace/augment/surpass DRAM?

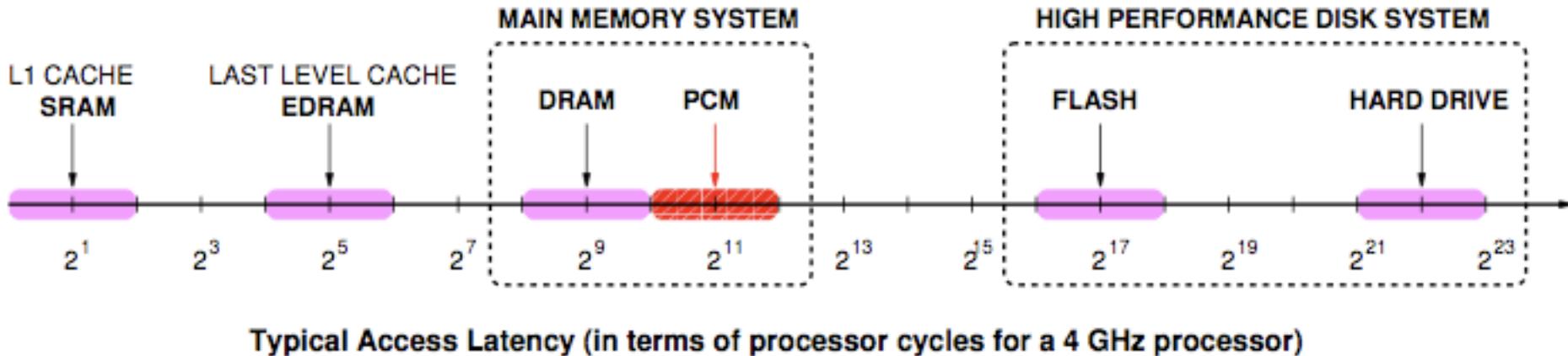
Hybrid Memory Systems



Hardware/software manage data allocation and movement
to achieve the best of multiple technologies

PCM Latency

- Latency comparable to, but slower than DRAM
 - Read Latency: 50ns (4x DRAM, 10-3x NAND Flash)
 - Write Latency: 150ns (12x DRAM)
 - Write Bandwidth: 5-10 MB/s (0.1x DRAM, 1x NAND Flash)



[slide ref: Mutlu]