Comparing the SFDR Performance of LUT size and DDS Spurious Improvement Algorithms

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***Abstract*—With the performance increase of high frequency digital to analog converters, digital synthesizers continue to replace traditional analog oscillator circuits. Traditional Direct Digital Synthesizers (DDS) use lookup tables to convert phase to sinusoidal amplitude. The phase truncation occurring in this architecture seriously limits the spectral performance of the generated signal in the form of spurs. This work uses MATLAB/Simulink to reproduce the frequency errors widely discussed in literature. The simulation framework is then used to apply various amplitude treatement algorithms to correct the signal and improve the spurious performance. Furthermore, the algorithms are compared against each other to find the best method in terms of spurious free dynamic range (SFDR), consumed hardware resources on FPGA and latency. The proposed design includes an 8 channel polyphase DDS with linear interpolation correction and an expected SFDR of below -105 dBc.**

***Index Terms*—Direct Digital Synthesis, Bit True Simulation, Spurious Performance Analysis, High Frequency Signal Generation**

I. INTRODUCTION

USING digital signal processing to synthesize analog waveforms is a well established method generate a sinewaves of variable frequency. A commonly used architecture is that of the Direct Digital Synthesis (DDS). One major disadvantage of a DDS system is that a truncation of the phase accumulator needs to be implemented to keep the memory size of the sine look up table (LUT) reasonably small. This truncation leads to phase errors and inevitably truncation spurs in the spectral domain. Many signal processing algorithms have been proposed in the past. Their goal is to minimize truncation spurs while maintaining small LUT sizes.

However, there appears to be no general overview and comparison of the algorithms that anwers the following question quickly: What combination of LUT size and correction algorithm do I need to achieve a signal with x dB spurious free dynamic range?

This work aims to build a bit-true simulation model in Python to simulate the traditional DDS as well as several spurious correction algorithms in order to compare them in the spectral domain. Not only are the effects of phase truncation and quantization visible, but all the DSP calculations are performed using fixed point arithmetic. The example chosen are the DSP48E2 Slices available in Xilinx FPGA, capable of working with a minimum of 18 bits precision.

Manuscript received Month xx, 2023.

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A. Results

II. CONCLUSION

ACKNOWLEDGMENT

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