

## Industry-Standard Dual Operational Amplifiers

### 1 Features

- Wide Supply Range of 3 V to 36 V (B Version)
- Supply-Current of 300  $\mu$ A (B Version, Typical)
- Unity-Gain Bandwidth of 1.2 MHz (B Version)
- Common-Mode Input Voltage Range Includes Ground, Enabling Direct Sensing Near Ground
- Low Input Offset Voltage of 3 mV at 25°C (A and B Versions, Maximum)
- Internal RF and EMI Filter (B Version)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

### 2 Applications

- Merchant Network and Server Power Supply Units
- Multi-Function Printers
- Power Supplies and Mobile Chargers
- Motor Control: AC Induction, Brushed DC, Brushless DC, High-Voltage, Low-Voltage, Permanent Magnet, and Stepper Motor
- Desktop PC and Motherboard
- Indoor and Outdoor Air Conditioners
- Washers, Dryers, and Refrigerators
- AC Inverters, String Inverters, Central Inverters, and Voltage Frequency Drives
- Uninterruptible Power Supplies
- Programmable Logic Controllers
- Electronic Point-of-Sale Systems

### 3 Description

The LM358B and LM2904B devices are the next-generation versions of the industry-standard LM358 and LM2904 devices, which include two high-voltage (36-V) operational amplifiers (op amps). These devices provide outstanding value for cost-sensitive applications, with features including low offset (300  $\mu$ V, typical), common-mode input range to ground, and high differential input voltage capability.

The LM358B and LM2904B devices simplify circuit design with enhanced features such as unity-gain stability, lower offset voltage of 3 mV (maximum at room temperature), and lower quiescent current of 300  $\mu$ A (typical). High ESD (2 kV, HBM) and integrated EMI and RF filters enable the LM358B and LM2904B devices to be used in the most rugged, environmentally challenging applications.

The LM358B and LM2904B devices are available in micro-size packages, such as TSOT-8 and WSON, as well as industry standard packages, including SOIC, TSSOP, and VSSOP.

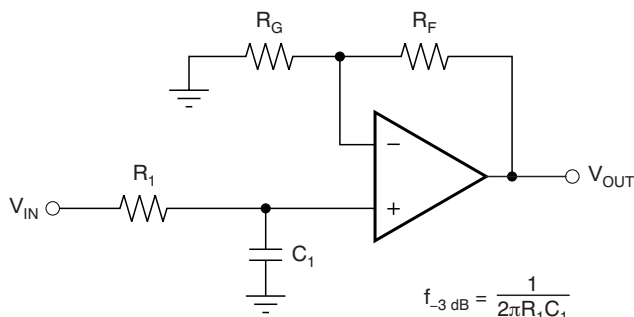
**Device Information<sup>(1)</sup>**

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM358B <sup>(2)</sup> , LM2904B <sup>(2)</sup> , LM358, LM358A, LM2904, LM2904V, LM258, LM258A	SOIC (8)	4.90 mm × 3.90 mm
LM358, LM358A, LM2904, LM2490V	TSSOP (8)	3.00 mm × 4.40 mm
LM358, LM358A, LM2904, LM2904V, LM258, LM258A	VSSOP (8)	3.00 mm × 3.00 mm
LM358, LM2904	SO (8)	5.20 mm × 5.30 mm
LM358, LM2904, LM358A, LM258, LM258A	PDIP (8)	9.81 mm × 6.35 mm
LM158, LM158A	CDIP (8)	9.60 mm × 6.67 mm
LM158, LM158A	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Package is for preview only

**Single-Pole, Low-Pass Filter**



$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1 C_1}\right)$$



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision U (January 2017) to Revision V	Page
• Changed the data sheet title .....	1
• Changed first four items in the <i>Features</i> section .....	1
• Changed the first item in the Applications section and added four new items .....	1
• Changed voltage values in the first paragraph of the <i>Description</i> section .....	1
• Changed text in the second paragraph of the <i>Description</i> section .....	1
• Added devices LM358B and LM2904B to data sheet .....	1
• Changed the first three rows of the <i>Device Information</i> table and added a cross-referenced note for PREVIEW-status devices .....	1
• Added <i>Device Comparison</i> table .....	4
• Added a table note to the <i>Pin Functions</i> table .....	5
• Changed "free-air temperature" to "ambient temperature" in the <i>Absolute Maximum Ratings</i> condition statement .....	6
• Changed all entries in the <i>Absolute Maximum Ratings</i> table except $T_J$ and $T_{stg}$ .....	6
• Deleted lead temperature and case temperature from <i>Absolute Maximum Ratings</i> .....	6
• Changed device listings and their voltage values in the <i>ESD Ratings</i> table .....	6
• Changed "free-air temperature" to "ambient temperature" in the <i>Recommended Operating Conditions</i> condition statement .....	7
• Changed table entries for all parameters in the <i>Recommended Operating Conditions</i> table .....	7
• Added rows to the Thermal Information table, and a table note regarding device-package combinations .....	7
• Added two Electrical Characteristics tables with five additional devices, and redistributed the seven original devices differently among the tables .....	8
• Deleted the <i>Operating Conditions</i> table .....	13
• Added a condition statement to the <i>Typical Characteristics</i> section .....	14
• Changed specific voltages to a <i>Recommended Operating Conditions</i> reference .....	17

## Revision History (continued)

• Changed unity-gain bandwidth from 0.7 MHz for all devices to 1.2 MHz for B-version devices.....	18
• Changed slew rate from 3 V/μs for all devices to 0.5 V/μs for B-version devices.....	18
• Changed the <a href="#">Input Common Mode Range</a> section in multiple places throughout.....	18
• Changed $V_{CC}$ to $V_S$ in the <a href="#">Application Information</a> section .....	19
• Subscripted the suffixes from $R_i$ and $R_F$ .....	19
• Changed <i>Operational Amplifier Board Layout for Noninverting Configuration</i> with an image that includes a dual op amp	21
• Added Preview designation to the LM358B and LM2904B devices in <a href="#">Table 1</a> .....	22

## Changes from Revision T (April 2015) to Revision U Page

• Changed data sheet title.....	1
• Added <i>Receiving Notification of Documentation Updates</i> section and <i>Community Resources</i> section .....	22

## Changes from Revision S (January 2014) to Revision T Page

• Added <i>Applications</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
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## Changes from Revision R (July 2010) to Revision S Page

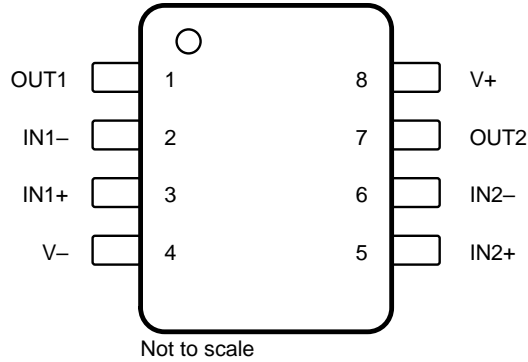
• Converted this data sheet from the QS format to DocZone using the PDF on the web .....	1
• Deleted <i>Ordering Information</i> table .....	1
• Updated <i>Features</i> to include Military Disclaimer .....	1
• Added Typical Characteristics section.....	14
• Added ESD warning .....	23

## 5 Device Comparison Table

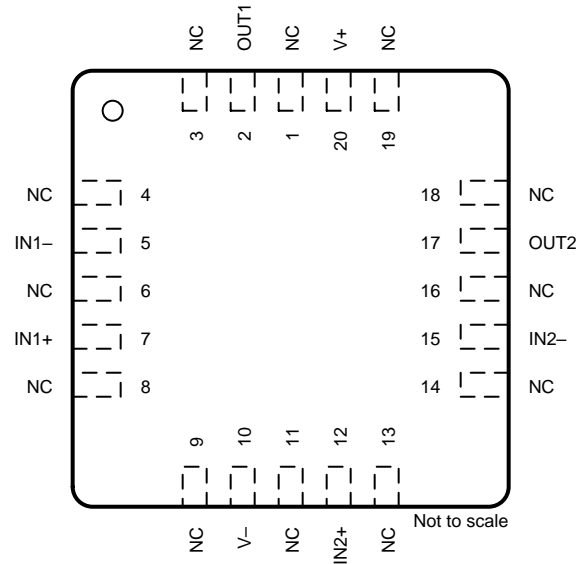
PART NUMBER	SUPPLY VOLTAGE	TEMPERATURE RANGE	V <sub>OS</sub> (MAXIMUM AT 25°C)	I <sub>Q</sub> / CH (TYPICAL AT 25°C)	INTEGRATED EMI FILTER	PACKAGE
LM358B	3 V–36 V	–40°C to 85°C	3 mV	300 µA	Yes	D, PW
LM2904B	3 V–36 V	–40°C to 125°C	3 mV	300 µA	Yes	D, PW
LM358	3 V–32 V	0°C to 70°C	7 mV	350 µA	No	D, PW, DGK, P, PS
LM2904	3 V–26 V	–40°C to 125°C	7 mV	350 µA	No	D, PW, DGK, P, PS
LM358A	3 V–32 V	0°C to 70°C	3 mV	350 µA	No	D, PW, DGK, P
LM2904V	3 V–32 V	–40°C to 125°C	3 mV	350 µA	No	D, PW
LM158	3 V–32 V	–55°C to 125°C	5 mV	350 µA	No	JG, FK
LM158A	3 V–32 V	–55°C to 125°C	3 mV	350 µA	No	JG, FK
LM258	3 V–32 V	–25°C to 85°C	5 mV	350 µA	No	D, DGK, P
LM258A	3 V–32 V	–25°C to 85°C	3 mV	350 µA	No	D, DGK, P

## 6 Pin Configuration and Functions

**D, DGK, P, PS, PW, and JG Packages**  
**8-Pin SOIC, VSSOP, PDIP, SO, TSSOP, and CDIP**  
**Top View**



**FK Package**  
**20-Pin LCCC**  
**Top View**



NC - No internal connection

### Pin Functions

PIN		I/O	DESCRIPTION
NAME	LCCC <sup>(1)</sup>		
IN1–	5	I	Negative input
IN1+	7	I	Positive input
IN2–	15	I	Negative input
IN2+	12	I	Positive input
OUT1	2	O	Output
OUT2	17	O	Output
V–	10	—	Negative (lowest) supply or ground (for single-supply operation)
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	No internal connection
V+	20	—	Positive (highest) supply

(1) For a listing of which devices are available in what packages, see [Device Comparison Table](#).

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
Supply voltage, $V_S = ([V+] - [V-])$		LM358B, LM358BA, LM2904B, LM2904BA	−0.3	±20 or 40	V
		LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	−0.3	±16 or 32	
		LM2904	−0.3	±13 or 26	
Differential input voltage, $V_{ID}^{(2)}$		LM358B, LM358BA, LM2904B, LM2904BA, LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	−32	32	V
		LM2904	−26	26	
Input voltage, $V_I$	Either input	LM358B, LM358BA, LM2904B, LM2904BA	−0.3	40	V
		LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	−0.3	32	
		LM2904	−0.3	26	
Duration of output short circuit (one amplifier) to ground at (or below) $T_A = 25^{\circ}\text{C}$ , $V_S \leq 15\text{ V}^{(3)}$			Unlimited		s
Operating ambient temperature, $T_A$		LM158, LM158A	−55	125	$^{\circ}\text{C}$
		LM258, LM258A	−25	85	
		LM358B, LM358BA	−40	85	
		LM358, LM358A	0	70	
		LM2904B, LM2904BA, LM2904, LM2904V	−40	125	
Operating virtual-junction temperature, $T_J$				150	$^{\circ}\text{C}$
Storage temperature, $T_{\text{stg}}$			−65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Differential voltages are at  $IN+$ , with respect to  $IN-$ .
- (3) Short circuits from outputs to  $V_S$  can cause excessive heating and eventual destruction.

### 7.2 ESD Ratings

		VALUE	UNIT
LM358B, LM358BA, LM2904B, AND LM2904BA			
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±750	
LM158, LM258, LM358, LM158, LM258A, LM358A, LM2904, AND LM2904V			
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage, V <sub>S</sub> = ([V+] – [V–])	LM358B, LM358BA, LM2904B, LM2904BA		V
		LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V		
		LM2904		
V <sub>CM</sub>	Common-mode voltage	V–	V <sub>S</sub> – 2	V
T <sub>A</sub>	Operating ambient temperature	LM358B, LM358BA		°C
		LM2904B, LM2904BA, LM2904, LM2904V		
		LM358, LM358A		
		LM258, LM258A		
		LM158, LM158A		

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM258, LM258A, LM358, LM358A, LM358B, LM358BA, LM2904, LM2904B, LM2904BA, LM2904V <sup>(2)</sup>					LM158, LM158A		UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	PS (SO)	PW (TSSOP)	FK (LCCC)	JG (CDIP)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	20 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	124.7	181.4	80.9	116.9	171.7	—	—	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	66.9	69.4	70.4	62.5	68.8	5.61	14.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	67.9	102.9	57.4	68.6	99.2	—	—	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	19.2	11.8	40	21.9	11.5	—	—	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	67.2	101.2	56.9	67.6	97.9	—	—	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	12.1	—	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(2) For a listing of which devices are available in what packages, see [Device Comparison Table](#)

## 7.5 Electrical Characteristics: LM358B and LM358BA

For  $V_S = (V_+) - (V_-) = 5\text{ V}$  to  $36\text{ V}$  ( $\pm 2.25\text{ V}$  to  $\pm 18\text{ V}$ ),  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{CM} = V_{OUT} = V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT	
OFFSET VOLTAGE								
V <sub>OS</sub>	Input offset voltage	LM358B			1	3	mV	
			T <sub>A</sub> = −40°C to 85°C			4		
		LM358BA			0.5	1.8		
			T <sub>A</sub> = −40°C to 85°C			2.5		
dV <sub>OS</sub> /dT	Input offset voltage drift		T <sub>A</sub> = −40°C to 85°C		±3.5		μV/°C	
PSRR	Power-supply rejection ratio (ΔV <sub>IO</sub> /ΔV <sub>S</sub> )				±1	15	μV/V	
	Channel separation, dc	At dc				120	dB	
INPUT VOLTAGE RANGE								
V <sub>CM</sub>	Common-mode input voltage range	V <sub>S</sub> = 3 V to 36 V		(V−)	(V+) − 1.5		V	
			T <sub>A</sub> = −40°C to 85°C	(V−)	(V+) − 2			
CMRR	Common-mode rejection ratio	(V−) < V <sub>CM</sub> < (V+) − 1.5 V		80	103		dB	
		(V−) < V <sub>CM</sub> < (V+) − 2 V	T <sub>A</sub> = −40°C to 85°C	70	96			
INPUT BIAS CURRENT								
I <sub>B</sub>	Input bias current				10	35	nA	
			T <sub>A</sub> = −40°C to 85°C			50		
I <sub>OS</sub>	Input offset current				0.5	4	nA	
			T <sub>A</sub> = −40°C to 85°C			5		
NOISE								
E <sub>n</sub>	Input voltage noise	f = 0.1 to 10 Hz			8		μV <sub>PP</sub>	
e <sub>n</sub>	Input voltage noise density	f = 1 kHz			40		nV/√Hz	
INPUT IMPEDANCE								
Z <sub>ID</sub>	Differential				10    0.1		MΩ    pF	
Z <sub>IC</sub>	Common-mode				4    1.5		GΩ    pF	
OPEN-LOOP GAIN								
A <sub>OL</sub>	Open-loop voltage gain	V <sub>S</sub> = 15 V, V <sub>O</sub> = 1 V to 11 V, R <sub>L</sub> ≥ 2 kΩ		70	140		V/mV	
			T <sub>A</sub> = −40°C to 85°C	35				
FREQUENCY RESPONSE								
GBW	Gain-bandwidth product				1.2		MHz	
SR	Slew rate	G = +1			0.5		V/μs	
φ <sub>m</sub>	Phase margin	G = +1, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 20 pF			56		°	
t <sub>S</sub>	Settling time	To 0.1%, V <sub>S</sub> = 5 V, 2-V step , G = +1, C <sub>L</sub> = 100 pF			4		μs	
t <sub>OR</sub>	Overload recovery time	V <sub>IN</sub> × gain > V <sub>S</sub>			30		μs	
THD + N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V <sub>O</sub> = 3.53 V <sub>RMS</sub> , RL = 100 kΩ			0.001%			
OUTPUT								
V <sub>O</sub>	Voltage output swing from rail	Positive Rail (V+)	I <sub>OUT</sub> = 50 μA		1.35	1.5	V	
			I <sub>OUT</sub> = 1 mA		1.4	1.6		
			I <sub>OUT</sub> = 5 mA		1.5	1.75		
		Negative Rail (V-)		I <sub>OUT</sub> = 50 μA		0.1		0.15
				I <sub>OUT</sub> = 1 mA		0.75		1
I <sub>SC</sub>	Short-circuit current	V <sub>S</sub> = 20 V			±40	60	mA	
C <sub>LOAD</sub>	Capacitive load drive				100		pF	
R <sub>O</sub>	Open-loop output resistance	f = 1 MHz, I <sub>O</sub> = 0 A			300		Ω	
POWER SUPPLY								
I <sub>Q</sub>	Quiescent current per amplifier	V <sub>S</sub> = 5 V; V <sub>O</sub> = 2.5 V; I <sub>O</sub> = 0 A			300	460	μA	
		V <sub>S</sub> = 36 V; V <sub>O</sub> = 2.5 V; I <sub>O</sub> = 0 A	T <sub>A</sub> = − 40°C to 85°C			800		

(1) All typical values are  $T_A = 25^\circ\text{C}$ .



## 7.6 Electrical Characteristics: LM2904B and LM2904BA

For  $V_S = (V+) - (V-) = 5\text{ V to }36\text{ V}$  ( $\pm 2.25\text{ V to } \pm 18\text{ V}$ ),  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{CM} = V_{OUT} = V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN		TYP <sup>(1)</sup>		MAX		UNIT	
OFFSET VOLTAGE											
V <sub>OS</sub>	Input offset voltage	LM2904B		1		3		mV			
			T <sub>A</sub> = −40°C to 125°C	4							
		LM2904BA		0.5		1.8					
			T <sub>A</sub> = −40°C to 125°C	2.5							
dV <sub>OS</sub> /dT	Input offset voltage drift		T <sub>A</sub> = −40°C to 125°C	±3.5				μV/°C			
PSRR	Power-supply rejection ratio (ΔV <sub>IO</sub> /ΔV <sub>S</sub> )						±1	15	μV/V		
	Channel separation, dc	At dc		120					dB		
INPUT VOLTAGE RANGE											
V <sub>CM</sub>	Common-mode input voltage range	V <sub>S</sub> = 3 V to 36 V		(V−)	(V+) − 1.5		V				
			T <sub>A</sub> = −40°C to 125°C	(V−)	(V+) − 2						
CMRR	Common-mode rejection ratio	(V−) < V <sub>CM</sub> < (V+) − 1.5 V		80	103		dB				
		(V−) < V <sub>CM</sub> < (V+) − 2 V	T <sub>A</sub> = −40°C to 125°C	70	96						
INPUT BIAS CURRENT											
I <sub>B</sub>	Input bias current			10		35		nA			
			T <sub>A</sub> = −40°C to 125°C	50							
I <sub>OS</sub>	Input offset current			0.5		4		nA			
			T <sub>A</sub> = −40°C to 125°C	5							
NOISE											
E <sub>n</sub>	Input voltage noise	f = 0.1 to 10 Hz			8		μV <sub>PP</sub>				
e <sub>n</sub>	Input voltage noise density	f = 1 kHz			40		nV/√Hz				
INPUT IMPEDANCE											
Z <sub>ID</sub>	Differential				10    0.1		MΩ    pF				
Z <sub>IC</sub>	Common-mode				4    1.5		GΩ    pF				
OPEN-LOOP GAIN											
A <sub>OL</sub>	Open-loop voltage gain	V <sub>S</sub> = 15 V; V <sub>O</sub> = 1 V to 11 V; R <sub>L</sub> ≥ 2 kΩ		70	140		V/mV				
			T <sub>A</sub> = −40°C to 125°C	35							
FREQUENCY RESPONSE											
GBW	Gain-bandwidth product				1.2		MHz				
SR	Slew rate	G = +1			0.5		V/μs				
φ <sub>m</sub>	Phase margin	G = +1, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 20 pF			56		°				
t <sub>S</sub>	Settling time	To 0.1%, V <sub>S</sub> = 5 V, 2-V step , G = +1, C <sub>L</sub> = 100 pF			4		μs				
t <sub>OR</sub>	Overload recovery time	V <sub>IN</sub> × gain > V <sub>S</sub>			30		μs				
THD + N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V <sub>O</sub> = 3.53 V <sub>RMS</sub> , R <sub>L</sub> = 100 kΩ			0.001%						
OUTPUT											
V <sub>O</sub>	Voltage output swing from rail	Positive rail (V+)	I <sub>OUT</sub> = 50 μA	1.35		1.5		V			
			I <sub>OUT</sub> = 1 mA	1.4		1.6					
			I <sub>OUT</sub> = 5mA	1.5		1.75					
		Negative rail (V−)	I <sub>OUT</sub> = 50 μA	0.1		0.15					
			I <sub>OUT</sub> = 1 mA	0.75		1					
I <sub>SC</sub>	Short-circuit current	V <sub>S</sub> = 20 V			±40		60 mA				
C <sub>LOAD</sub>	Capacitive load drive				100		pF				
R <sub>O</sub>	Open-loop output resistance	f = 1 MHz, I <sub>O</sub> = 0 A			300		Ω				
POWER SUPPLY											
I <sub>Q</sub>	Quiescent current per amplifier	V <sub>S</sub> = 5 V; V <sub>O</sub> = 2.5 V; I <sub>O</sub> = 0 A		300		460		μA			
		V <sub>S</sub> = 36 V; V <sub>O</sub> = 2.5 V; I <sub>O</sub> = 0 A	T <sub>A</sub> = −40°C to 125°C			800					

(1) All typical values are  $T_A = 25^\circ\text{C}$ .

## 7.7 Electrical Characteristics: LM358, LM358A

For  $V_S = (V_+) - (V_-) = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>			MIN	TYP <sup>(2)</sup>	MAX	UNIT
OFFSET VOLTAGE								
V <sub>OS</sub>	Input offset voltage	V <sub>S</sub> = 5 V to 30 V; V <sub>CM</sub> = 0 V; V <sub>O</sub> = 1.4 V	LM358			3	7	mV
				T <sub>A</sub> = 0°C to 70°C		9		
			LM358A			2	3	
				T <sub>A</sub> = 0°C to 70°C		5		
dV <sub>OS</sub> /dT	Input offset voltage drift		LM358	T <sub>A</sub> = 0°C to 70°C		7		μV/°C
			LM358A	T <sub>A</sub> = 0°C to 70°C		7	20	
PSRR	Input offset voltage vs power supply (ΔV <sub>IO</sub> /ΔV <sub>S</sub> )	V <sub>S</sub> = 5 V to 30 V			65	100		dB
V <sub>O1</sub> / V <sub>O2</sub>	Channel separation	f = 1 kHz to 20 kHz				120		dB
INPUT VOLTAGE RANGE								
V <sub>CM</sub>	Common-mode voltage range	V <sub>S</sub> = 5 V to 30 V	LM358		(V–)	(V+) – 1.5	V	
		V <sub>S</sub> = 30 V	LM358A					
		V <sub>S</sub> = 5 V to 30 V	LM358	T <sub>A</sub> = 0°C to 70°C	(V–)	(V+) – 2		
		V <sub>S</sub> = 30 V	LM358A					
CMRR	Common-mode rejection ratio	V <sub>S</sub> = 5 V to 30 V; V <sub>CM</sub> = 0 V			65	80		dB
INPUT BIAS CURRENT								
I <sub>B</sub>	Input bias current	V <sub>O</sub> = 1.4 V	LM358			–20	–250	nA
				T <sub>A</sub> = 0°C to 70°C		–500		
			LM358A			–15	–100	
				T <sub>A</sub> = 0°C to 70°C		–200		
I <sub>OS</sub>	Input offset current	V <sub>O</sub> = 1.4 V	LM358			2	50	nA
				T <sub>A</sub> = 0°C to 70°C		150		
			LM358A			2	30	
				T <sub>A</sub> = 0°C to 70°C		75		
dI <sub>OS</sub> /dT	Input offset current drift					10		pA/°C
	LM358A	T <sub>A</sub> = 0°C to 70°C		300				
NOISE								
e <sub>n</sub>	Input voltage noise density	f = 1 kHz				40		nV/√Hz
OPEN-LOOP GAIN								
A <sub>OL</sub>	Open-loop voltage gain	V <sub>S</sub> = 15 V; V <sub>O</sub> = 1 V to 11 V; R <sub>L</sub> ≥ 2 kΩ			25	100		V/mV
				T <sub>A</sub> = 0°C to 70°C	15			
FREQUENCY RESPONSE								
GBW	Gain bandwidth product					0.7		MHz
SR	Slew rate	G = +1				0.3		V/μs
OUTPUT								
V <sub>O</sub>	Voltage output swing from rail	Positive rail	V <sub>S</sub> = 30 V; R <sub>L</sub> = 2 kΩ	T <sub>A</sub> = 0°C to 70°C		4	V	
			V <sub>S</sub> = 30 V; R <sub>L</sub> ≥ 10 kΩ		2	3		
			V <sub>S</sub> = 5 V; R <sub>L</sub> ≥ 2 kΩ			1.5		
			Negative rail	V <sub>S</sub> = 5 V; R <sub>L</sub> ≤ 10 kΩ	T <sub>A</sub> = 0°C to 70°C		5	20
I <sub>O</sub>	Output current	V <sub>S</sub> = 15 V; V <sub>O</sub> = 0 V; V <sub>ID</sub> = 1 V	Source		–20	–30	mA	
				LM358A		–60		
				T <sub>A</sub> = 0°C to 70°C	–10			
		V <sub>S</sub> = 15 V; V <sub>O</sub> = 15 V; V <sub>ID</sub> = –1 V	Sink		10	20		
					T <sub>A</sub> = 0°C to 70°C	5		
				LM358		12		
	V <sub>ID</sub> = –1 V; V <sub>O</sub> = 200 mV				30		μA	
I <sub>SC</sub>	Short-circuit current	V <sub>S</sub> = 10 V; V <sub>O</sub> = V <sub>S</sub> / 2				±40	±60	mA
POWER SUPPLY								
I <sub>Q</sub>	Quiescent current per amplifier	V <sub>O</sub> = 2.5 V; I <sub>O</sub> = 0 A	T <sub>A</sub> = 0°C to 70°C			350	600	μA
		V <sub>S</sub> = 30 V; V <sub>O</sub> = 15 V; I <sub>O</sub> = 0 A			500	1000		

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum  $V_S$  for testing purposes is 30 V for LM358 and LM358A.  
(2) All typical values are  $T_A = 25^\circ\text{C}$ .

## 7.8 Electrical Characteristics: LM2904, LM2904V

For  $V_S = (V+) - (V-) = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>			MIN	TYP <sup>(2)</sup>	MAX	UNIT
OFFSET VOLTAGE								
V <sub>OS</sub>	Input offset voltage	V <sub>S</sub> = 5 V to maximum; V <sub>CM</sub> = 0 V; V <sub>O</sub> = 1.4 V	Non-A suffix devices		3		7	mV
			A-suffix devices	T <sub>A</sub> = −40°C to 125°C	10			
					1	2		
				T <sub>A</sub> = −40°C to 125°C	4			
dV <sub>OS</sub> /dT	Input offset voltage drift				T <sub>A</sub> = −40°C to 125°C	7		μV/°C
PSRR	Input offset voltage vs power supply (ΔV <sub>ID</sub> /ΔV <sub>S</sub> )	V <sub>S</sub> = 5 V to 30 V			65	100		dB
V <sub>O1</sub> / V <sub>O2</sub>	Channel separation	f = 1 kHz to 20 kHz			120			dB
INPUT VOLTAGE RANGE								
V <sub>CM</sub>	Common-mode voltage range	V <sub>S</sub> = 5 V to maximum			(V−)	(V+) − 1.5		V
			T <sub>A</sub> = −40°C to 125°C		(V−)	(V+) − 2		
CMRR	Common-mode rejection ratio	V <sub>S</sub> = 5 V to maximum; V <sub>CM</sub> = 0 V			65	80		dB
INPUT BIAS CURRENT								
I <sub>B</sub>	Input bias current	V <sub>O</sub> = 1.4 V			−20	−250		nA
			T <sub>A</sub> = −40°C to 125°C		−500			
I <sub>OS</sub>	Input offset current	V <sub>O</sub> = 1.4 V	Non-V suffix device		2	50		nA
				T <sub>A</sub> = −40°C to 125°C	300			
			V-suffix device		2	50		
				T <sub>A</sub> = −40°C to 125°C	150			
dI <sub>OS</sub> /dT	Input offset current drift				T <sub>A</sub> = −40°C to 125°C	10		pA/°C
NOISE								
e <sub>n</sub>	Input voltage noise density	f = 1 kHz			40			nV/√Hz
OPEN-LOOP GAIN								
A <sub>OL</sub>	Open-loop voltage gain	V <sub>S</sub> = 15 V; V <sub>O</sub> = 1 V to 11 V; R <sub>L</sub> ≥ 2 kΩ			25	100		V/mV
			T <sub>A</sub> = −40°C to 125°C		15			
FREQUENCY RESPONSE								
GBW	Gain bandwidth product				0.7			MHz
SR	Slew rate	G = +1			0.3			V/μs
OUTPUT								
V <sub>O</sub>	Voltage output swing from rail	Positive rail	R <sub>L</sub> ≥ 10 kΩ		V <sub>S</sub> − 1.5		V	
			Non-V suffix device	V <sub>S</sub> = maximum; R <sub>L</sub> = 2 kΩ	T <sub>A</sub> = −40°C to 125°C	22		
				V <sub>S</sub> = maximum; R <sub>L</sub> ≥ 10 kΩ		23		24
			V-suffix device	V <sub>S</sub> = maximum; R <sub>L</sub> = 2 kΩ		26		
				V <sub>S</sub> = maximum; R <sub>L</sub> ≥ 10 kΩ		27		28
		Negative rail		V <sub>S</sub> = 5 V; R <sub>L</sub> ≤ 10 kΩ	T <sub>A</sub> = −40°C to 125°C	5	20	mV
		I <sub>O</sub>	Output current	V <sub>S</sub> = 15 V; V <sub>O</sub> = 0 V; V <sub>ID</sub> = 1 V	Source		−20	−30
T <sub>A</sub> = −40°C to 125°C	−10					20		
V <sub>S</sub> = 15 V; V <sub>O</sub> = 15 V; V <sub>ID</sub> = −1 V	Sink				10	20		
				T <sub>A</sub> = −40°C to 125°C	5			
V <sub>ID</sub> = -1 V; V <sub>O</sub> = 200 mV	Non-V suffix device			30		μA		
	V-suffix device			12	40			
I <sub>SC</sub>	Short-circuit current	V <sub>S</sub> = 10 V; V <sub>O</sub> = V <sub>S</sub> / 2			±40		±60	mA
POWER SUPPLY								
I <sub>Q</sub>	Quiescent current per amplifier	V <sub>O</sub> = 2.5 V; I <sub>O</sub> = 0 A		T <sub>A</sub> = −40°C to 125°C	350	600	μA	
		V <sub>S</sub> = maximum; V <sub>O</sub> = maximum / 2; I <sub>O</sub> = 0 A			500	1000		

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum  $V_S$  for testing purposes is 26 V for LM2904 and 32 V for LM2904V.
- (2) All typical values are  $T_A = 25^\circ\text{C}$ .

## 7.9 Electrical Characteristics: LM158, LM158A

For  $V_S = (V_+) - (V_-) = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>			MIN	TYP <sup>(2)</sup>	MAX	UNIT
OFFSET VOLTAGE								
V <sub>OS</sub>	Input offset voltage	V <sub>S</sub> = 5 V to 30 V; V <sub>CM</sub> = 0 V; V <sub>O</sub> = 1.4 V	LM158		3	5	mV	
				T <sub>A</sub> = −55°C to 125°C	7			
			LM158A			2		
				T <sub>A</sub> = −55°C to 125°C	4			
dV <sub>OS</sub> /dT	Input offset voltage drift		LM158	T <sub>A</sub> = −55°C to 125°C	7		μV/°C	
			LM158A	T <sub>A</sub> = −55°C to 125°C	7	15 <sup>(3)</sup>		
PSRR	Input offset voltage vs power supply (ΔV <sub>IO</sub> /ΔV <sub>S</sub> )	V <sub>S</sub> = 5 V to 30 V				65	100	dB
V <sub>O1</sub> / V <sub>O2</sub>	Channel separation	f = 1 kHz to 20 kHz					120	dB
INPUT VOLTAGE RANGE								
V <sub>CM</sub>	Common-mode voltage range	V <sub>S</sub> = 5 V to 30 V	LM158		(V−)	(V+) − 1.5	V	
		V <sub>S</sub> = 30 V	LM158A					
		V <sub>S</sub> = 5 V to 30 V	LM158	T <sub>A</sub> = −55°C to 125°C	(V−)	(V+) − 2		
		V <sub>S</sub> = 30 V						LM158A
CMRR	Common-mode rejection ratio	V <sub>S</sub> = 5 V to 30 V; V <sub>CM</sub> = 0 V				70	80	dB
INPUT BIAS CURRENT								
I <sub>B</sub>	Input bias current	V <sub>O</sub> = 1.4 V	LM158		−20	−150	nA	
				T <sub>A</sub> = −55°C to 125°C	−300			
			LM158A		−15	−50		
				T <sub>A</sub> = −55°C to 125°C	−100			
I <sub>OS</sub>	Input offset current	V <sub>O</sub> = 1.4 V	LM158		2	30	nA	
				T <sub>A</sub> = −55°C to 125°C	100			
			LM158A		2	10		
				T <sub>A</sub> = −55°C to 125°C	30			
dI <sub>OS</sub> /dT	Input offset current drift				10		pA/°C	
			LM158A	T <sub>A</sub> = −55°C to 125°C	200			
NOISE								
e <sub>n</sub>	Input voltage noise density	f = 1 kHz				40		nV/√Hz
OPEN-LOOP GAIN								
A <sub>OL</sub>	Open-loop voltage gain	V <sub>S</sub> = 15 V; V <sub>O</sub> = 1 V to 11 V; R <sub>L</sub> ≥ 2 kΩ			50	100	V/mV	
			T <sub>A</sub> = −55°C to 125°C		25			
FREQUENCY RESPONSE								
GBW	Gain bandwidth product				0.7			MHz
SR	Slew rate	G = +1						V/μs
V <sub>O</sub>	Voltage output swing from rail	Positive rail	V <sub>S</sub> = 30 V; R <sub>L</sub> = 2 kΩ	T <sub>A</sub> = −55°C to 125°C	4		V	
			V <sub>S</sub> = 30 V; R <sub>L</sub> ≥ 10 kΩ		2	3		
			V <sub>S</sub> = 5 V; R <sub>L</sub> ≥ 2 kΩ		1.5			
		Negative rail	V <sub>S</sub> = 5 V; R <sub>L</sub> ≤ 10 kΩ	T <sub>A</sub> = −55°C to 125°C	5	20	mV	
I <sub>O</sub>	Output current	V <sub>S</sub> = 15 V; V <sub>O</sub> = 0 V; V <sub>ID</sub> = 1 V	Source		−20	−30	mA	
				LM158A	−60			
				T <sub>A</sub> = −55°C to 125°C	−10			
		Sink		10	20			
			T <sub>A</sub> = −55°C to 125°C	5				
	V <sub>ID</sub> = −1 V; V <sub>O</sub> = 200 mV				12	30	μA	
I <sub>SC</sub>	Short-circuit current	V <sub>S</sub> = 10 V; V <sub>O</sub> = V <sub>S</sub> / 2				±40	±60	mA
POWER SUPPLY								
I <sub>Q</sub>	Quiescent current per amplifier	V <sub>O</sub> = 2.5 V; I <sub>O</sub> = 0 A	T <sub>A</sub> = −55°C to 125°C		350	600	μA	
		V <sub>S</sub> = 30 V; V <sub>O</sub> = 15 V; I <sub>O</sub> = 0 A			500	1000		

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.

Maximum  $V_S$  for testing purposes is 30 V for LM158 and LM158A.

(2) All typical values are  $T_A = 25^\circ\text{C}$ .

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 7.10 Electrical Characteristics: LM258, LM258A

For  $V_S = (V_+) - (V_-) = 5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>			MIN	TYP <sup>(2)</sup>	MAX	UNIT
OFFSET VOLTAGE								
V <sub>OS</sub>	Input offset voltage	V <sub>S</sub> = 5 V to 30 V; V <sub>CM</sub> = 0 V; V <sub>O</sub> = 1.4 V	LM258		3	5	mV	
				T <sub>A</sub> = −25°C to 85°C	7			
			LM258A		2	3		
				T <sub>A</sub> = −25°C to 85°C	4			
dV <sub>OS</sub> /d <sub>T</sub>	Input offset voltage drift		LM258	T <sub>A</sub> = −25°C to 85°C	7		μV/°C	
			LM258A	T <sub>A</sub> = −25°C to 85°C	7	15		
PSRR	Input offset voltage vs power supply (ΔV <sub>IO</sub> /ΔV <sub>S</sub> )	V <sub>S</sub> = 5 V to 30 V			65	100		dB
V <sub>O1</sub> / V <sub>O2</sub>	Channel separation	f = 1 kHz to 20 kHz				120		dB
INPUT VOLTAGE RANGE								
V <sub>CM</sub>	Common-mode voltage range	V <sub>S</sub> = 5 V to 30 V	LM258		(V−)	(V+) − 1.5		V
		V <sub>S</sub> = 30 V	LM258A					
		V <sub>S</sub> = 5 V to 30 V	LM258	T <sub>A</sub> = −25°C to 85°C	(V−)	(V+) − 2		
		V <sub>S</sub> = 30 V				LM258A		
CMRR	Common-mode rejection ratio	V <sub>S</sub> = 5 V to 30 V; V <sub>CM</sub> = 0 V			70	80		dB
INPUT BIAS CURRENT								
I <sub>B</sub>	Input bias current	V <sub>O</sub> = 1.4 V	LM258		−20	−150	nA	
				T <sub>A</sub> = −25°C to 85°C	−300			
			LM258A		−15	−80		
				T <sub>A</sub> = −25°C to 85°C	−100			
I <sub>OS</sub>	Input offset current	V <sub>O</sub> = 1.4 V	LM258		2	30	nA	
				T <sub>A</sub> = −25°C to 85°C	100			
			LM258A		2	15		
				T <sub>A</sub> = −25°C to 85°C	30			
dI <sub>OS</sub> /d <sub>T</sub>	Input offset current drift				10		pA/°C	
LM258A	T <sub>A</sub> = −25°C to 85°C	200						
NOISE								
e <sub>n</sub>	Input voltage noise density	f = 1 kHz				40		nV/√Hz
OPEN-LOOP GAIN								
A <sub>OL</sub>	Open-loop voltage gain	V <sub>S</sub> = 15 V; V <sub>O</sub> = 1 V to 11 V; R <sub>L</sub> ≥ 2 kΩ			50	100	V/mV	
			T <sub>A</sub> = −25°C to 85°C		25			
FREQUENCY RESPONSE								
GBW	Gain bandwidth product					0.7		MHz
SR	Slew rate	G = +1				0.3		V/μs
OUTPUT								
V <sub>O</sub>	Voltage output swing from rail	Positive rail	V <sub>S</sub> = 30 V; R <sub>L</sub> = 2 kΩ		T <sub>A</sub> = −25°C to 85°C		4	V
			V <sub>S</sub> = 30 V; R <sub>L</sub> ≥ 10 kΩ				2	
			V <sub>S</sub> = 5 V; R <sub>L</sub> ≥ 2 kΩ				1.5	
		Negative rail	V <sub>S</sub> = 5 V; R <sub>L</sub> ≤ 10 kΩ		T <sub>A</sub> = −25°C to 85°C		5	20
I <sub>O</sub>	Output current	V <sub>S</sub> = 15 V; V <sub>O</sub> = 0 V; V <sub>ID</sub> = 1 V	Source			−20	−30	mA
				LM258A		−60		
		V <sub>S</sub> = 15 V; V <sub>O</sub> = 15 V; V <sub>ID</sub> = −1 V	Sink	T <sub>A</sub> = −25°C to 85°C		−10	20	
				T <sub>A</sub> = −25°C to 85°C		5		
V <sub>ID</sub> = −1 V; V <sub>O</sub> = 200 mV					12	30		μA
I <sub>SC</sub>	Short-circuit current	V <sub>S</sub> = 10 V; V <sub>O</sub> = V <sub>S</sub> / 2				±40	±60	mA
POWER SUPPLY								
I <sub>Q</sub>	Quiescent current per amplifier	V <sub>O</sub> = 2.5 V; I <sub>O</sub> = 0 A		T <sub>A</sub> = −25°C to 85°C	350	600	μA	
		V <sub>S</sub> = 30 V; V <sub>O</sub> = 15 V; I <sub>O</sub> = 0 A			500	1000		

- All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum  $V_S$  for testing purposes is 30 V for LM258 and LM258A.
- All typical values are  $T_A = 25^\circ\text{C}$ .

## 7.11 Typical Characteristics

Typical characteristics section is applicable for LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V

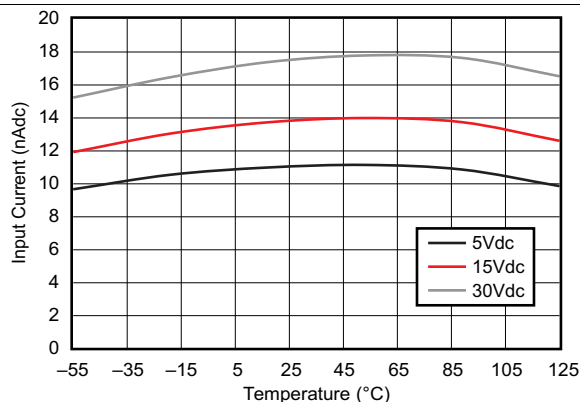


Figure 1. Input Current vs. Temperature

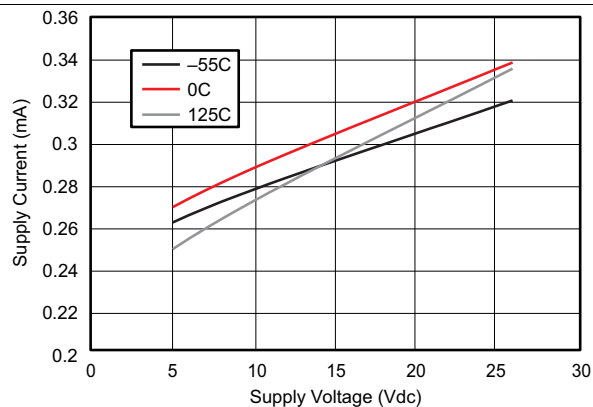


Figure 2. Supply Current vs. Supply Voltage

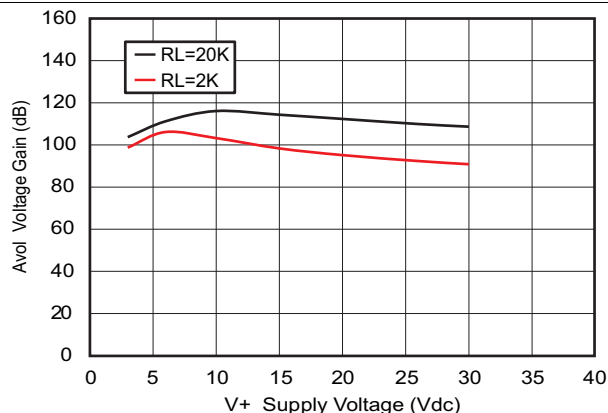


Figure 3. Voltage Gain vs. Supply Voltage

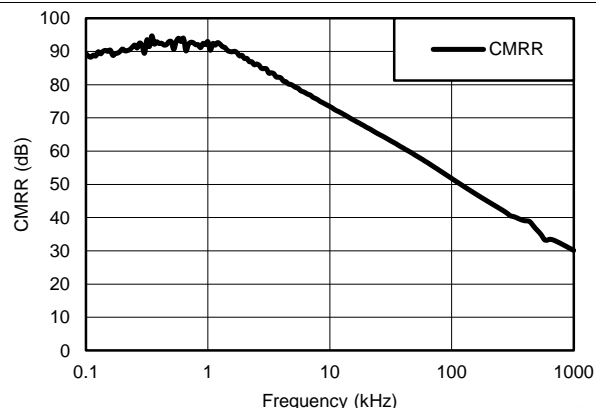


Figure 4. Common-Mode Rejection Ratio vs. Frequency

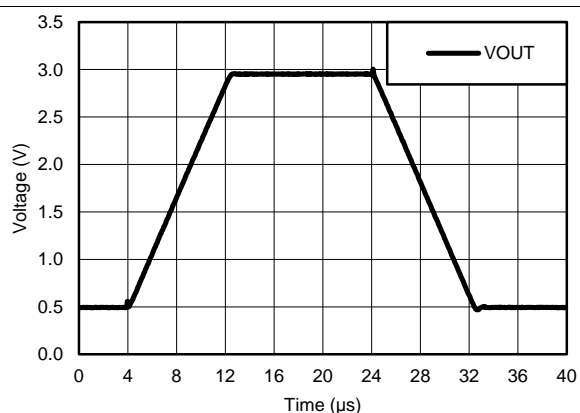


Figure 5. Voltage Follower Large Signal Response (50 pF)

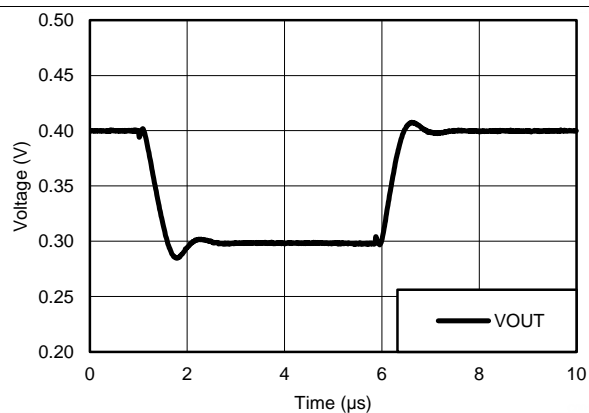
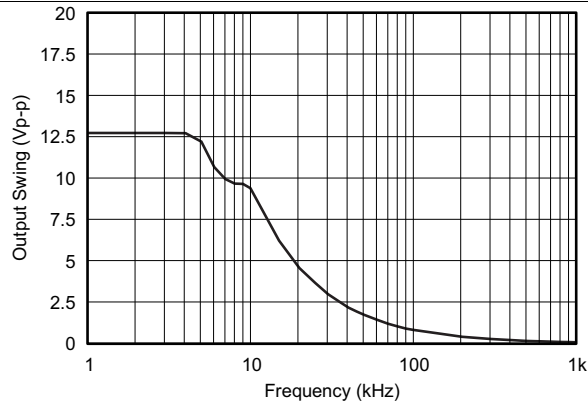


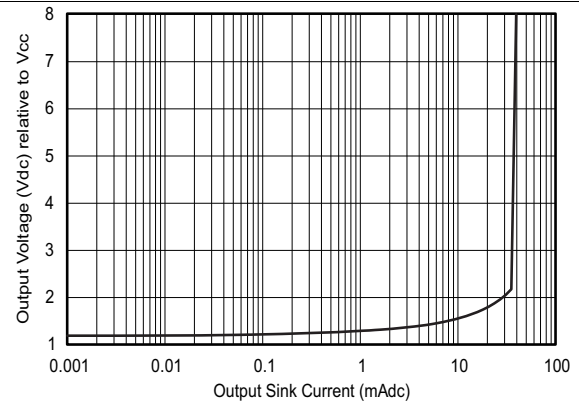
Figure 6. Voltage Follower Small Signal Response (50 pF)

## Typical Characteristics (continued)

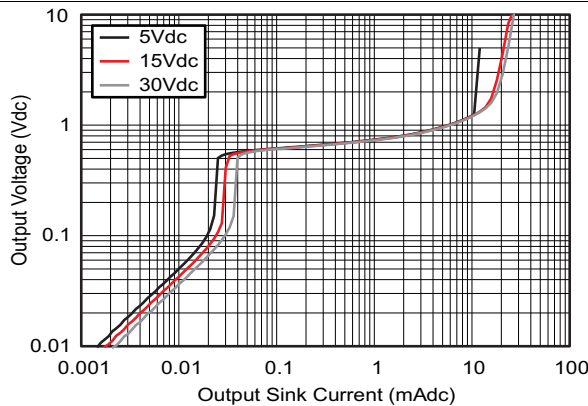
Typical characteristics section is applicable for LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V



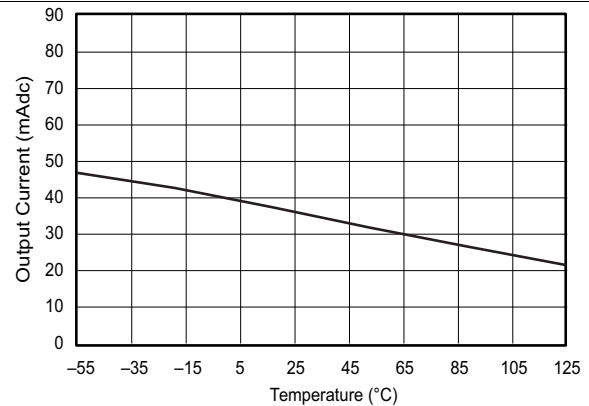
**Figure 7. Maximum Output Swing vs. Frequency**  
( $V_{CC} = 15\text{ V}$ )



**Figure 8. Output Sourcing Characteristics**



**Figure 9. Output Sinking Characteristics**



**Figure 10. Source Current Limiting**

## 8 Parameter Measurement Information

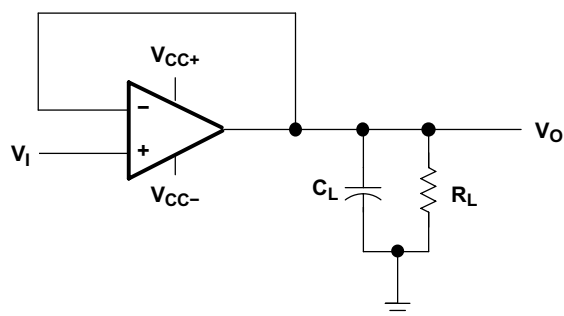


Figure 11. Unity-Gain Amplifier

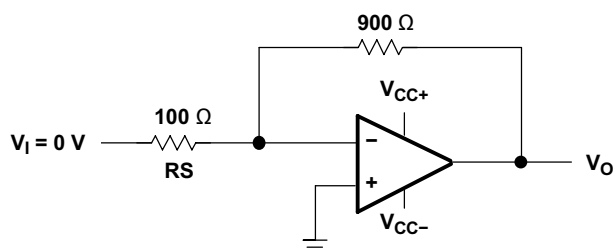


Figure 12. Noise-Test Circuit



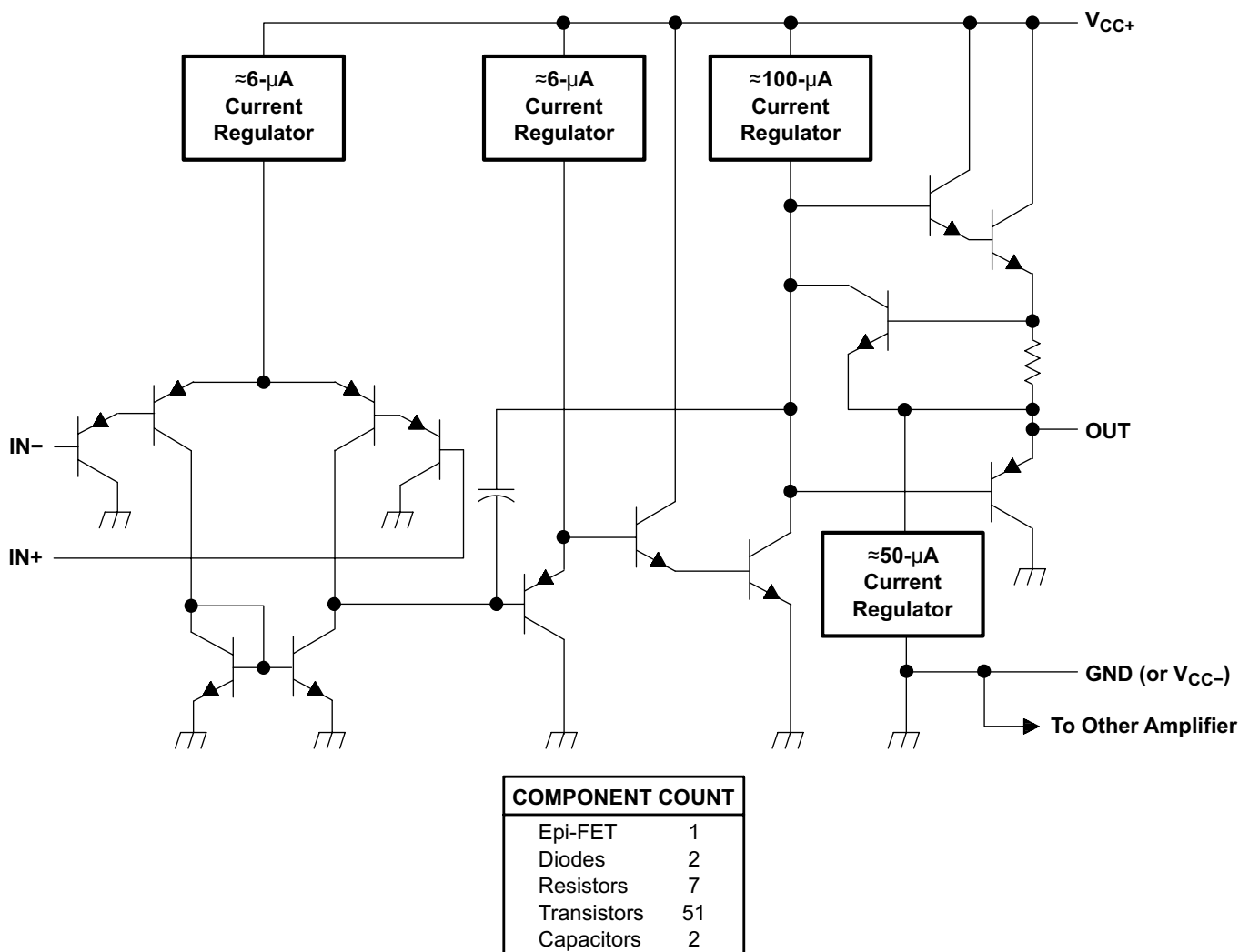
## 9 Detailed Description

### 9.1 Overview

These devices consist of two independent, high-gain frequency-compensated operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is within the supply voltage range specified in the [Recommended Operating Conditions](#) section, and  $V_S$  is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, these devices can be operated directly from the standard 5-V supply used in digital systems and easily can provide the required interface electronics without additional  $\pm 5$ -V supplies.

### 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. These devices have a 1.2-MHz unity-gain bandwidth (B Version).

### 9.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.5-V/ $\mu$ s slew rate (B Version).

### 9.3.3 Input Common Mode Range

The valid common mode range is from device ground to  $V_S - 1.5$  V ( $V_S - 2$  V across temperature). Inputs may exceed  $V_S$  up to the maximum  $V_S$  without device damage. At least one input must be in the valid input common-mode range for the output to be the correct phase. If both inputs exceed the valid range, then the output phase is undefined. If either input more than 0.3 V below  $V_-$  then input current should be limited to 1 mA and the output phase is undefined.

## 9.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier, depending on the application.

## 10 Application and Implementation

### NOTE

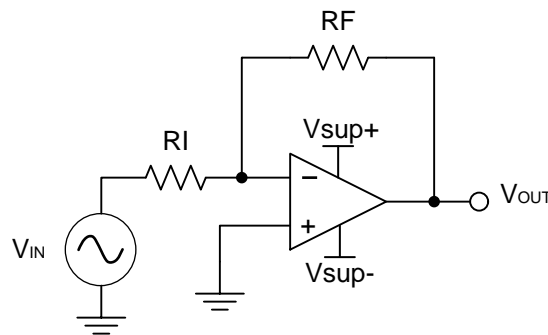
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The LMx58 and LM2904 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before  $V_S$  for flexibility in multiple supply circuits.

### 10.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.



**Figure 13. Application Schematic**

#### 10.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of  $\pm 0.5$  V to  $\pm 1.8$  V. Setting the supply at  $\pm 12$  V is sufficient to accommodate this application.

#### 10.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#):

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for  $R_I$  or  $R_F$ . [Subscripts should be fixed in the accompanying figures and equations also.] Choosing a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliamperage range. This ensures the part does not draw too much current. This example uses 10 k $\Omega$  for  $R_I$  which means 36 k $\Omega$  is used for  $R_F$ . This was determined by [Equation 3](#).

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

## Typical Application (continued)

### 10.2.3 Application Curve

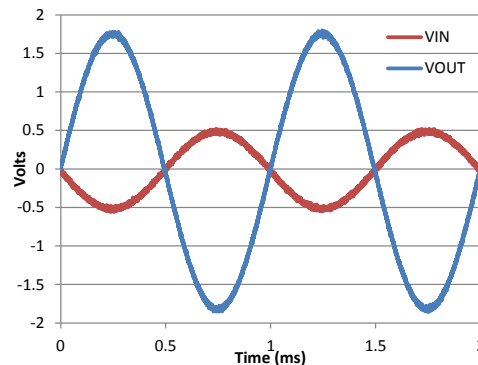


Figure 14. Input and Output Voltages of the Inverting Amplifier

## 11 Power Supply Recommendations

### CAUTION

Supply voltages larger than specified in the recommended operating region can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- $\mu$ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout](#) section.

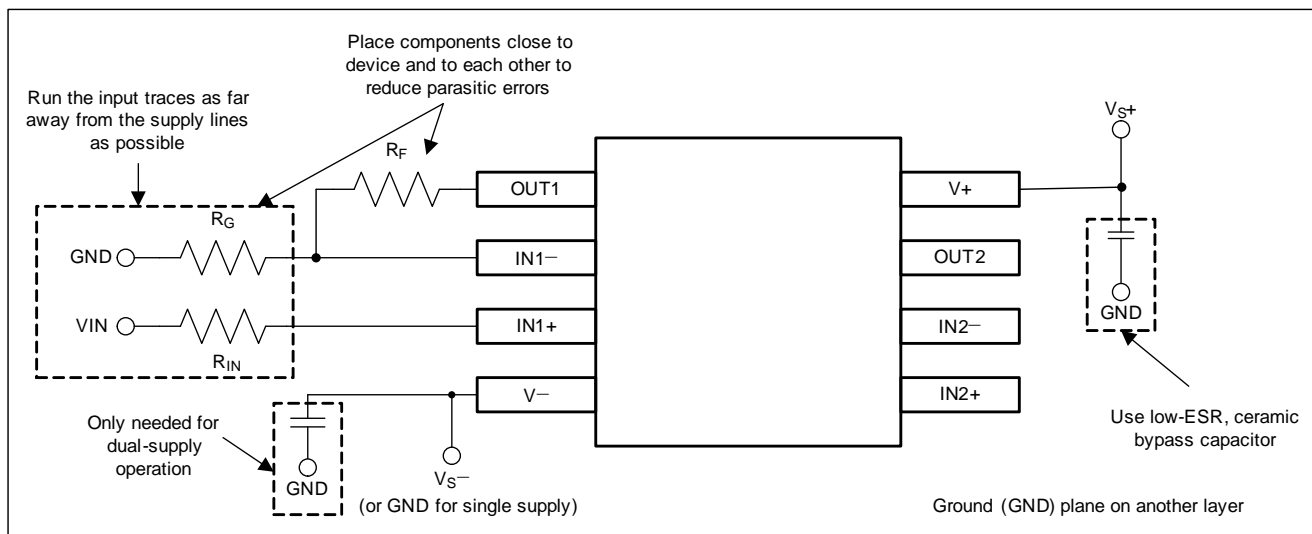
## 12 Layout

### 12.1 Layout Guidelines

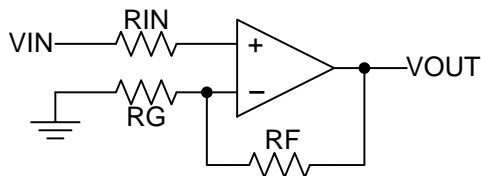
For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace. [Things in parallel never cross, by definition]
- Place the external components as close to the device as possible. Keeping  $R_F$  and  $R_G$  close to the inverting input minimizes parasitic capacitance, as shown in [Layout Examples](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 12.2 Layout Examples



**Figure 15. Operational Amplifier Board Layout for Noninverting Configuration**



**Figure 16. Operational Amplifier Schematic for Noninverting Configuration**

## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

- Texas Instruments, [Circuit Board Layout Techniques](#).

### 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM158	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM158A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM258	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM258A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM358	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM358A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM358B <sup>(1)</sup>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM2904	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM2904B <sup>(1)</sup>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM2904V	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

(1) Device is currently Preview

### 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.5 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser based versions of this data sheet, see the left-hand navigation pane.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87710012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87710012A LM158FKB	<a href="#">Samples</a>
5962-8771001PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8771001PA LM158	<a href="#">Samples</a>
5962-87710022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87710022A LM158AFKB	<a href="#">Samples</a>
5962-8771002PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8771002PA LM158A	<a href="#">Samples</a>
LM158AFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87710022A LM158AFKB	<a href="#">Samples</a>
LM158AJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	LM158AJG	<a href="#">Samples</a>
LM158AJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8771002PA LM158A	<a href="#">Samples</a>
LM158FKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87710012A LM158FKB	<a href="#">Samples</a>
LM158JG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	LM158JG	<a href="#">Samples</a>
LM158JGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8771001PA LM158	<a href="#">Samples</a>
LM258AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	<a href="#">Samples</a>
LM258ADGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(M3L, M3P, M3S, M3 U)	<a href="#">Samples</a>
LM258ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-25 to 85	LM258A	<a href="#">Samples</a>
LM258ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	<a href="#">Samples</a>
LM258ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	<a href="#">Samples</a>
LM258AP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	N / A for Pkg Type	-25 to 85	LM258AP	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM258APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-25 to 85	LM258AP	<a href="#">Samples</a>
LM258D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(M2L, M2P, M2S, M2 U)	<a href="#">Samples</a>
LM258DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	(M2L, M2P, M2S, M2 U)	<a href="#">Samples</a>
LM258DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	N / A for Pkg Type	-25 to 85	LM258P	<a href="#">Samples</a>
LM258PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-25 to 85	LM258P	<a href="#">Samples</a>
LM2904AVQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	<a href="#">Samples</a>
LM2904AVQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	<a href="#">Samples</a>
LM2904AVQPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	<a href="#">Samples</a>
LM2904AVQPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	<a href="#">Samples</a>
LM2904BIDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		
LM2904D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2904DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(MBL, MBP, MBS, MB U)	<a href="#">Samples</a>
LM2904DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(MBL, MBP, MBS, MB U)	<a href="#">Samples</a>
LM2904DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	N / A for Pkg Type	-40 to 125	LM2904P	<a href="#">Samples</a>
LM2904PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	LM2904P	<a href="#">Samples</a>
LM2904PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PWRG3	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PWRG4-JF	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	<a href="#">Samples</a>
LM2904QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	<a href="#">Samples</a>
LM2904VQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	<a href="#">Samples</a>
LM2904VQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	<a href="#">Samples</a>
LM2904VQPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2904VQPWGR4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	<a href="#">Samples</a>
LM358AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358ADE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358ADGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M6L, M6P, M6S, M6 U)	<a href="#">Samples</a>
LM358ADGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(M6L, M6P, M6S, M6 U)	<a href="#">Samples</a>
LM358ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358AP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	N / A for Pkg Type	0 to 70	LM358AP	<a href="#">Samples</a>
LM358APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LM358AP	<a href="#">Samples</a>
LM358APW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L358A	<a href="#">Samples</a>
LM358APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	L358A	<a href="#">Samples</a>
LM358APWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L358A	<a href="#">Samples</a>
LM358BIDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85		
LM358D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M5L, M5P, M5S, M5 U)	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM358DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(M5L, M5P, M5S, M5 U)	<a href="#">Samples</a>
LM358DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	N / A for Pkg Type	0 to 70	LM358P	<a href="#">Samples</a>
LM358PE3	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	LM358P	<a href="#">Samples</a>
LM358PE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	LM358P	<a href="#">Samples</a>
LM358PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PWRG3	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PWRG4-JF	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
PLM2904BIDR	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
PLM358BIDR	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

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**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LM258A, LM2904, LM2904B :**

- Automotive: [LM2904-Q1](#), [LM2904B-Q1](#)
- Enhanced Product: [LM258A-EP](#), [LM2904-EP](#)

**NOTE:** Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

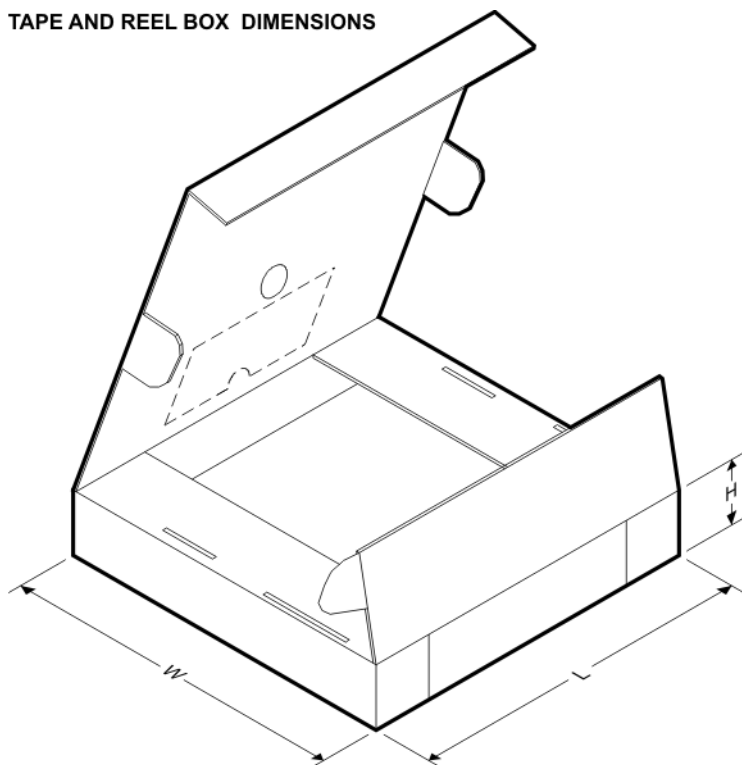

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM258ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDRG4	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904AVQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2904DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWRG4-JF	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358APWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWRG4-JF	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM258ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM258ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM258ADR	SOIC	D	8	2500	367.0	367.0	35.0
LM258ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM258ADRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM258ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM258DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM258DR	SOIC	D	8	2500	367.0	367.0	35.0
LM258DR	SOIC	D	8	2500	340.5	338.1	20.6
LM258DR	SOIC	D	8	2500	364.0	364.0	27.0
LM258DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM258DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM258DRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM258DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2904AVQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2904AVQDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2904AVQPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2904AVQPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2904DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM2904DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2904DR	SOIC	D	8	2500	333.2	345.9	28.6
LM2904DR	SOIC	D	8	2500	340.5	338.1	20.6
LM2904DR	SOIC	D	8	2500	367.0	367.0	35.0
LM2904DR	SOIC	D	8	2500	364.0	364.0	27.0
LM2904DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM2904DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM2904DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2904DRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM2904PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2904PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2904PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2904PWRG4-JF	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2904QDR	SOIC	D	8	2500	350.0	350.0	43.0
LM2904VQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2904VQPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2904VQPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM358ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM358ADR	SOIC	D	8	2500	333.2	345.9	28.6
LM358ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM358ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM358ADR	SOIC	D	8	2500	367.0	367.0	35.0
LM358ADRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM358ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM358APWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM358APWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358APWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM358DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM358DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM358DR	SOIC	D	8	2500	367.0	367.0	35.0
LM358DR	SOIC	D	8	2500	340.5	338.1	20.6
LM358DR	SOIC	D	8	2500	364.0	364.0	27.0
LM358DR	SOIC	D	8	2500	333.2	345.9	28.6
LM358DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM358DRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM358DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM358PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM358PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM358PWRG4-JF	TSSOP	PW	8	2000	367.0	367.0	35.0

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004



**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

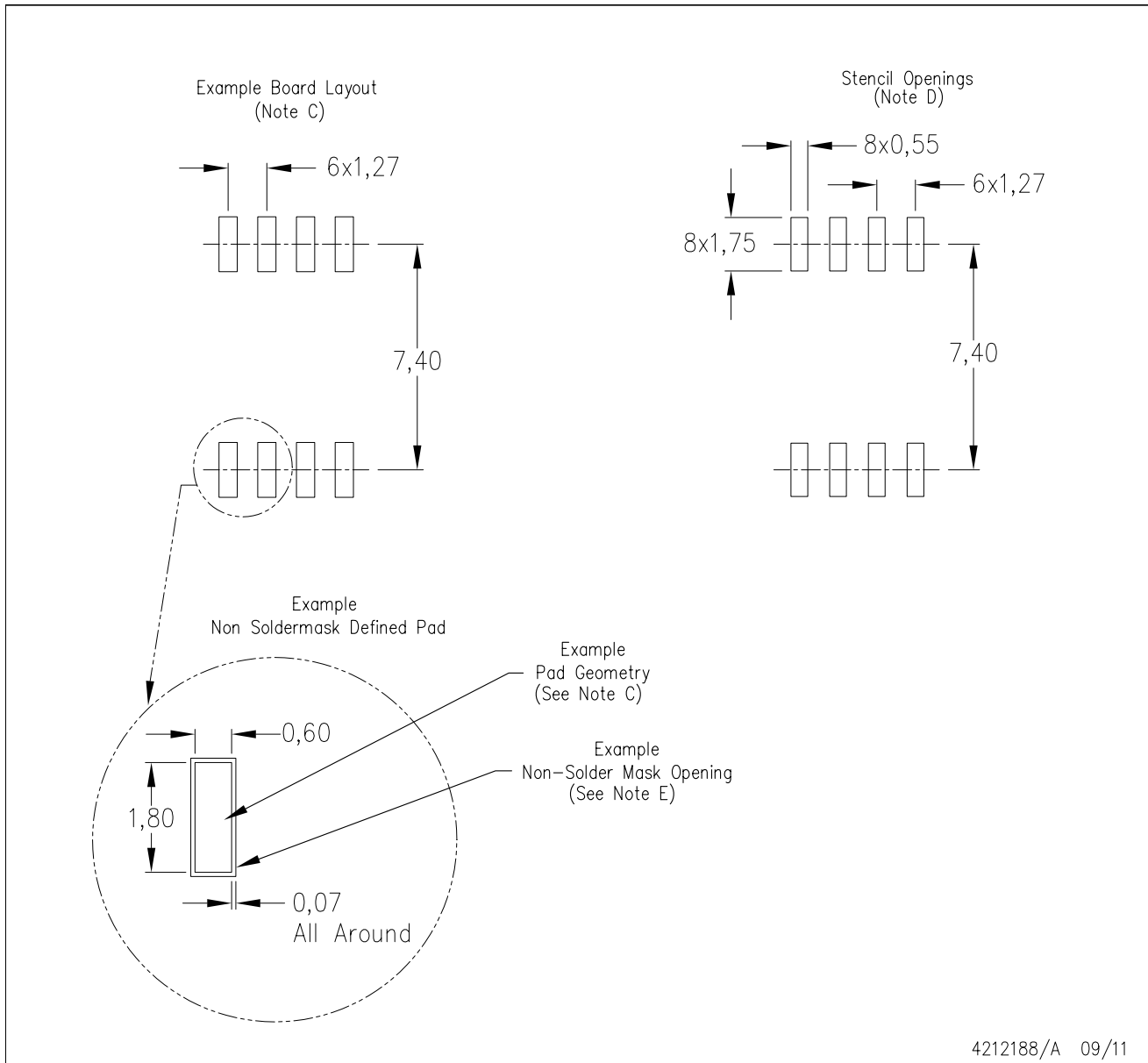


4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## PS (R-PDSO-G8)

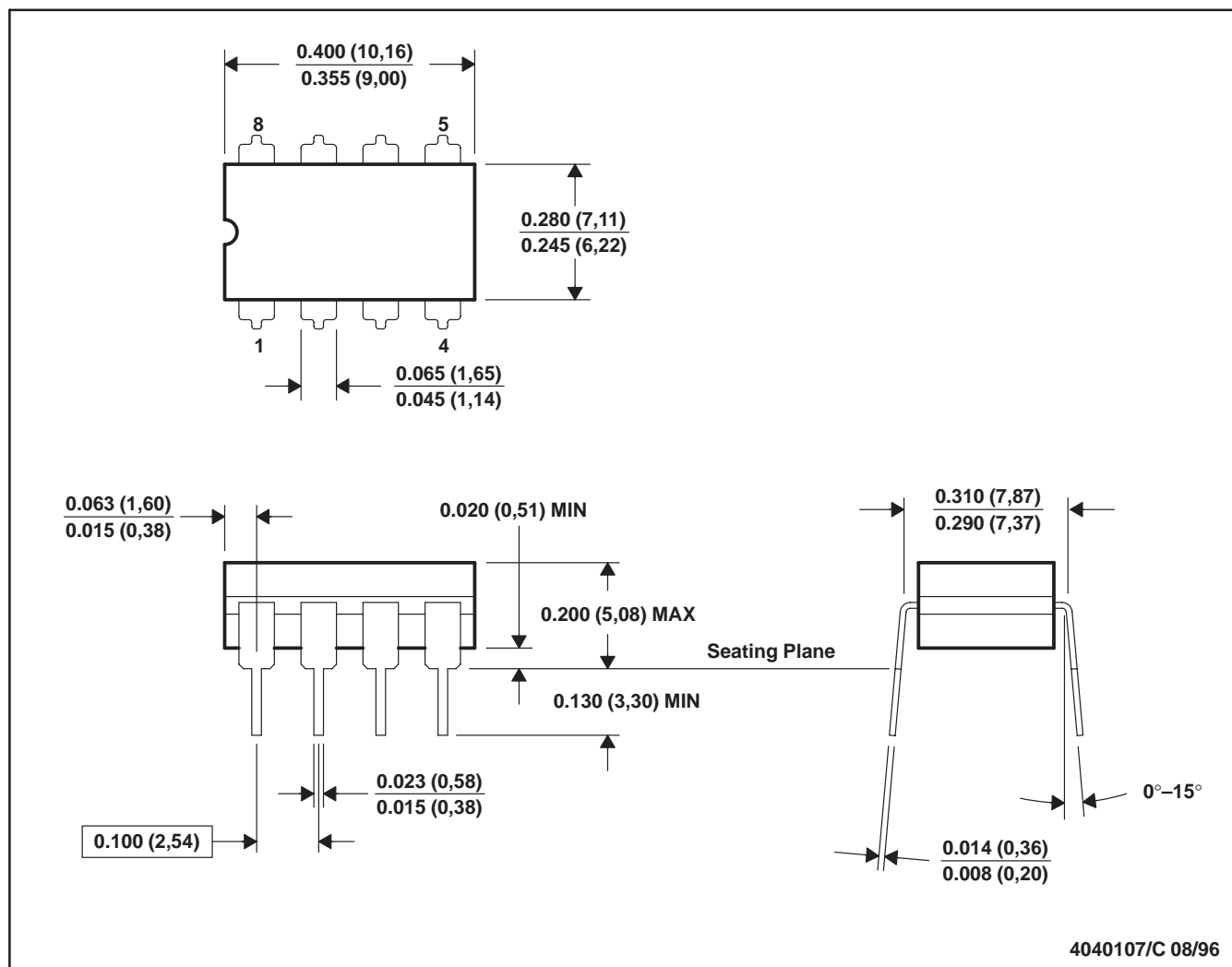
## PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## JG (R-GDIP-T8)

## CERAMIC DUAL-IN-LINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification.
  - E. Falls within MIL STD 1835 GDIP1-T8



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

## DGK (S-PDSO-G8)

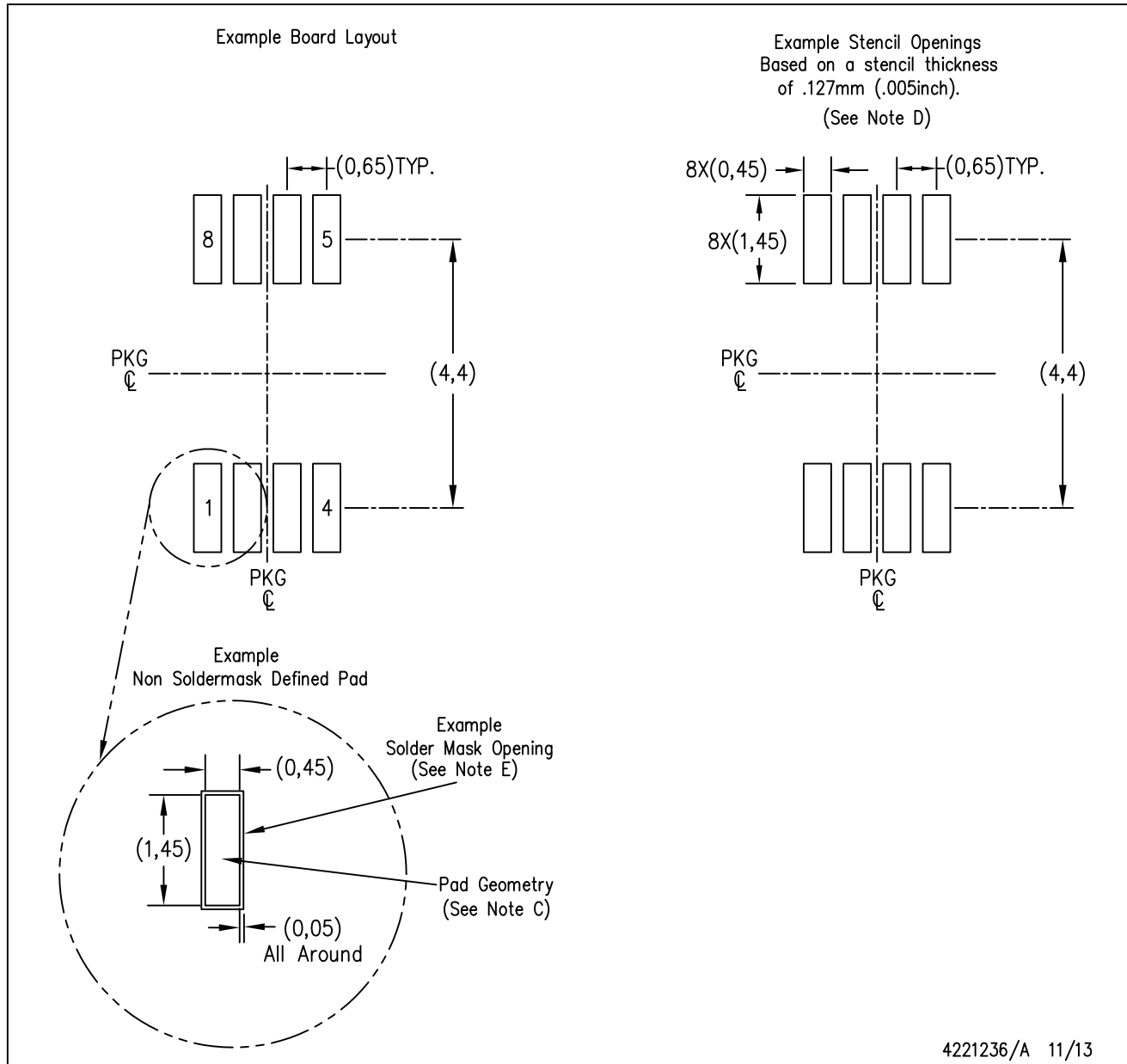
## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

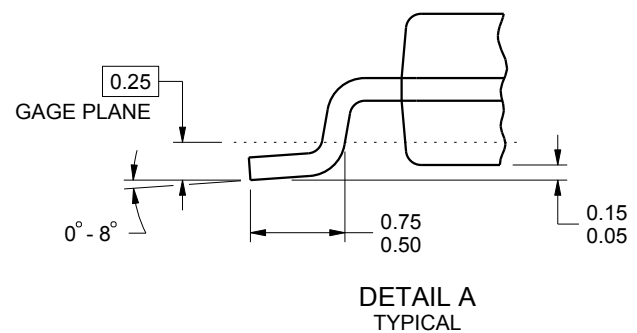
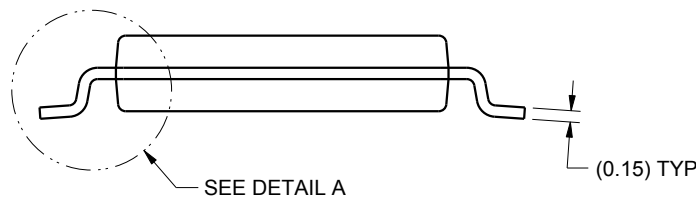
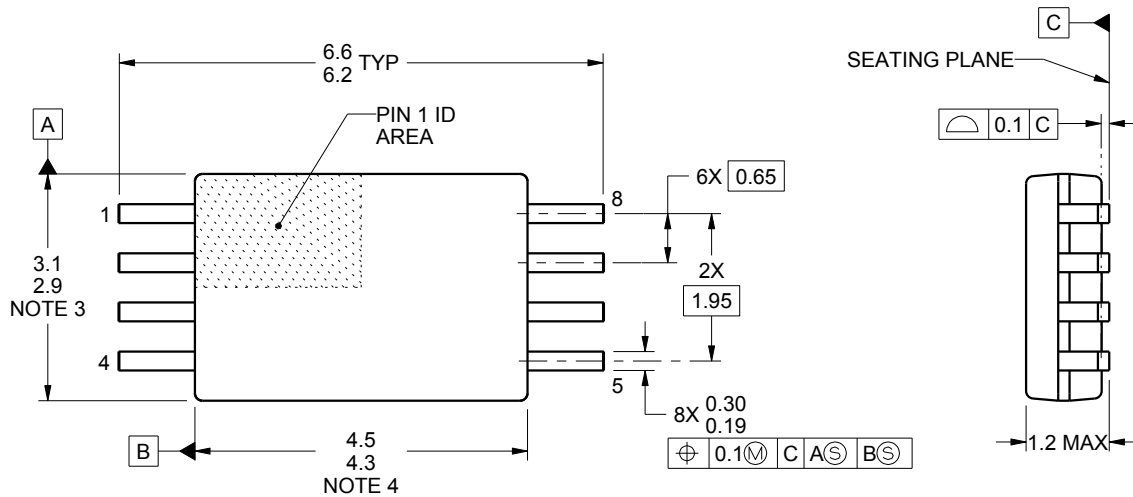
PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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### NOTES:

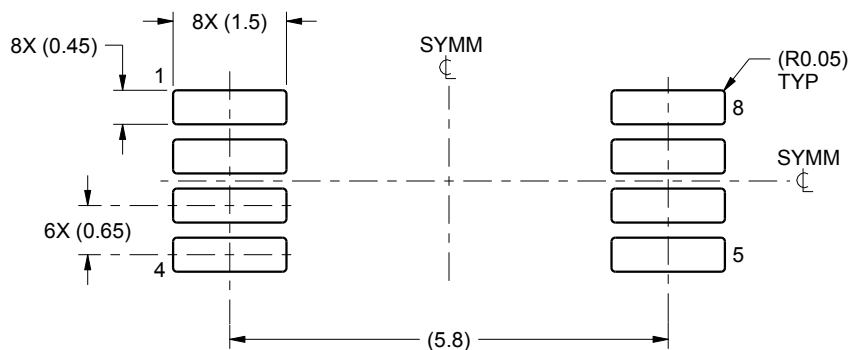
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

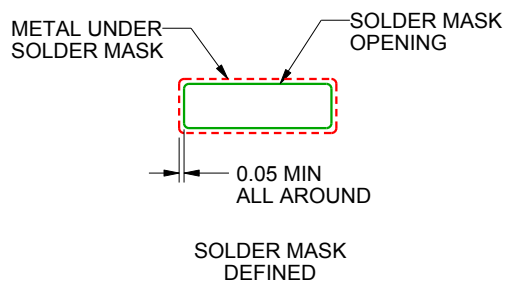
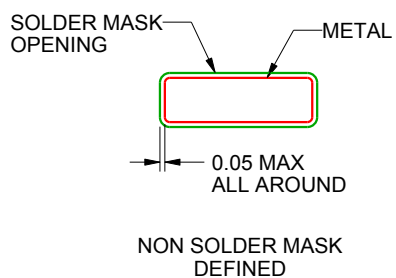
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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