EGB240 Electronic Design

Assessment 1: PCB Alarm Circuit Design Portfolio

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Executive Summary

This portfolio documents the design, simulation, and fabrication process for an alternating frequency buzzer. The board was designed to the following specifications:

- Power supply from two AA batteries (nominally 3V).
- 3kHz and 5kHz tone switching tones at 2Hz, with 41% duty cycle.
- 74HC14 hex Schmitt trigger inverter must be used to create the multi-tone sound.
- 50mA current draw.

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1. Circuit schematic

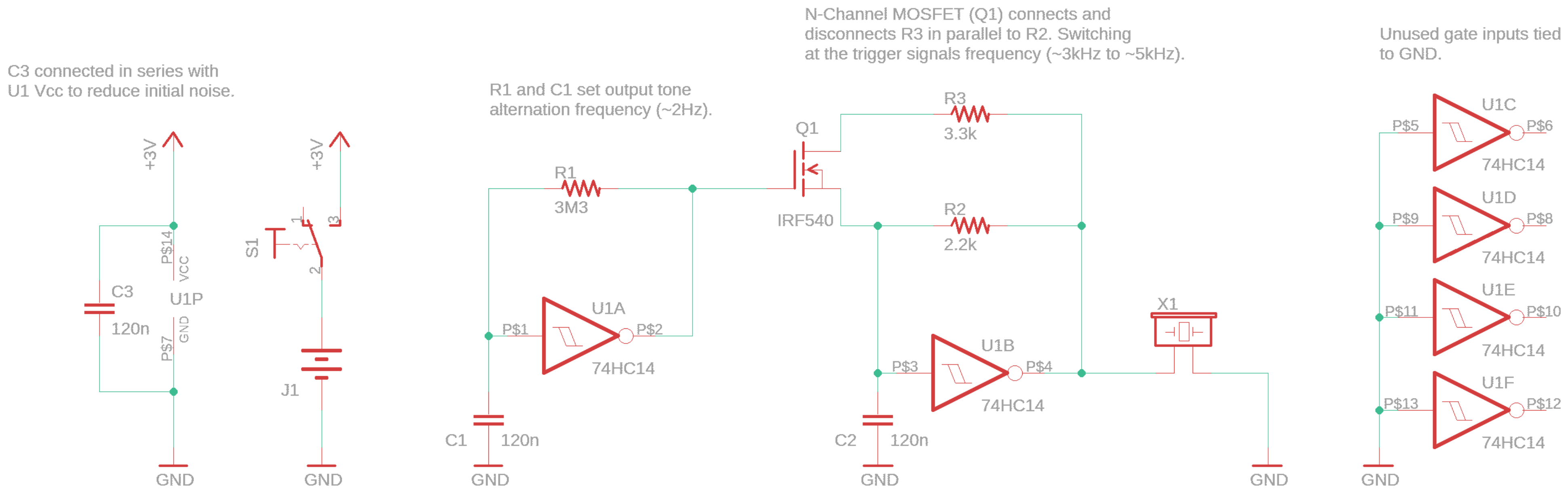


Figure 1: PCB siren circuit schematic with annotations.

2. Summary of design and operation

The assigned task was to design a simple circuit for a two-tone siren, driven by two AA batteries. The design includes a piezoelectric buzzer. When voltage is applied to either side of the buzzer, the piezoelectric material (crystal or ceramic) mechanically deforms ((Rose, 2018)). The change in shape causes vibrations, and pressure waves, producing an audible sound. The frequency of the voltage applied to the buzzer correlates to the vibration frequency, producing sounds at a given frequency.

The type of buzzer chosen was the PS1720P02, this was chosen due to its suitability in a siren/alarm application, as the datasheet states "For warning and alarm sounds of home appliances" (PS1720P02 datasheet). The range of audible sounds is restricted to 20Hz to 20kHz (Purves et al., 2001), which must be accounted for when designing the relaxation oscillator.

Choosing frequencies

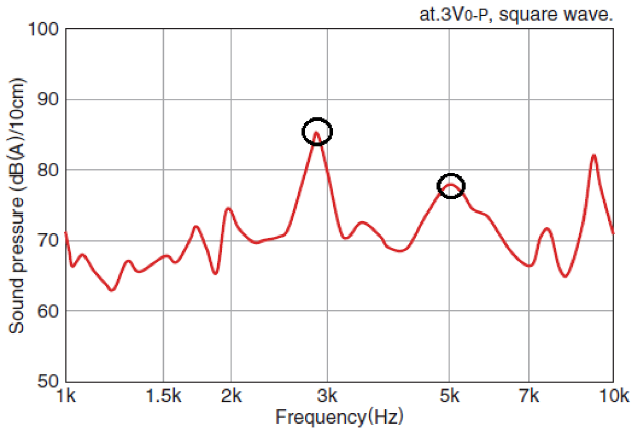
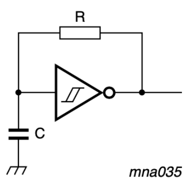


Figure 2: PS1720P02 frequency vs sound pressure (with chosen frequencies).

The human ear is most sensitive to frequencies in the 2000 Hz to 5000 Hz range (Widex, 2021). As seen in Figure 2, 3kHz and 5kHz produce the greatest sound pressure in the human hearing range, therefore these frequencies were chosen.

Design Overview and Selection of Components



For 74HC14 and 74HCT14: $f = \frac{1}{T} \approx \frac{1}{K \times RC}$

Figure 3: Recommended relaxation oscillator design and frequency formula.

The 74HC14 Schmitt trigger data sheet included a recommended design for a relaxation oscillator and the output frequency based on component values (see Figure 3). The Schmitt trigger utilises hysteresis to discretise an analogue signal. In this design, the analogue component is the voltage across the capacitor. As the capacitor charges and discharges, the inverter discretises this into square waves and inverts the signal. The frequency can be decreased by increasing the capacitance and resistance,

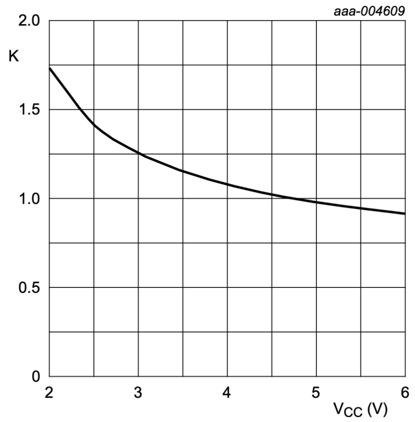


Figure 4: K value associated with Vcc.

this will cause the capacitor to take longer to charge, hence longer periods. The 'K factor' in $f = \frac{1}{KRC}$ depends on the source voltage (see Figure 4).

The power supply in this design was 2xAA batteries (3V), giving a K value of 1.25. Using this information, and the desired frequency, resistor and capacitor values were derived.

The design (refer to Figure 5) uses two inverting Schmitt triggers to create three distinct frequencies. The first frequency was designed to oscillate at 2.02 Hz, this slow oscillation is used as a trigger signal and is fed into the gate pin of the IRF540 N-channel enhancement MOSFET. The output voltage of the 74HC14 inverter ranges between the logic levels defined by the supply voltage (V_{CC}=3V) and ground (0V). When the inverter output is high (3V) it can turn on the MOSFET, as it meets the requirements of the gate-source threshold voltage of the IRF540 MOSFET (2V-4V, see references), allowing current to flow between the drain and source terminals.

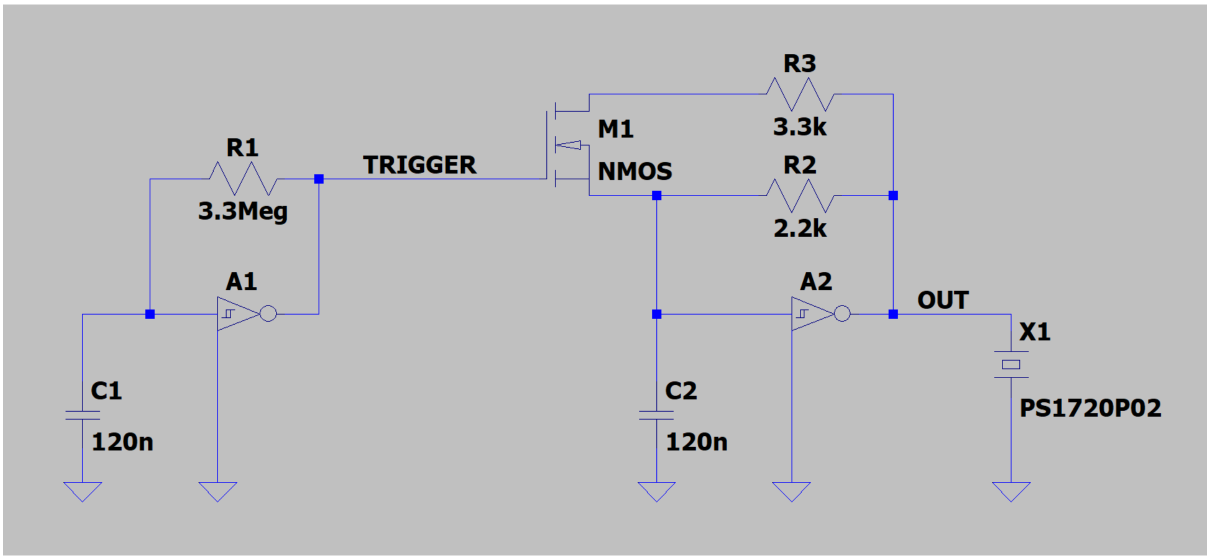


Figure 5: Circuit diagram of siren.

The transistor's drain and source pins are connected in intersection with two resistors (R2 and R3) in parallel. When the trigger signal oscillator output is low voltage, R3 is disconnected and the equivalent resistance across the second Schmitt trigger is equal to R2. When the gate terminal receives a high voltage from the slow oscillator, R3 and R2 are connected in parallel causing the equivalent resistance across the Schmitt trigger to decrease to $R_T = \frac{R_2 \times R_3}{R_2 + R_3} = 1320\Omega$. This decrease in resistance periodically alternates the frequency from $\frac{1}{R_2 \times C_2 \times K} = 3030Hz$ to $\frac{1}{R_T \times C_2 \times K} = 5051Hz$.

3. PCB layout

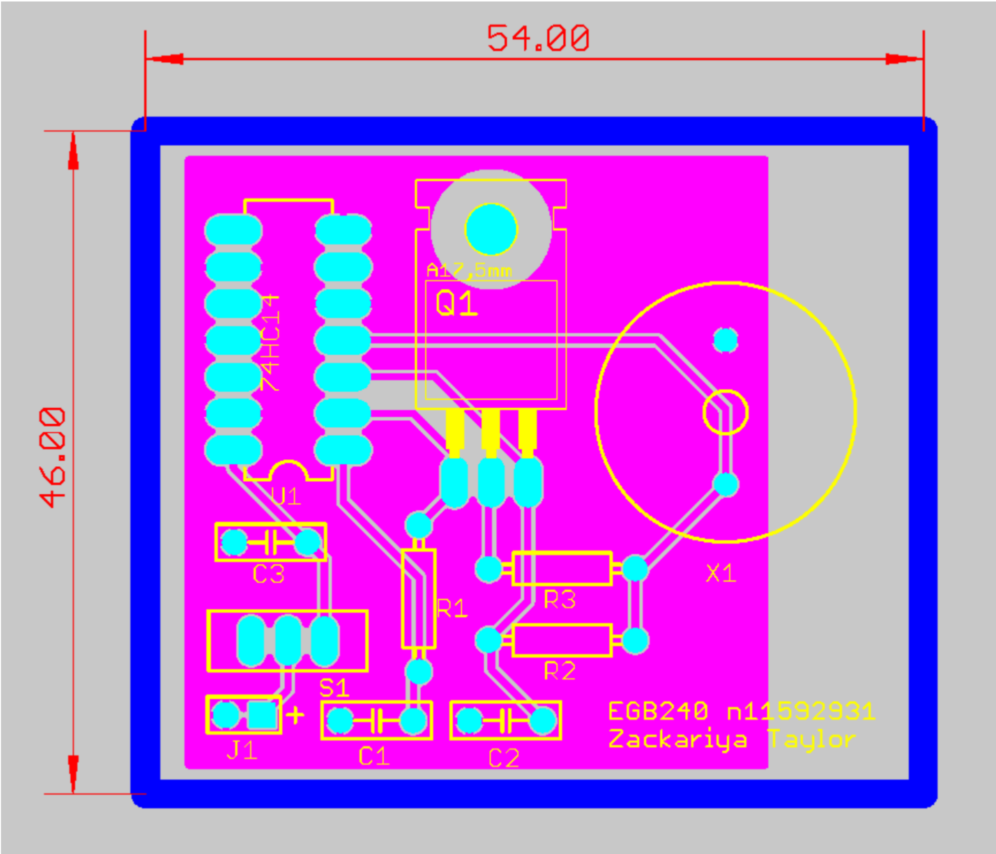


Figure 6: PCB layout of siren circuit (top side view), with board dimensions.

The board and schematic were designed in EAGLE. The tracks only occupy the bottom layer, for simplicity and low-cost production. As there were many ground points positioned throughout the board, this caused difficult track arrangement and 90-degree track angles. Narrow track angles can introduce electromagnetic interference (EMI) radiating at sharp corners, producing noise (Altium Designer, 2024). To overcome this issue a ground plane was used, this eliminates the need for long tracks and tracks with sharp corners. Although EMI is negligible at low frequencies, it was implemented into the design for reusability and versatility for higher-frequency applications.

4. Bill of materials

Designator	Value	Description	Quantity	Footprint
J1		Battery holder, 3V, 2xAA, flying leads	1	BATT-3V
C1	120n	Capacitor, Radial, Non-polarised	1	CAP-DISC-P5.08
C2	120n	Capacitor, Radial, Non-polarised	1	CAP-DISC-P5.08
C3	120n	Capacitor, Radial, Non-polarised	1	CAP-DISC-P5.08
Q1	IRF540	N-Channel Enhancement MOSFET (HEXFET);	1	IRF540
R1	3M3	Resistor, Axial, 0.25W	1	RESISTOR-AXIALHORIZONTAL
R2	2k2	Resistor, Axial, 0.25W	1	RESISTOR-AXIALHORIZONTAL
R3	3k3	Resistor, Axial, 0.25W	1	RESISTOR-AXIALHORIZONTAL
S1		Switch, SPDT, Slide, On-On, 0.1" pitch	1	SS-12
U1	74HC14	IC, Hex Schmitt trigger INVERTER, DIP-14	1	DIP-14
U1		IC socket, DIP-14	1	DIP-14
X1		Piezoelectonic buzzer	1	PS1720P02

Table 1: Bill of Materials (BOM) for PCB siren circuit design (1).

Designator	Manufacturer	MPN	Supplier	SKU	MOQ	Price ($)
J1	Generic	Battery holder, 3V, 2xAA, flying leads	Jaycar	PH-9202	2	0.95
C1	Generic	100nF 35VDC Tantalum Capacitor	Jaycar	RZ6620	1	0.75
C2	Generic	100nF 35VDC Tantalum Capacitor	Jaycar	RZ6620	1	0.75
C3	Generic	100nF 35VDC Tantalum Capacitor	Jaycar	RZ6620	1	0.75
Q1	IOR	N-Channel, MOSFET, 100V, 33A, to 220AB	Element14	2565835	1	1.57
R1	Generic	3M3 Ohm 1W Metal Film Resistors	Jaycar	RR2858	2	0.68
R2	Generic	2.2k Ohm 0.5W Metal Film Resistors	Jaycar	RR0580	8	0.85
R3	Generic	3.3k Ohm 0.5W Metal Film Resistors	Jaycar	RR0584	8	0.85
S1	NKK Switches	SS12SDP4	Digikey	360-2922-ND	1	3.42
U1	Texas Instruments	SN74HC14N	Jaycar	ZC-4821	1	1.15
U1	Generic	IC socket, DIP-14	Jaycar	PI-6501	1	0.35
X1	TDK	PS1720P02	Element14	1669968	1	0.95

Table 2: Bill of Materials (BOM) for PCB siren circuit design (2).

5. Assembly overlay

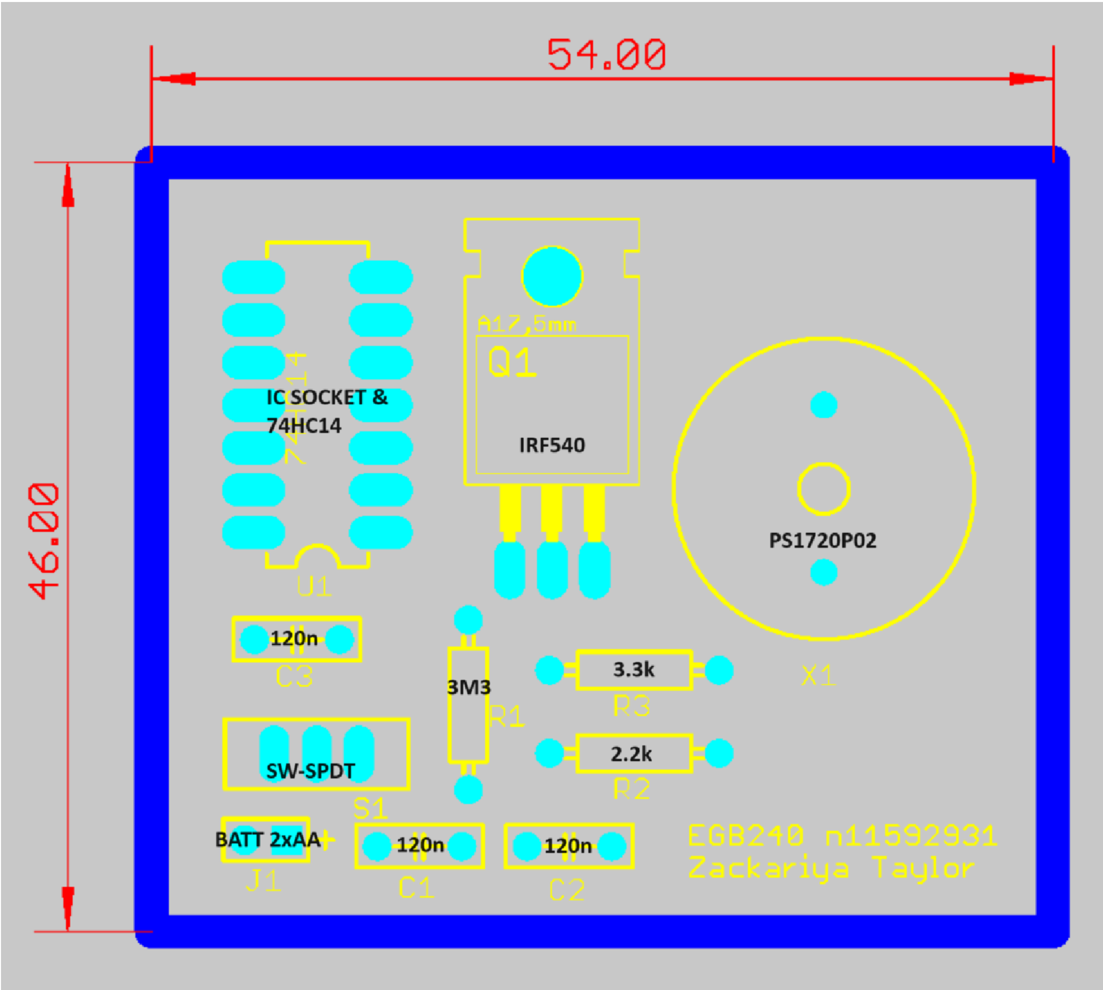


Figure 7: Assembly overlay and instructions for PCB siren circuit design.

An assembly guide can be seen in Figure 7. Ensure the IC socket is soldered onto the board prior to inserting the IC. Soldering the IC straight onto the board may cause damage to the chip due to the soldering iron (300 degrees), exceeding the chip's recommended operating temperature (125 degrees, see 74HC14 datasheet).

6. Photos of assembled prototype

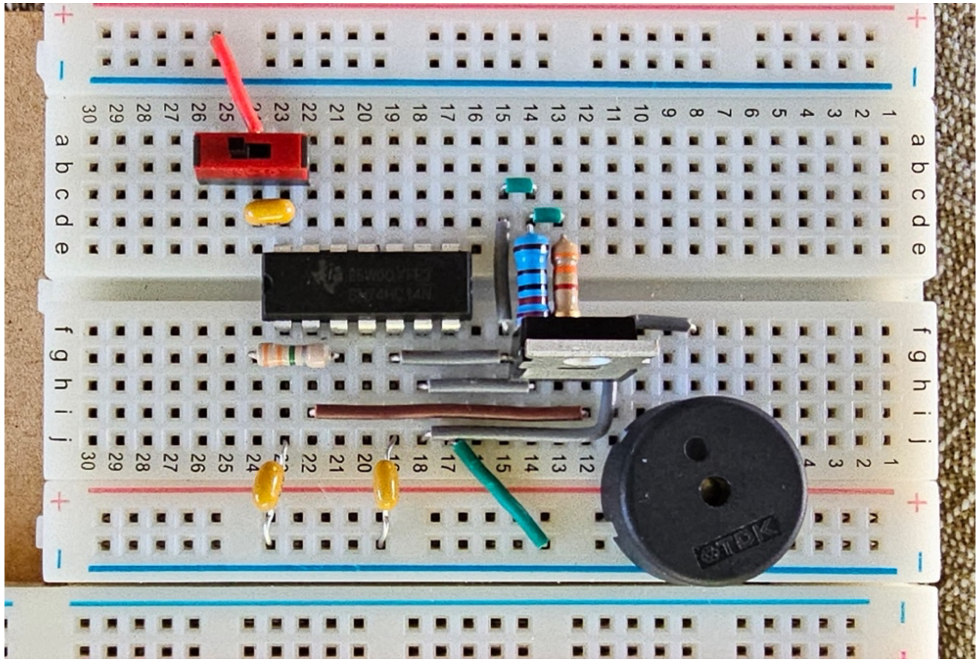


Figure 9: Assembled prototype of siren circuit design.

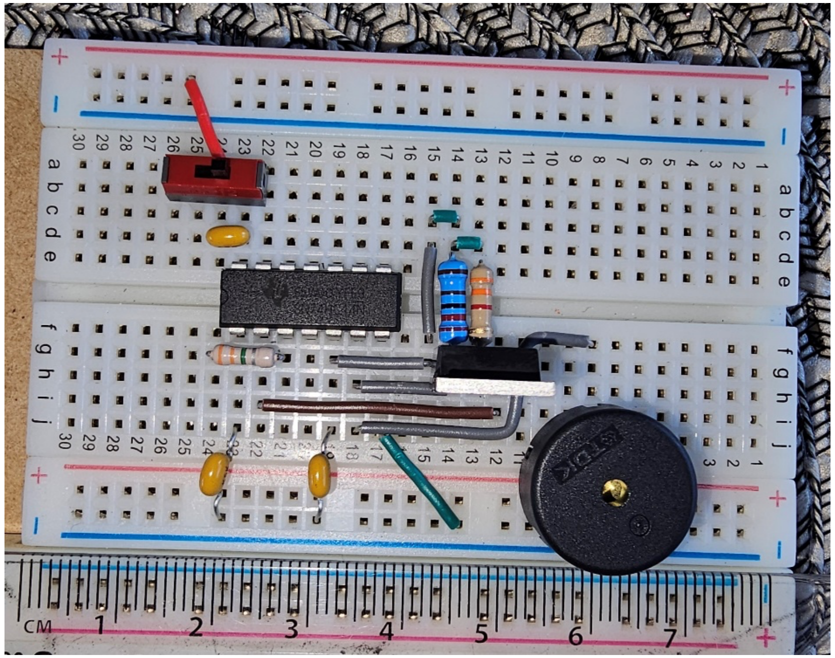


Figure 8: Assembled prototype with indicated scale (centimetres).

There are several benefits to prototyping a circuit design before fabrication. The siren was prototyped using a breadboard, this enables convenient modification, troubleshooting, and testing of design theories to determine the most optimal design (Mcl, 2024). The breadboard prototype was evaluated using an oscilloscope and compared against theoretical, and simulation results.

7. Simulation circuit and results

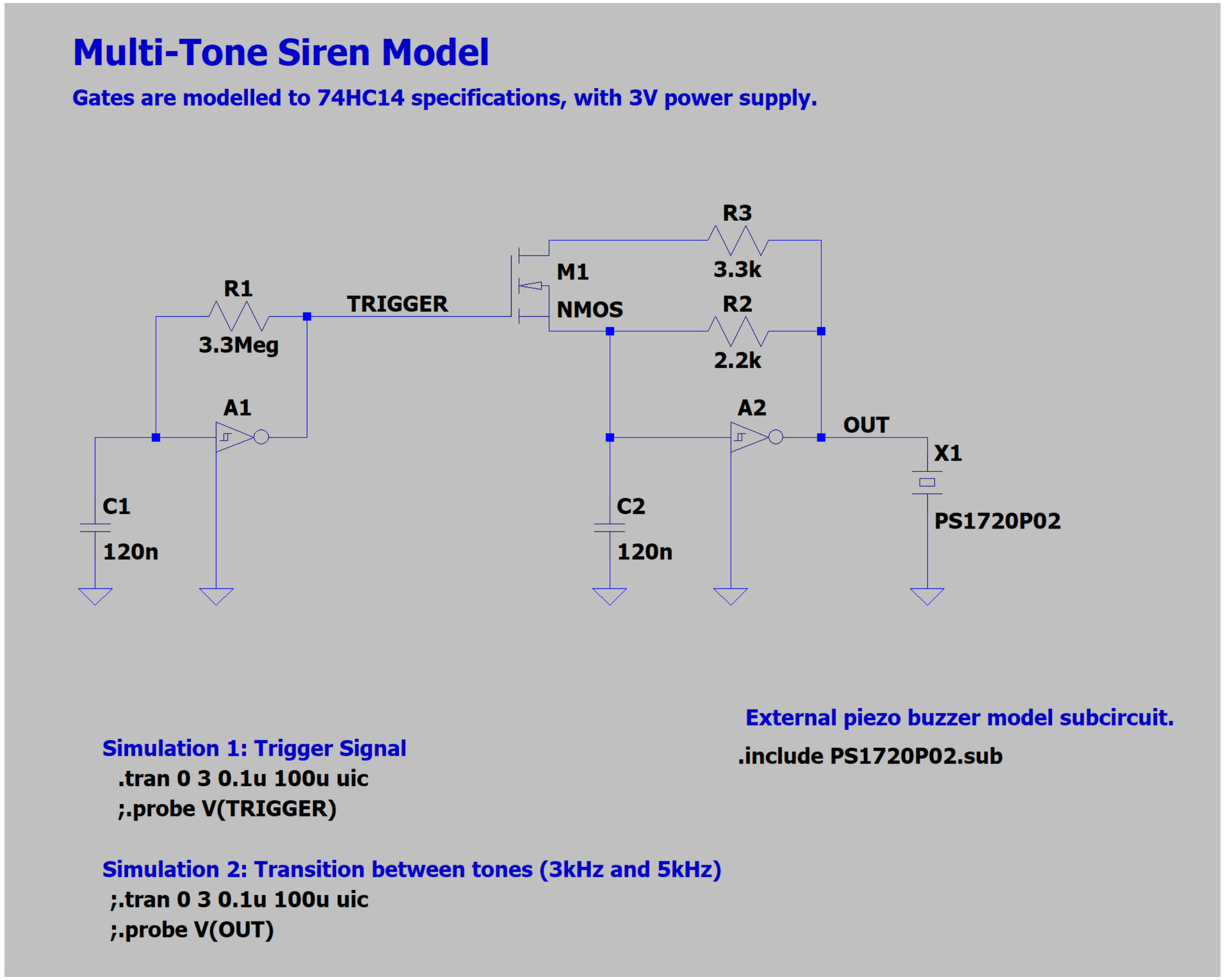


Figure 10: LTspice circuit model used to simulate and validate circuit design.

Simulation model netlist (LTspice)

LTspice netlist for the circuit model presented in Figure X:

```
A1 N002 0 0 0 0 TRIGGER 0 0 SCHMITT Vhigh=3 Rhigh=34 Rlow=41 Cout=200p Vt=1.27 Vh=0.40 td=31n
R1 TRIGGER N002 3.3Meg
C1 N002 0 120n
R3 OUT N001 3.3k
R2 OUT N003 2.2k
A2 N003 0 0 0 0 OUT 0 0 SCHMITT Vhigh=3 Rhigh=34 Rlow=41 Cout=200p Vt=1.27 Vh=0.40 td=31n
C2 N003 0 120n
XX1 OUT 0 PS1720P02

M1 N001 TRIGGER N003 N003 NMOS
.model NMOS NMOS
.lib C:\Users\zacka\AppData\Local\LTspice\lib\cmp\standard.mos
.tran 0 3 0.1u 100u uic
.include PS1720P02.sub

* Multi-Tone Siren Model
* Gates are modelled to 74HC14 specifications, with 3V power supply.
* External piezo buzzer model subcircuit.
* Simulation 1: Trigger Signal
* Simulation 2: Transition between tones (3kHz and 5kHz)

.probe V(OUT)
.probe V(TRIGGER)
.backanno
.end
```

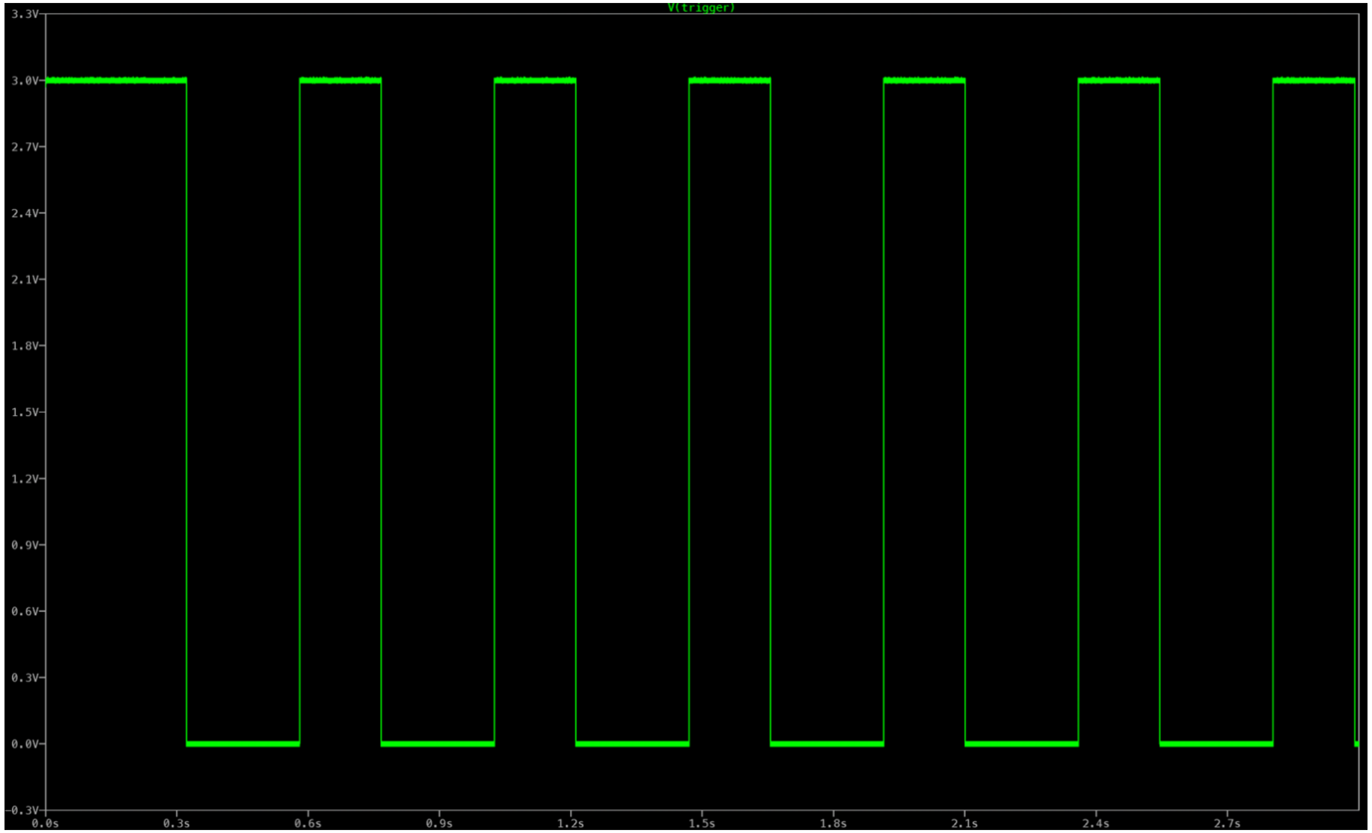


Figure 11: Plot of voltage v time for simulation 1.

Simulation 1 shows the output from the slow oscillator (trigger signal), which is driven into the gate pin of the MOSFET. The frequency of the simulated trigger signal was 2.25Hz and 49% duty cycle.

Unfortunately, simulation 2 was unable to produce expected results due to the IRF540 MOSFET not being available on LTspice. However, two equivalent circuits were created to replicate the on/off behaviour of the MOSFET.

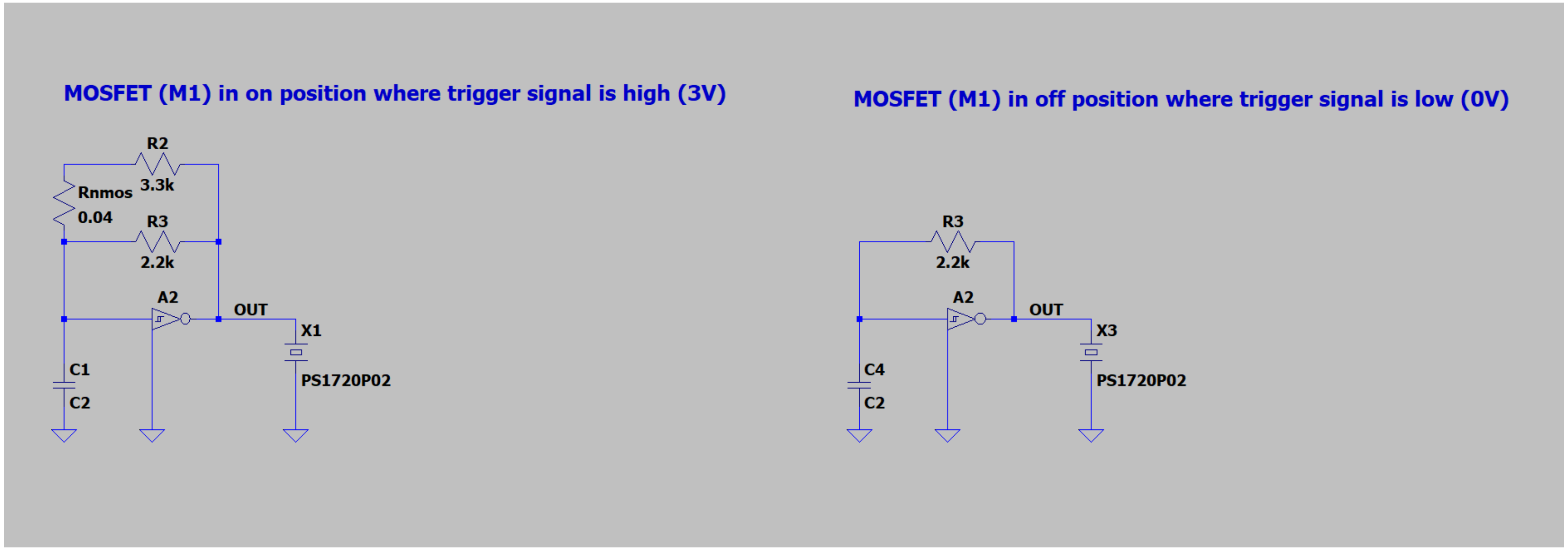


Figure 12: Equivalent circuits to replicate output behaviour.

‘Rnmos’ replicates the maximum resistance that the IRF540 MOSFET produces when it is on between the drain and source terminals.

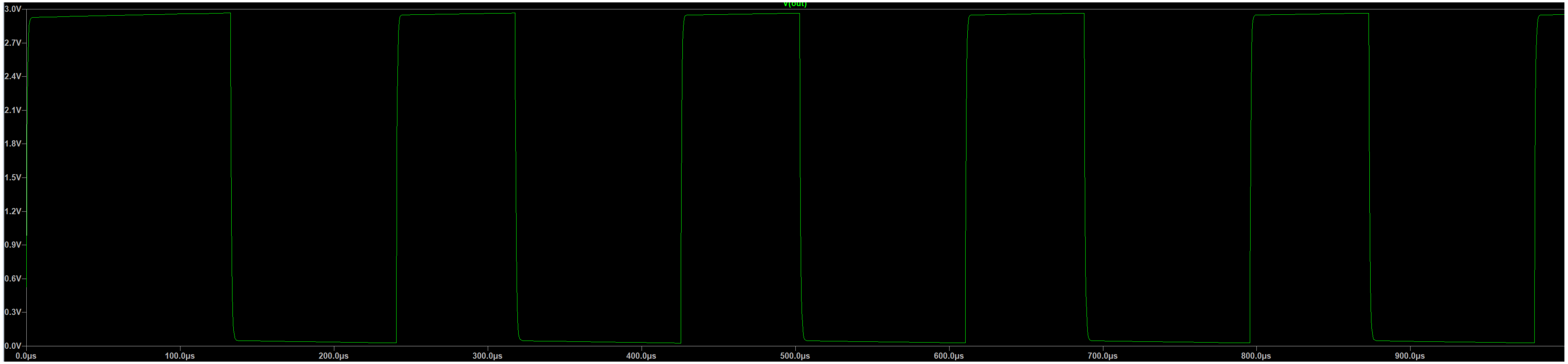


Figure 13: Simulation results when MOSFET on (5.4kHz, 41% duty cycle).

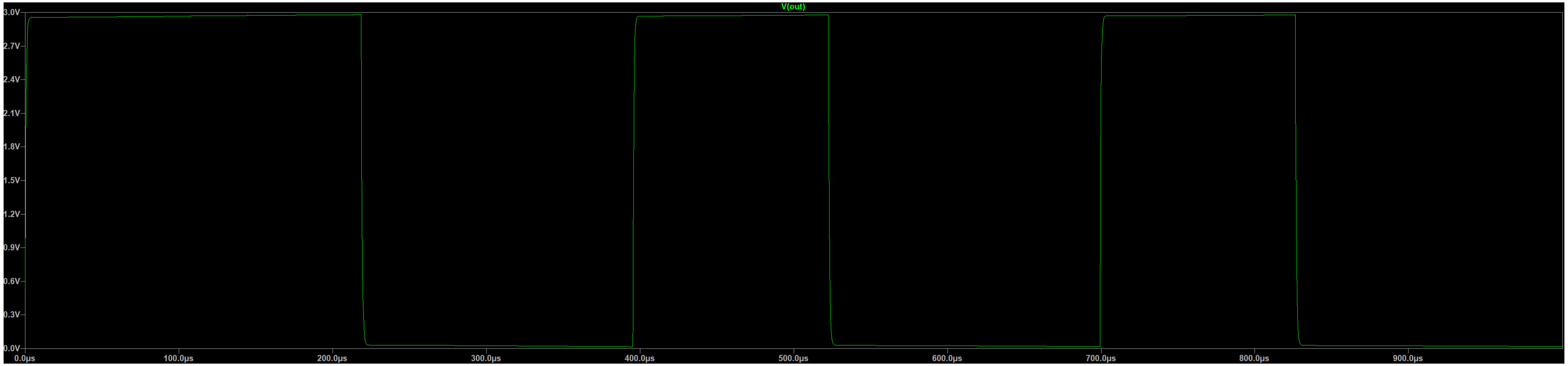


Figure 14: Simulation results when MOSFET off (3.3kHz, 41% duty cycle).

8. Experimental results

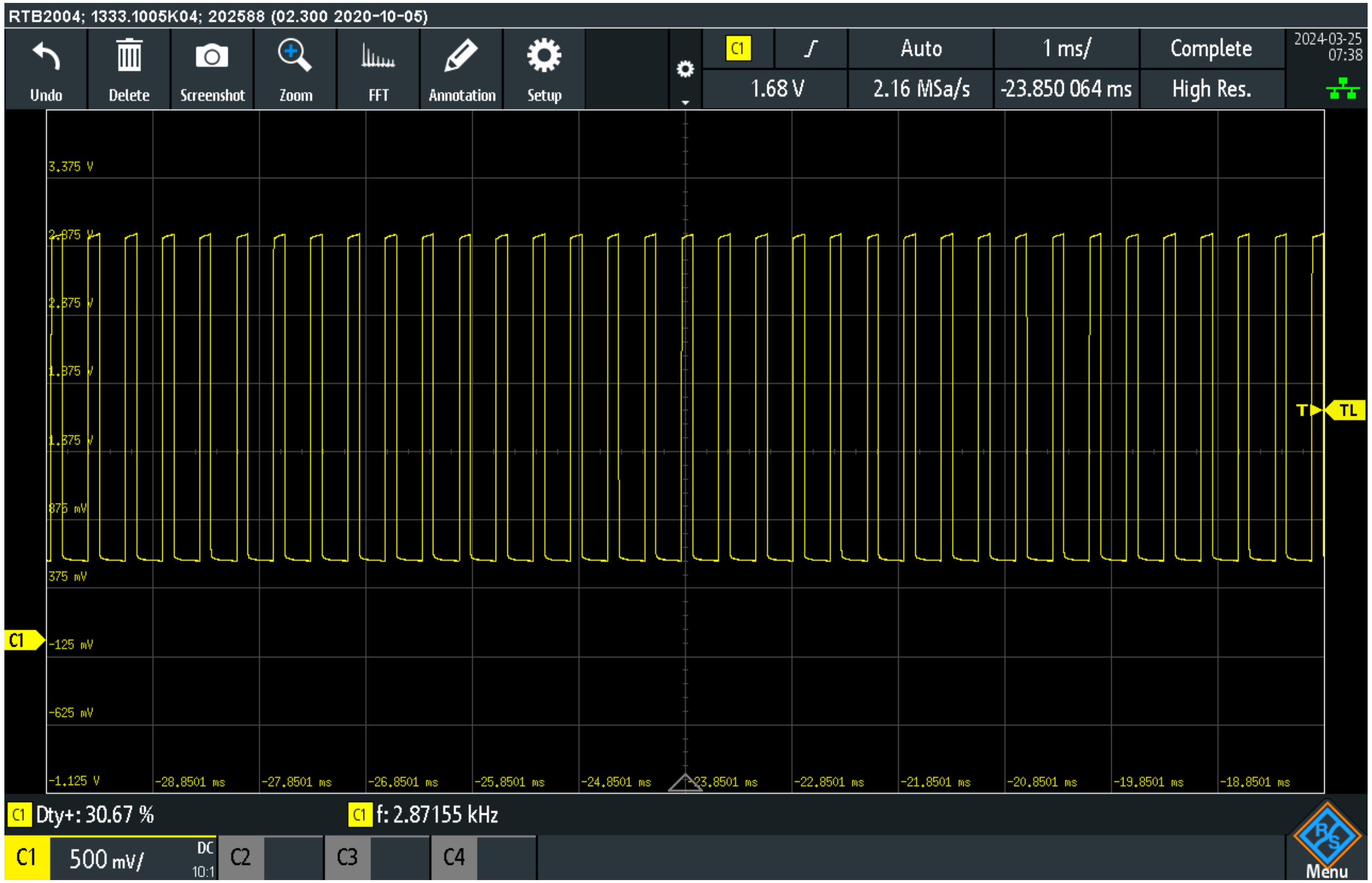


Figure 15: Oscilloscope reading of first frequency tone (2.87kHz and 31% duty cycle).

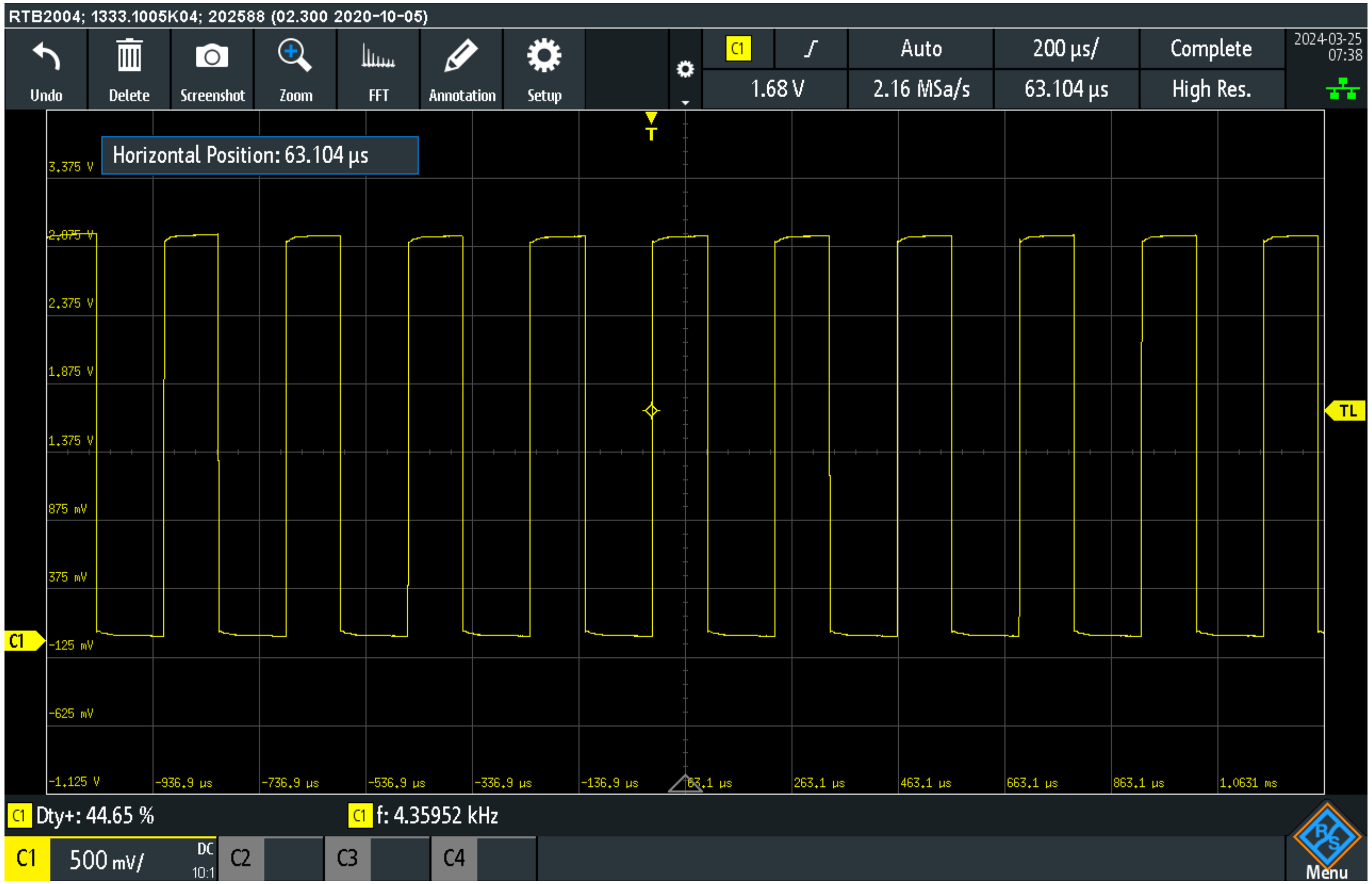


Figure 16: Oscilloscope reading of second frequency tone (4.4kHz and 45% duty cycle).

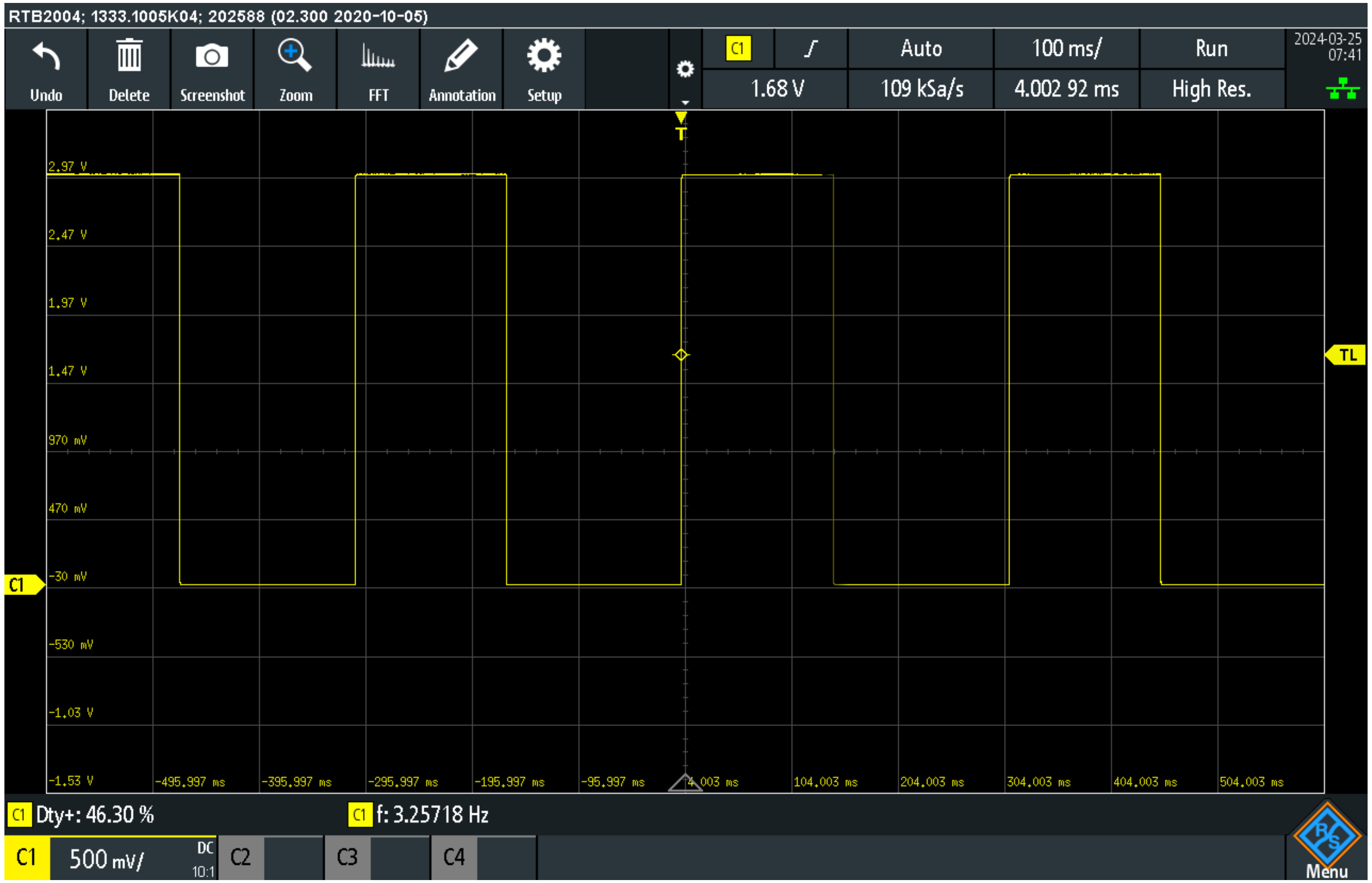


Figure 17: Oscilloscope reading of slow oscillator trigger signal (3.3Hz and 46% duty cycle).

Results comparison

	Theoretical	Simulation	Experimental
Slow oscillator frequency (Hz)	2.02	2.25	3.25
Slow oscillator duty cycle (%)		45	46
Tone 1 frequency (Hz)	3030	3300	2870
Tone 1 duty cycle (%)		41	31
Tone 2 frequency (Hz)	5051	5400	4350
Tone 2 duty cycle (%)		41	45

Table 3: Theoretical, simulation, and experimental results

Table 1 represents the differences in the values calculated and derived from theory and testing. The frequency observed from the LTspice simulation was on average a 9.1% increase in frequency. However, the experimental results for tones 1 and 2 were on average 9.6% less than expected, while the slow oscillator was 61% greater than the theoretical value.

The differences in theoretical and experimental values could be from the use of ideal components in calculations, component tolerances, or environmental factors. Although the differences in the output tones (less than 10%) are unrecognisable by the human ear, the 61% difference in the slow oscillator is unlikely to be caused by component tolerances and other factors and could possibly be the outcome of human error (bad connections in the breadboard, incorrect power supply parameters, etc). An improvement on the design would be to have the output tones going through a buffer, this may aid in correcting the frequency.

References

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