Visa Status: F1

Md Omar Faruque

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Personal Website
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Objective

Hardware security researcher working towards my PhD currently seeking internship roles leveraging 2+ years of academic and research background in VLSI design, verification, FPGA prototyping, RTL coding, neural network accelerator design, and deep learning frameworks. Knowledgeable in digital logic, computer architecture, analog circuits, digital signal processing, data mining, and deep learning algorithms. Passionate about contributing to projects involving SoC/IP/AI accelerator design, processor pipelines, memory architectures, analog/mixed-signal circuits, data analytics, and machine learning.

Education

- **New Mexico State University (NMSU)** — Las Cruces, NM, USA
  PhD in Electrical and Computer Engineering (ECE) — *Aug 2022 - Spring 2026 (Expected)*
  Major: Computer Engineering, CGPA: 3.81/4.00
- **Ahsanullah University of Science and Technology (AUST)** — Dhaka, Bangladesh
  BSc. in Electrical and Electronic Engineering (EEE) — *Jun 2015 - Aug 2019*
  Major: Electronics, GPA: 3.77/4.00

Skills Summary

- **Programming Languages**: C/C++, Python, MATLAB, Verilog HDL, TCL, Bash
- **EDA Tools & IDEs**: Cadence Virtuoso, Xilinx Vivado, Vitis HLS, OrCAD PSpice, Quartus Prime, HSPICE, PSpice
- **Microcontrollers & Dev Boards**: Arduino UNO, Xilinx Zybo Z7, Xilinx PYNQ-Z1, Basys 3, Intel Altera DE2
- **ML Frameworks & Libraries**: Scikit, TensorFlow, Keras, Numpy, Pandas, PyTorch, Hugging Face
- **Communication Protocols & Interfaces**: SPI, UART, IIC, Ethernet, TCP/IP, DNS, DHCP, SSH
- **Code Management and Deployment Platforms**: Git, Docker, Linux

Research Experience

- **Research Assistant at PEARL Lab** — May 2023 - Present
  Department of ECE, New Mexico State University — *Las Cruces, NM, USA*
  - **NN Accelerator Security**: Working on developing novel hardware trojan attacks for accuracy loss and developing countermeasures against various attacks on neural network accelerators.
- **Research Assistant** — Aug 2022 - May 2023
  Under the supervision of Dr. Wenjie Che, Department of ECE, NMSU — *Las Cruces, NM, USA*
  - **PUF Based Authentication**: Developed a technique to increase the entropy and reliability of a PUF-based authentication scheme. The proposed technique implemented on Xilinx Zynq7010 FPGA improves the portion of reliable (quadratically large) entropy bits by 20% and 100%, respectively, for different offset ranges. **(Paper Accepted, ISQED'23) | Presentation recording**

Professional Experience

- **Graduate Teaching Assistant** — Jan 2023 - Present
  Department of ECE, New Mexico State University — *Las Cruces, NM, USA*
  - **(EE 317) Semiconductors & Electronics, Spring'23, Fall'23** : Instructed 30+ undergrad students in practical labs related to the analysis and design of op-amp circuits, diode circuits, MOS and BJT amplifiers using spice simulators.
- **Lecturer** — Dec 2019 - Jul 2022
  Dept. of EEE, City University — *Dhaka, Bangladesh*
  - **Responsibilities**: Preparing course outline, course calendar and lesson plan for students; Conducting theoretical, tutorial, and practical classes; Preparing questions, invigilating tests and exams; Marking and grading scripts and assignments; Guiding and supervising project work, dissertation or thesis; Conducting research and experiments to advance knowledge in the respective field; Serving on Laboratory committee for the development of lab manual with equipment.
  - **Courses Instructed**: Power Electronics, Power Electronics Laboratory, Analog Integrated Circuits, Structured Programming Language (C++), Digital System Design Laboratory, VLSI Design Laboratory.

Selected Publications

- **Conference Paper**: **Md. O. Faruque** and W. Che, "Enlarging Reliable Pairs via Inter-Distance Offset for a PUF Entropy-Boosting Algorithm," 2023 24th International Symposium on Quality Electronic Design (ISQED), San Francisco, CA, USA, 2023, pp. 1-8. **Paper Link | Presentation Slides**
- **Conference Paper**: Md. R. Maruf, **Md. O. Faruque**, S. Mahmood, N. N. Nelima, Md. G. Muhtasim, and Md. Jahedul. A. Pervez, "Effects of Noise on RASTA-PLP and MFCC based Bangla ASR Using CNN," 2020 IEEE Region 10 Symposium (TENSYMP), 2020. [IEEE Region 10 flagship conference] **Paper Link | GitHub**
- **Conference Paper**: S. R. H. Remu, **Md. O. Faruque**, R. Ferdous, Md. M. Arifeen, S. Sakib, and S. M. S. Reza, "Naive Bayes based Trust Management Model for Wireless Body Area Networks" 2020 International Conference on Computing Advancements (ICCA), January 2020. [ACM] **Paper Link | GitHub**
- **Conference Paper**: **Md. O. Faruque**, T. Hasan, and S. Al Imam, "Performance comparison between Graphene Nano-Ribbon FET and conventional CMOS based on Arithmetic Logic Unit (ALU)," 2019 1st International Conference on Advances in Science, Engineering and Robotics Technology (ICASERT), May 2019. [IEEE] **Paper Link | Presentation Slides**

Relevant Coursework In Grad

- Hardware & Software Co-design
- Computer Architecture
- Analog VLSI Design
- Hardware Security and Trust
- Random Signal Analysis
- Data Mining

Relevant Coursework in Undergrad

- Power Electronics
- Analog Integrated Circuits
- Digital Logic Design
- Microprocessor and Interfacing
- VLSI I
- Digital Signal Processing
- Optoelectronics
- Solid State Devices
- Processing and Fabrication Technology

Certifications

- Deep Learning Specialization (Coursera)
- TensorFlow Developer Specialization (Coursera)
- High-Level Synthesis for FPGA (Udemy)

Projects

- **Cache Memory Simulator**: Wrote a trace-based cache simulator in C to implement various cache mapping, cache replacement and cache write policies. **Tech: C | GitHub**
- **Design and Implementation of a 32-bit MIPS CPU**: Designed and implemented a 32-bit multi-cycle MIPS RISC processor with pipelined datapath and FSM control unit in Verilog HDL. Simulated the functionality of the CPU using testbenches and synthesized the RTL on an FPGA for prototyping. **Tech: Verilog HDL, Vivado Design Suite, Xilinx Zybo Board | GitHub**
- **Physical Layout Design of a 4-Bit Arithmetic Logic Unit** : Designed a complete schematic and layout of a 4-bit Arithmetic Logic Unit (ALU) with seven different functionalities and performed LVS, DRC and STA analysis in gpdk090 technology using Cadence. **Tech: Cadence Virtuoso | Project Report**
- **Face Mask and Temperature Detection Door Security**: Developed a face detector model using Single Shot Detector (SSD) architecture and transfer learning to detect the presence or absence of a face mask and control the door accordingly. The results show that the model performs well on the test data with 100% and 99% precision and recall. **Tech: OpenCV, Python**
- **Customer Query Intent Prediction with Fine Tuning a Pretrained Transformers Model**: Utilized RoBERTa pretrained model for intent classification, finetuning with 18K queries across 150 intents. Achieved 100% validation accuracy in just 20 minutes and demonstrated 96.6% accuracy on the test set via transfer learning. Employed multi-GPU parallel training with 2 GPUs and a batch size of 760 for accelerated RoBERTa fine-tuning. **Tech: Hugging Face Transformers Library, PyTorch, GPU Acceleration | GitHub**

Academic Honors

- **Runners Up, NMSU Data Mining Contest** — NMSU, USA
  Achieved 97% accuracy in customer query intent classification challenge — *2023*
- **Dean's List of Honor** — AUST, Bangladesh
  Awarded for the excellent undergraduate result of CGPA 3.75 or above — *2019*
- **Government Scholarship** — Bangladesh
  Received govt. scholarship in junior scholarship examination — *2009*