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Performance comparison between Graphene Nano-Ribbon FET & conventional CMOS based on Arithmetic Logic Unit (ALU)

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***Abstract*— This paper presents the implementation and analysis of GNRFET and Conventional CMOS based 1-bit and multi-bit Arithmetic Logic Unit (ALU). The simulation results calculated using HSPICE have reported to show 2.79% reduction in Propagation Delay (PD), 57.59% reduction in Average Power Consumption, 61.98% reduction in Power Delay Product (PDP) and 66.44% reduction in Energy Delay Product (EDP) for GNRFET base 1-bit ALU as compared to Conventional CMOS based 1-bit ALU at 32nm technology.**

Keywords—GNRFET, Power delay product, Energy delay product

I. INTRODUCTION

The advancement in IC technology rendering area optimized and fast ICs is primarily attributed to the MOSFET scaling theory. As the process technology reached the nanometer regime, silicon CMOS started developing short-channel effects which led to increased power dissipation. Much research has been conducted to find a potential replacement for Conventional CMOS. Graphene Nano-Ribbon Field-Effect Transistor (GNRFET) proved to be a potential replacement to traditional CMOS. Thus, analysis of the circuits built using GNRFET is necessary to demonstrate its merits. The driving engine for the exponential growth of digital information processing systems is scaling down the transistor dimensions. Although there are some improvements still at the end of the International Technology Roadmap for Semiconductors (ITRS) [1] roadmap industry needs more improved and fast switching devices compare to the current trend. With the introduction to new techniques in fabrication nanomaterials with carbon group are emerging in Field-effect transistors [2],[3]. They have very good electrical properties along with capabilities to be integrated. The most studied are carbon nanotube FETs (CNFETs) and graphene nanoribbon FETs (GNRFETs). Compared to cylindrical CNTs, GNRs can be grown through a silicon-compatible, transfer-free, and in situ process [4],[5]. Graphene [6] and carbon nanotube (CNT) [7] are the two carbon allotropes, which have become prominent contenders to substitute silicon in post-CMOS technology. With fast switching capability as 2D electron gas in graphene gives high velocity and concentration in carrier which makes large mobility and hence fast switching compared to traditional Si-based CMOS technology [8]. It makes the transistor current quite high as electrons are injected from the source and transit to the drain terminal [7],[8]. In this paper, an ALU has been designed with the emerging Graphene Nano Ribbon-based FET (GNRFET) at 32nm technology node. The results have been optimized by varying the number of graphene nanoribbons (GNRs). Lastly, the results are compared with a CMOS based ALU to get a realistic idea of its performance, as compared to the state of art technology. Delay, Power & Power-Delay Product (PDP) and energy-delay product (EDP) has been chosen as parameters of comparison between the aforementioned devices. The MOSFET type GNRFET model has been used for simulation purposes on the HSPICE platform.

II. GNRFET MODELING

This paper explores circuit-level simulations by using the SPICE models of MOS-GNRFETs from [10],[11]. We simulated the ideal cases of MOS-GNRFETs and Si-based CMOS technology. In MOS-GNRFET circuits, a contact resistance of 20 kΩ is added to all graphene-metal vias. The 32nm Si-CMOS libraries from Predictive Technology Models (PTM) are adopted as comparisons, and the GNRFETs are set to have matching dimensions. The impacts of supply voltage and process variation are evaluated on 1-bit arithmetic and logical unit and the performance of the design is evaluated. Table I defines the default values and their definitions.

TABLE I. DEVICE PARAMETER DEFINITIONS AND USED VALUES

Device Parameter	Description	Used values
L	Physical channel length	32nm
T_{OX}	The thickness of top gate dielectric material	0.95nm
nRib	The number if GNRs in the device.	6
N	The number of dimmer lines in the GNR lattice	12
dop	Source and Drain reservoirs doping fractions	0.001
T_{OX2}	Oxide thickness between channel and substrate/bottom gate	20nm
2*sp	The spacing between the edges of two adjacent GNRs within the same device.	2.0nm

III. ARITHMETIC LOGIC UNIT DESIGN

The ALU that have been implemented in this paper performs arithmetic operations such as addition & subtraction and logical operations such as AND & OR. In the 1-bit ALU shown in Fig. 1, the logical operations are performed by the 2 input AND & OR gate while the arithmetic operations are performed by the full adder-subtractor unit. The output 'S/D' of the full adder-subtractor unit indicates

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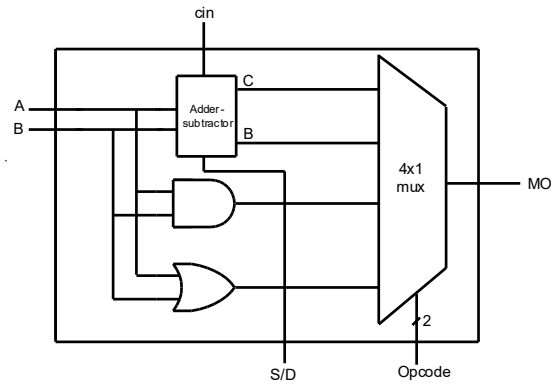

Fig. 1. *Block Diagram of 1-bit ALU.*

'Sum/Difference' bit as they are both the same in the case of addition and subtraction operations. The output 'C' of the full adder-subtractor unit indicates 'Carry' bit in case of addition operation and output 'B' indicates 'Borrow' bit in case of subtraction operation. The 2-bit opcode of 4x1 mux selects the result of either logical or arithmetic block which will be the output 'MO' of the ALU. The following Table II summarizes the select lines and operations performed by the ALU.

TABLE II. ALU OPERATION

Opcode		**Operations**
S_0	**S_1**	
0	0	ADD
0	1	SUB
1	0	AND
1	1	OR

IV. RESULT AND DISCUSSION

Timing diagrams of Fig. 2, Fig. 3 and Fig. 4 represents the arithmetic and logical operations of GNRFET and MOSFET based 1-bit ALU. In arithmetic unit operation A, B & Cin are the three input pins and S_0 and S_1 are the opcodes. The unit operates addition when the opcode is in 00 combinations and works subtraction when it is in 01 combinations.

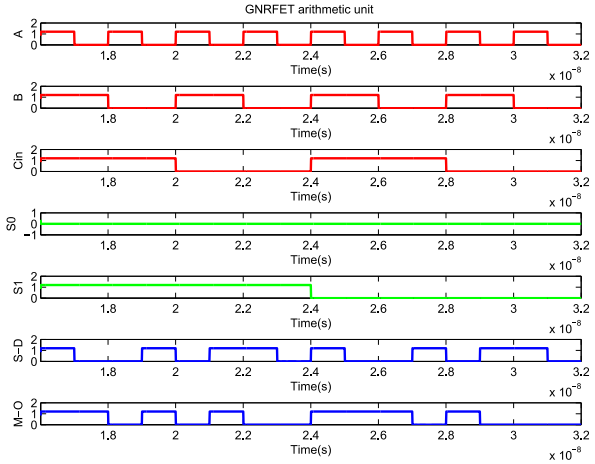

Fig. 2. *Arithmetic unit timing diagram for GNRFET*

The 1-bit ALU based on the University of Illinois (UIUC) MOS-GNRFET model is implemented and analyzed at 32nm technology. Another 1-bit ALU based on 32nm Berkeley Short-channel IGFET Model (BSIM4) for bulk CMOS is also implemented and analyzed for comparison, both having the same design. The ALU circuits are designed using static logic and simulated in HSPICE with a supply voltage of 1.2V. In logical unit operation, both opcodes are varied to get different logical operations. ALU performs AND operation where the output is high only when both inputs are high. In addition to different combinations, the unit performs OR operation with high output when one or more of its input is high. The resultant output performs different performance analysis with two sets of unlike structure. The results are compared at the nominal voltage of 1.2V and the number of nanoribbons is kept equal to 6 for making dimensions of GNRFET comparable to that of Si-CMOS. In this case, the delay of GNRFET based ALU is found to be 1.003ns whereas the delay of the Si-CMOS based is 1.031ns. Propagation delay has been taken between the 50% transition points of the input and output and hence calculated. Power consumption is another figure of merit for this ALU.

TABLE III. COMPARISON BETWEEN GNRFET AND MOSFET

Figure of Merit	**GNRFET (32nm) 1-bit**	**MOSFET (32nm) 1-bit**
Propagation Delay (PD)(s)	1.003×10^{-09}	1.031×10^{-09}
Average Power consumption (W)	6.498×10^{-06}	1.024×10^{-05}
Power delay Product (PDP)(J)	6.517×10^{-15}	1.056×10^{-14}
Energy delay Product (EDP)(Js)	6.537×10^{-24}	1.088×10^{-23}

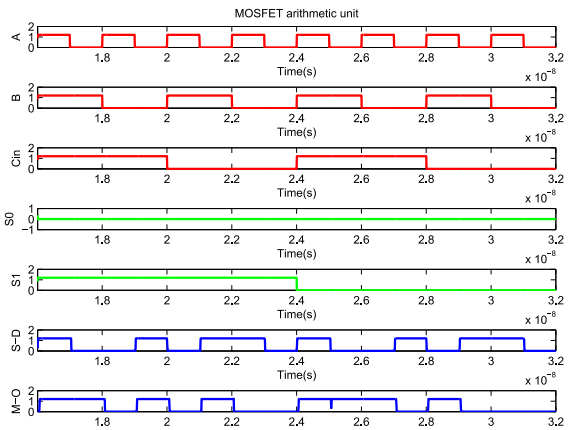

Fig. 3. *Arithmetic unit timing diagram for MOSFET.*

The results in Table III show that GNRFET based 1-bit ALU has 2.79% reduction in Propagation Delay (PD), 57.59% reduction in Average Power Consumption, 61.98% reduction in Power Delay Product (PDP), 66.44% reduction in Energy Delay Product (EDP) as compared to Conventional CMOS based 1-bit ALU. Simulation results have illustrated a substantial improvement in the performance of 1-bit 32nm GNRFET based design over 1-bit 32nm CMOS based design.

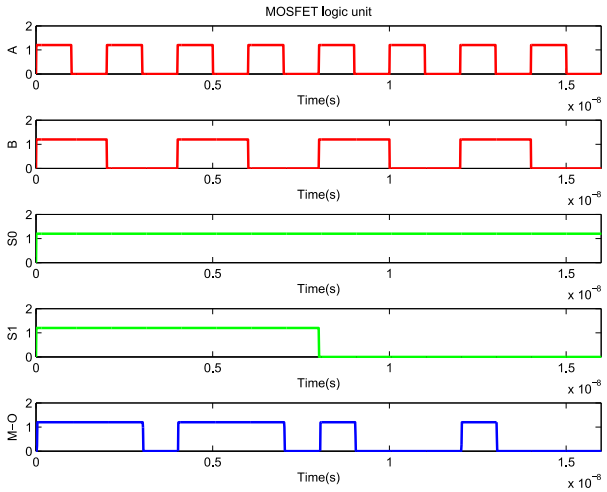

Fig. 4. *Logical unit timing diagram for MOSFET.*

TABLE IV. COMPARISON BETWEEN GNRFET(32NM) AND GNRFET(10NM) 1 BIT ALU.

Figure of Merit	**GNRFET (32nm) 1 bit**	**GNRFET (10nm) 1 bit**
Propagation Delay (PD)(s)	1.003×10^{-09}	1.002×10^{-09}
Average Power consumption (W)	6.498×10^{-06}	2.118×10^{-06}
Power delay Product (PDP)(J)	6.517×10^{-15}	2.122×10^{-15}
Energy delay Product (EDP)(Js)	6.537×10^{-24}	2.126×10^{-24}

Simulation results tabulated in Table IV show that GNRFET (10nm) based 1-bit ALU has 0.09% reduction in Propagation Delay (PD), 67.41% reduction in Average Power Consumption, 67.44% reduction in Power Delay Product (PDP), 67.48% reduction in Energy Delay Product (EDP) as compared to GNRFET (32nm) based 1-bit ALU. From Table V, GNRFET (32nm) based 2-bit ALU has 1.22% reduction in Propagation Delay (PD), 28.14% increase in Average Power Consumption, 27.28% increase in Power Delay Product (PDP), 26.38% increase in Energy Delay Product (EDP) as compared to Conventional CMOS based 2-bit ALU.

TABLE V. COMPARISON BETWEEN GNRFET(32NM) 2 BIT AND MOSFET(32NM) 2 BIT ALU.

Figure of Merit	**GNRFET (32nm) 2 bit**	**MOSFET (32nm) 2 bit**
Propagation Delay (PD)(s)	5.507×10^{-09}	5.574×10^{-09}
Average Power consumption (W)	2.874×10^{-05}	2.065×10^{-05}
Power delay Product (PDP)(J)	1.583×10^{-13}	1.151×10^{-13}
Energy delay Product (EDP)(Js)	8.716×10^{-22}	6.416×10^{-22}

V. CONCLUSIONS

The performance analysis of a single-bit and multi-bit ALU is done with two different transistor structures and technology node in this paper. In case of 1-bit ALU based on 32nm technology, the paper reports a small percentage of reduction in PD along with more than 60% of average power consumption with a significant amount of PDP reduction on GNR based device over the conventional one. Reduction of feature size (to 10nm for GNRFET) leads to a small reduction in PD and a significant amount of reduction in EDP, PDP and average power as compared to 32nm based GNRFET. But in the case of 2-bit ALU, 32nm GNRFET based design shows a small reduction only in PD as compared to conventional 32nm based CMOS design. So, in the case of the 1-bit combinational unit, the performance parameter of graphene-based architecture has the upper hand over the Conventional CMOS based unit.

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