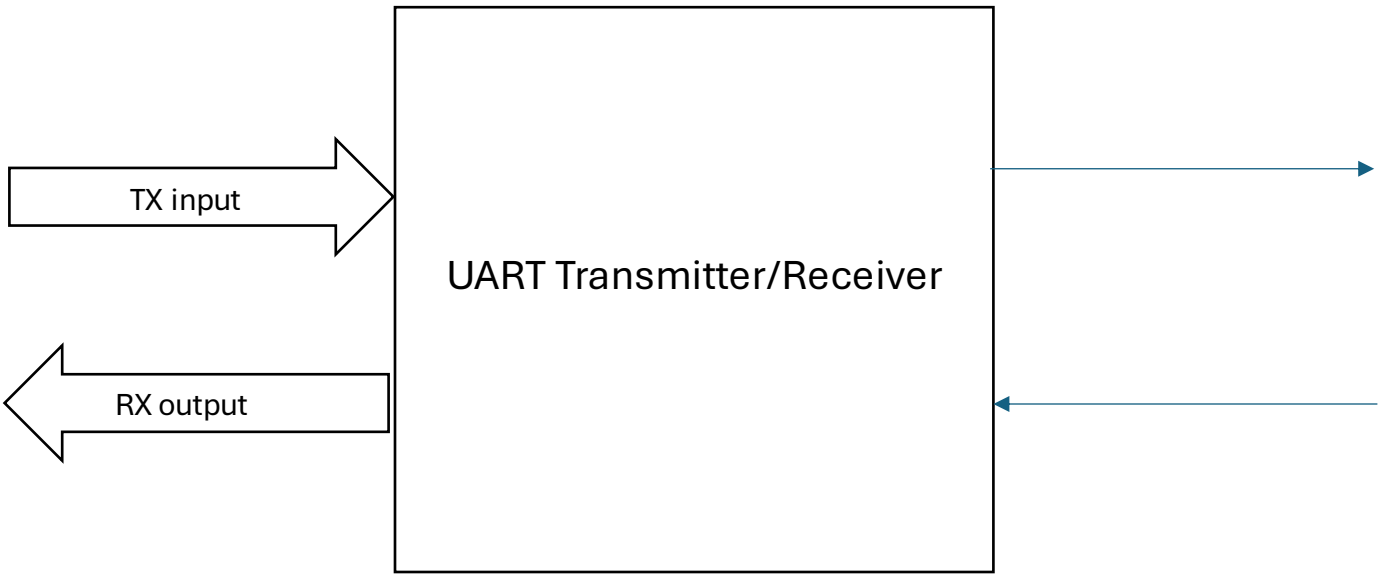
UART Transmitter & Receiver

Design a UART Transmitter/Receiver with both TX and RX paths.



TX PATH:

The TX path will have a synchronous parallel input with DATA_WIDTH bits and will be operating on valid ready protocol. Input will also have an error bit.

The output for the TX path will be a one-bit serial bus for UART protocol.

RX PATH:

The input for RX path will be 1 bit serial UART bus.

The output will be synchronous parallel bus with DATA_WIDTH bits and valid signal and error output.

Requirements:

The design will be running on 576 Khz clock.

The design should support the following data widths: 8,16,24,32.

You will have the following configurations for the design:

- parity per byte: if enabled the design will send a parity bit for each byte of data.
- Speed: UART should support the following rates (in KHz): 9600, 19200, 38400, 57600.