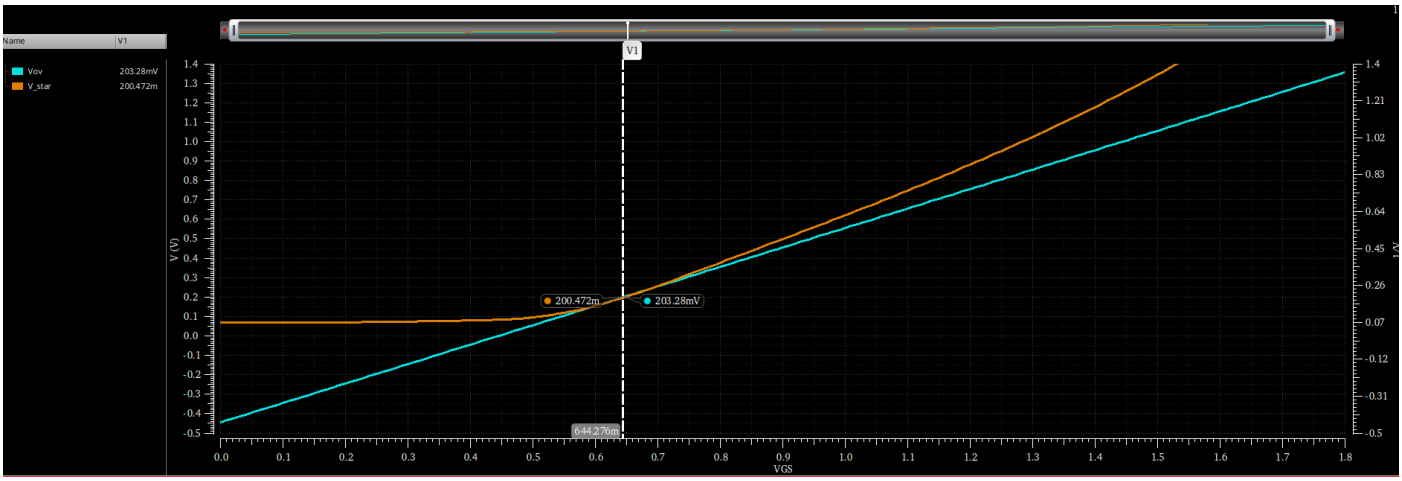
IEEE ASUSB AIC design Winter Workshop 2025 – LAB 3

Part 1: Sizing Chart

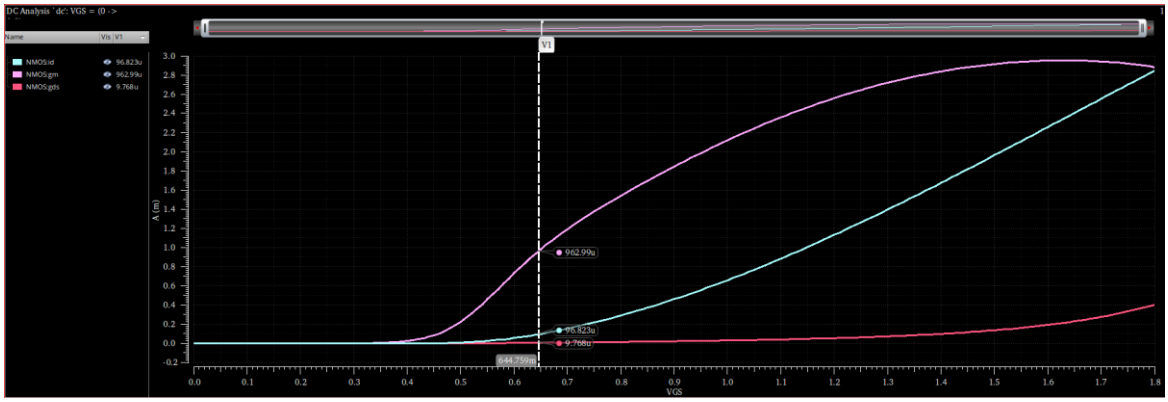
An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200mV$. *We want to design CS and cascode amplifiers with the parameters below. The given specs are* $L = 0.5um, V^* = 200mV, V_{DD} = 1.8V$ *and current consumption of* $20uA$.

The remaining variable in the design is to calculate W. *Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation. Create a testbench for NMOS transistor as shown below (we will use NMOS only in this lab). Use* $W = 10um$ *(we will understand why shortly) and* $L = 0.5um$ *(the same* L *selected before). Sweep* V_{GS} *from 0 to* $\sim V_{th} + 0.4$ *with* $10mV$ *step. Set* $V_{DS} = \frac{V_{DD}}{2}$. *We want to compare* $V^* = \frac{2I_D}{g_m}$ *and* $V_{OV} = V_{GS} - V_{th}$ *by plotting them overlaid. Use the calculator to create expressions for* V^* *and* V_{OV}. *You can save the expressions to reuse them later. Plot* V^* *and* V_{OV} *overlaid vs* V_{GS}. *Make sure the y-axis of both curves has the same range. An often used sweet-spot that provides good compromise between different trade-offs is* $V^* = 200mV$. *On the* V^* *and* V_{OV} *chart locate the point at which* $V^* = 200mV$. *Find the corresponding* V_Q^* *and* V_{GSQ}.



Required plot. $V_{OVQ} = 203mV$ *and* $V_{GSQ} = 644mV$.

Plot I_D, g_m, *and* g_{ds} *vs* V_{GS}. *Find their values at* V_{GSQ}. *Let's name these values* I_{DX}, g_{mX}, *and* g_{dsX}.



I_{DX}, g_{mX} and g_{dsX} at V_{GSQ}

Now back to the assumption that we made that $W = 10um$. *This is not the actual value that we will use for our design. But the good news is that* I_D *is always proportional to* W *irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be* $I_{DQ} = 20uA$ *as given in the specs. Calculate* W *as shown below.*

$W_X = 10um$	$I_{DX} = 96.8uA$
$W_Q = ??$	$I_{DQ} = 20uA$

$$W_Q \approx 2um.$$

Now we are almost done with the design of the amplifier. Note that g_m *is also proportional to* W *as long as* V_{OV} *is constant. On the other hand,* $r_O = \frac{1}{g_{ds}}$ *is* ***inversely*** *proportional to* W (I_D) *as long as* L *is constant. Before leaving this part, calculate* g_{mQ} *and* g_{dsQ} *using ratio and proportion (cross-multiplication).*

$W_X = 10um$	$g_{mX} = 963uS$
$W_Q = 2um$	$g_{mQ} = ??$

$$g_{mQ} = 192.6uS.$$

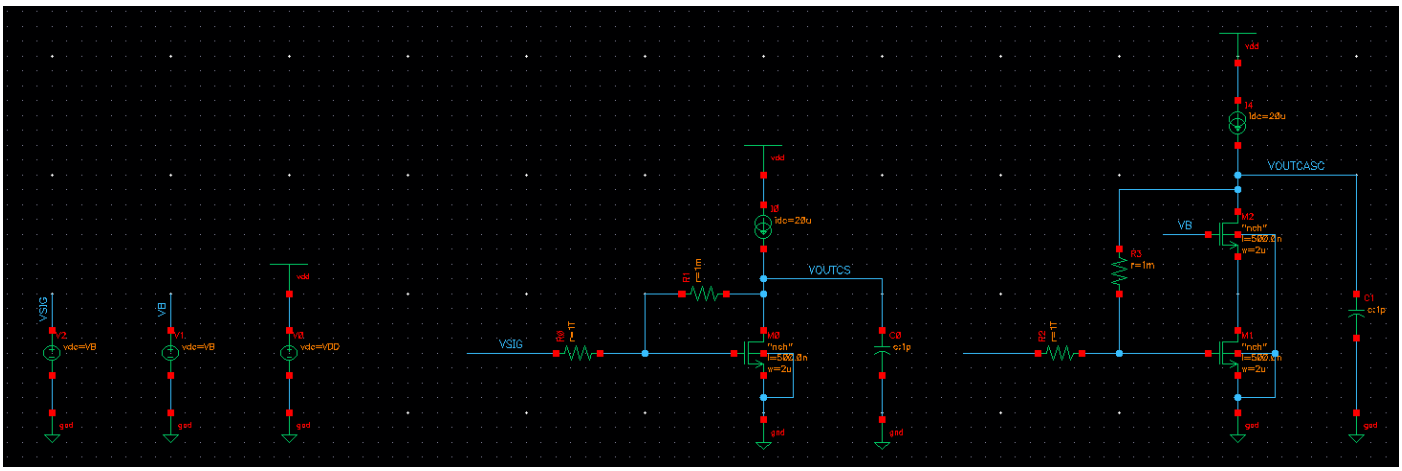
$W_X = 10um$	$g_{dsX} = 9.8uS$
$W_Q = 2um$	$g_{dsQ} = ??$

$$g_{dsQ} = 1.96uS.$$

PART 2: Cascode for Gain

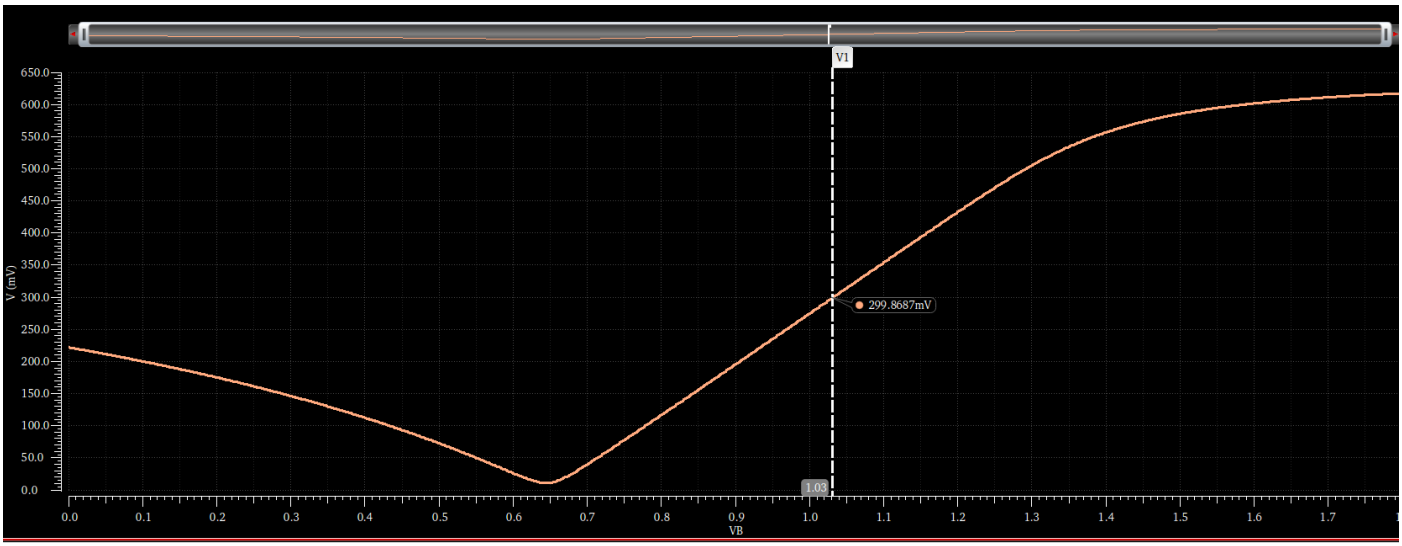
1. OP Analysis

Create a new cell and schematic. Construct the circuit shown below. Use $I_B = 20uA, L = 0.5um, W$ *as selected in Part 1, and* $C_L = 1pF$.



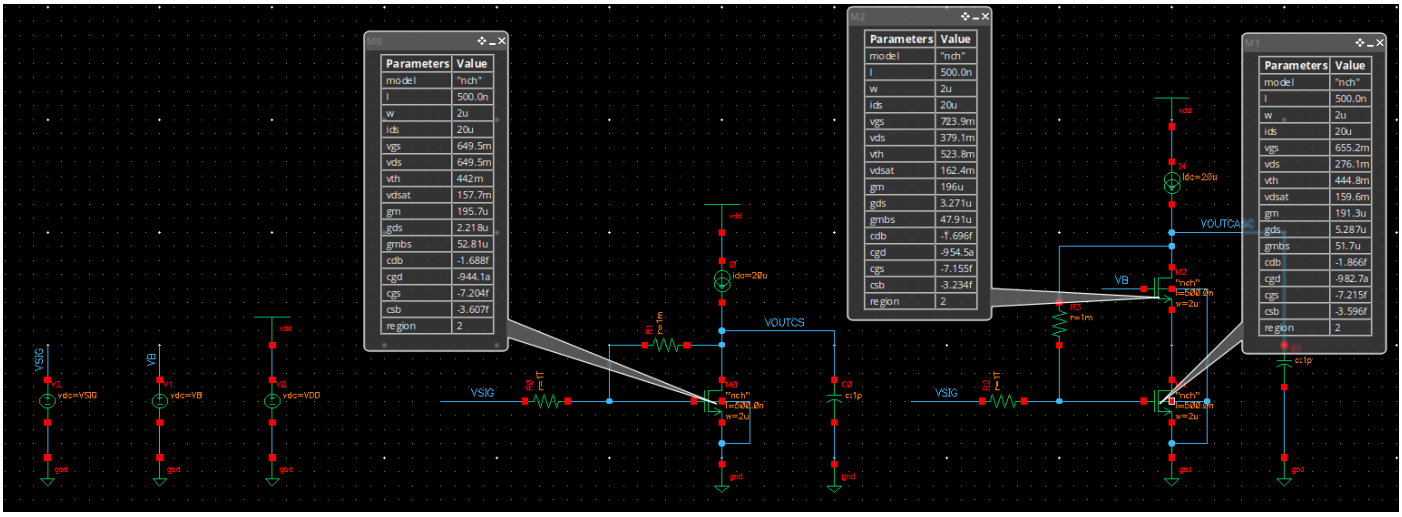
Required schematic

Choose V_B *(the cascode device bias voltage) such that* $M2$ *has* $V_{DS} = V^* + 100mV$ *(you may sweep* V_B *and plot* V_{DS} *vs* V_B *to help you choose a good value for* V_B*).*



V_{DS2} *VS* V_B*.* V_B *is chosen to be* $1V$

Simulate the DC OP point of the above CS and cascode amplifiers. Report a snapshot showing the following parameters for M1, M2 and M3 in addition to DC node voltages clearly annotated.



DC OP annotated on the schematic

Check that all transistors operate in saturation.

- All the devices are operating in saturation region, as indicated by region number "2".

Do all transistors have the same V_{th}*? Why?*

- The cascode device has a slightly higher threshold voltage due to the presence of a voltage difference between its source and bulk terminals (body effect).

What is the relation $(\ll, <, =, >, \gg)$ *between* g_m *and* g_{ds}*?*

- $g_m \gg g_{ds}$.

What is the relation $(\ll, <, =, >, \gg)$ *between* g_m *and* g_{mb}*?*

- $g_m > g_{mb}$.

What is the relation $(\ll, <, =, >, \gg)$ *between* C_{gs} *and* C_{gd}*?*

- $C_{gs} \gg C_{gd}$.

What is the relation $(\ll, <, =, >, \gg)$ *between* C_{sb} *and* C_{db}*?*

- $C_{sb} > C_{db}$.

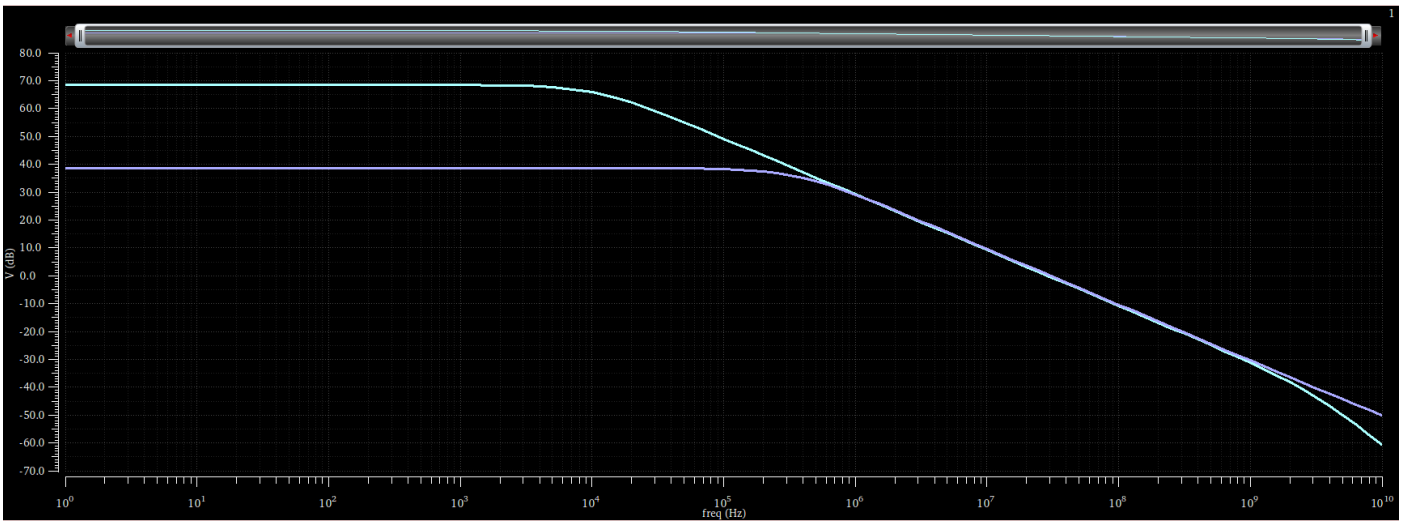
2. AC Analysis

Create a new simulation configuration. Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth. Use calculator to create expressions for circuit parameters (DC gain, BW, GBW, and UGF) and export them to adexl.

Test	Output	Nominal	Spec	Weight	Pass/Fail
IEEE_ASUSB:cascode:1	Ao_CS_dB	38.91			
IEEE_ASUSB:cascode:1	Ao_casc_dB	68.74			
IEEE_ASUSB:cascode:1	Ao_CS_mag	88.24			
IEEE_ASUSB:cascode:1	Ao_casc_mag	2.734k			
IEEE_ASUSB:cascode:1	BW_CS	352.4k			
IEEE_ASUSB:cascode:1	BW_casc	10.88k			
IEEE_ASUSB:cascode:1	GBW_CS	31.17M			
IEEE_ASUSB:cascode:1	GBW_casc	29.83M			

Required calculations

Report the Bode plot (magnitude) of CS and cascode ***appended on the same plot.***



Magnitude Bode plots for both CS and cascode stages

Using small signal parameters from OP simulation, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.

Quantity	*CS*	*Cascode*
DC gain	$A_v = g_m r_O = \frac{195.7u}{2.2u} \approx 88.95$	$A_v = g_{mi}[r_{Ocasc}(g_{mcasc}r_{Oi})] \approx 2140$
BW	$BW = \frac{1}{R_{out}C_L} \approx 350khz$	$BW = \frac{1}{R_{out}C_L} \approx 14kHz$
GBW	$\sim 31M$	$\sim 30M$

Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis.

Quantity	*Simulated*		*Calculated*	
DC gain	*CS:* 88.24	*Casc:* 2734	*CS:* 88.95	*Casc:* 2140
BW	*CS:* $352k$	*Casc:* $10.9k$	*CS:* $350k$	*Casc:* $14k$
GBW	*CS:* $31M$	*Casc:* $29.8M$	*CS:* $31M$	*Casc:* $30M$

Comment on the results.

- It is very clear that the addition of the cascode transistor has done the job predicted from it as the gain of the cascode stage is much higher than that of the CS stage. This gain boosting acquired by using the cascode is obtained on the behalf of the BW, since the GBWs of both stages are very close to each other. The deviation between simulation and hand calculations results of the cascode is due to some "overapproximating" the formulae used in the calculaitions.