IEEE ASUSB AIC Winter Workshop 2025 - LAB 4

Part 1: Sizing Chart

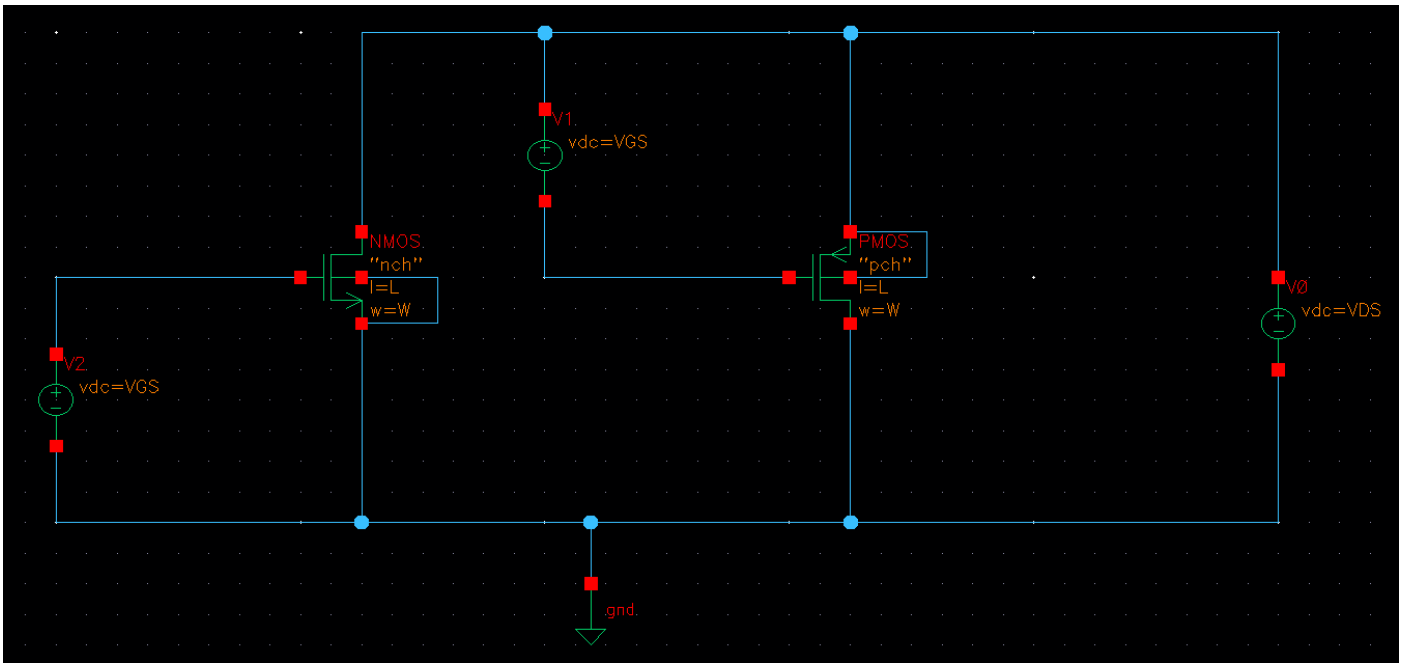
We want to design a differential amplifier with the specifications below (listed in lab instructions file). Note that the bias current is split between two transistors; each transistor gets $I_D = 20uA$. *Choose* R_D *to meet the CM output level spec.*

$$Given\ I_D = 20uA, V_{O,CM} = V_{R_D} = 0.7V \rightarrow R_D = \frac{V_{R_D}}{I_D} = 35k\Omega.$$

Choose V^* *to meet the differential gain spec.*

$$Given\ A_{vd} = \frac{2V_{R_D}}{V^*} = 8, V_{R_D} = 0.7V \rightarrow V^* = 175mV.$$

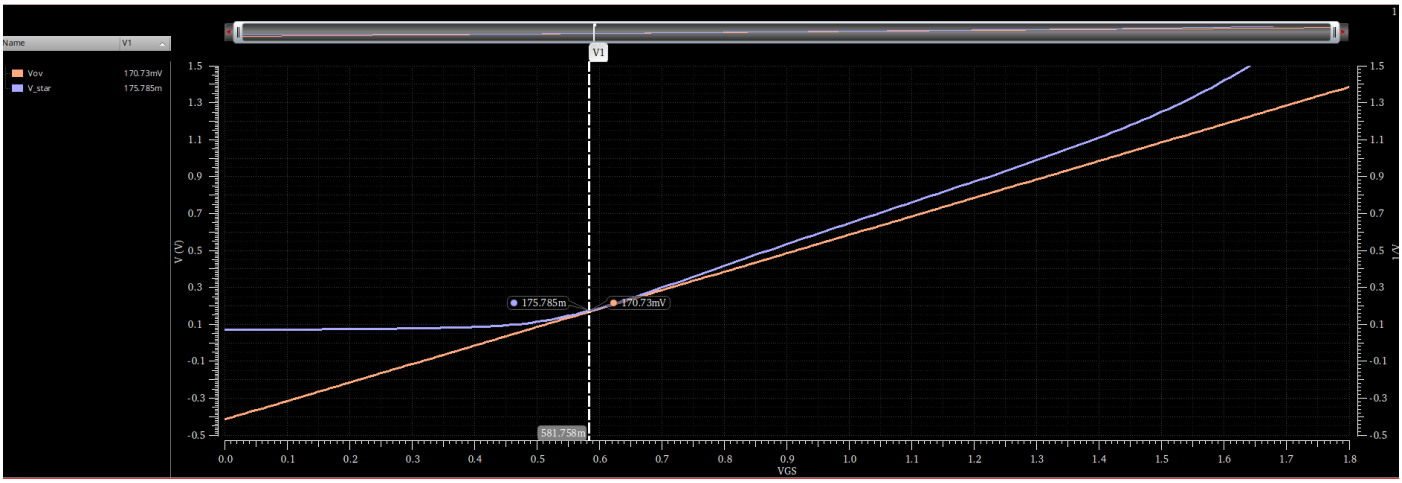
The remaining variable in the design is to calculate W. *Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation. Create a testbench for PMOS transistor as shown below (**we will use PMOS only in this lab**). Use* $W = 10um$ *(we will understand why shortly).*



Required testbench

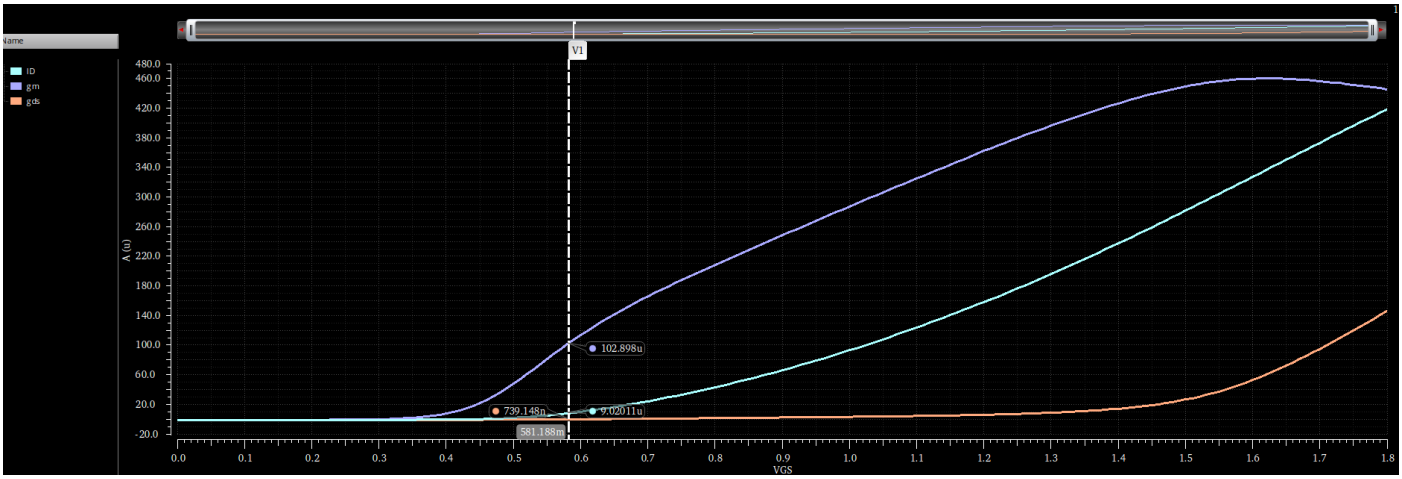
Sweep V_{GS} *from 0 to* $\sim V_{th} + 0.4V$ *with* $10mV$ *step. Set* $V_{DS} = \frac{V_{DD}}{2}$. *We want to compare* $V^* = \frac{2I_D}{g_m}$ *and* $V_{OV} = V_{GS} - V_{th}$ *by plotting them overlaid. Use the calculator to create expressions for* V^* *and* V_{OV}. *You can save the expressions to reuse them later. Plot* V^* *and* V_{OV} *overlaid vs* V_{GS}. *Make sure the y-axis of both curves has the same range. On the* V^* *and* V_{OV} *chart locate the point at*

which V^* is equal to the value your previously calculated to meet the gain spec. Find the corresponding V_{OVQ} and V_{GSQ}.



Required plot with a cursor positioned at required region

Plot I_D, g_m, and g_{ds} vs V_{GS}. Find their values at V_{GSQ}. Let's name these values I_{DX}, g_{mX}, and g_{dsX}.



ID, gm and gds VS VGS

Now back to the assumption that we made that $W = 10um$. This is not the actual value that we will use for our design. But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be I_{DQ} as given in the specs. Calculate W as shown below (in lab instructions file).

$W_X = 10um$	$I_{DX} = 9uA$
$W_Q = ??$	$I_{DQ} = 20uA$

$W_Q \approx 22um.$

Now we are almost done with the design of the amplifier. Note that g_m *is also proportional to* W *as long as* V_{OV} *is constant. On the other hand,* $r_O = \frac{1}{g_{ds}}$ ***inversely*** *proportional to* W (I_D) *as long as* L *is constant. Before leaving this part, calculate* g_{mQ} *and* g_{dsQ} *using ratio and proportion (cross-multiplication).*

$W_X = 10um$	$g_{mX} = 103uS$
$W_Q = 22um$	$g_{mQ} = ??$

$g_{mQ} \approx 227uS.$

$W_X = 10um$	$g_{dsX} = 740nS$
$W_Q = 22um$	$g_{dsQ} = ??$

$g_{dsQ} \approx 1.6uS.$

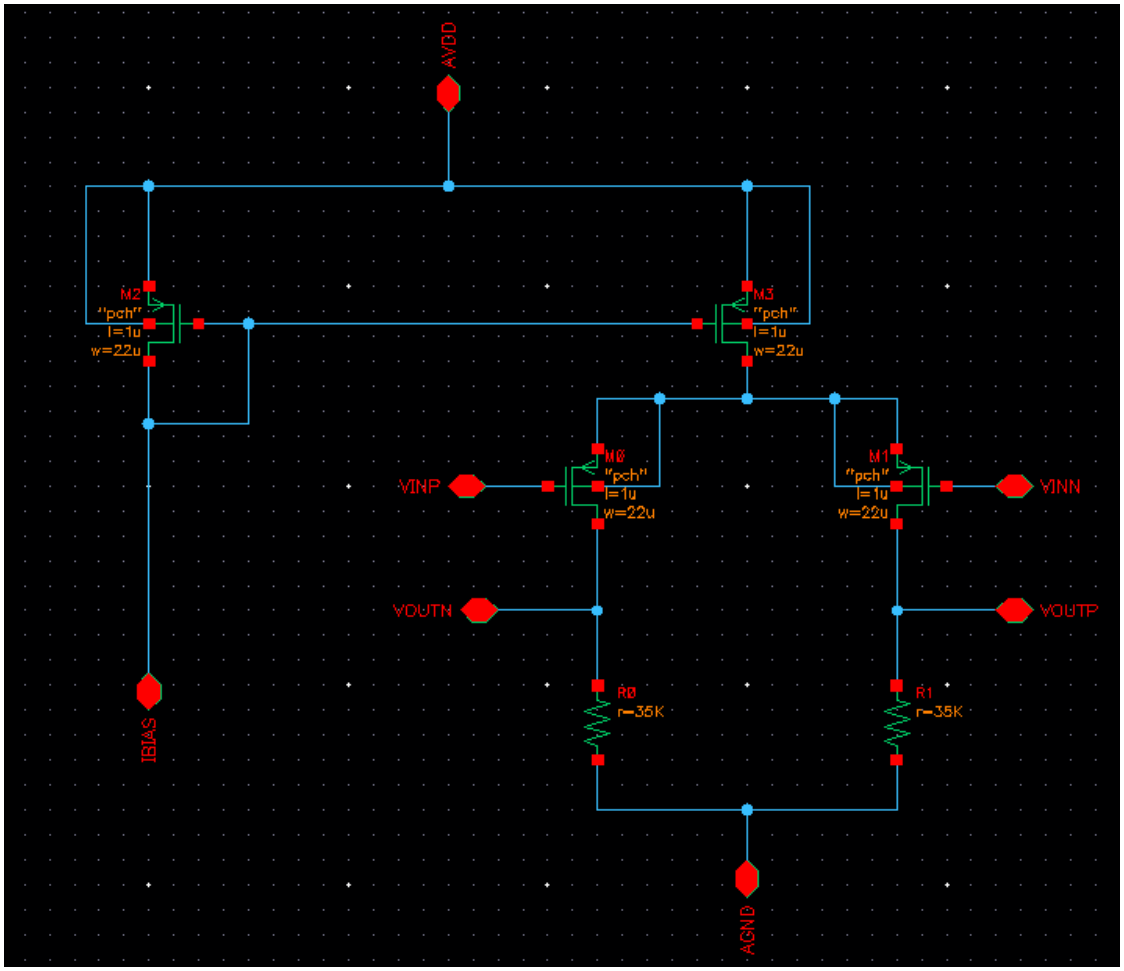
Part 2: Differential Amplifier

Create a new cell for the diff amp "lab_04_diff_amp".

Create the schematic of a differential amplifier with PMOS input stage and resistive load.

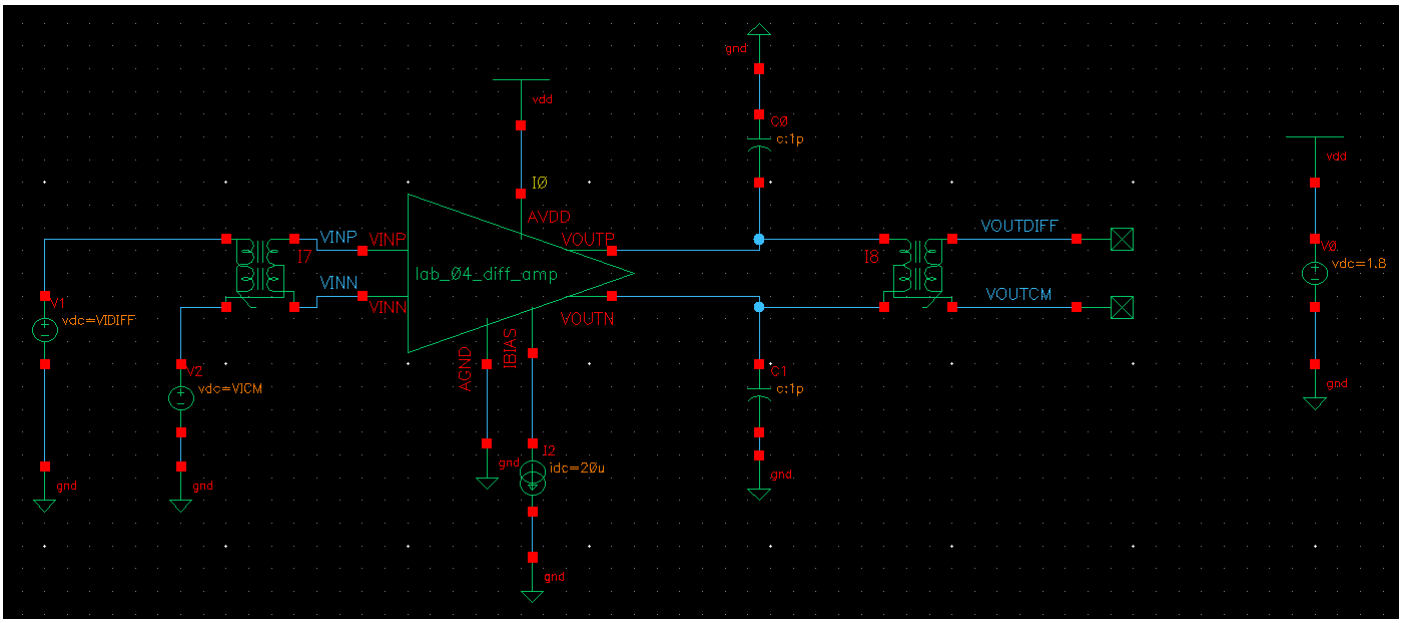
Use a simple current mirror for the bias current source as shown in the first figure in this document.

Create a symbol for the diff pair (use Create -> Cellview -> From Cellview). Edit the diff amp symbol to be as shown below.



Required schematic

Create a new cell for the testbench "lab_04_diff_amp_tb". Create testbench schematic as shown below.



Required testbench

Analytically calculate the valid range for Vicm: the common mode input range (CMIR). Set Vicm at the center of this range.

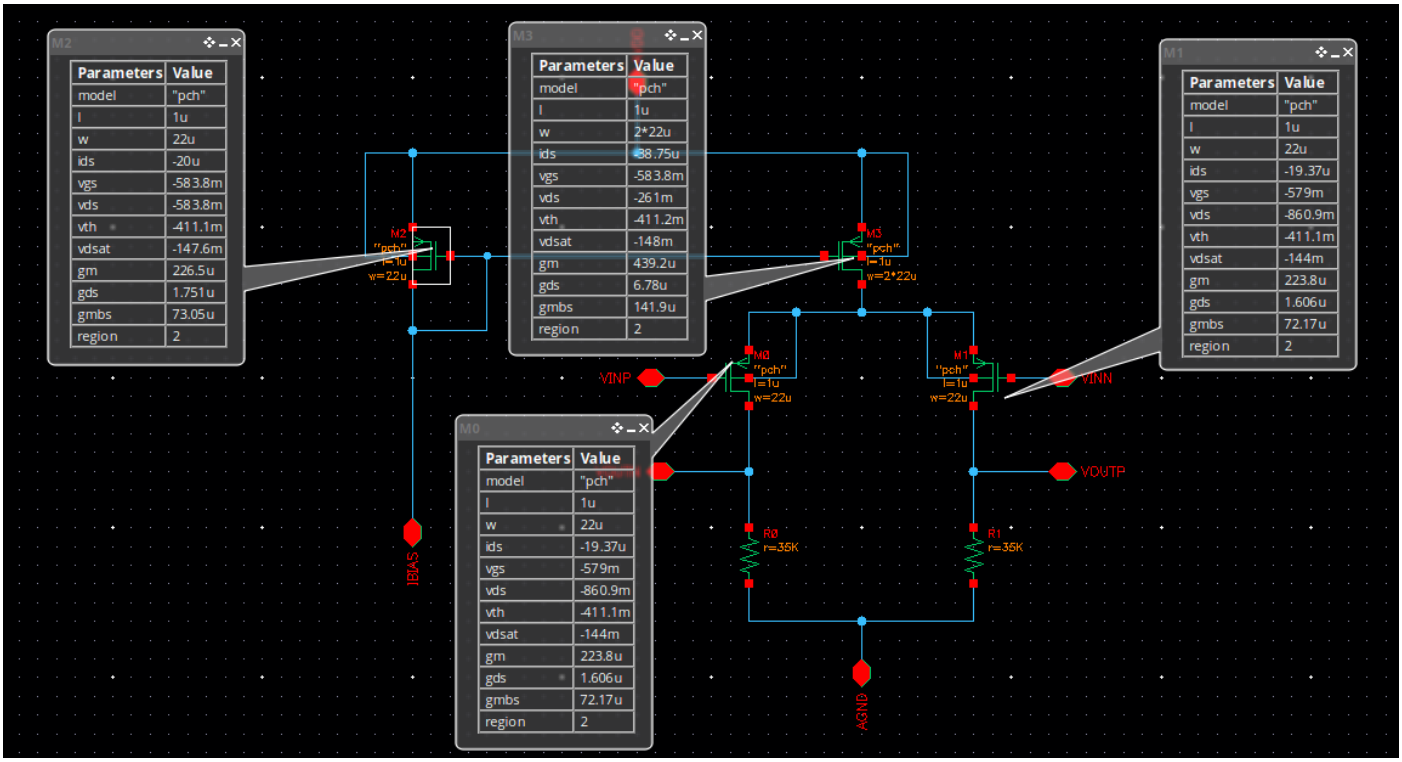
$$V_{DD} - V_{Dsat} > V_{iCM} > V_{oCM} - |V_{th}|$$
$$V_{DD} - V_{Dsat} \sim V_{DD} - V^* = 1.8V - 175mV = 1.625V.$$
$$V_{oCM} - |V_{th}| \approx 0.7 - 0.4 = 300mV.$$
$$1.625V > V_{iCM} > 300mV.$$
$$V_{iCM} = \frac{0.3+1.625}{2} \approx 960mV.$$

Report the following:

➔ *OP simulation*

Report the schematic of the diff pair with DC OP point clearly annotated: id, vgs, vds, vth, vdsat, gm, gds, gmb, region.

Check that all transistors operate in saturation.



Required snapshot

- *All transistors are operating in saturation, as indicated by "region" slot in the balloons.*

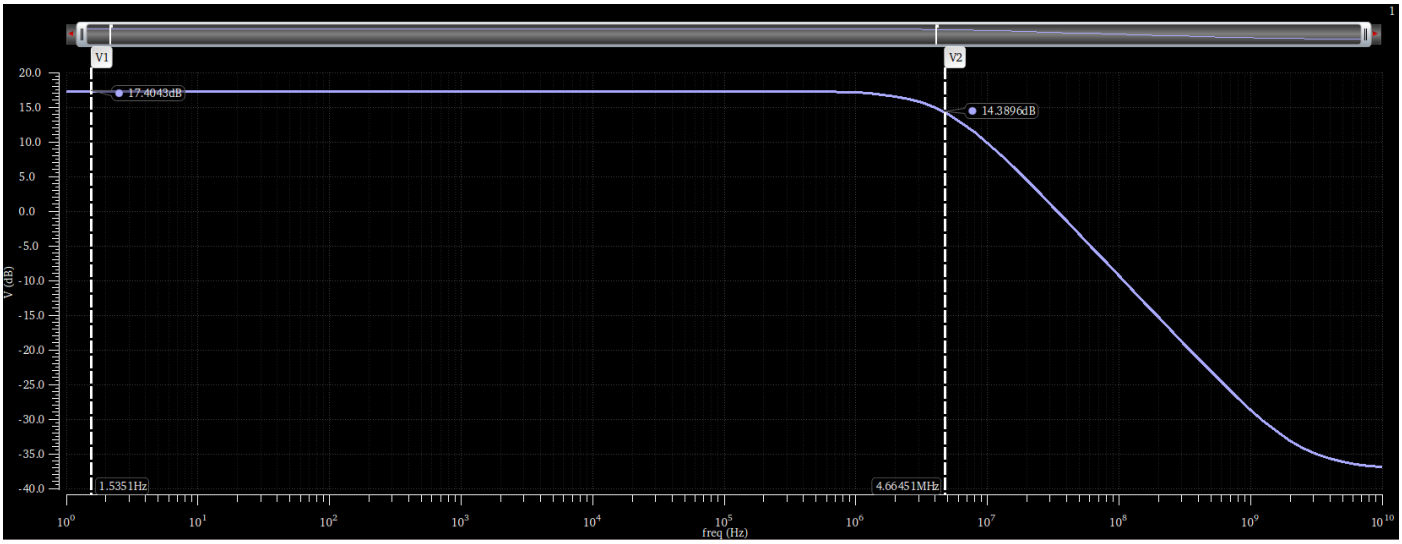
➔ ***Diff small signal ccs***

Use AC magnitude = 1 for the diff source (and AC magnitude = 0 for the CM source).

Set Vicm at the center of the CMIR.

Run AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).

Report the Bode plot of small signal diff gain.



Bode mag plot of small signal diff gain

Compare the DC diff gain and BW with hand analysis in a table.

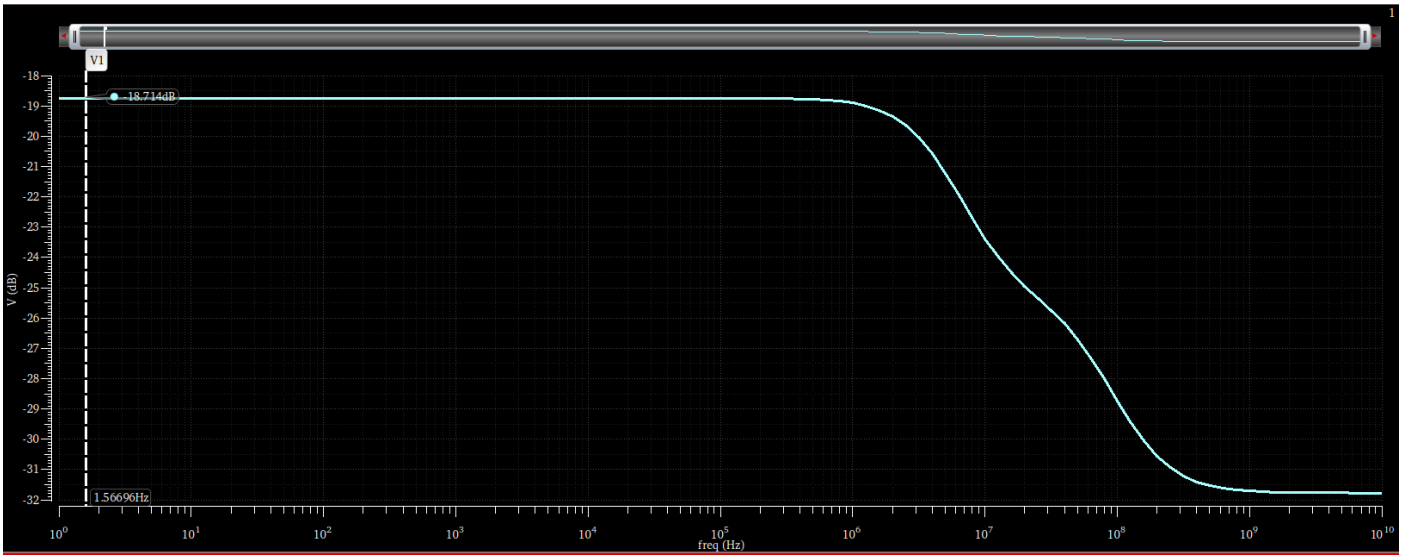
Quantity	*Simulated*	*Calculated*
DC gain	$\approx 17.5dB$	$\sim g_m R_D \approx 225u * 35k = 7.9 = 17.9dB$
BW	$\approx 4.7MHz$	$\approx \frac{1}{2\pi R_D C_L} = \frac{1}{2\pi * 1p * 35k} \approx 4.54M$

➔ ***CM small signal ccs***

Use AC magnitude = 1 for the CM source (and AC magnitude = 0 for the diff source).

Run AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).

Report the Bode plot of small signal CM gain.



Bode mag plot of small signal CM gain

Compare the DC CM gain with hand analysis in a table. Is it smaller than "1"? Why?

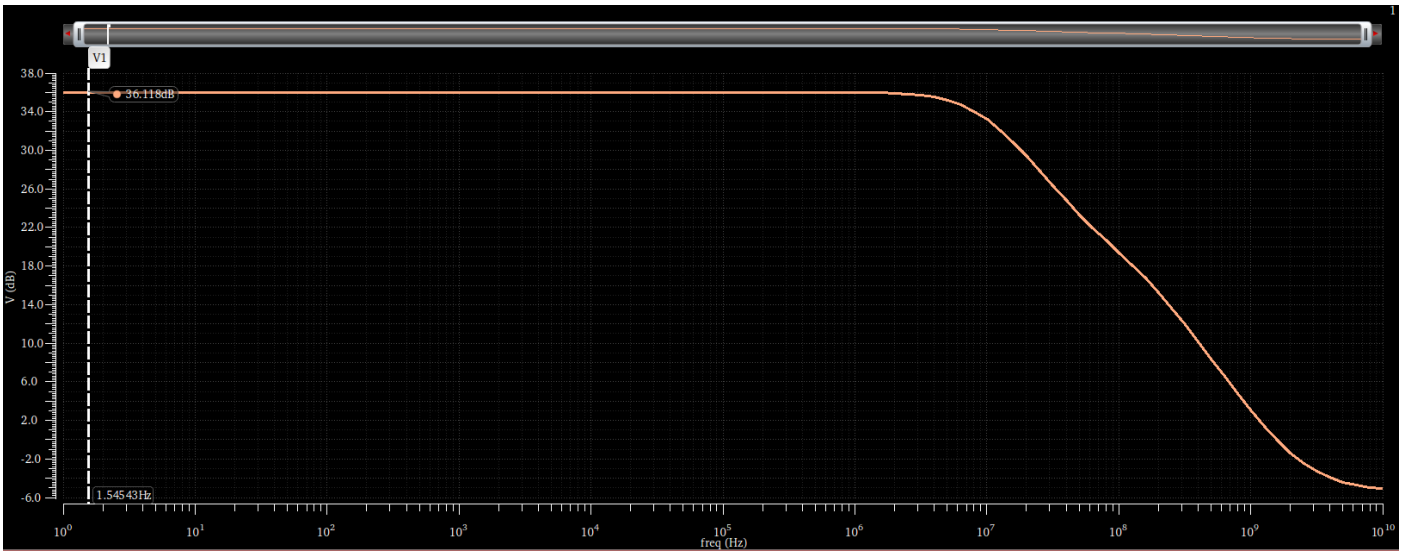
Simulated	*Calculated*
$-18.7dB$	$= \frac{g_m R_D}{1 + 2g_{me}R_{SS}} \approx 0.088 = -21dB$

- *It IS smaller than 1 due to half circuit principle that resulted in a large amount of degeneration in CM compared to diff operation.*

Justify the variation of A_{vCM} vs frequency.

- *The presence of capacitors connected to the o/p is translated into an o/p impedance which is frequency dependent, and this, in turn, affects the gain when frequency changes as the gain is a function of o/p impedance.*

Plot Avd/Avcm in dB. Compare Avd/Avcm @ DC with hand analysis in a table.



Required plot

Simulated	*Calculated*
$35dB$	$1 + 2g_m R_{SS} \approx 67.4 = 36.6dB$

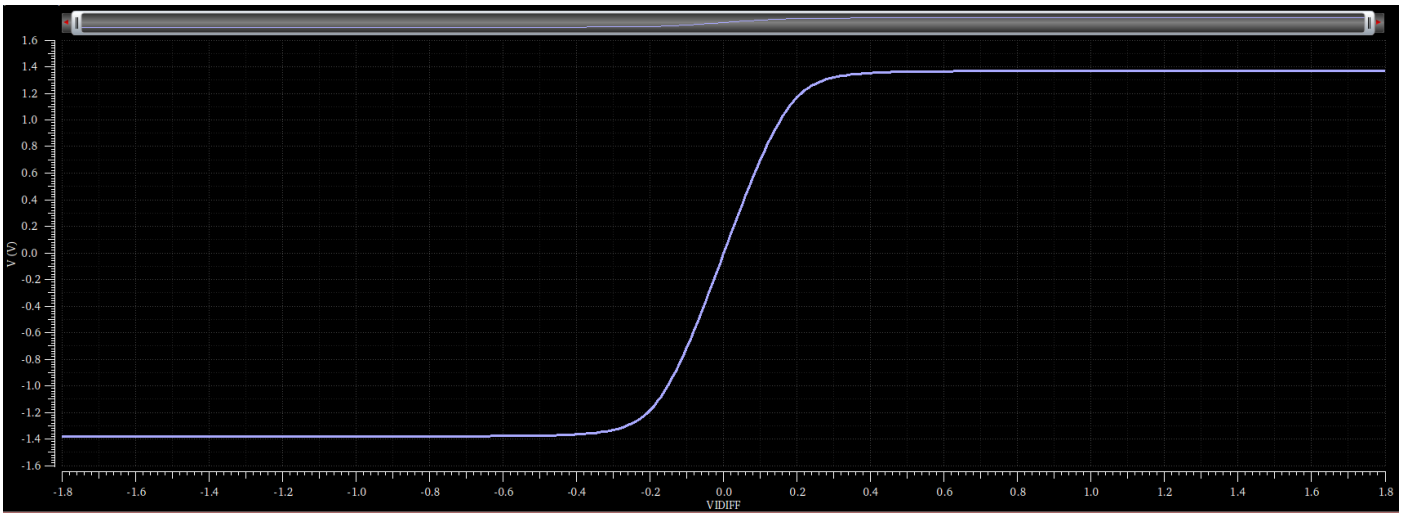
Justify the variation of Avd/Avcm with frequency.

- *The presence of capacitors connected to the o/p is translated into an o/p impedance which is frequency dependent, and this, in turn, affects the gain when frequency changes as the gain is a function of o/p impedance.*

➔ *Diff large signal ccs*

Use dc sweep (not parametric sweep) for Vid = -VDD:10m:VDD. Set Vicm at the center of the CMIR.

Report diff large signal ccs (VODIFF vs VIDIFF). Compare the extreme values with hand analysis in a table.



Differential large signal CCs

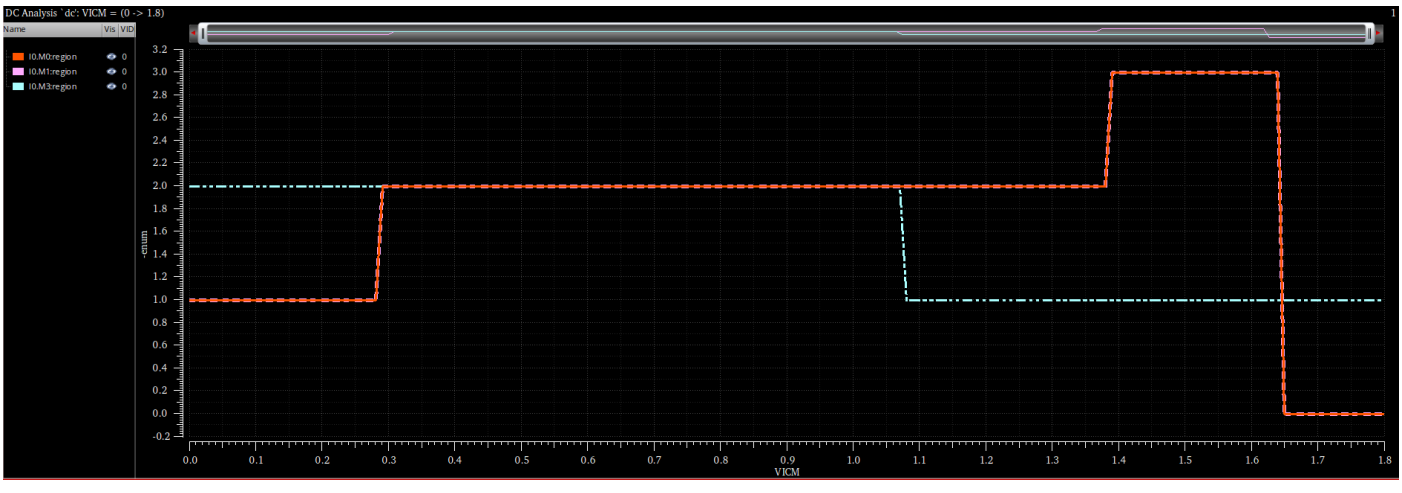
Simulated	*Calculated*
$\pm 1.4V$	$= \pm I_{SS}R_D = 40u * 35k = \pm 1.4V$

➔ *CM large signal ccs (region vs VICM)*

We will use the region parameter to know the operating region of each transistor vs sweep variable.

Use DC sweep (not parametric sweep) for Vicm = 0:10m:VDD (no need to run AC sim). Disable ac analysis.

Plot "region" OP parameter vs VICM for the input pair and the tail current source.



Required plot. The different plot is of the tail CS

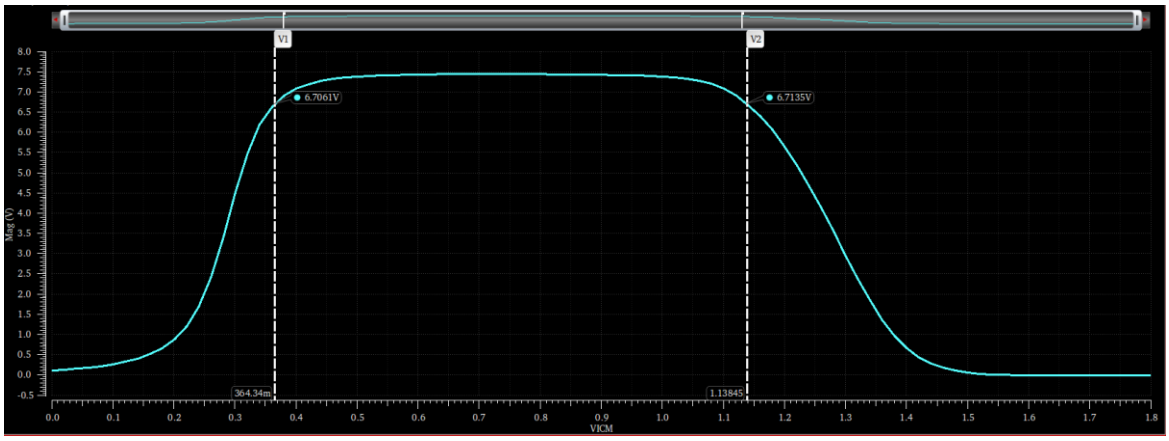
Find the CM input range (CMIR). Compare with hand analysis in a table.

- *CMIR can be inferred from the previous plot by noticing the voltage range corresponding to the input pair being operated in region 2 (sat).*

Simulated	*Calculated*
$0.3V < CMIR < 1.4V$	$0.3V < CMIR < 1.625V$

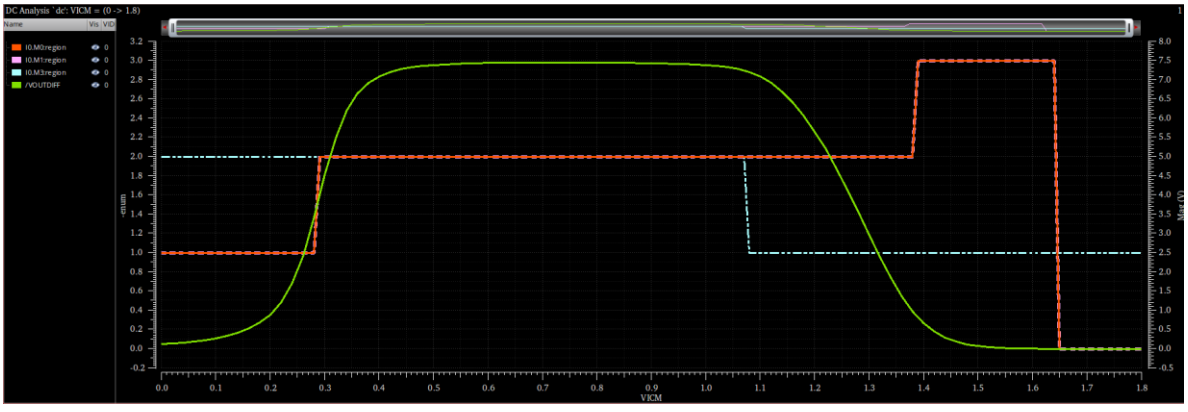
➔ *CM large signal ccs (GBW vs Vicm)*

Use ac analysis (start = 1, stop = 1, pts(linear) = 1) to get Avd. Use parametric sweep (not dc sweep) for Vicm = 0:20m:VDD.
Report CM large signal ccs (Avd vs Vicm). Assume the valid range for Vicm (CMIR) is defined by the condition that Avd is within 90% of the max gain, i.e., 10% drop in gain.



Avd VS ViCM. Employing 'ymax' function resulted in 7.458.

Plot the results overlaid on the results of the previous method (region parameter). Find the CM input range. Compare with the previous method in a table.



Required plot overlaid with the results of the previous method

Previous method	*This method*
$0.3V < CMIR < 1.4V$	$10\%\ drop\ in\ A_{vd} \rightarrow 0.9 * 7.458 = 6.7$ *(As indicated by V cursors added to the plot)* $365mV < CMIR < 1.14V$