IEEE ASUSB AIC Design Winter Workshop – LAB 2

PART 1: Sizing Chart

We would like to design a resistive loaded CS amplifier that meets the specifications below. The design process involves selecting the sizing of the transistor (W and L), the bias point (V_{GS}), and the resistive load (R_D). The first design decision is to choose L. Since there is no spec on bandwidth (speed), we may choose a relatively long L to provide large r_o and avoid short channel effects. Note that r_o appears in parallel with R_D. Assume we will choose $L = 2\mu m$.

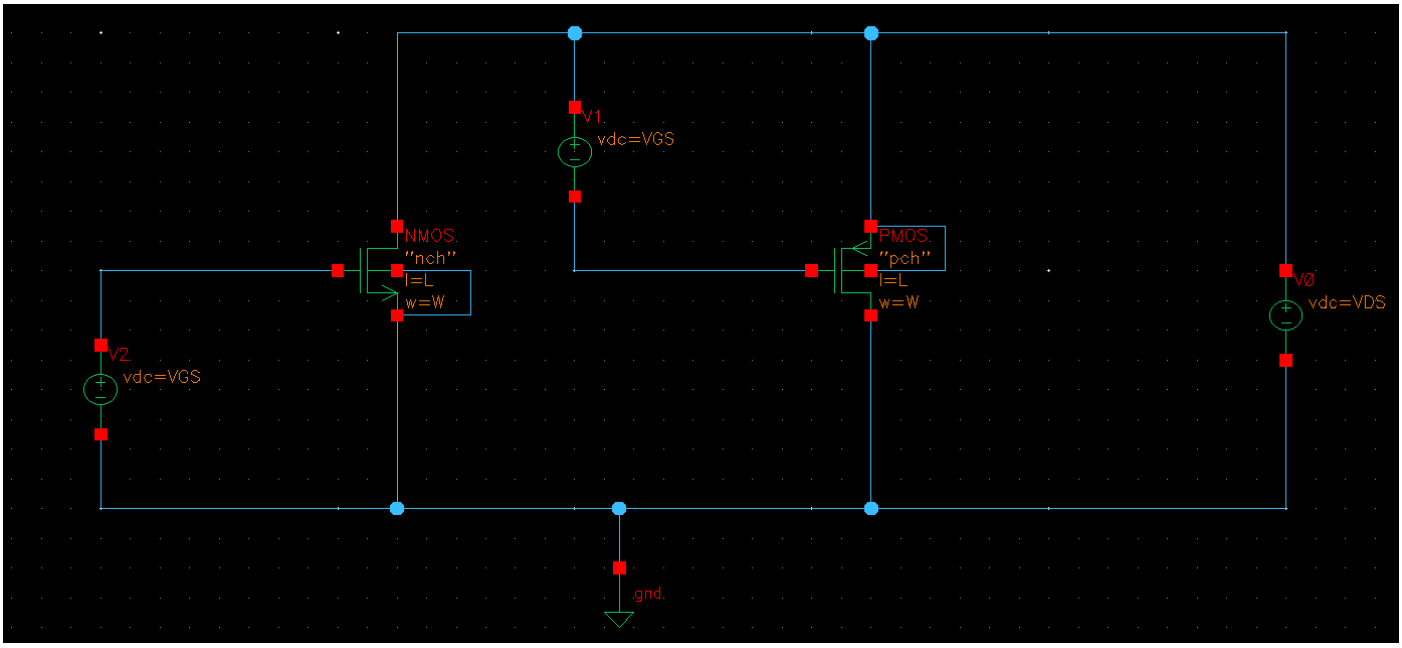
Assuming CM output $= V_{R_D} = \frac{V_{DD}}{2}$ *and given the DC bias current, determine the value of* R_D.

$$V_{R_D} = 0.9 = 100u * R_D \rightarrow R_D = 9k\Omega$$

Given A_v *and* V_{R_D}, *calculate the required* V^* *(again note that* $V^* \neq V_{OV}$ *for a real MOSFET). Let's name this value* V_Q^*.

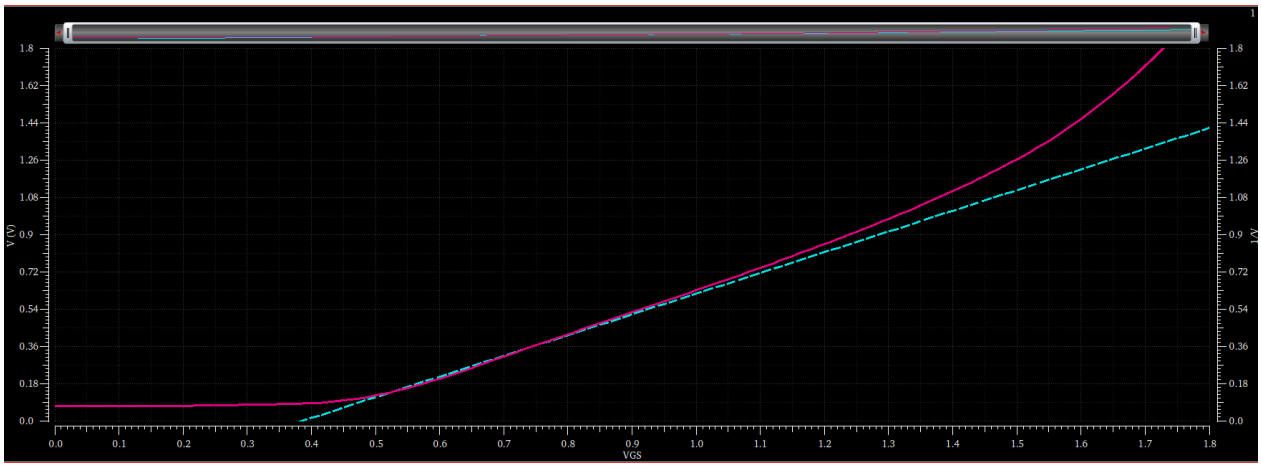
$$A_v = \frac{2V_{R_D}}{V^*}. \; Given \; A_v = 8 \; and \; V_{R_D} = 0.9 \rightarrow V_Q^* = 225mV.$$

The remaining variable in the design is to calculate W. *Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation. Create a testbench for NMOS and PMOS characterization (we will use the PMOS later in Part 2 of this lab). Use* $W = 10um$ *(we will understand why shortly) and* $L = 2um$ *(the same* L *that we chose before).*



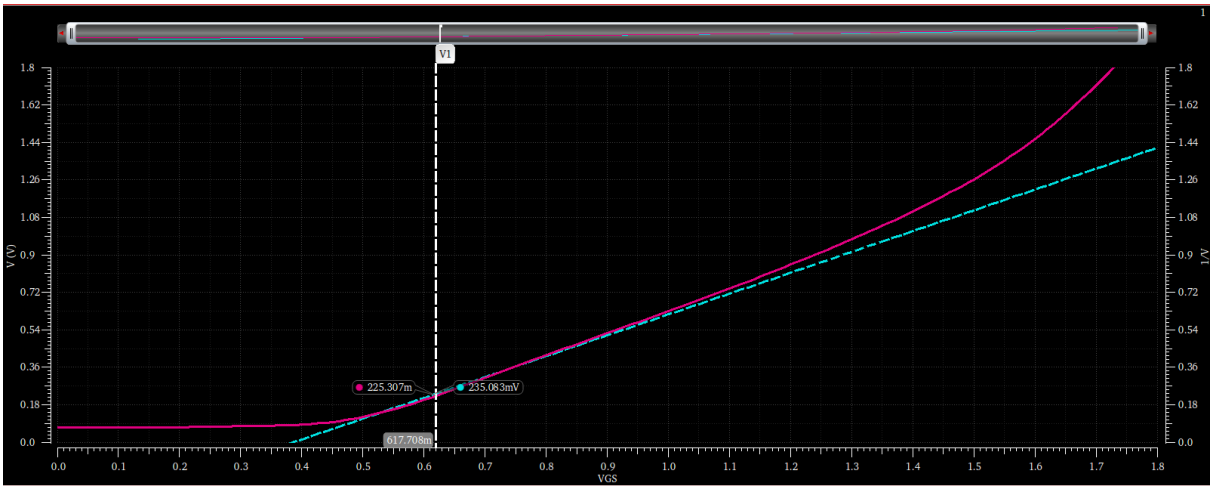
Required testbench

Sweep V_{GS} from 0 to $V_{th} + 0.4$ with $10mV$ step. Set $V_{DS} = \frac{V_{DD}}{2}$. We want to compare $V^* = \frac{2I_D}{g_m}$ and $V_{OV} = V_{GS} - V_{th}$ by plotting them overlaid. Use the calculator to create expressions for V^* and V_{OV}. Export the expressions to adexl. Plot V^* and V_{OV} overlaid vs V_{GS}. Make sure the y-axis of both curves has the same range.

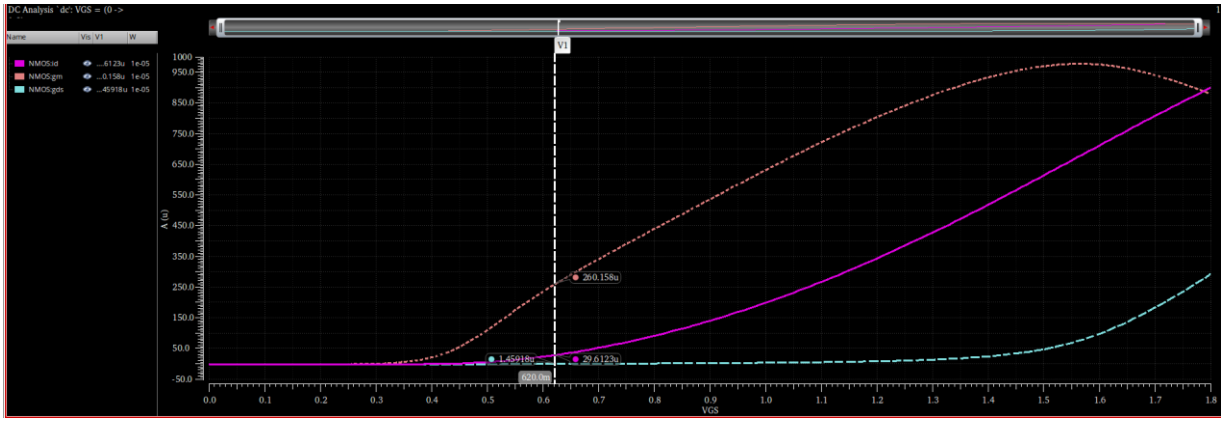


Vov and V_star VS VGS overlaid

On the V^* and V_{OV} chart locate the point at which $V^* = V_Q^*$. Find the corresponding V_{OVQ} and V_{GSQ}.



V_starQ and corresponding VGSQ and VovQ



ID, gm and gds VS VGS

$g_{ds,actual} \approx 5uS$

Now back to the assumption that we made that $W = 10um$. *This is not the actual value that we will use for our design. But the good news is that* I_D *is always proportional to* W *irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be* $I_{DQ} = 100uA$ *as given in the specs. Calculate* W *as shown below.*

$W_x = 10um$	$I_{DX} = 29.5uA$
$W_{actual} = ??$	$I_{D,actual} = 100uA$

$W_{actual} \approx 34um$

Now we are almost done with the design of the amplifier. Note that g_m *is also proportional to* W *as long as* V_{OV} *is constant. On the other hand,* $r_O = \frac{1}{g_{ds}}$ *is* ***inversely*** *proportional to* W *(*I_D*) as long as* L *is constant. Before leaving this part, calculate* g_{mQ} *and* g_{dsQ} *using ratio and proportion (cross-multiplication) and double check that* $A_v = g_m(R_D||r_O)$ *meet the required gain spec.*

$g_{mX} = 260uS$	$W_X = 10um$
$g_{m,actual} = ??$	$W_{actual} = 34um$

$g_{m,actual} \approx 885uS$

$g_{dsX} \approx 1.5uS$	$W_X = 10um$
$g_{ds,actual} = ??$	$W_{actual} = 34um$

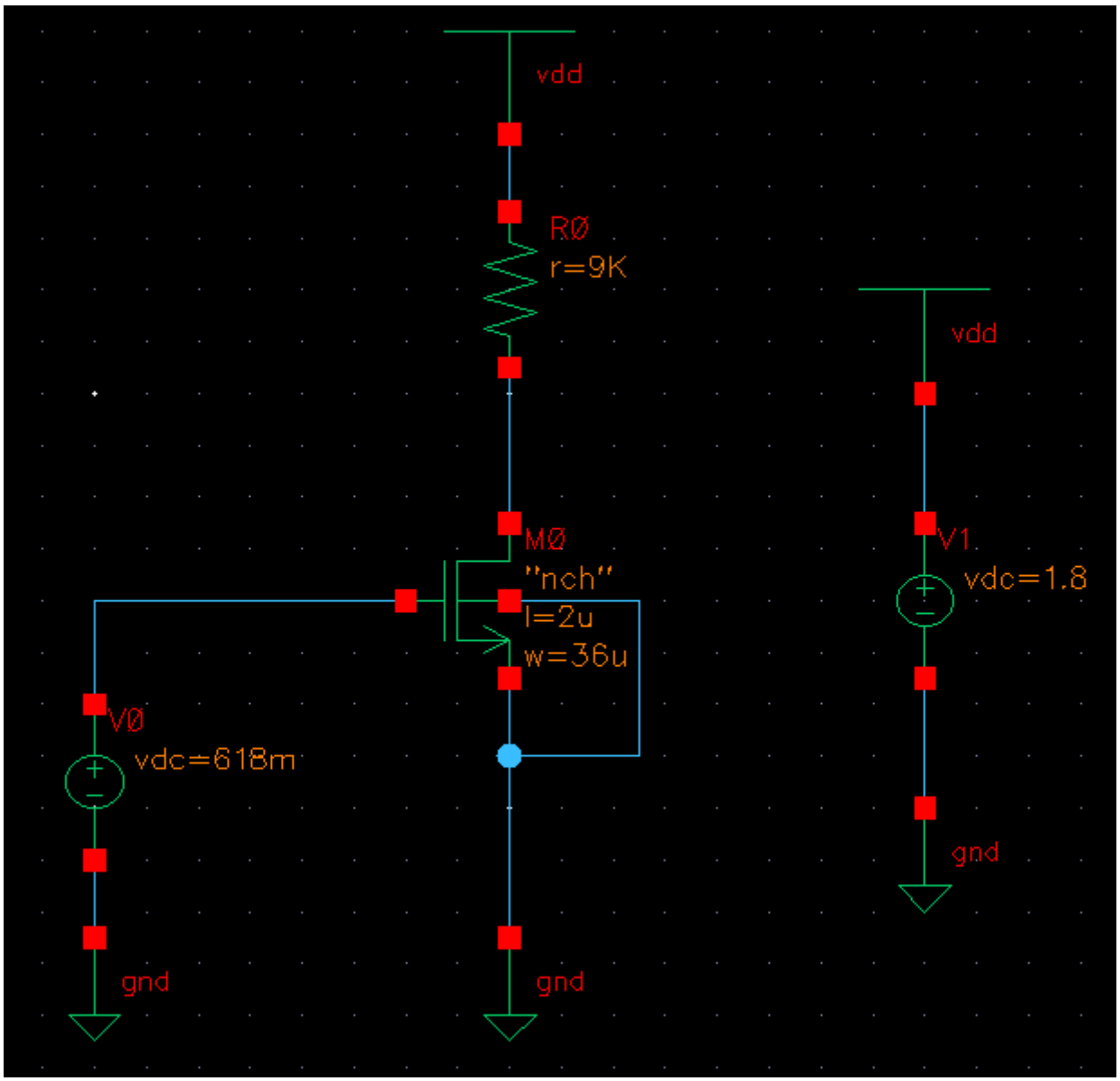
$A_v = 885u(9k\|\|\frac{1}{5u}) \approx 7.9$

Required gain is not achieved. If W *is set to, say* $36um$, *and the calculations are redone, the gain would be* 8.

PART 2: CS Amplifier

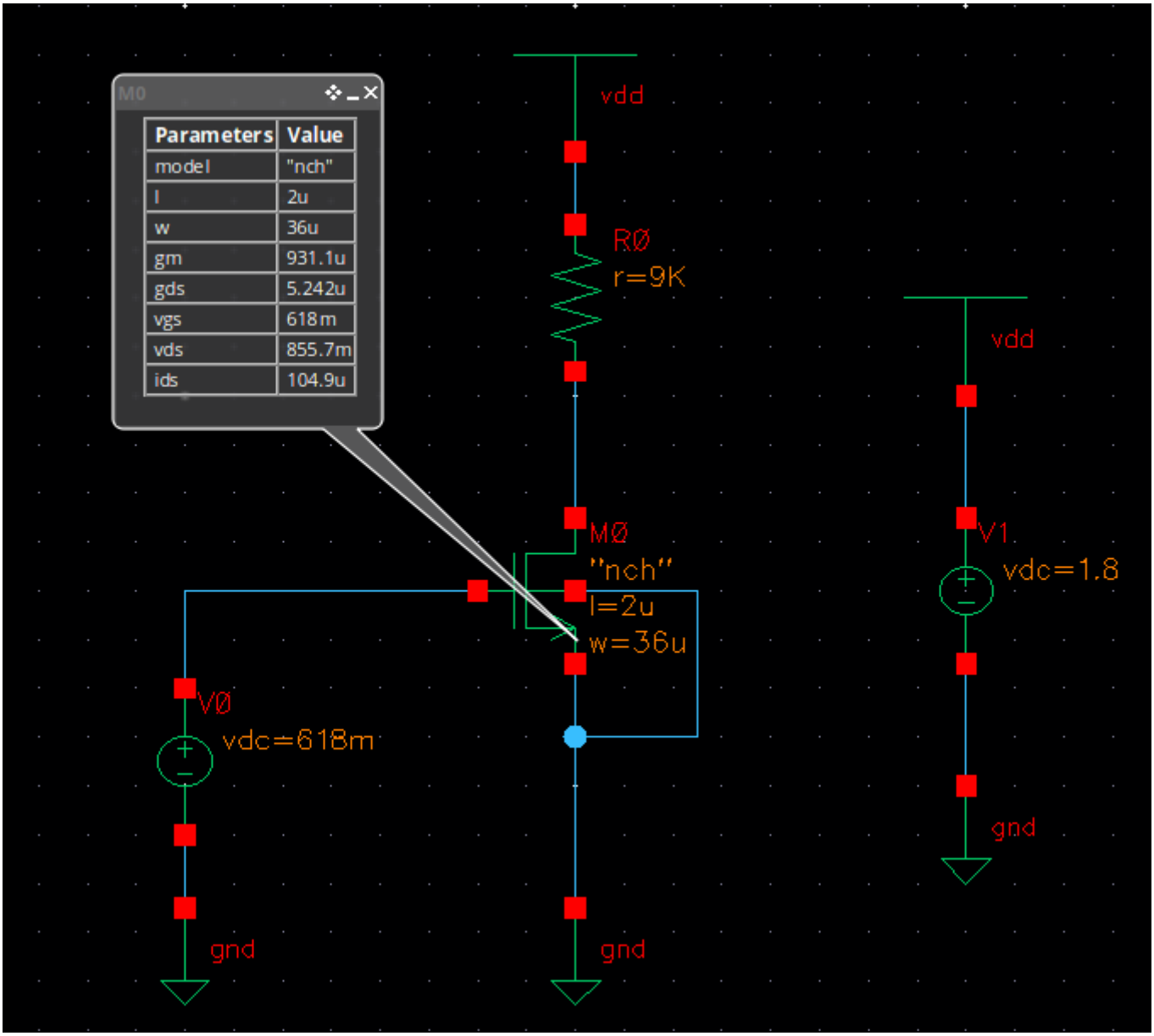
1. OP and AC Analysis

- Create a testbench for the resistive loaded CS amplifier using the V_{GSQ}, R_D, L, and W that you got from the previous part.



Required testbench

- Simulate the DC OP. Report a snapshot for the key operating point (OP) parameters. Compare the results with the results you obtained in Part 1. Since we used chart-based design, the results should agree well.



A snapshot of key OP parameters

- The key OP parameters are very close to those calculated in part one. The deviation is due to not stating the calculation results after changing W *from* $34um$ *to* $36um$.

- Compare r_O *and* R_D. *Is the assumption of ignoring* r_O *justified in this case? Do you expect the error to remain the same if we use min* L*?*

- $R_D = 9k\Omega, r_O = \frac{1}{g_{ds}} \approx 190k\Omega$.

- It is very clear that r_O *is much larger than* R_D. *Thus, the assumption of ignoring* r_O *is justified. If min* L *is used, the error of this assumption would be higher, since* r_O *is directly proportional to channel length, and the lower the resistor connected in parallel with another one, the less accurate the assumption of ignoring it.*

- *Calculate the intrinsic gain of the transistor.*

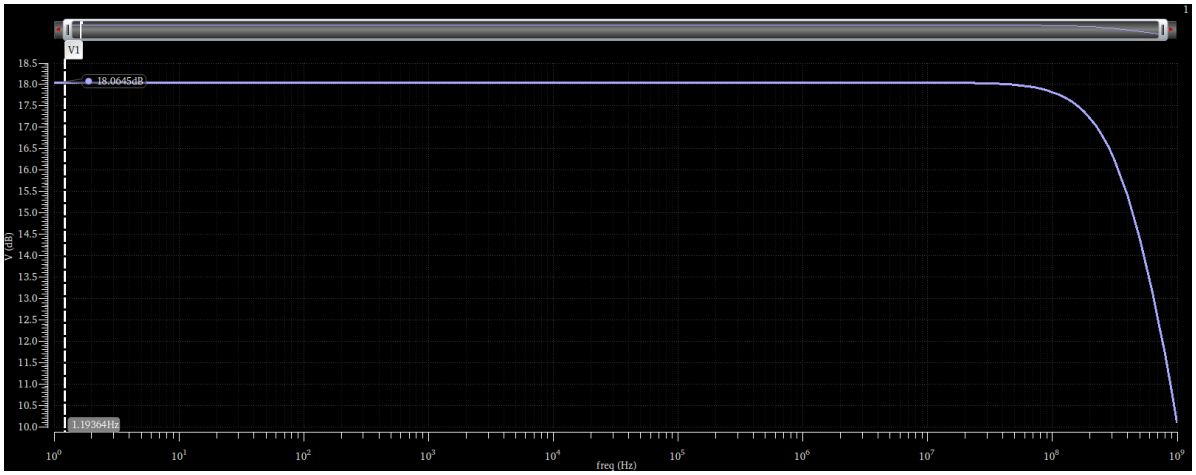
$$A_{v,intrinsic} = g_m r_O \approx 177$$

- *Calculate the amplifier gain analytically. What is the relation* $(\ll, <, \approx, >, \gg)$ *between the amplifier gain and the intrinsic gain?*

$$A_v = g_m(R_D || r_O) \approx 7.99$$

- $A_{v,intrinsic} \gg A_v$.

- *Create a new simulation configuration and run AC analysis (from 1Hz to 1GHz). Report the gain vs frequency. Annotate the DC gain and make sure it meets the spec.*

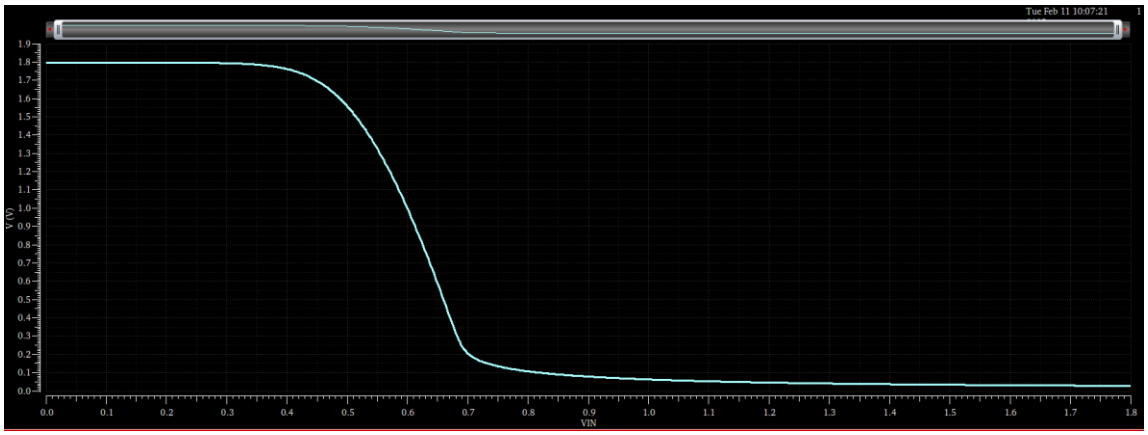


VOUT VS frequency

- $A_{vO} = 18dB = 7.94$ *(meets the spec).*

2. Gain Non-Linearity

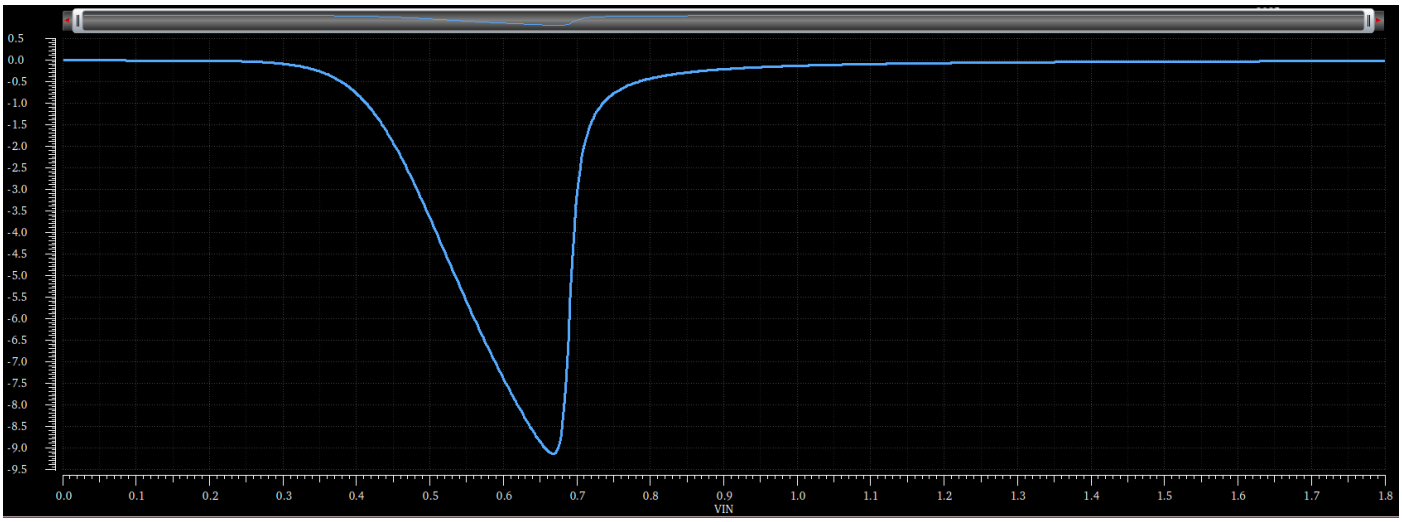
- *Create a new simulation configuration. Perform a DC sweep for the input voltage from 0 to VDD with 2mV step. Report VOUT vs VIN. Is the relation linear? Why?*



VOUT VS VIN

- The relation is not linear since the device whose parameters are swept is simply a "nonlinear device" and due to the correspondence between the change in input voltage and the change in the operating region.

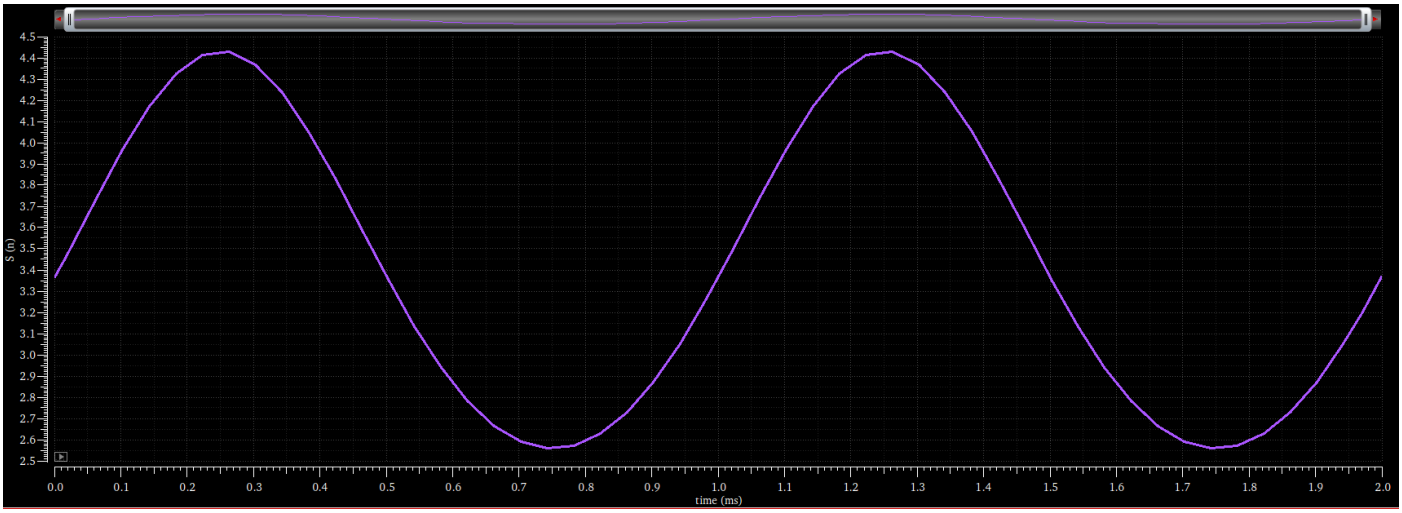
- Calculate the derivative of VOUT using calculator. Plot the derivative vs VIN. The derivative is itself the small signal gain. Is the gain linear (independent of the input)? Why?



Deriv (VOUT) VS VIN

- The small signal gain is not independent of the input. The gain, A_v, is equal to $g_m r_O$. g_m is a function of V_{GS}, which is the input voltage. r_O is a function of I_D which is in turn a function of V_{GS}, which is, again, the input voltage. Overall the small signal gain is a strong function of the input voltage. This curve, in a way or another, refers to the great role of degeneration in the process of linearizing the MOS device, as the degeneration resistance "absorbs" a noticeable amount of the input voltage, which makes the allowable range of variation of v_{gs} much smaller when compared to an un-degenerated CS stage.

- Set the properties of the voltage source to apply a transient stimulus (sine wave of 1kHz frequency and 10mV amplitude superimposed on the DC input voltage). Create a new simulation configuration. Run transient simulation for 2ms. Plot g_m vs time. Does g_m vary with the input signal? What does that mean?



Required transient analysis

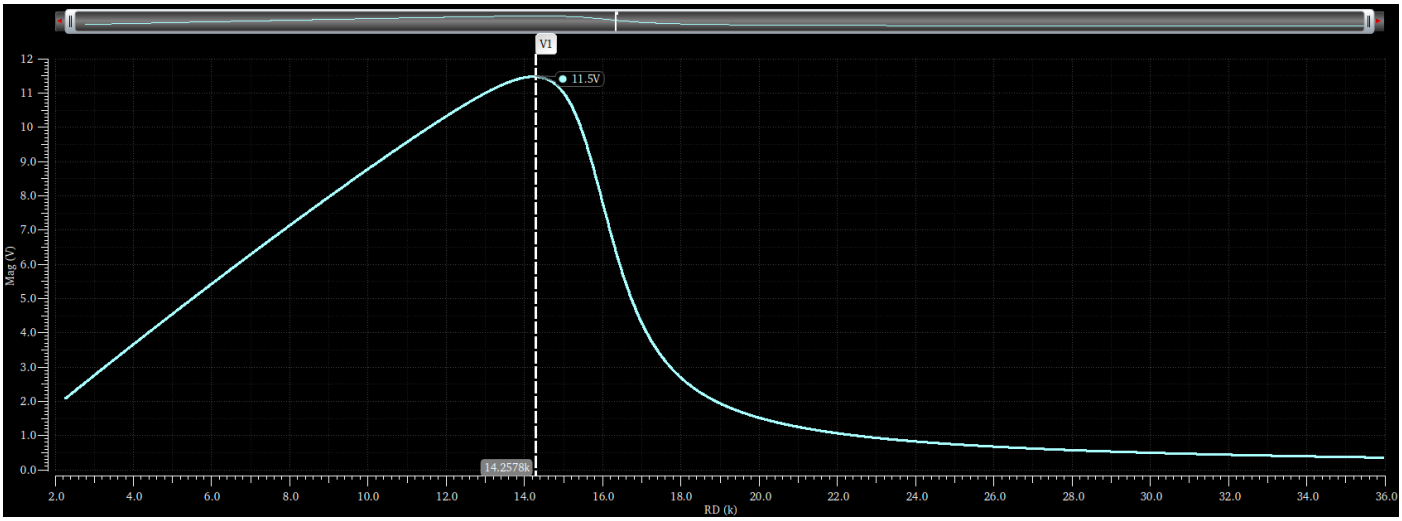
- Yes, g_m varies with input voltage. The significance of this refers to the fact that g_m is a function of the input voltage.

- Is this amplifier linear? Comment.

- The amplifier is not linear. Nonlinear systems have a lot of problems that can be compensated by the continuous trials to linearize them. As this linearization gets more and more accurate, the system tends to behave more ideally which at the end leads to having high performance electronic circuits and systems. Linearization IS a key tool in system performance optimization.

3. [Optional] Maximum Gain

- We want to investigate the variation of gain vs R_D. We will use AC analysis to calculate the small signal gain. Set the source AC magnitude = 1. Note that AC analysis is a linear analysis, so we use a magnitude of one such that the output is itself the gain. Keep the DC value of V_{GS} constant at the DC value you selected in Part 1. Set AC simulation to sweep design variable (R_D from ¼ the value you selected in Part 1 to 4 times the value you selected in Part 1). Set the AC simulation frequency at 1 Hz (single frequency point). The purpose of the AC analysis here is just to get the small signal gain and not to investigate the frequency response. Use the calculator to plot the gain vs R_D. You will find that the gain increases with R_D and then decreases with R_D. Justify this behavior. What is the value of R_D that gives the highest gain? What is the highest gain?



Gain VS RD

- As mentioned in part 1, the gain increases as V_{R_D} $(R_D, since\ I_D is\ almost\ constant)$ *increases. The relation is almost linear. But when* R_D *exceeds some value, which is around* $14.2k\Omega$*, the gain begins to decrease as* R_D *is further increased. With* R_D *of this value, it has a voltage drop of* $V_{R_D} = I_D R_D \approx 1.5V$*, which corresponds to* $V_{DS} = V_{DD} - V_{R_D} \approx 300mV$*. This value is near to* V_{OVQ} *(but is not lower than* V_{OVQ}*, and I cannot justify this), which means that at this value of* R_D*, the device is near to the edge of saturation, and this is translated to lower gain. The highest gain is around* 11.5*.*

- Analytically calculate the value of R_D *that gives the highest gain and the highest gain using the expressions in Part 1. Compare simulation and analysis results.*

$$A_v = g_m\left(\frac{R_D r_O}{R_D + r_O}\right),\ \frac{dA_v}{dR_D} = g_m\left(\frac{(R_D + r_O)r_O - R_D r_O}{(R_D + r_O)^2}\right) = 0 \rightarrow R_D = ??:(($$

- What is the available signal swing at the point of maximum gain?

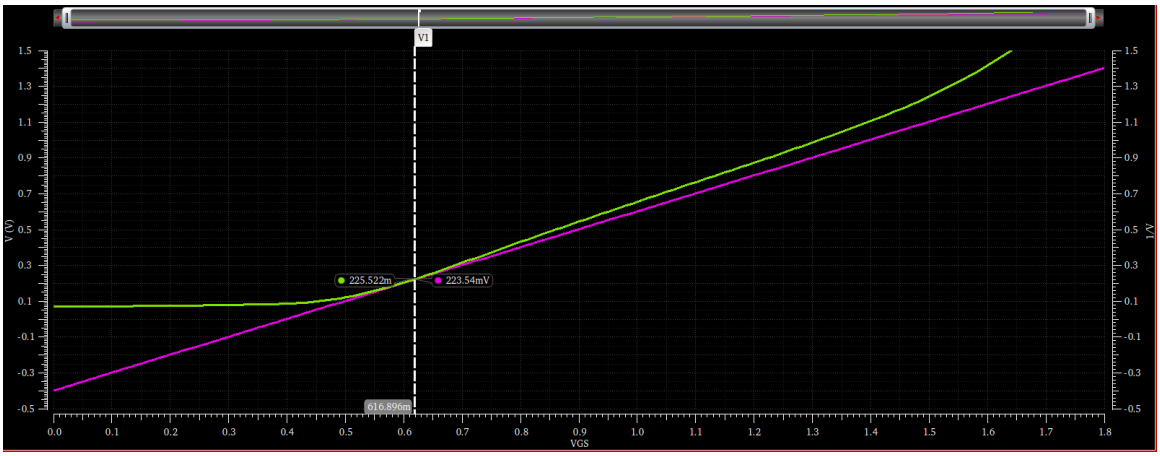
- At this point, $V_{DS} = 300mV$*, which is higher than the overdrive by* $75mV$*. This means that the signal can swing up till it reaches* V_{DD} *and has only* $75mV$ *of downswing headroom.*

- Is scaling down the supply voltage good for gain? Comment.

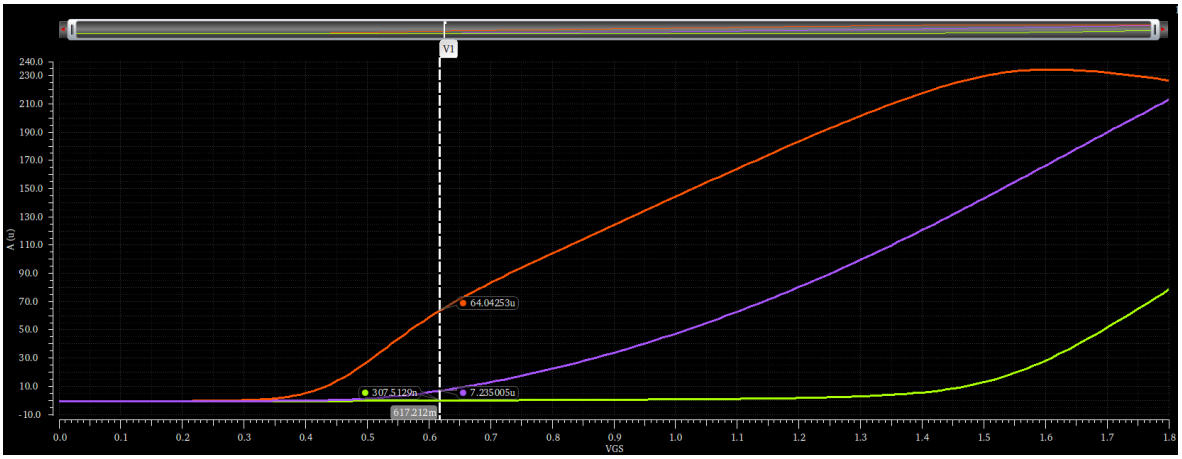
- Scaling down the supply voltage is not good for gain. Taking the circuit in this lab as an example for illustration, $A_v \approx \frac{2V_{R_D}}{V^*}$*. This expression tells us that the gain increases as* V_{R_D} *increases. But the maximum allowable* V_{R_D} *is limited by the supply.*

4. [Optional] Gain Linearization (feedback)

- We will use feedback to improve the gain non-linearity. We will study feedback in more detail later. Create a new schematic and copy the old schematic into it. Replace the resistive load with a PMOS current source (active load) as shown below. Create a sizing chart for the PMOS similar to what we did for NMOS in Part 1 using $L = 2um$ *and* $W = 10um$ *(you may use the same test bench used in Part 1). From the chart, assuming* V_Q^* *similar to NMOS, determine* V_{GSQ} *and* I_{DX}*. Using ratio and proportion (cross-multiplication) determine* W *similar to Part 1. Note that the PMOS load must have the same bias current as the NMOS input device. Note that it is better to bias the PMOS using a voltage source between the gate of the PMOS and VDD.*



V_starQ, VGSQ and VovQ of PMOS

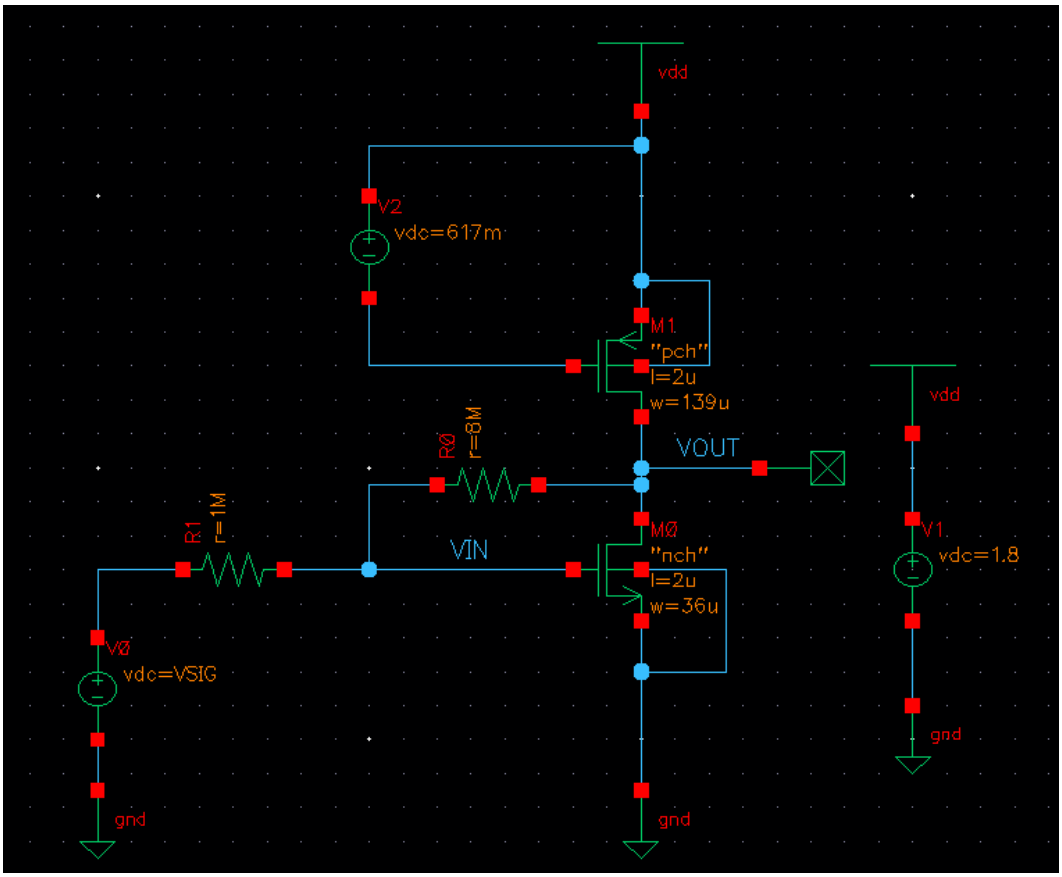


IDX, gmX and gdsX VS VGS

$W_X = 10um$	$I_{DX} = 7.2uA$
$W_{actual} = ??$	$I_{D,actual} = 100uA$

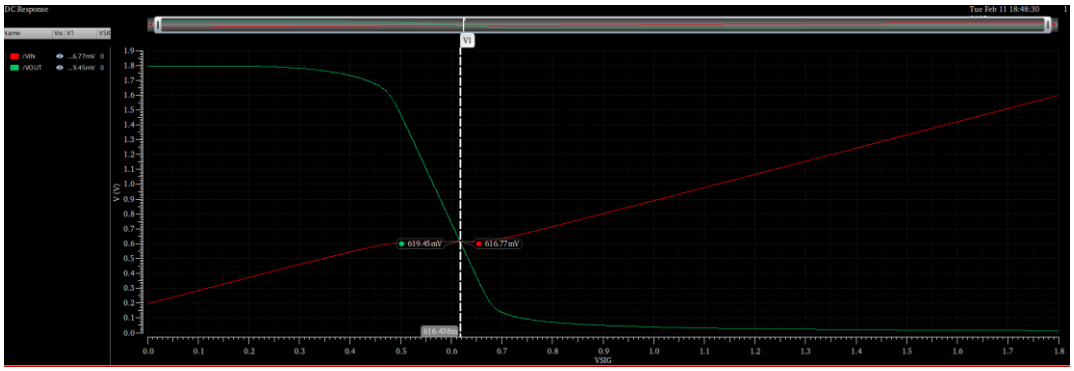
$W_{actual} \approx 139um$

- *Add two resistors: input resistor* $R_{in} = 1M$ *and feedback resistor* R_f*. Choose* R_f *to give a voltage gain approximately equal to* $\frac{R_f}{R_{in}} = A_v$ *as given in the specs.*



Required testbench

- *Perform a DC sweep for the input voltage (VSIG) from 0 to* VDD *with 2mV step. Report VIN and VOUT vs VSIG (overlaid). At what voltage do the two curves cross? Why?*



VOUT and VIN VS VSIG

- *The curves cross at* $V_{sig} = 620mV \approx V_{GSQ}$*. The reason of curve crossing at this point especially due to "idk :(".*