

*IEEE ASUSB Analog IC  
Design Winter Workshop*

*2025*

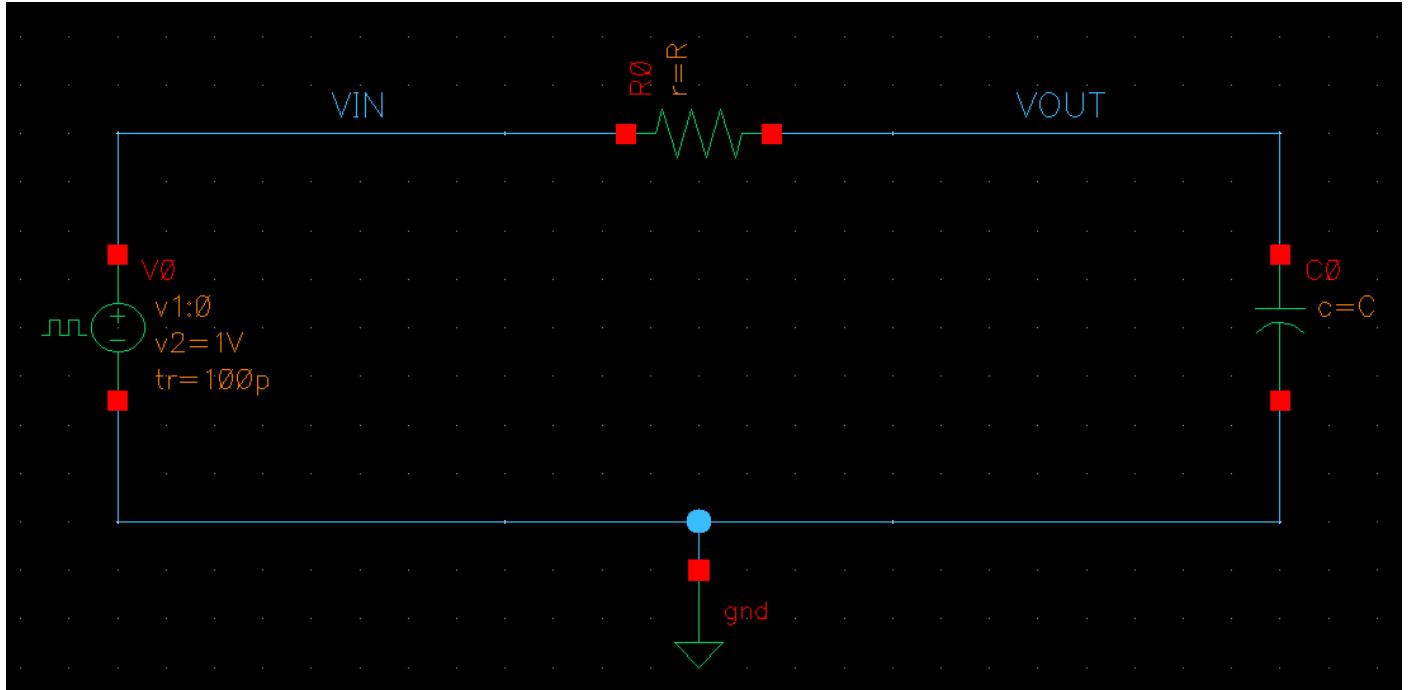
*LAB 1*

# PART 1: Low Pass Filter Simulation (LPF)

## 1. Transient Analysis

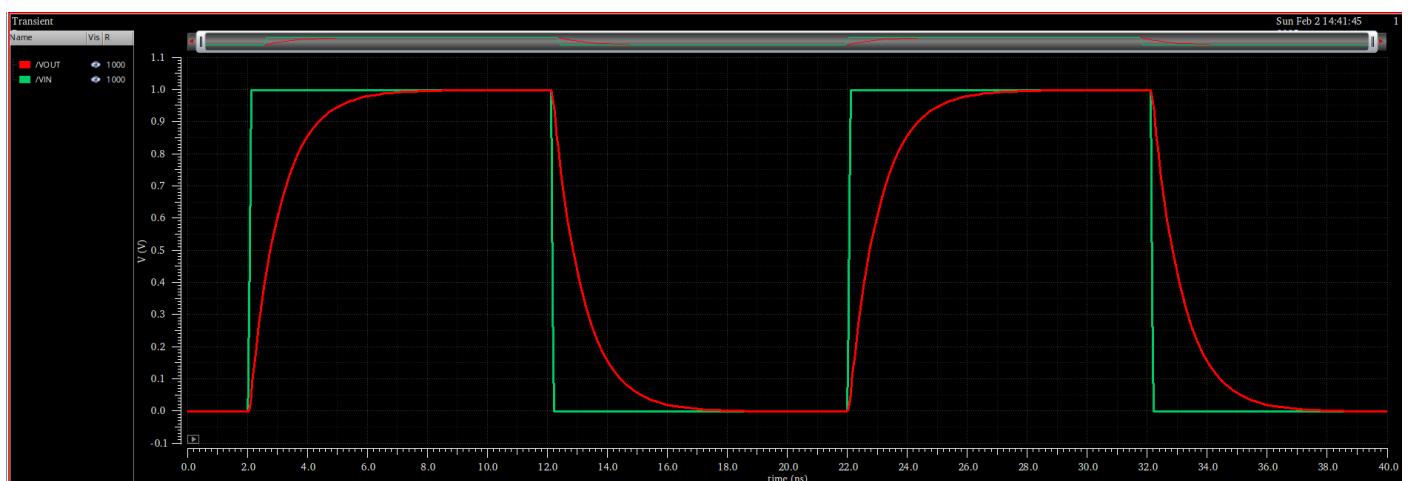
- Design a first order low pass filter that has  $R = 1k\Omega$  and  $1ns$  time constant. Apply a square wave input with  $T_{high} = \text{Pulse Width} = 10ns$ ,  $T_{clk} = \text{Period} = 20ns$ , and  $T_{rise} = T_{fall} = 100ps$ .

- Given  $\tau = 1ns, R = 1k\Omega \Rightarrow C = 1pF$ .



Required testbench

- Report transient analysis results for two periods (use max time step =  $T_{clk}/100$ ).



Required transient analysis

- Calculate rise and fall time (10% to 90%) using Cadence calculator expressions. Export the expressions to adexl.

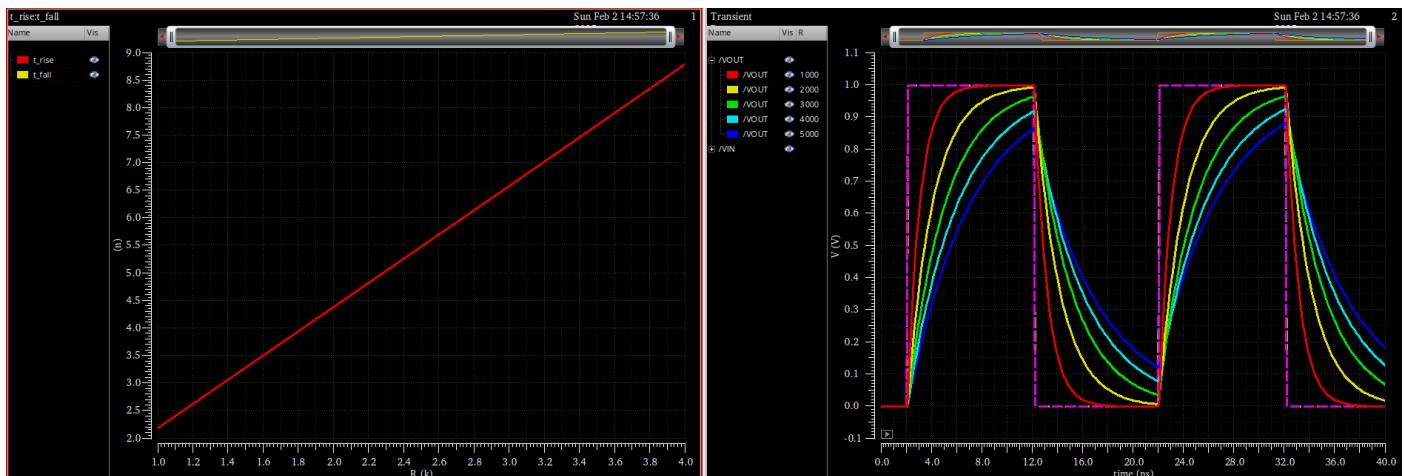
Test	Output	Nominal	Spec	Weight	Pass/Fail
IEEE_ASUSB:LPF_TB:1	t_rise	2.192 n			
IEEE_ASUSB:LPF_TB:1	t_fall	2.192n			

Rise and fall time calculated using Cadence calculator

- Compare simulation with analytical results in a table.

Calculated ( $t_r = t_f = 2.2\tau$ )	Simulated
$2.2\tau = 2.2ns$	2.192ns

- Do parametric sweep for  $R = 1: 1: 5k\Omega$ . Report overlaid results. Comment on the results.



Parametric sweep results overlaid

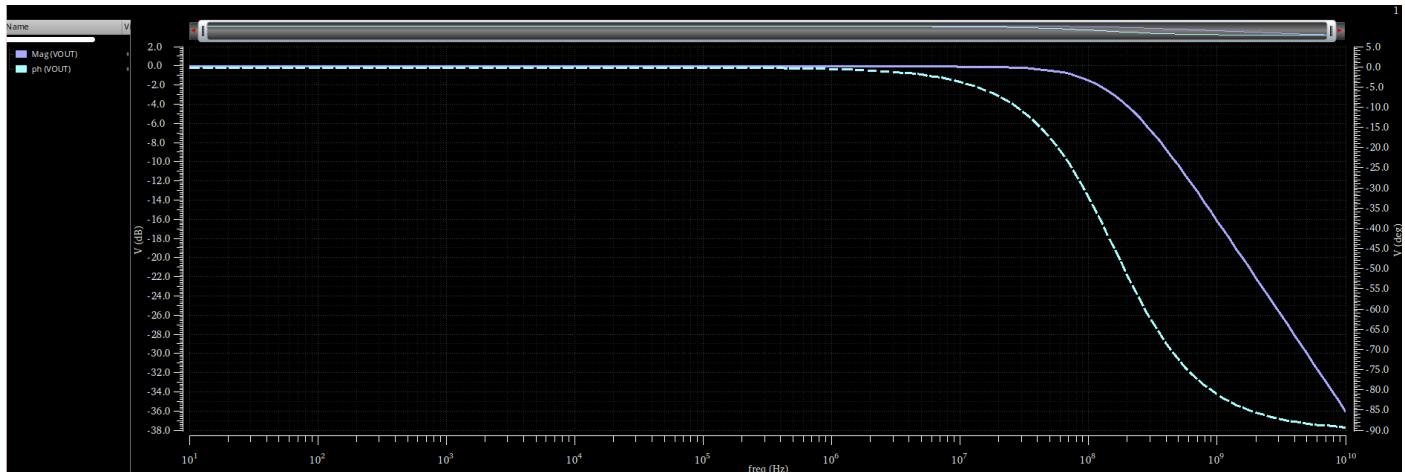
Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
<b>Parameters: R=1k</b>						
1	IEEE_ASUSB:LPF_TB:1	t_rise	2.192 n			
1	IEEE_ASUSB:LPF_TB:1	t_fall	2.192 n			
<b>Parameters: R=2k</b>						
2	IEEE_ASUSB:LPF_TB:1	t_rise	4.391 n			
2	IEEE_ASUSB:LPF_TB:1	t_fall	4.391 n			
<b>Parameters: R=3k</b>						
3	IEEE_ASUSB:LPF_TB:1	t_rise	6.59n			
3	IEEE_ASUSB:LPF_TB:1	t_fall	6.59n			
<b>Parameters: R=4k</b>						
4	IEEE_ASUSB:LPF_TB:1	t_rise	8.787 n			
4	IEEE_ASUSB:LPF_TB:1	t_fall	8.787 n			
<b>Parameters: R=5k</b>						
5	IEEE_ASUSB:LPF_TB:1	t_rise	eval err			
5	IEEE_ASUSB:LPF_TB:1	t_fall	eval err			

Rise and fall time calculation results

- Comment: At  $R = 5k$ , Cadence couldn't calculate rise and fall times due to the fact that at this value of resistance, the time constant is so long that the o/p couldn't reach 0.9 of its maximum value while rising and 0.1 while falling.

## 2. AC Analysis

- Report Bode Plot (magnitude and phase) for the previous LPF.



mag and ph plots pf o/p

- Calculate DC gain and 3dB bandwidth using Cadence calculator expressions. Export the expressions to adexl.

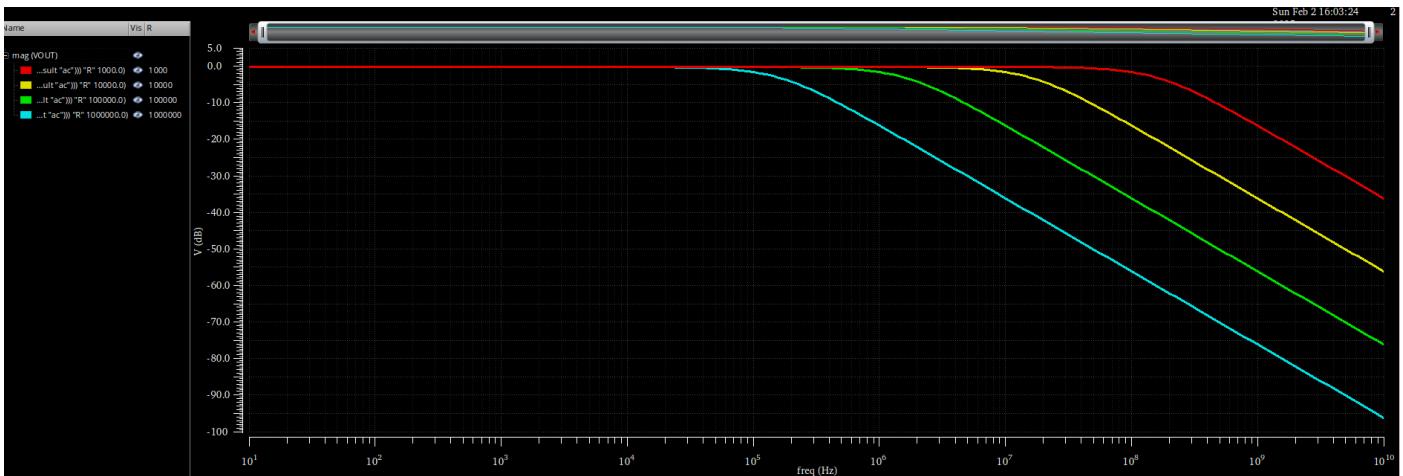
Test	Output	Nominal	Spec	Weight	Pass/Fail
IEEE_ASUSB:LPF_TB:1	Ao	1			
IEEE_ASUSB:LPF_TB:1	BW	158.8M			

Required calculations

- Compare simulation with analytical results in a table.

Spec	Calculated	Simulated
$A_o$	$A_o = H(0) = \frac{1}{RC(0) + 1} = 1$	$A_o = 1$
$BW$	$BW = \frac{1}{2\pi RC} = 159.15MHz$	$BW = 158.8MHz$

- Do parametric sweep for  $R = 1, 10, 100, 1000 k\Omega$ . Report overlaid results. Comment on the results.



*Required sweep*

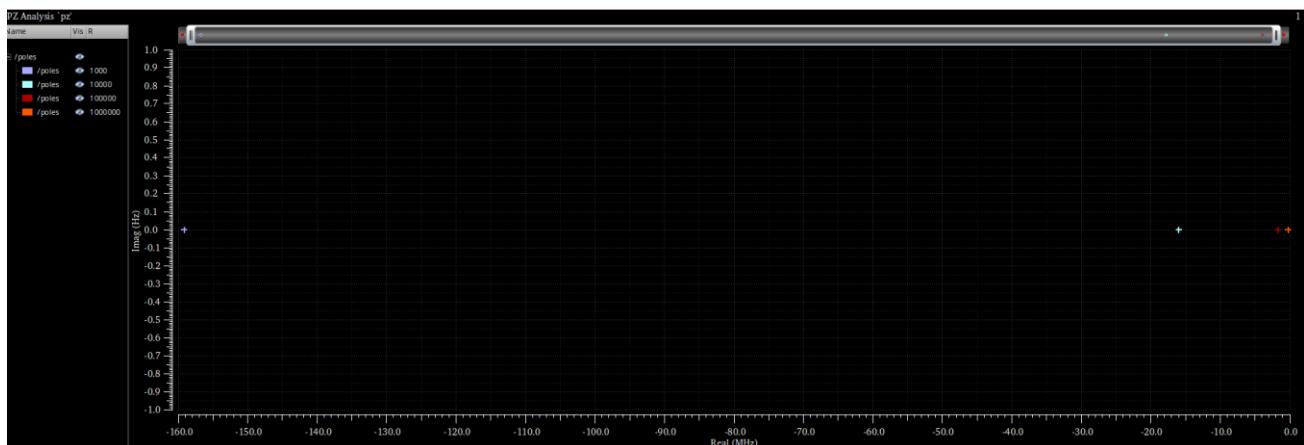
Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
<b>Parameters: R=1k</b>						
1	IEEE_ASUSB:LPF_TB:1	Ao	1			
1	IEEE_ASUSB:LPF_TB:1	BW	158.8M			
<b>Parameters: R=10k</b>						
2	IEEE_ASUSB:LPF_TB:1	Ao	1			
2	IEEE_ASUSB:LPF_TB:1	BW	15.88M			
<b>Parameters: R=100k</b>						
3	IEEE_ASUSB:LPF_TB:1	Ao	1			
3	IEEE_ASUSB:LPF_TB:1	BW	1.588M			
<b>Parameters: R=1M</b>						
4	IEEE_ASUSB:LPF_TB:1	Ao	1			
4	IEEE_ASUSB:LPF_TB:1	BW	158.8k			

*Required calculations*

- Comment: Nothing happened to DC gain across all values of  $R$  since this is a passive network that does not possess the ability to add any sort of gain to the i/p. The inverse relation between the BW and  $R$  can be readily noticed as per the relation given in BW calculations previously performed.

### 3. [Optional] Pole Zero Analysis

- Report pole zero analysis results.

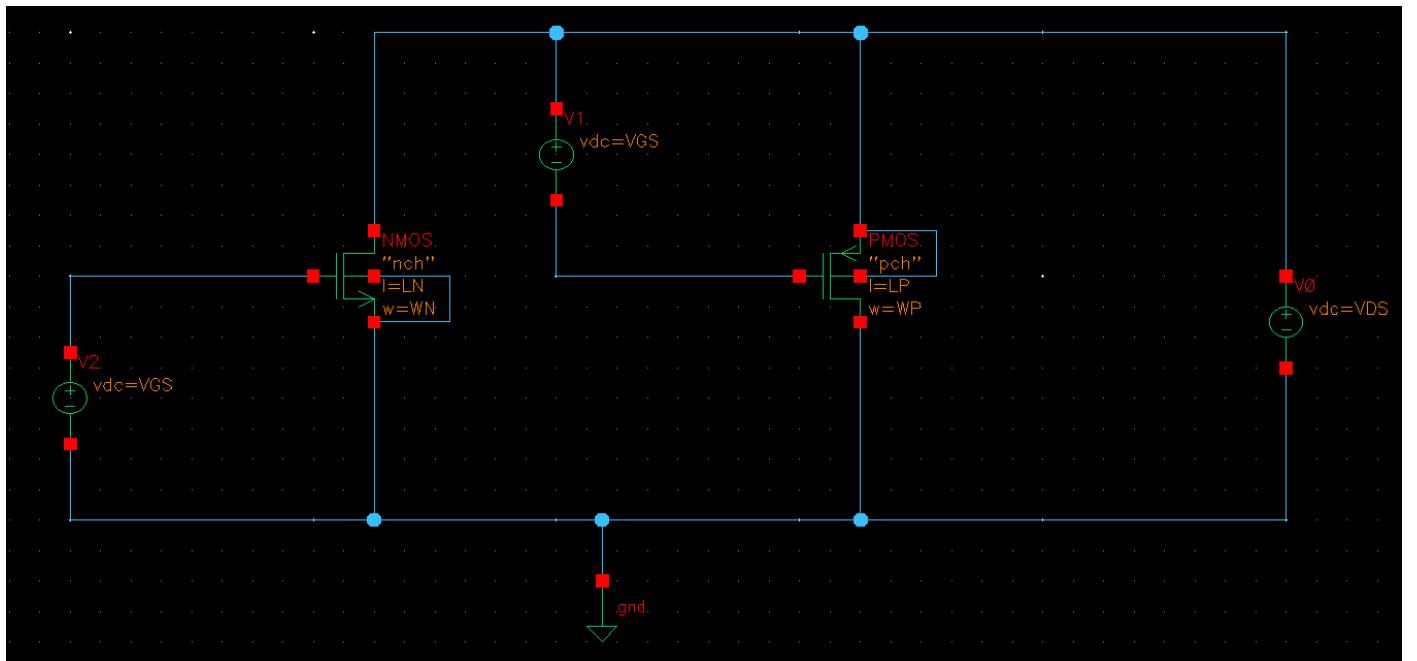


*pz analysis results*

- Find the pole frequency and compare it with the bandwidth calculated from AC analysis.
  - Pole frequencies are shown in the preceding figure and have exactly the values as BWs calculated from AC analysis.

## Part 2: MOSFET Characteristics

- Create a testbench to characterize NMOS and PMOS devices as shown in the figure below.



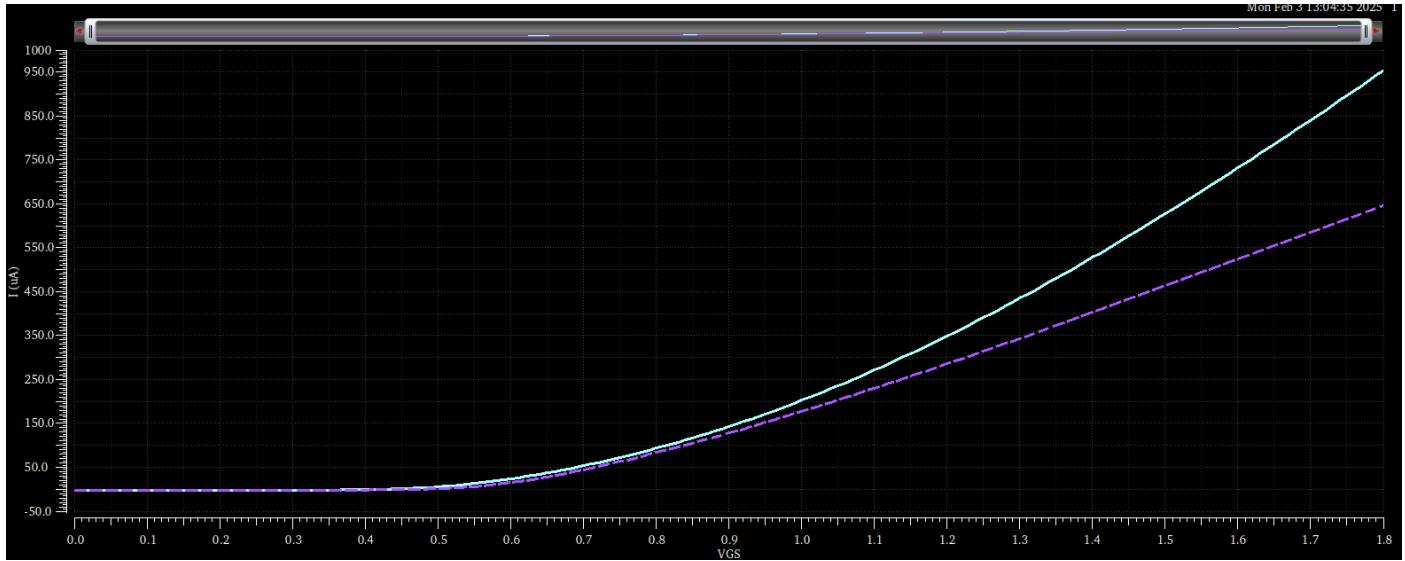
Required testbench

### 1. $ID$ vs $VGS$

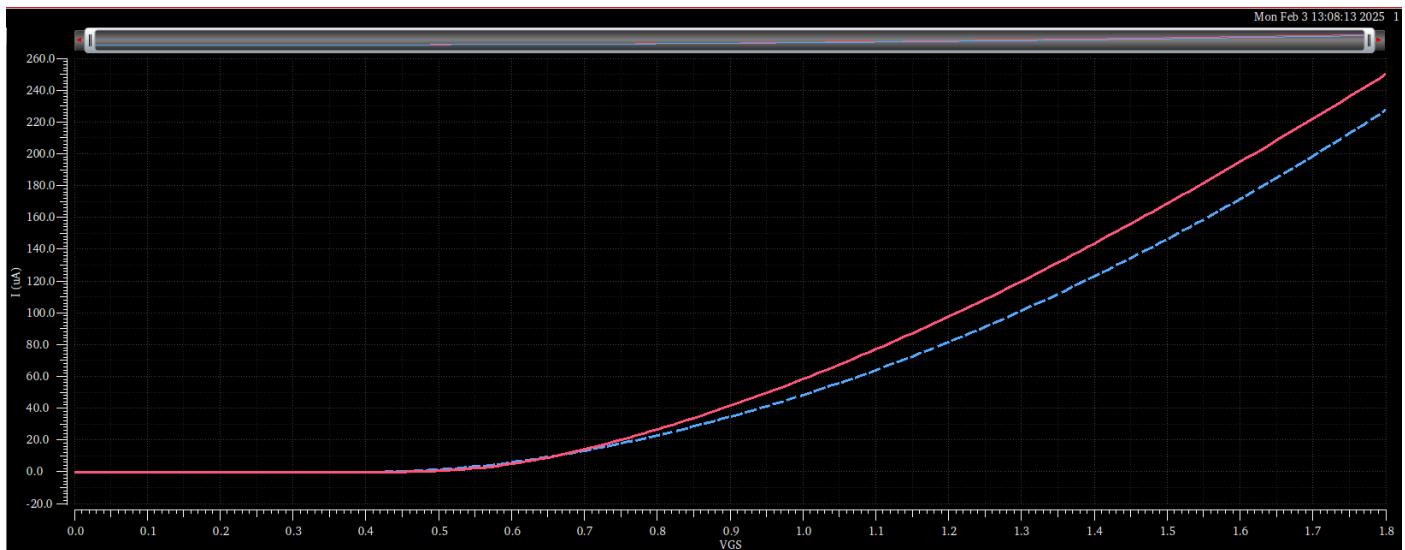
- Plot  $ID - VGS$  characteristics for NMOS and PMOS devices. Set  $VDS = VDD$ , and  $VGS = 0: 10m: VDD$ . Use  $VDD = 1.2V$  for 130nm technology and  $VDD = 1.8V$  for 180nm technology. Plot the results overlaid for the following:

- Short channel device:  $W = 1\mu m$  and  $L = 200nm$
- Long channel device:  $W = 10\mu m$  and  $L = 2\mu m$ .

Hint: Set  $L$  as a parameter and set  $W = 5 \times L$



*ID-VGS CCs of NMOS. Dashed line is of short channel device*



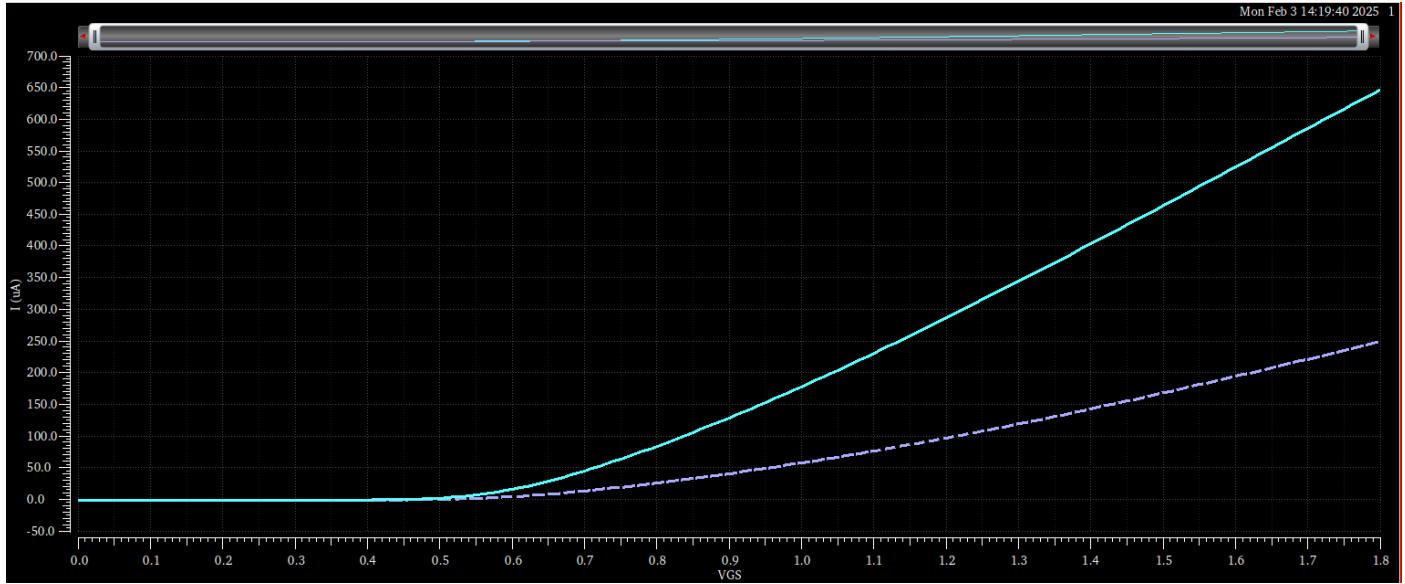
*ID-VGS CCs of PMOS device. Dashed line is of long channel device. abs function is used to get the absolute value of the CCs*

- Comment on the differences between short channel and long channel results.
  - Which one has higher current? Why?
  - Is the relation linear or quadratic? Why?
- Regarding NMOS, the long channel current is higher than the long channel current due to short channel effects that generally limit the current. The exact opposite scenario is present when talking about PMOS since short channel effects are less pronounced.
- In case of short channel, the relation is quadratic until  $V_{GS}$  reaches a value of  $V_{TH} + V_{DS,sat}$ , then it turns into a linear relation due to the strong effect of velocity saturation, while in the case of long channel, the relation is quadratic

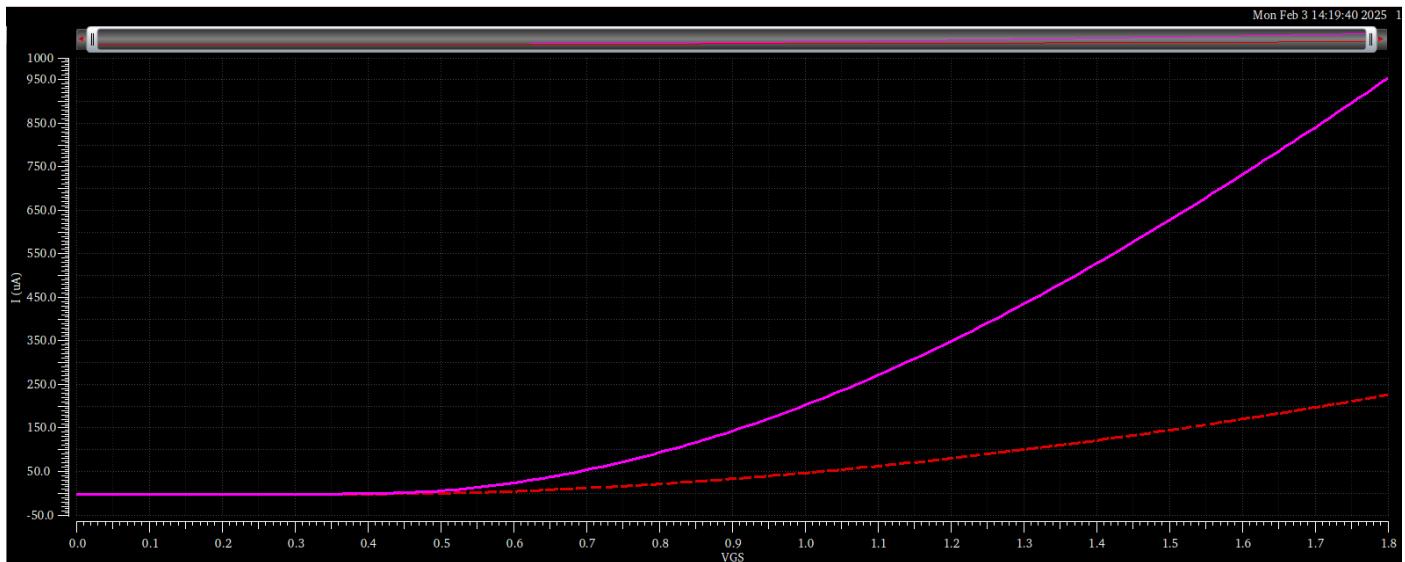
across all the values of  $V_{GS}$  that is higher than the threshold, since the effect of velocity saturation is much weaker.

- Comment on the differences between NMOS and PMOS.

- Which one has higher current? Why?
- What is the ratio between NMOS and PMOS currents at  $V_{GS} = VDD$ ?
- Which one is more affected by short channel effects?

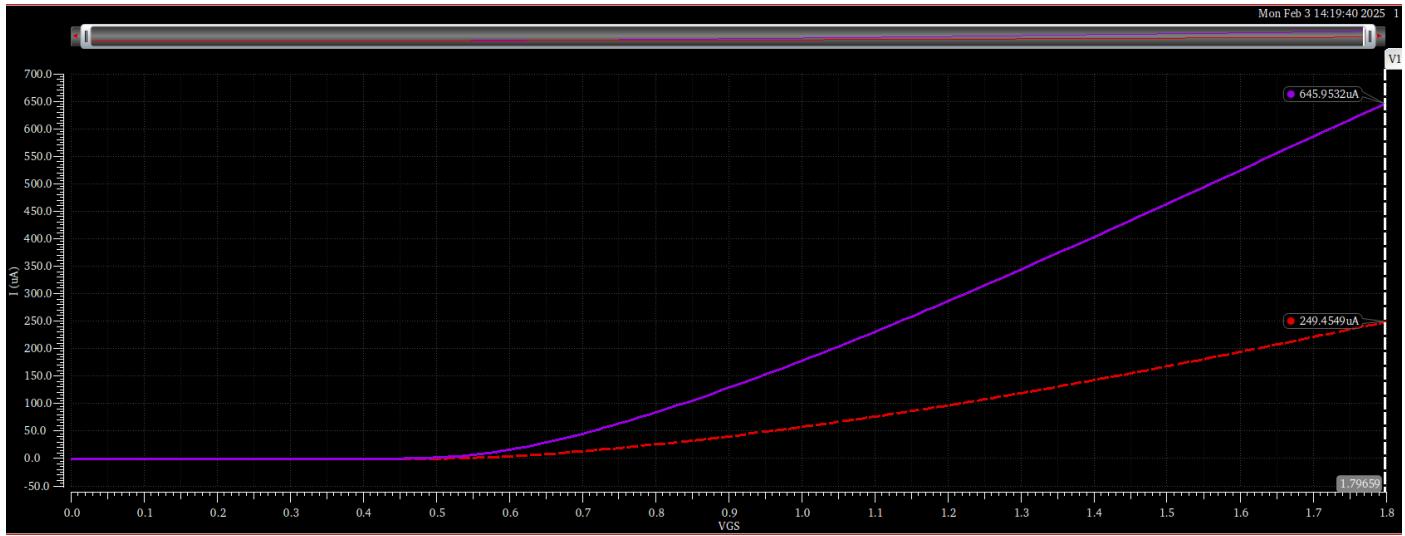


ID-VGS CCs of short channel NMOS and PMOS. PMOS CCs is dashed



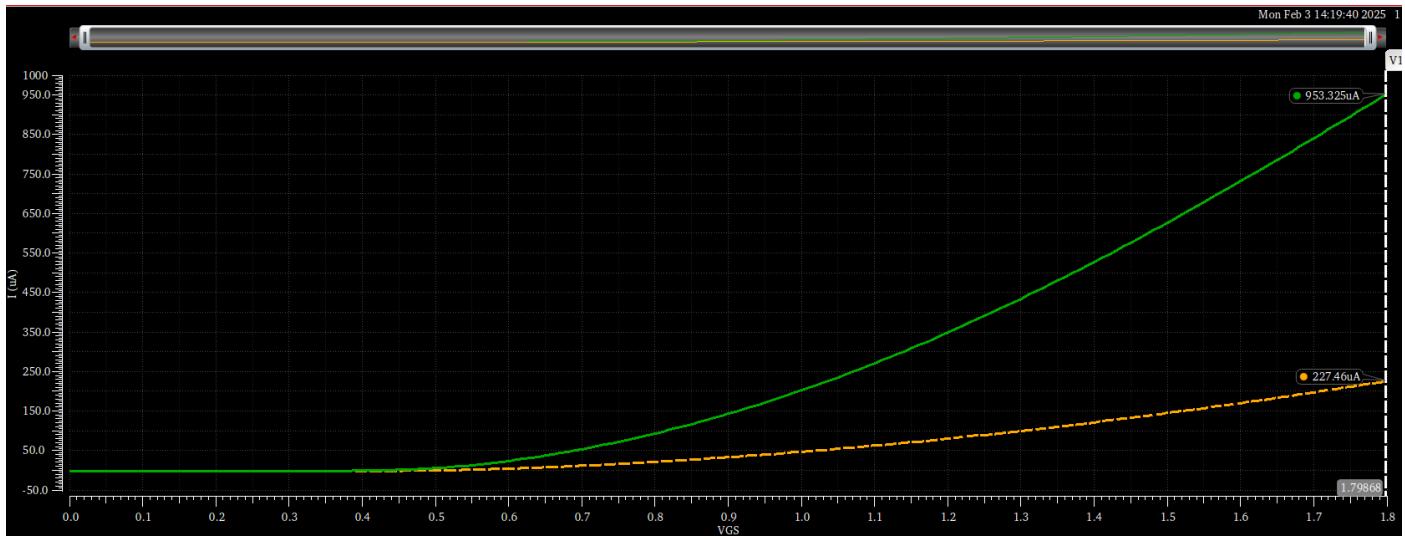
ID-VGS CCs of long channel NMOS and PMOS. PMOS CCs is dashed

- NMOS device, either short or long channel, has higher current than PMOS due to the higher carrier mobility.



Vertical cursor added to **short channel CCs**

$$- \frac{I_{DN}}{I_{DP}} = \frac{646}{250} \approx 2$$



Vertical cursor added to **long channel CCs**

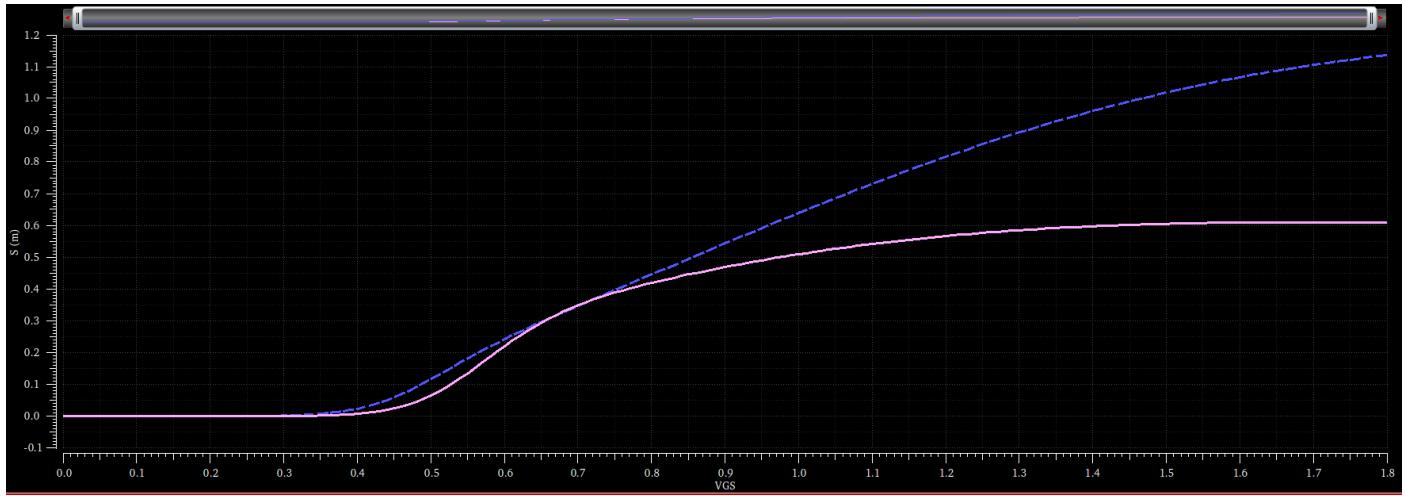
$$- \frac{I_{DN}}{I_{DP}} = \frac{953}{227} \approx 4.$$

- NMOS is more affected by short channel effects due to higher mobility which translates to smaller saturation drain-source voltage.

## 2. *gm vs VGS*

- Plot *gm* vs *VGS* for NMOS device. Set *VDS* = *VDD*, and *VGS* = 0: 10m: *VDD*. Plot the results overlaid for the following:

- Short channel device: *W* = 1μm and *L* = 200nm
- Long channel device: *W* = 10μm and *L* = 2μm.

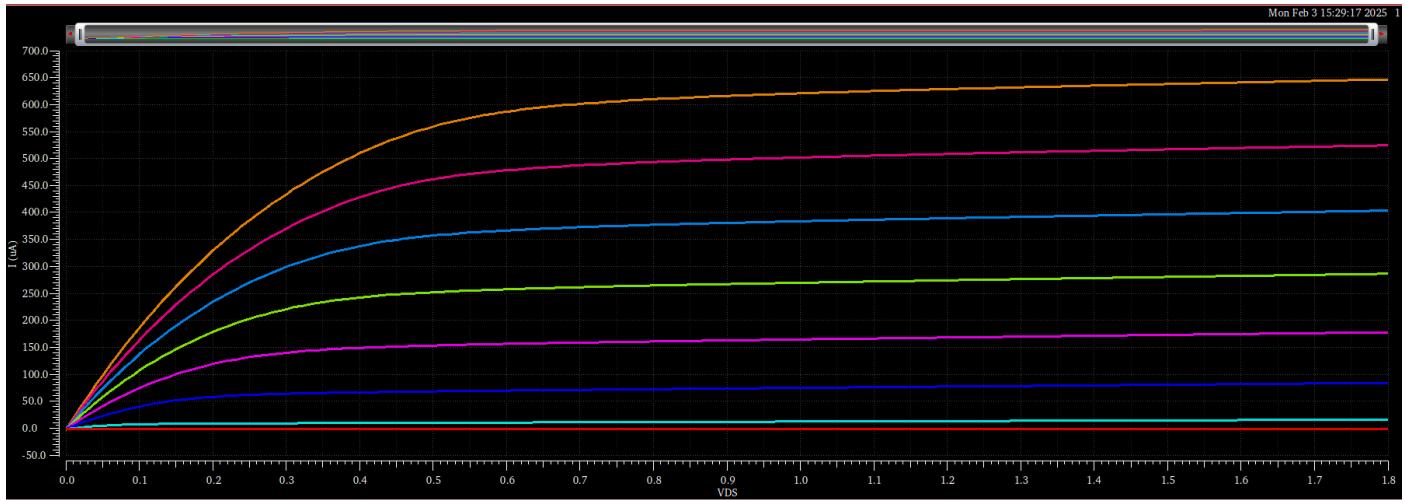


*gm VS VGS for short and long channel NMOS. Long channel is dashed*

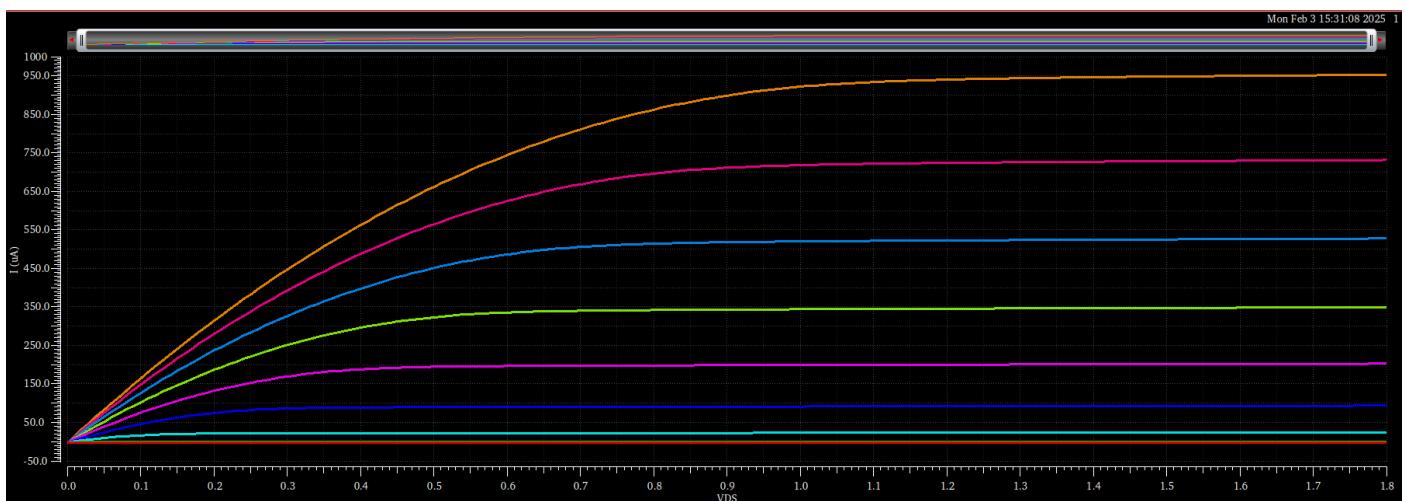
- Comment on the differences between short channel and long channel results.
- Does gm increase linearly? Why?
- Does gm saturate? Why?
- Essentially, for the long channel device, yes, gm increases linearly since it is the derivative of ID-VGS CCs, which is essentially (again, boring 😞) a quadratic curve. When the attention is turned to the short channel device, somethings change as the curve saturates after passing some value of gate-source voltage, before which the curve was very similar to that of long channel device. But after passing this value, short channel effects do what they do and alters the relationship between ID and VGS from being quadratic to be linear. Thus, gm, which is the derivative of this linear relationship, saturates and seems to be const.

### 3. ID vs VDS

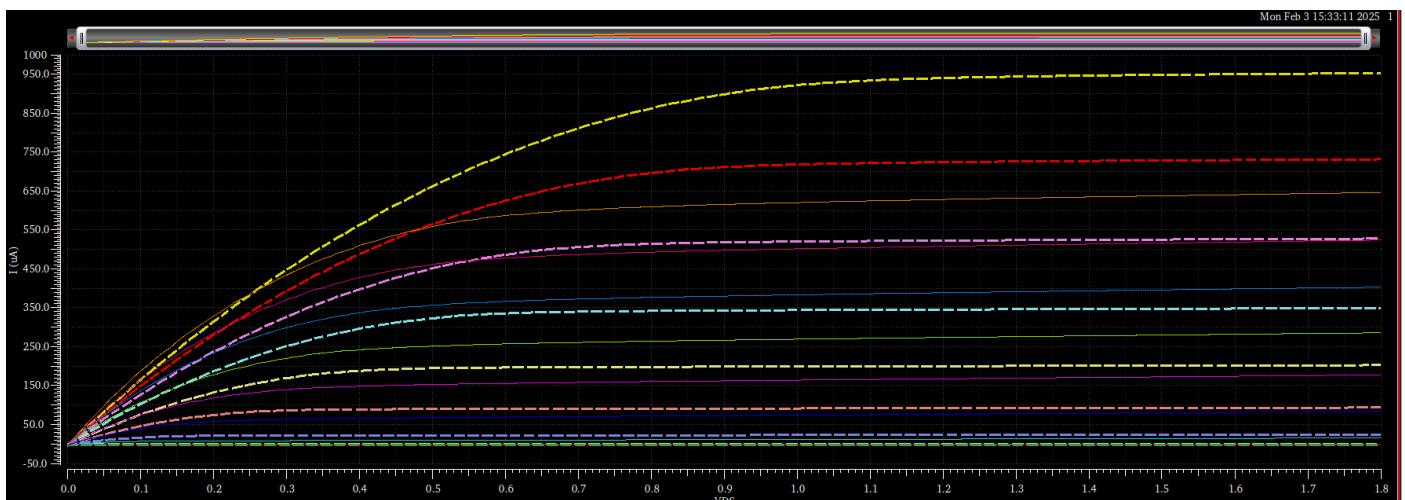
- Plot ID – VDS characteristics for NMOS device. Set VDS = 0: 10m: VDD, and VGS = 0: 0.2:VDD (nested sweep). Plot the results overlaid for the following:
- Short channel device:  $W = 1\mu m$  and  $L = 200nm$
- Long channel device:  $W = 10\mu m$  and  $L = 2\mu m$ .



Short channel NMOS ID-VDS CCs



Long channel NMOS ID-VDS CCs



Overlaid results. Long channel is dashed

- Comment on the differences between short channel and long channel results.
- Which one has higher current? Why?
- Which one has higher slope in the saturation region? Why?

- Clearly long channel device has higher current for given  $VGS$  and  $VDS$  due to short channel effects.

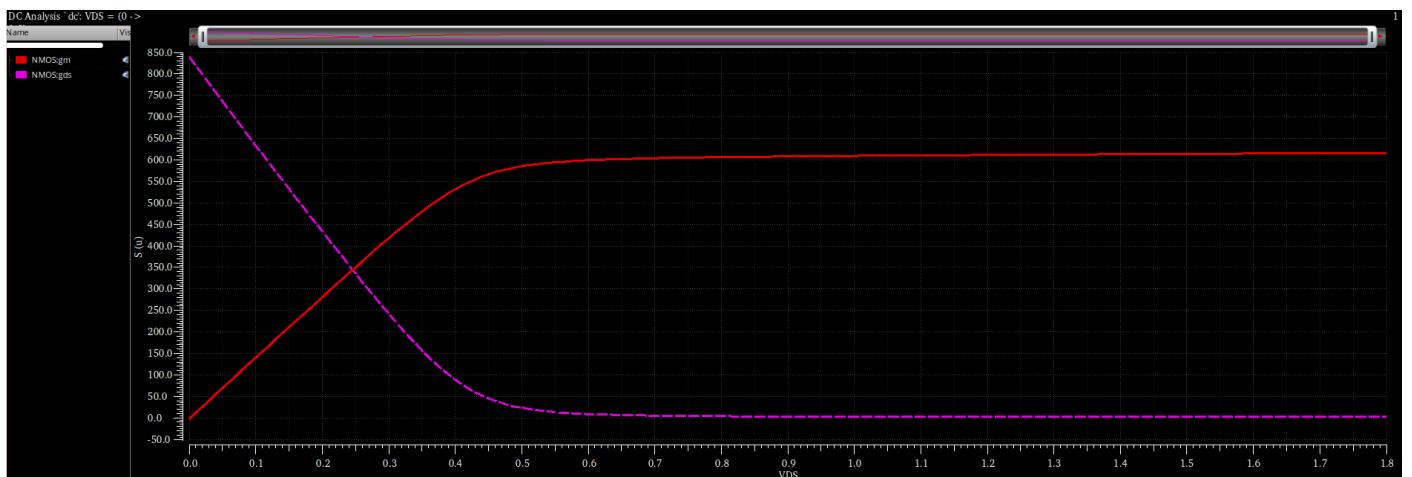
- The slope of short channel CCs at sat region is higher since shorter channel corresponds to smaller output resistance which translates to higher slope (smaller resistance  $\leftrightarrow$  larger conductance  $\leftrightarrow$  higher slope).

(I notice that the difference in slope between short and long channel CCs is not that large. Is this OK?)

#### 4. [Optional] $gm$ and $ro$ in Triode and Saturation

- Plot  $gm$  and  $ro$  vs  $VDS$  for NMOS device. Use  $W = 10\mu m$  and  $L = 2\mu m$ ,  $VDS = 0: 10m: VDD$ , and  $VGS \approx VTH + 0.5V$ .

- The value of threshold voltage is obtained from results browser, but I noticed that it varies with  $VDS$  (why?). Anyway I took the average of threshold voltage data, added half a volt which finally resulted in biasing the testbench at  $VGS$  of  $975mV$ .



$gm$  and  $gds$  VS  $VDS$

Comment on the variation of  $gm$  vs  $VDS$ .

- In the first part of the curve, is the relation linear? Why?
- Does  $gm$  saturate? Why?
- Where do you want to operate the transistor for analog amplifier applications? Why?
- Yes, if the expression of drain current at triode region is partially differentiated with respect to drain-source voltage, a linear equation would be obtained.

- Yes,  $gm$  saturates due to the weak influence of  $VDS$  on the overall performance of the transistor in sat region ( $gm$  is, clearly, included in this “overall”) (Is this expression accurate?)
- When designing an amplifier, it is highly desirable to bias all the devices deep into saturation to obtain the maximum obtainable  $gm$ . Thus, maximum obtainable gain which can deal with smaller and smaller input signals.
- Comment on the variation of  $ro$  vs  $VDS$ .
- Does  $ro$  saturate just after the transistor enters saturation similar to  $gm$ ? Why?
- Does  $ro$  increase if the transistor is biased more into saturation?
- Should we operate the transistor at the edge of saturation?
- Where do you want to operate the transistor for analog amplifier applications? Why?
- Yes, again, due to due to the weak influence of  $VDS$  on the overall performance of the transistor in sat region.
- Essentially no, the curve is similar to const curve much more being similar to any other sort of mathematical curves.
- At the edge of saturation, both  $gm$  and  $ro$  have strong nonlinear relationship with  $VDS$ , which may to linear approximation violation. (Is this answer accurate?)
- When designing an amplifier, it is highly desirable to bias all the devices deep into saturation to obtain the maximum obtainable  $ro$ . Thus, maximum obtainable gain which can deal with smaller and smaller input signals.