IEEE ASUSB AIC Design Winter Workshop 2025

Final Project

5T OTA Design

Part 2: OTA Design

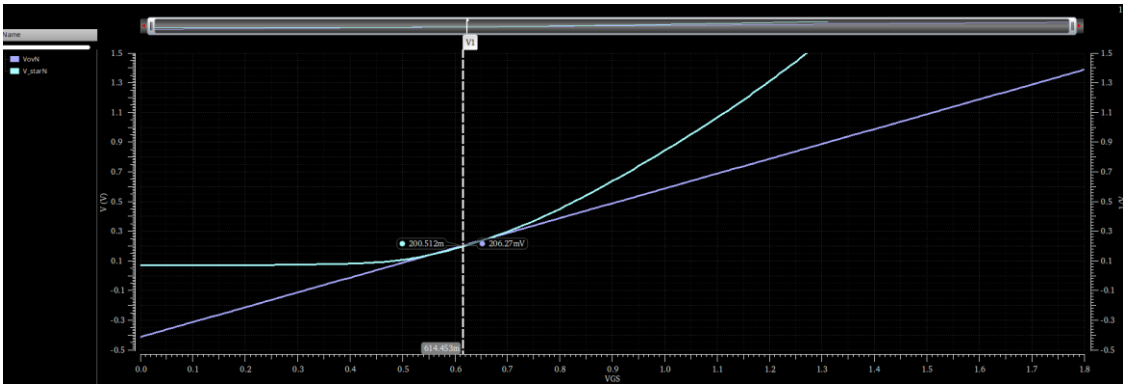
Use gm/ID methodology to design a diff input SE output operational transconductance amplifier (OTA) that achieves the following specs (listed in lab instructions file). Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec), but design your own current mirror.

- *I prefer not to use gm/ID design methodology. Rather the so called "cross multiplication" method is more suitable for me.*

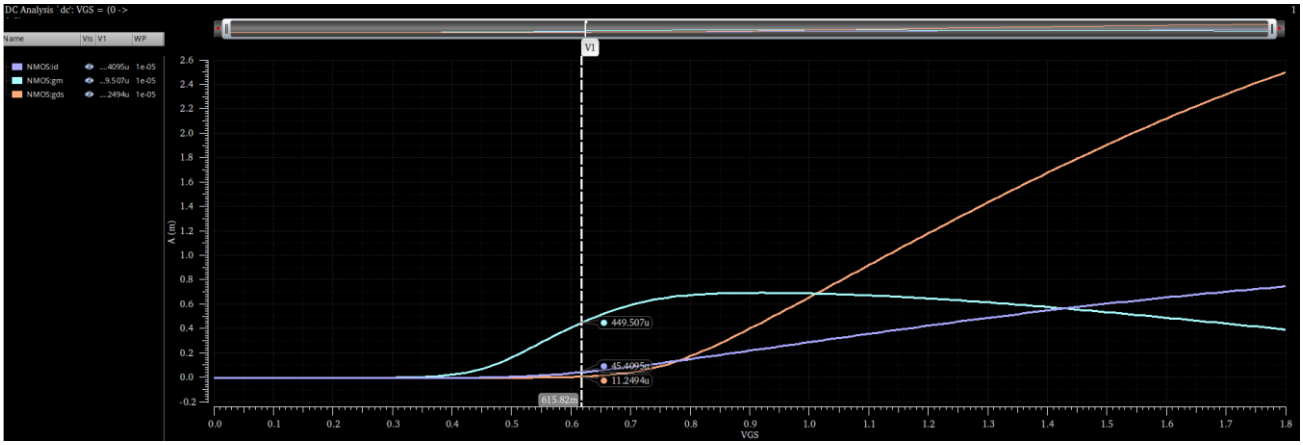
Report the following:

Detailed design procedure and hand analysis. You need to explain why you chose the architecture that you implemented.

- *The* ***CMIR*** *spec indicates that the architecture that should be used is the one with* ***NMOS*** *input pair, as CMIR range is closer to* V_{DD}.
- *Let the initial guess of the channel length of the tail CS and CM load be something like* $1um$ *(long channel). Long channels provide higher* r_o *which translates into more ideal behavior expected from the tail CS (more tendency to act as an ideal current source) and mitigate the effect of* V_{DS} *variations on the ideality of current mirroring action when it comes to CM load.*
- *Let the initial guess of* L *of the input pair be, say* $1\,um$. *This choice seems to be somehow arbitrary. Most likely it would be fine-tuned.*
- *The reference* W, *i.e.* W_X *would be* $10\,um$ *as usual.*
- *We may choose* $V^*_{i/p}$ *to be* $200mV$, *namely the soft spot. In the MOS tb,* V_{DS} *will be set to* $250mV$ *to bias the i/p pair a little deeper into sat (note that* V^* *can be considered as a good estimation for* V_{Dsat}*).*



$V_{OV,i/p}$ *and* $V^*_{i/p}$ *VS* V_{GS}. $V_{GSi/pQ} \approx 615mV$, $V_{OVi/pQ} = 206mV$.



The $I_{Di/p}$, $g_{mi/p}$ and $g_{dsi/p}$ VS V_{GS} and their values, $I_{Di/pX}$, $g_{mi/pX}$ and $g_{dsi/pX}$ at V_{GSQ}.

- *My favorite part, the* ***Cross Multiplication****.*

W

$W_X = 10um$	$I_{Di/pX} = 45.5uA$
$W_{i/pQ} = ??$	$I_{Di/pQ} = 10uA$

$$W_{i/pQ} \approx 2.2um.$$

g_m

$W_X = 10um$	$g_{mi/pX} = 450uS$
$W_{i/pQ} = 2.2um$	$g_{mi/pQ} = ??$

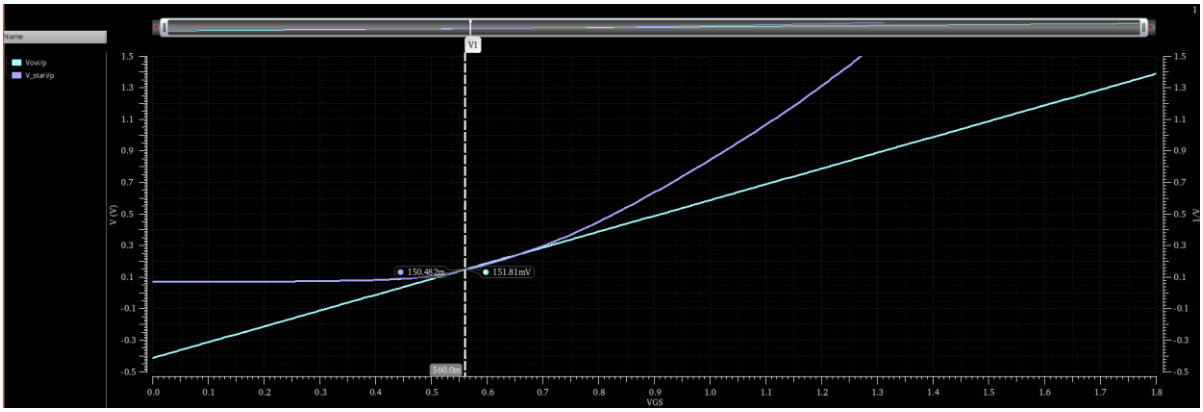
$$g_{mi/pQ} \approx 100uS.$$

g_{ds}

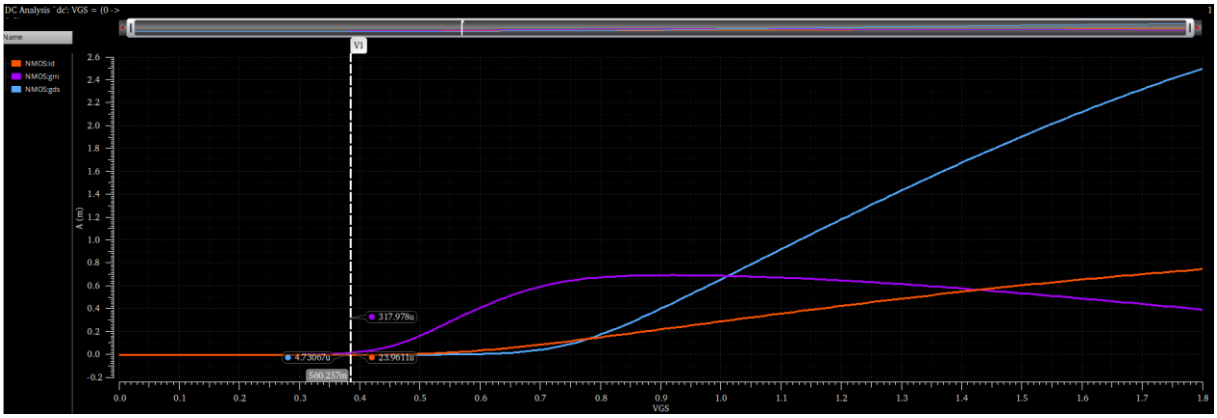
$W_X = 10um$	$g_{dsi/pX} = 11.2uS$
$W_{i/pQ} = 2.2um$	$g_{dsi/pQ} = ??$

$$g_{dsi/pQ} \approx 2.5uS, g_m r_O = \frac{g_m}{g_{ds}} \approx 40.6 < 50 \ (DC\ gain\ listed\ in\ specs\ sheet) :($$

- *Reducing $V^*_{i/p}$ seems like a good decision as one of the alternatives is increasing V_{DS} which will waste headroom. The former is better when thinking this way. Let $V^*_{i/p} = 150mV$.*



$V_{OVi/p}$ and $V^*_{i/p}$ VS V_{GS} after refining V^*. $V_{GSi/pQ} \approx 560mV$, $V_{OVi/pQ} \approx 150mV$.



The $I_{Di/p}$, $g_{mi/p}$ and $g_{dsi/p}$ VS V_{GS} and their values, $I_{Di/pX}$, $g_{mi/pX}$ and $g_{dsi/pX}$ at V_{GSQ}.

W

$W_X = 10um$	$I_{Di/pX} = 24uA$
$W_Q = ??$	$I_{Di/pQ} = 10uA$

$$W_{i/pQ} \approx 4.2um.$$

g_m

$W_X = 10um$	$g_{mi/pX} = 318uS$
$W_Q = 4.2um$	$g_{mi/pQ} = ??$

$$g_{mi/pQ} \approx 133uS.$$

g_{ds}

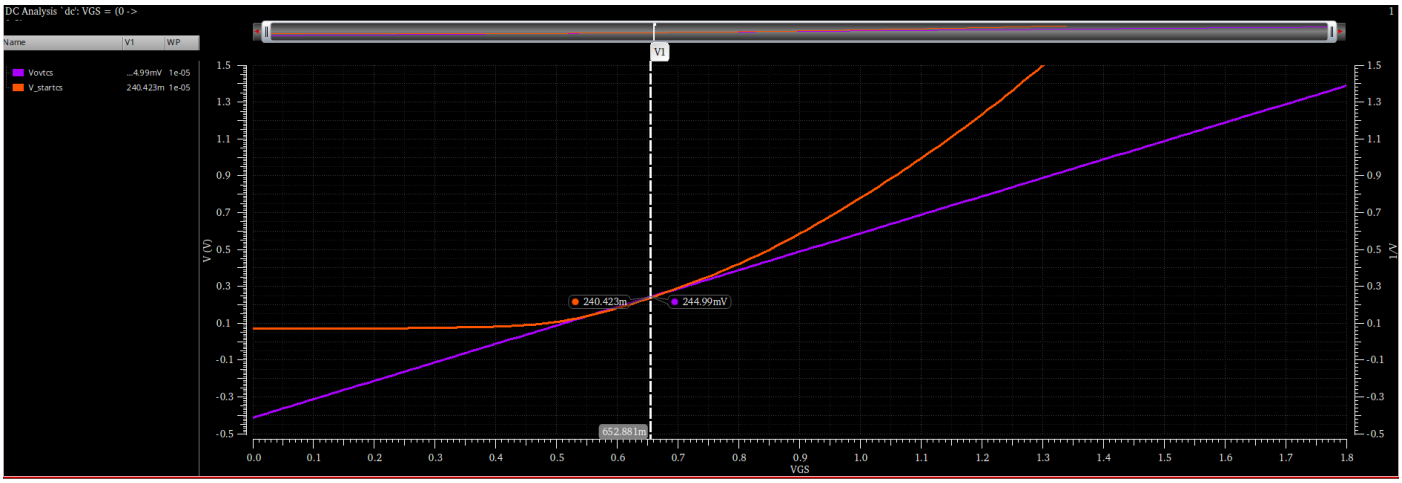
$W_X = 10um$	$g_{dsi/pX} = 4.7uS$
$W_Q = 4.2um$	$g_{dsNQ} = ??$

$$g_{dsNQ} \approx 2uS, g_m r_O = \frac{g_m}{g_{ds}} = 66.5 > 50 :D$$

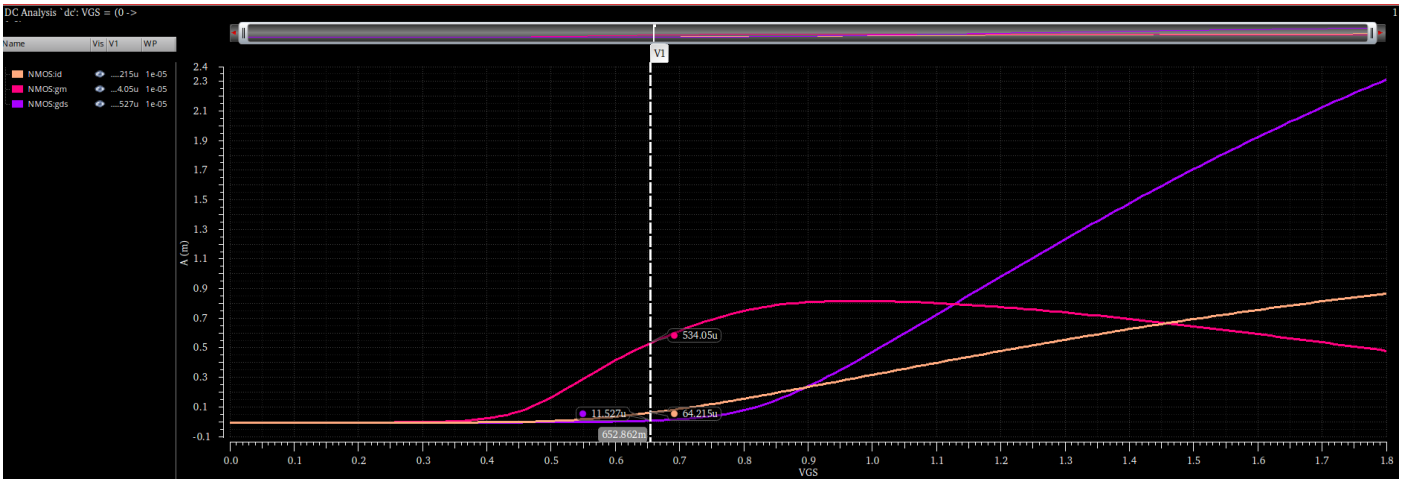
- *Let's design the tail current source.* V_{tcs}^{*} *would be determined from the lower limit of* $\boldsymbol{CMIR}$.

$Applying\ KVL: V_{ICMLo} - V_{GSi/pQ} - V_{tcs}^{*} = 0.$ $Given\ V_{GSi/pQ} = 560mV, V_{ICMLo} = 0.8V \rightarrow V_{tcs}^{*} = 240mV.$

- *Current sources need the largest* r_o *possible. One essential parameter contributing in maximizing* r_o *is* V_{DS}. *In MOS tb,* V_{DS} *would be set to* $300mV$ *to go some distance deeper into sat.*



V_{OVtcs} *and* V_{tcs}^{*} *VS* V_{GS}. $V_{GStcsQ} \approx 653mV$, $V_{OVtcsQ} \approx 245mV$.



The I_{Dtcs}, g_{mtcs} *and* g_{dstcs} *VS* V_{GS} *and their values,* I_{DtcsX}, g_{mtcsX} *and* g_{dstcsX} *at* V_{GSQ}.

W

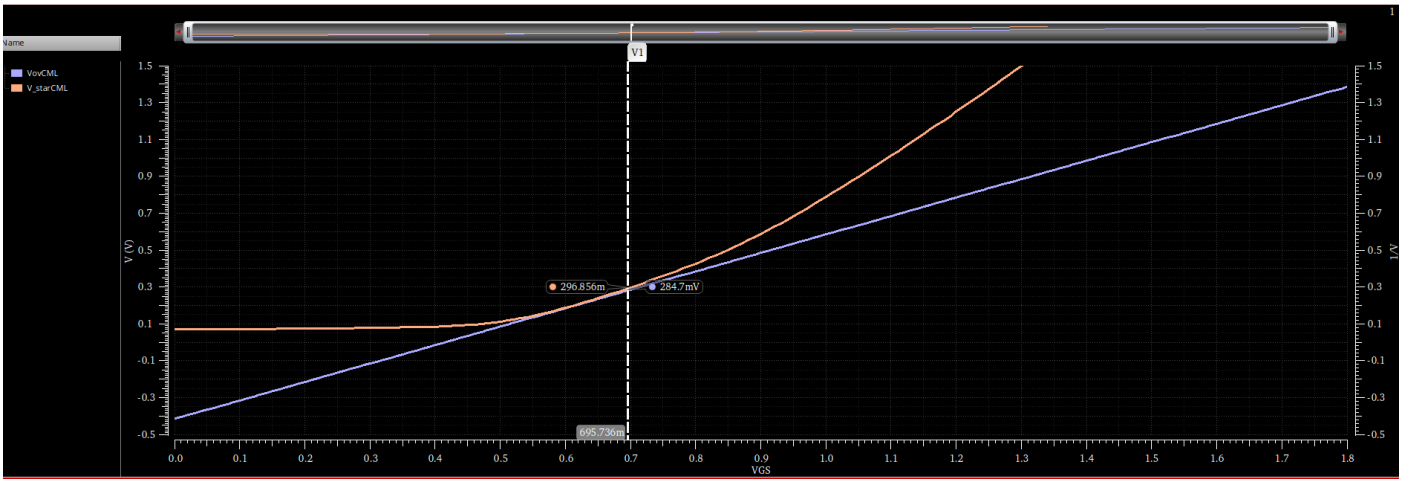
$W_X = 10um$	$I_{DtcsX} = 64uA$
$W_Q = ??$	$I_{DtcsQ} = 20uA$

$W_{tcsQ} \approx 3.1um.$

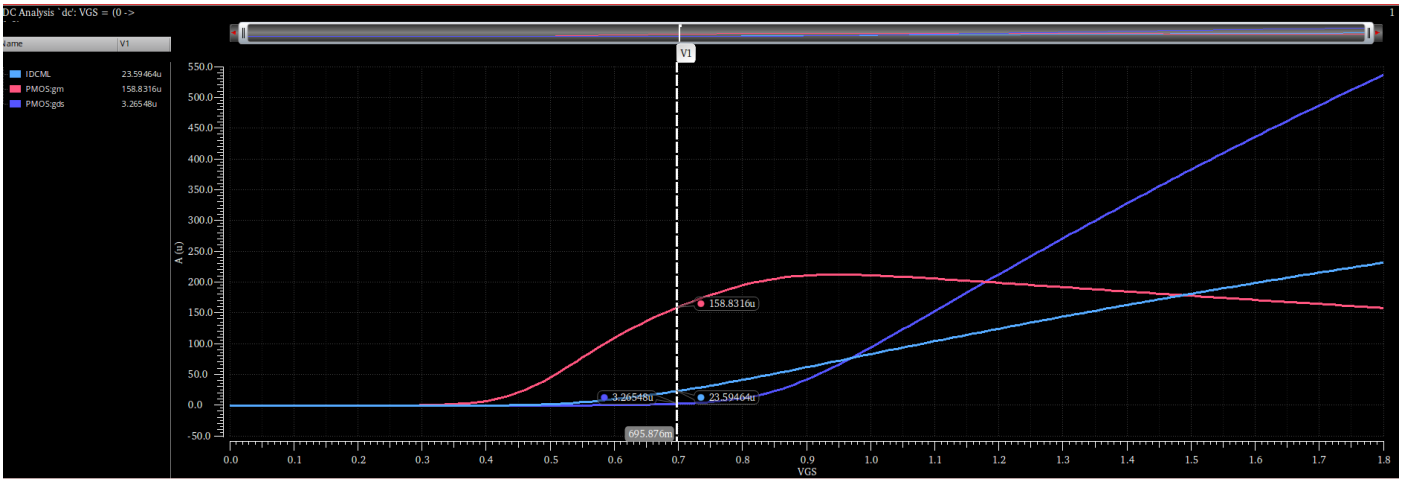
- *It's time to move the attention to CM load.* V_{CML}^* *would be determined from the upper limit of* $\boldsymbol{CMIR}$ *spec.*

$$Applying\ KVL: V_{CML}^* = V_{DD} - V_{iCMHi} - |V_{THP}| + V_{THN}.$$
$$Given\ V_{DD} = 1.8V, V_{iCMHi} = 1.5V, |V_{THP}| = 411mV, V_{THN} = 407mV$$
$$V_{CML}^* = 297mV.\ (V_{TH}\ data\ is\ obtained\ from\ DC\ OP)$$

- *Again, to go deeper into sat,* V_{DS} *would be set to* $350mV$ *in MOS tb.*



V_{OVCML} *and* V_{CML}^* *VS* V_{GS}. $V_{GSCMLQ} \approx 696mV$, $V_{OVCMLQ} \approx 285mV$.



The I_{DCML}, g_{mCML} *and* g_{dsCML} *VS* V_{GS} *and their values,* I_{DCMLX}, g_{mCMLX} *and* g_{dsCMLX} *at* V_{GSQ}.

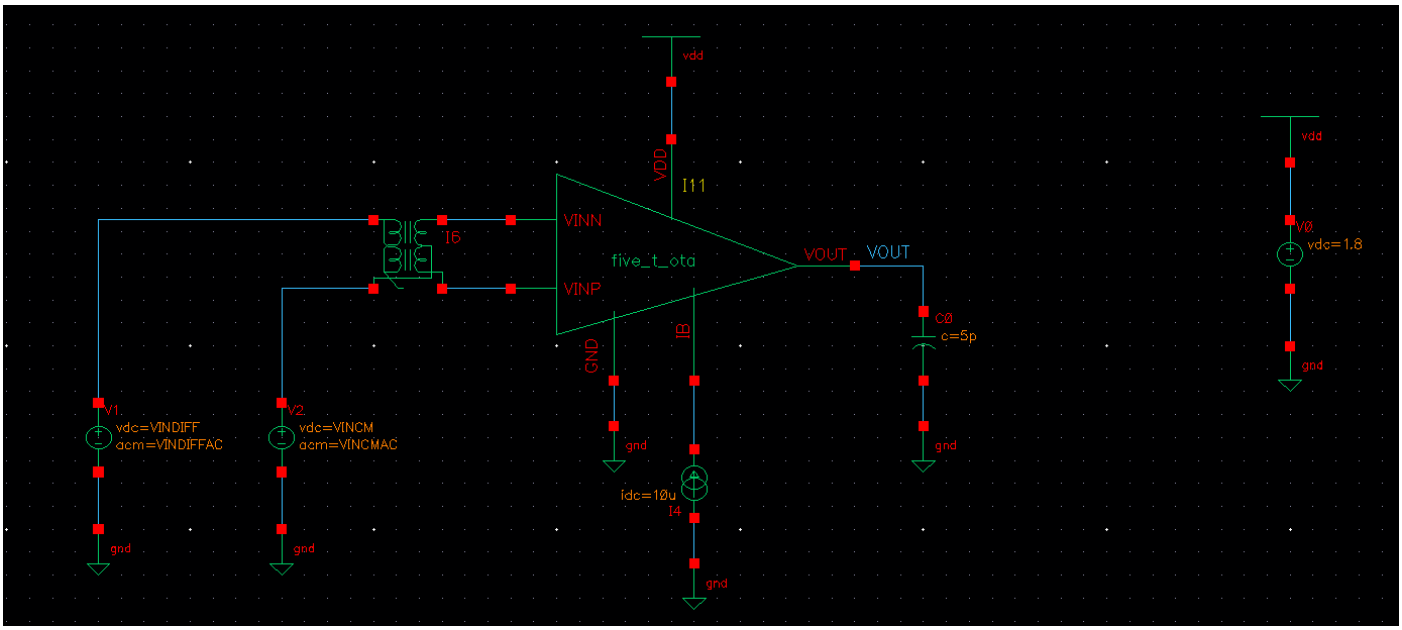
W

$W_X = 10um$	$I_{DCMLX} = 23.6uA$
$W_Q = ??$	$I_{DCMLQ} = 10uA$

$$W_{CMLQ} \approx 4.2um.$$

Part 3: Open-Loop OTA Simulation

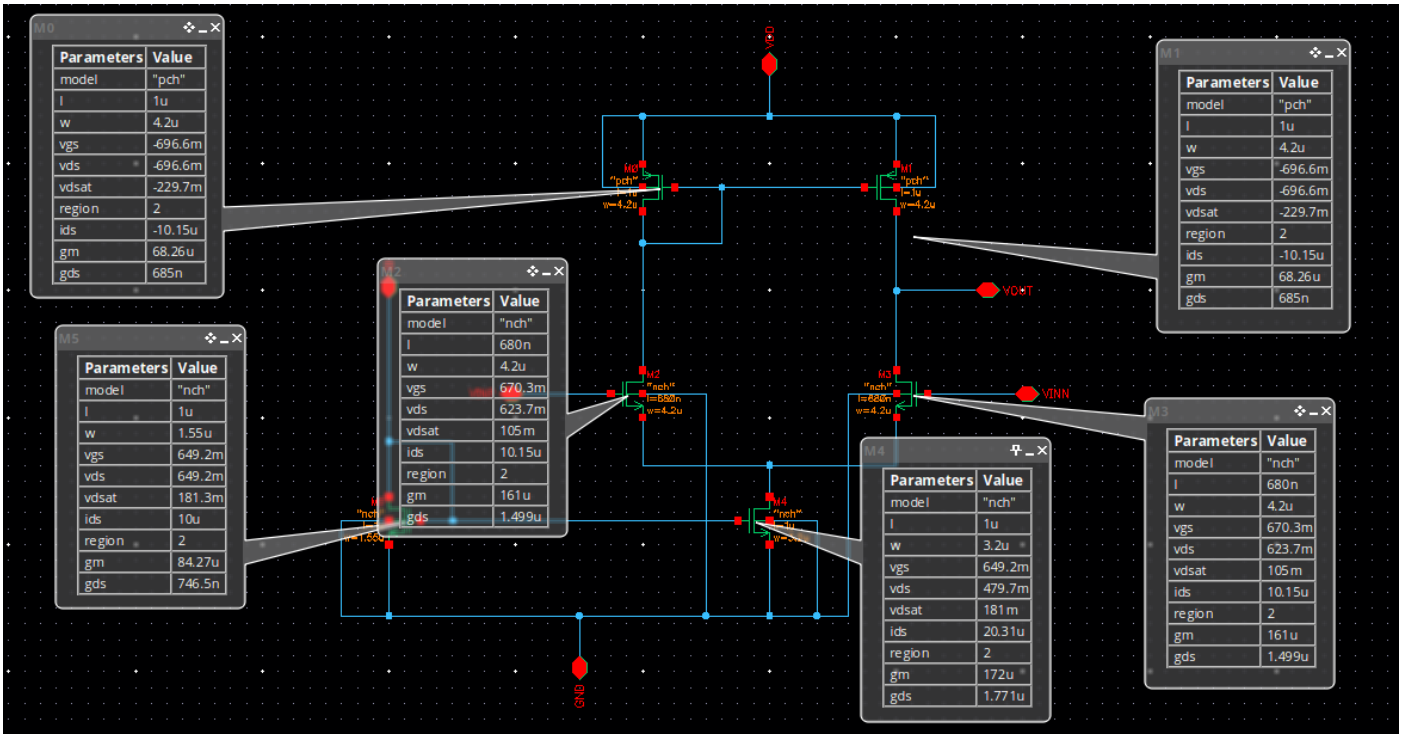
Create a testbench as shown above. Note that IDC connection (sinking or sourcing) in the test bench may be different from the one shown above depending on the type of your input pair (PMOS/NMOS).



Required schematic

Schematic of the OTA with DC node voltages clearly annotated.

- *Use VICM at the middle of the CMIR.*



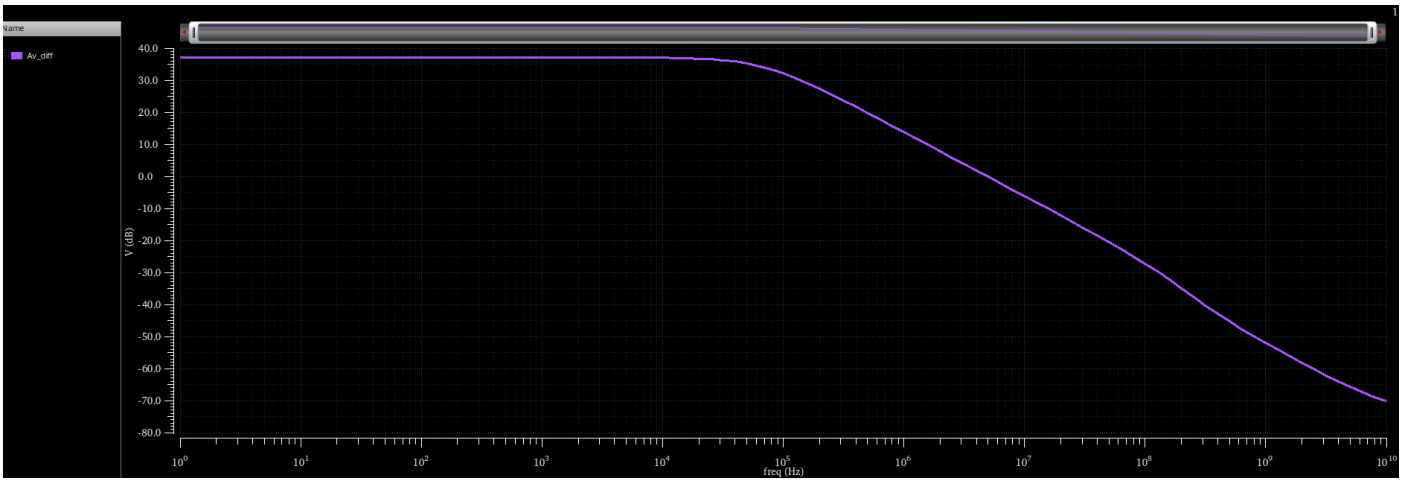
Required snapshot

- *Is the current (and gm) in the input pair* ***exactly*** *equal?*
  Yes.
- *What is DC voltage at VOUT? Why?*

$$V_{OCM} \approx 1.1 = \frac{V_{in1} + V_{in2}}{2} = V_{in1,2}$$

Diff small signal ccs:

- *Use AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).*
  Set VIDAC = 1 and VICMAC = 0.
  Use VICM at the middle of the CMIR.
  Plot diff gain (in dB) vs frequency.



Bode mag plot of diff gain

Test	Output	Nominal	Spec	Weight	Pass/Fail
IEEE_ASUSB:five_t_ota_tb:1	Av_diff_mag	73.36			
IEEE_ASUSB:five_t_ota_tb:1	Av_diff_dB	37.31			
IEEE_ASUSB:five_t_ota_tb:1	BW	68.64k			
IEEE_ASUSB:five_t_ota_tb:1	UGF	5.033M			
IEEE_ASUSB:five_t_ota_tb:1	GBW	5.048M			

Required calculations

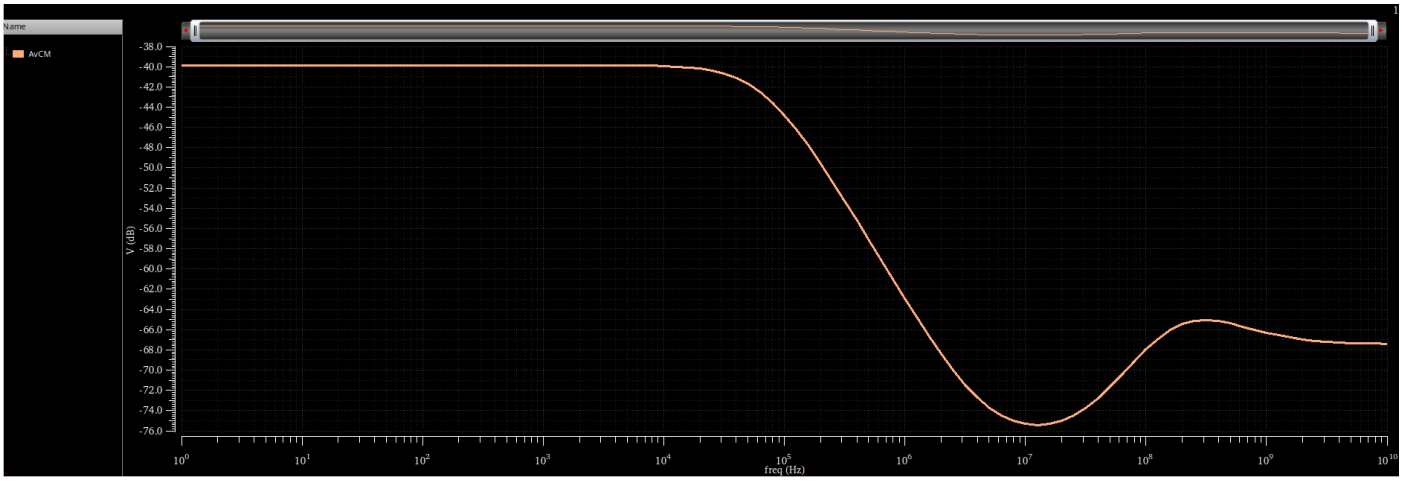
- *Compare simulation results with hand calculations in a table.*

Quantity	*Simulated*	*Calculated*
DC gain	73.4	$g_{m12}(r_{O2}\|\|r_{O4}) \approx 73.7$
BW	$68.6kHz$	$\frac{1}{2\pi R_{out} C_L} \approx 69.6kHz$
GBW	$5.048MHz$	$5.12MHz$

CM small signal ccs:

- *Use AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).*

Set VICMAC = 1 and VIDAC = 0.
Use VICM at the middle of the CMIR.
Plot CM gain in dB vs frequency.



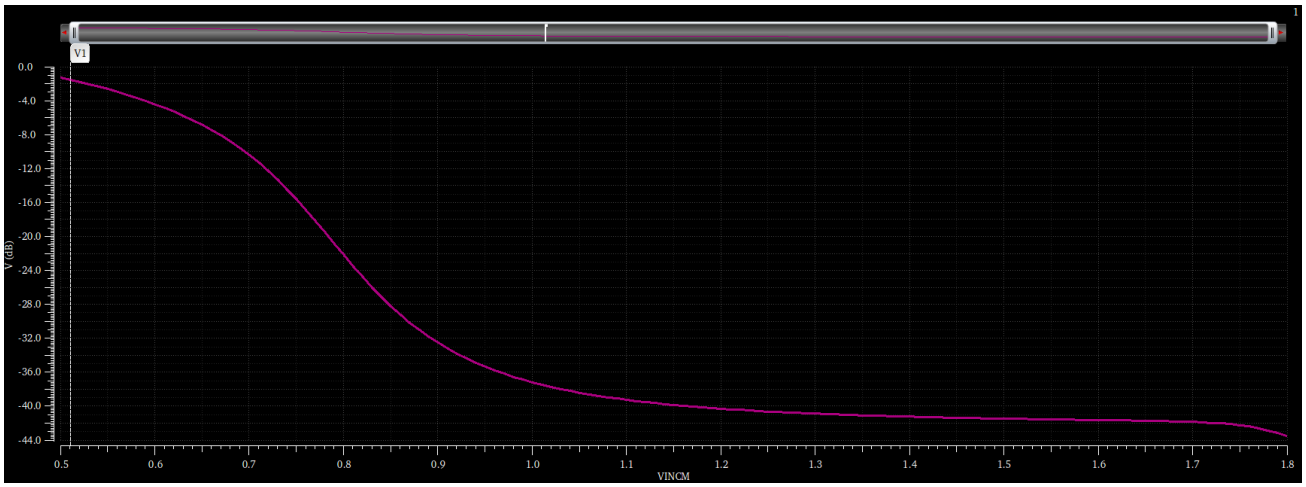
Bode Mag plot of CM gain

- *Compare simulation results with hand calculations in a table.*

Quantity	*Simulated*	*Calculated*
A_{vCM}	$\approx -40dB$	$\frac{g_{dstcs}}{2g_{m34}} \approx 13.2e-3$ $= -37.6dB$

(Optional) Avcm vs VICM:

- *Use **parametric** sweep (**not DC sweep**) for VICM = CMIR-low:10m:CMIR-high.*
  Plot CM gain at 1Hz in dB vs VICM.



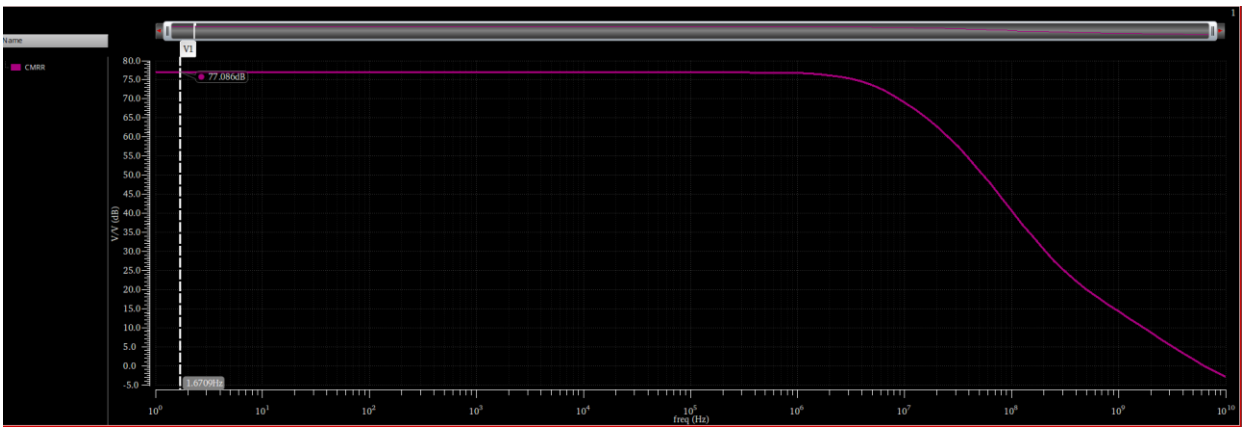
Required plot

- *Justify the results.*

As V_{ICM} increases, V_{DStcs} increases in response. Thus, r_{Otcs}, or the so-called R_{SS} also increases. This R_{SS} is inversely proportional to A_{vCM}. This can be summarized as follows: $V_{ICM} \uparrow \rightarrow V_{DStcs} \uparrow \rightarrow R_{SS} \propto \frac{1}{A_{vCM}} \uparrow \rightarrow A_{vCM} \downarrow$.

CMRR:

- *Use VICM at the middle of the CMIR.*
  Plot CMRR in dB vs frequency at VICM at the middle of the CMIR.



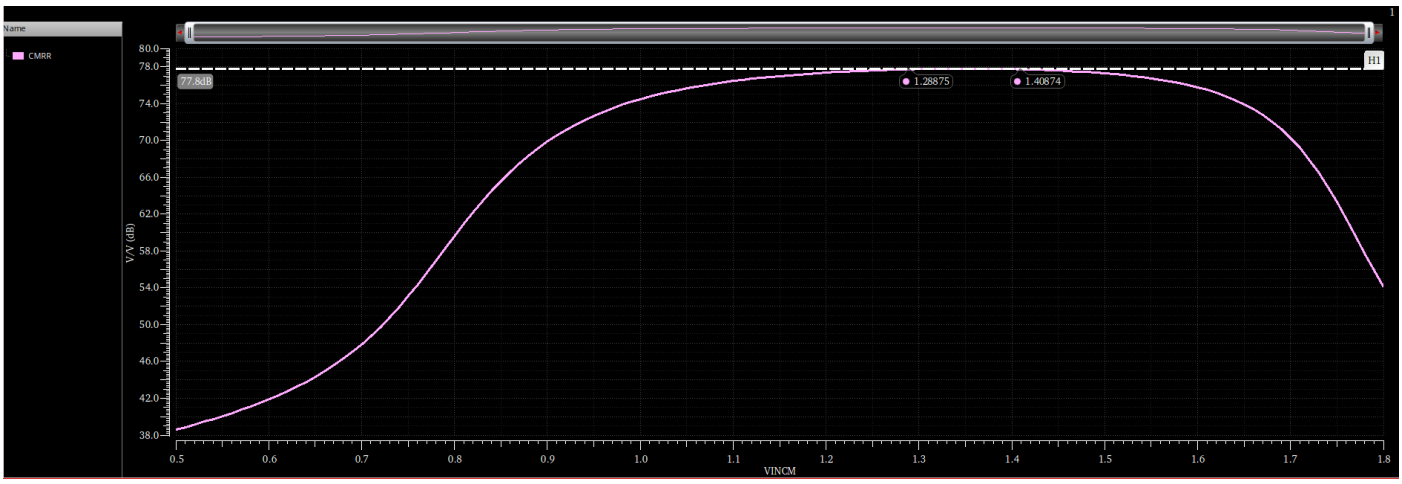
Required plot

- *Compare simulation results with hand calculations in a table.*

Quantity	*Simulated*	*Calculated*
CMRR	*77dB*	$= A_{vddB} - A_{vCMdB} \approx 77dB$

(Optional) CMRR vs VICM:

- *Use **parametric** sweep (**not DC sweep**) for VICM = CMIR-low:10m:CMIR-high.*
  Plot CMRR at 1Hz in dB vs VICM.

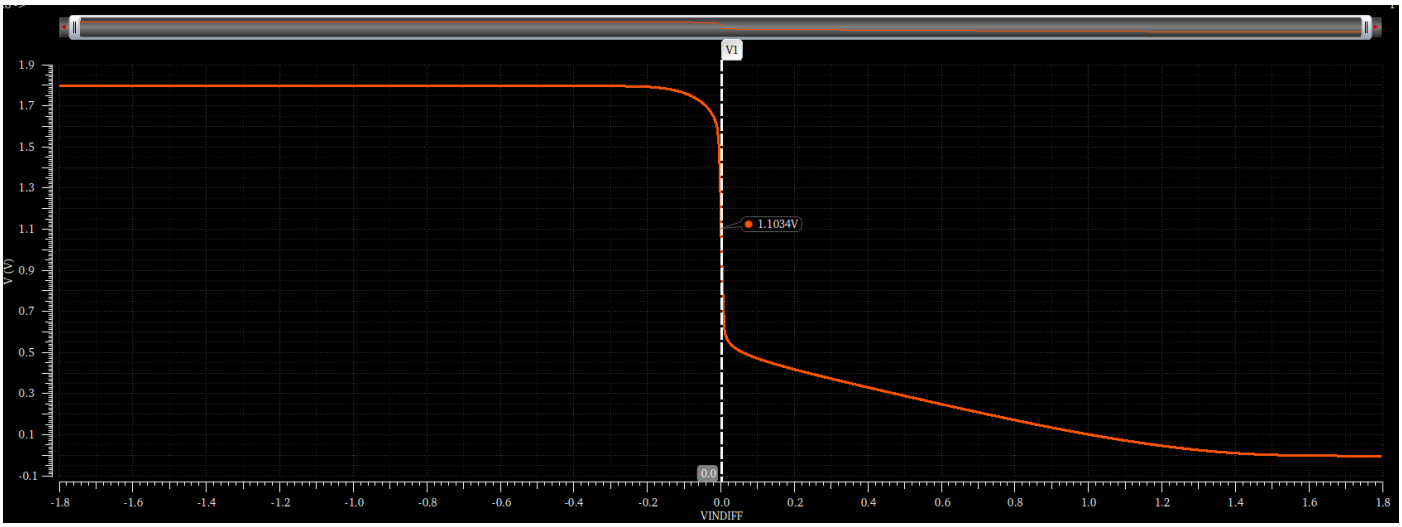


Required plot

- *Justify the results.*
  *At V_{iCMLO}, V_{DStcs} is at its lowest limit and so is R_{SS}. Thus A_{vCM} is maximum as there is inverse proportionality between R_{SS} and A_{vCM}, as mentioned above. This can be related to the poor CMRR ($\max(A_{vCM}) \leftrightarrow \min(CMRR)$). Increasing V_{iCM} leads to A_{vCM} degradation and thus **$CMRR$** increases. When V_{iCM} approaches its maximum allowable value, CMRR begins to decrease since the i/p pair gets closer to the edge of sat which is a region characterized by poor g_m and r_O, and this corresponds to poor A_{vd} and thus poor CMRR.*

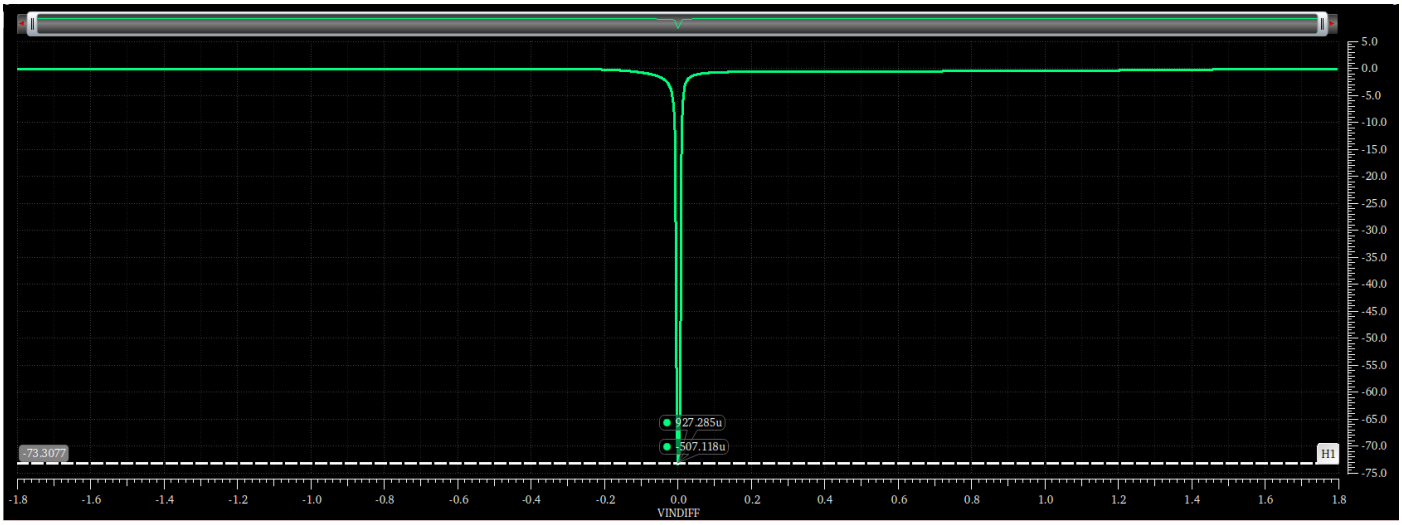
Diff large signal ccs:

- *Use VICM at the middle of the CMIR.*
  *Use DC sweep (**not parametric sweep**) VID = -VDD:1m:VDD. You must use a small step (1mV) because the gain region is very small (steep slope).*
  Plot VOUT vs VID. From the plot, what is the value of Vout at VID = 0? Why?



Required plot

- $V_O(0) \approx 1.1V$. *This value is the same as the one obtained in DC OP analysis, and they are similar since the inputs to the circuit in both cases are **exactly** the same. In DC OP analysis, the CM input was set to the middle of CMIR and so is the case here. Additionally, in the former analysis, no diff excitation was present and **so the case here** as $V_{id} = 0$.*
- *Plot the derivative of VOUT vs VID. Compare the peak with Avd.*

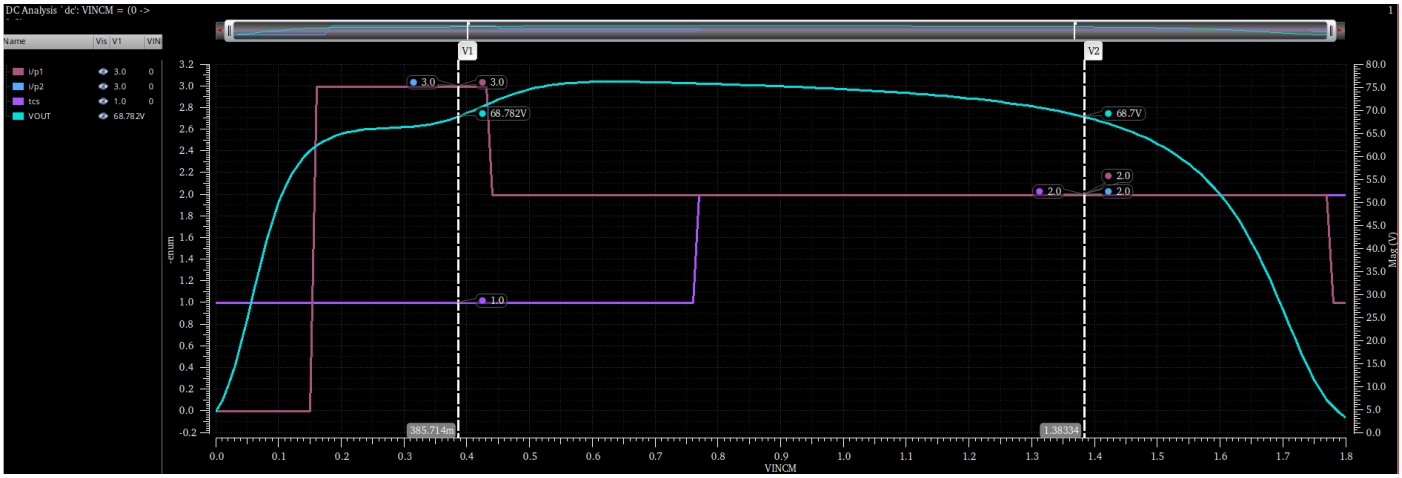


Required plot

- $\max\left(deriv(A_{vd})\right) = 73 = A_{vd}$.

CM large signal ccs (region vs VICM):

- *Use* ***DC sweep*** *(not parametric sweep) VICM = 0:10m:VDD. Plot "region" OP parameter vs VICM for the input pair and the tail current source (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown). Plot the results overlaid on the results of the previous method (10% reduction of GBW).*

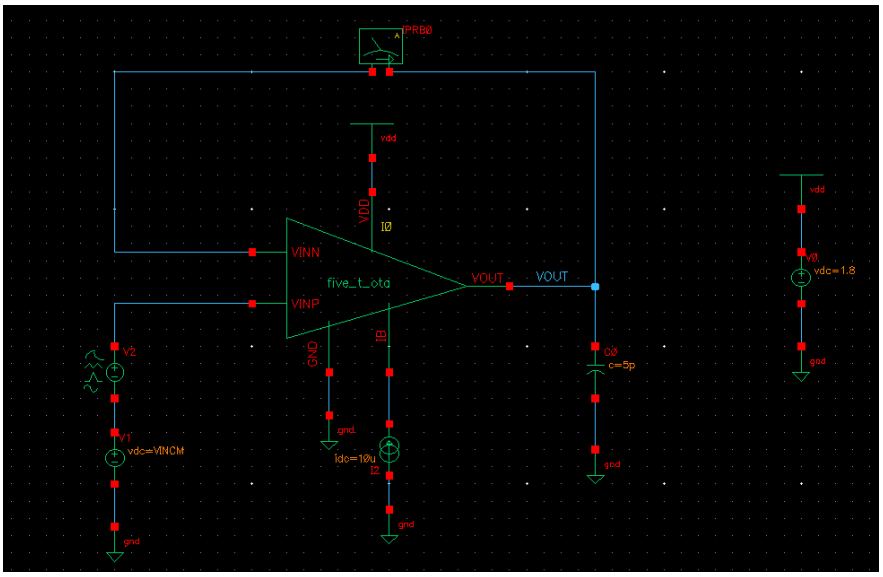


Required plot. Ymax(Vout)=76.35, 10% reduction of Vout corresponds to Vout =68.7.

$0.8V < CMIR < 1.8V\ (from\ region\ data)$
$385mV < CMIR < 1.4V\ (from\ 10\%\ gain\ drop\ data)$

Part 4: Closed-Loop OTA Simulation

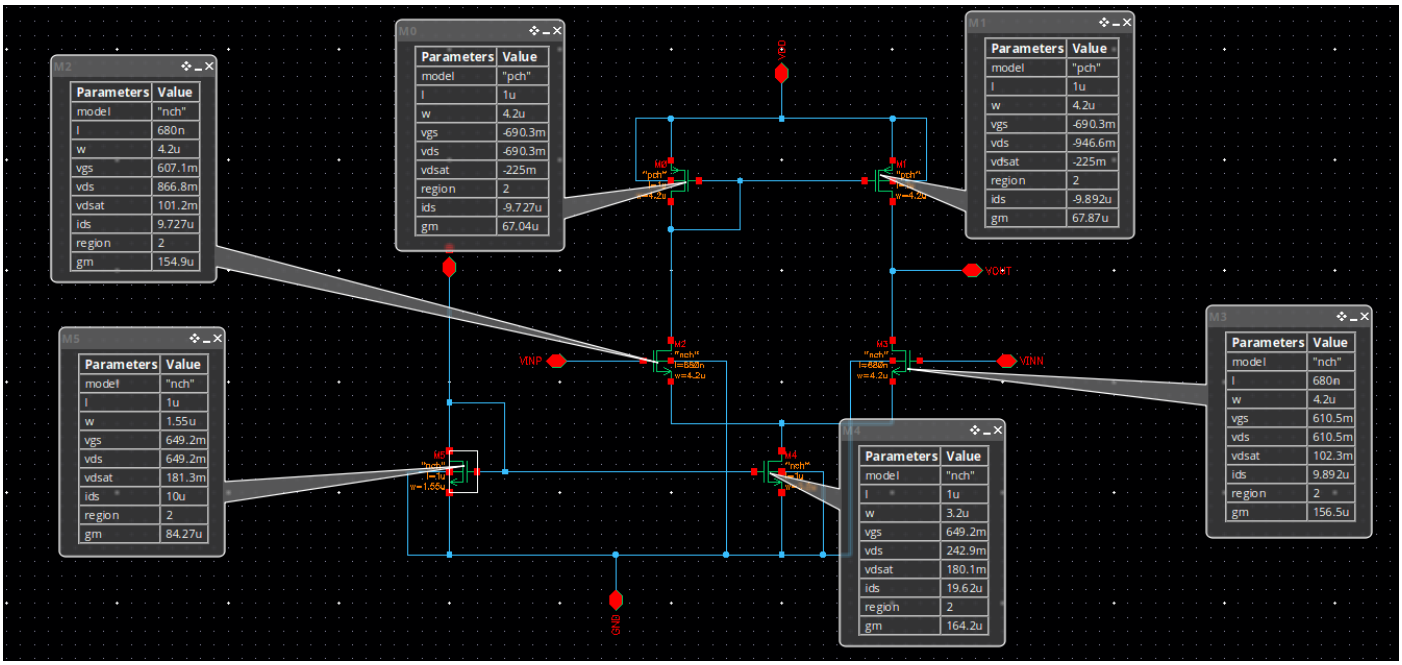
Create a testbench as shown above.



Required testbench

Report the following:

- *Schematic of the OTA with DC OP point clearly annotated in unity gain buffer configuration. Use VIN = CMIR-low + 50mV.*



Required snapshot

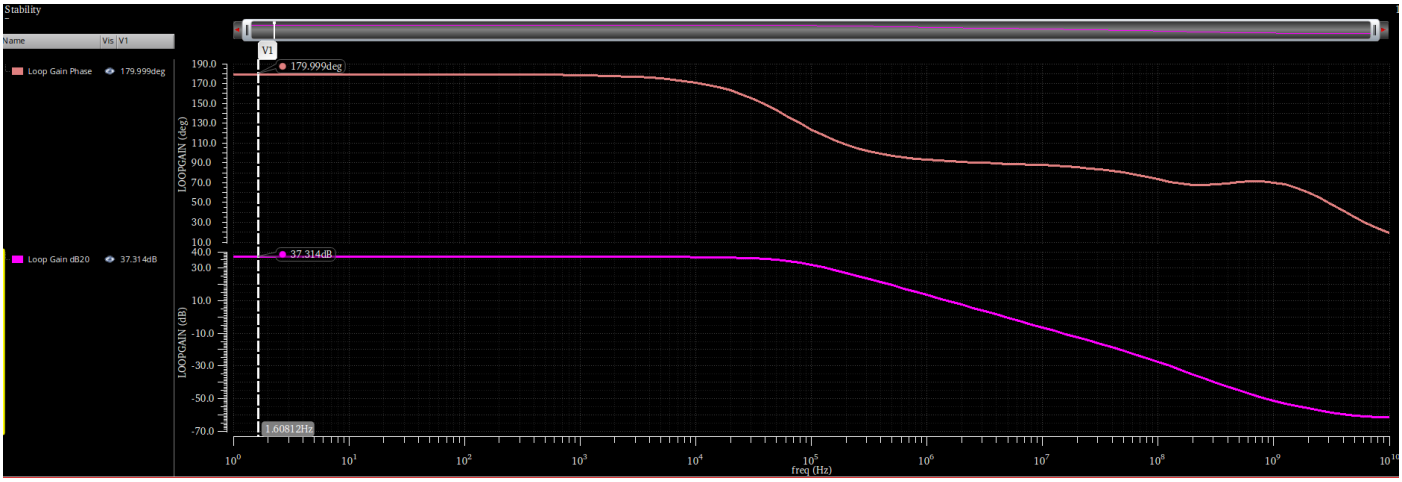
- *Is the current (and g_m) in the input pair exactly equal? Why?*
  No. There is a slight difference due to a similar difference in V_{GS} resulting from the finite practical (deviation from ideality) difference present between the inverting and non-inverting terminals of the OTA.

- *Calculate the mismatch in I_D and g_m.*

$\%\Delta I_D = \frac{I_{DLeft} - I_{DRight}}{I_{DRight}} \approx 1.66\%$ *(Assuming the reight half is the ref)*
$\%\Delta g_m = \frac{g_{mLeft} - g_{mRight}}{g_{mRight}} \approx 1.02\%$ *(Assuming the reight half is the ref)*

Loop gain:

- *Use STB analysis (1Hz:10GHz, logarithmic, 10 points/decade) in unity gain buffer configuration.*
  Use VICM at the middle of the CMIR.
  Plot loop gain in dB and phase vs frequency.



Bode Mag and φ plots of loop gain

Test	Output	Nominal	Spec	Weight	Pass/Fail
IEEE_ASUSB:five_t_ota_cl_tb:1	GBW	5.028M			

LG GBW

- *Compare DC gain and GBW with those obtained from open-loop simulation. Comment.*

Quantity	*OL sim results*	*LG sim results*
DC gain	37.3dB	37.3dB
GBW	5MHZ	5MHz

As the feedback loop is built in unity gain configuration, $\beta = 1$ and thus $LG = \beta A_{OL} = A_{OL}$. This justifies the equality between A_{OL} and LG and the BW of both quantities.

- Compare simulation results with hand calculations in a table.

Quantity	*Simulated*	*Calculated*
DC gain	$37.3dB$	$37.3dB$
GBW	$5MHZ$	$5.12MHz$

Exactly the same as OL Calculations as $\beta = 1$ *and is frequency independent, thus it has no ability to make any difference between* A_{OL} *and* LG.