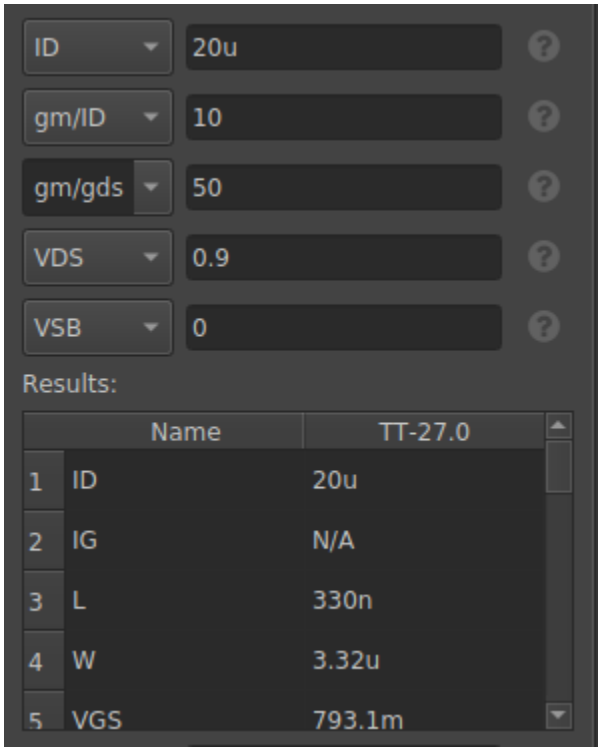
CMOS AIC design - ITI - Lab 3

Part 1: Device Sizing using ADT SA

- Take the values of L,W and VGS0 to xschem

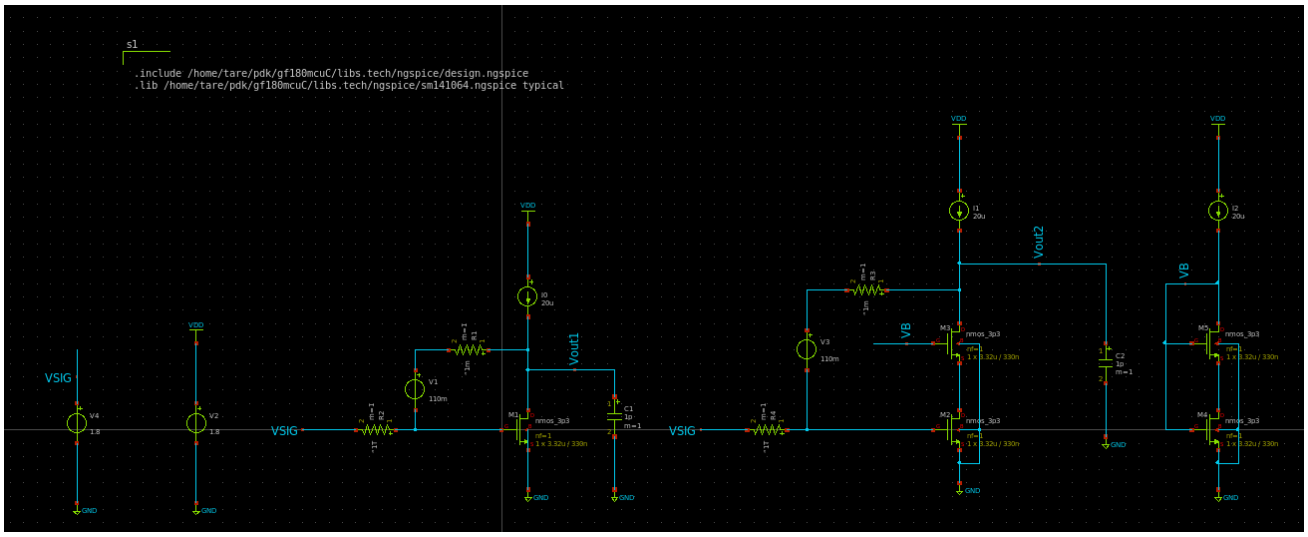


Values of W, L and VGS0

PART 2: Cascode for Gain

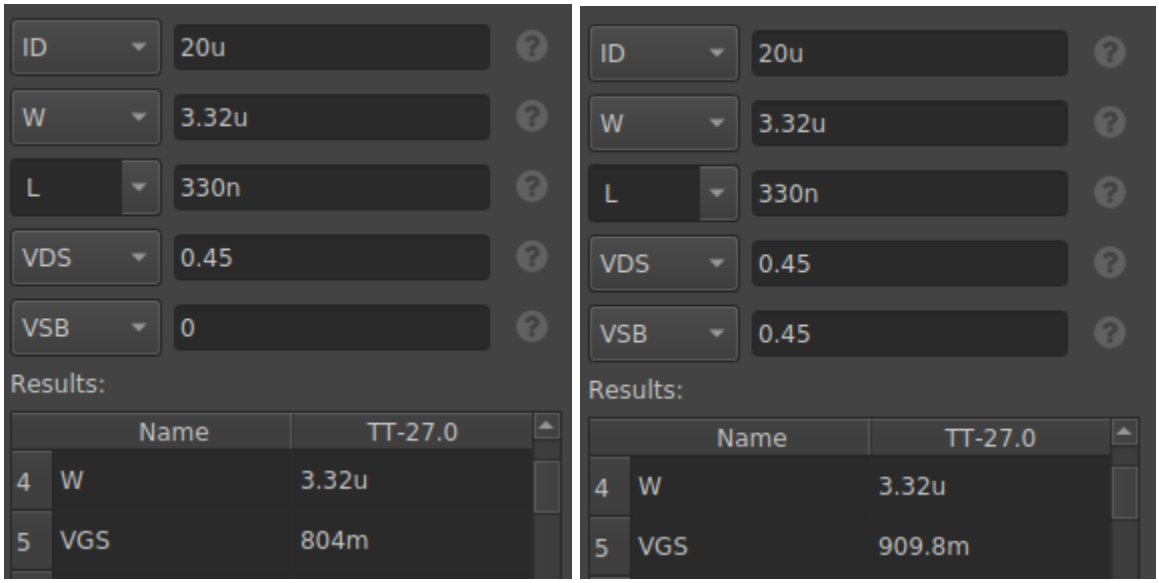
1. OP Analysis

- Create a new schematic. Construct the circuit shown below. Use $I_B = 20\mu A$. Use L and W as selected in Part 1 for M0, M1, M2, and M4. Use the same W for M3 but it will have different L as will be shown later. Use $C_L = 1pF$.



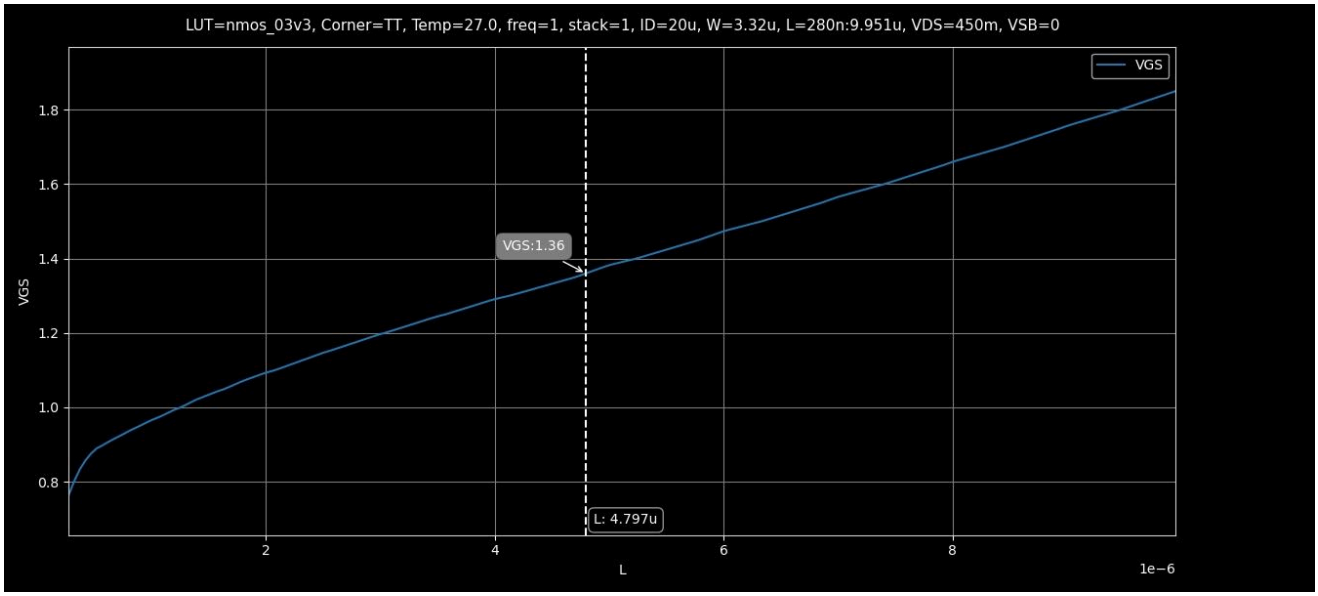
Required circuit

- $X = V_{DS} - V_{GS} = 0.9 - 790m = 110mV.$



VGS1 (left) and VGS2 (right)

- $V_B = V_{GS2} + V_{DS1} = 910 + 450 = 1.36V.$



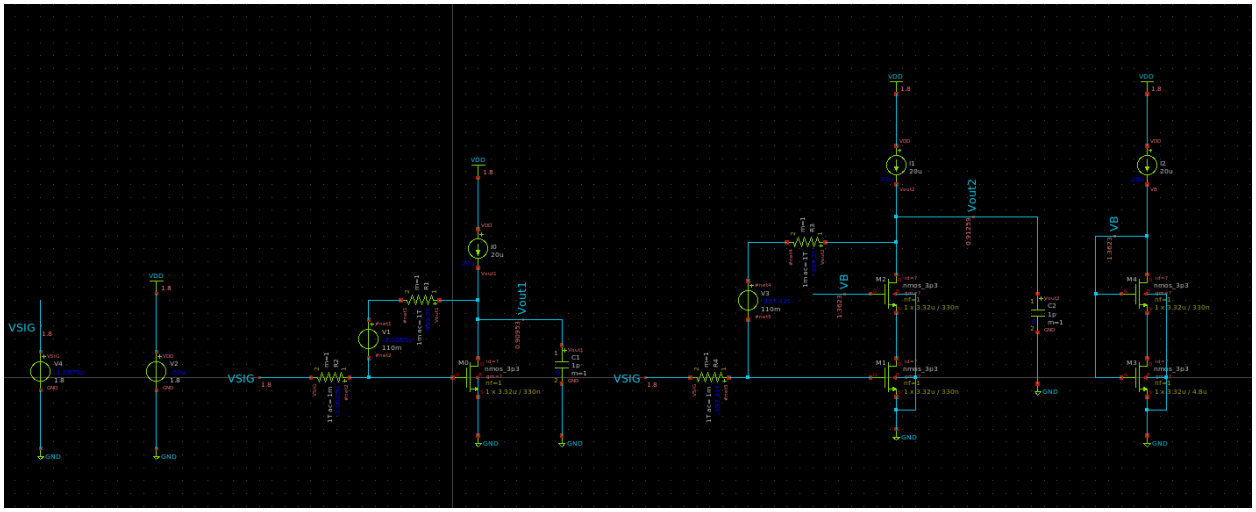
L3=4.8um

- Simulate the DC OP point of the above CS and cascode amplifiers (ngspice interactive). Report a snapshot showing the following parameters for M0 to M4 in addition to DC node voltages clearly annotated.

```
igain0 = 4.709365e+01
igain1 = 1.472122e+03
binary raw file "lab3.raw"
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device              m.xm3.m0              m.xm4.m0              m.xm2.m0
      model           nmos_3p3.10            nmos_3p3.8            nmos_3p3.8
         id                 2e-05                 2e-05                 2e-05
        vgs               1.36188               0.89429              0.918428
        vds              0.467575              0.894283              0.471727
        vth              0.655211              0.765221              0.783969
      vdsat              0.548127              0.164367              0.167981
         gm           4.64087e-05           0.000198544           0.000195551
        gds           1.17144e-05           4.56889e-06           5.66809e-06
       gmbs           1.79444e-05           4.08522e-05           4.10553e-05
        cdb          -8.10978e-15          -1.98582e-16          -2.0581e-16
        cgd           -4.1443e-15           2.53688e-17           2.08393e-17
        cgs          -4.50086e-14          -2.36991e-15          -2.3946e-15
        csb          -1.07759e-14          -2.97466e-16          -3.06532e-16

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device              m.xm1.m0              m.xm0.m0
      model            nmos_3p3.8            nmos_3p3.8
         id                 2e-05                 2e-05
        vgs              0.805187              0.788612
        vds              0.443437              0.898604
        vth              0.672999              0.662321
      vdsat              0.164615              0.160693
         gm           0.000196005           0.000199136
        gds           5.55792e-06           4.22852e-06
       gmbs           5.35504e-05           5.40463e-05
        cdb          -2.67679e-16          -2.61351e-16
        cgd           1.40214e-17           1.94042e-17
        cgs          -2.34111e-15          -2.31112e-15
        csb          -3.98209e-16          -3.91504e-16
```

DC OP simulation results



Annotated DC node voltages

- Put the OP of all transistors in a table with the appropriate units.

#	I_D	V_{GS}	V_{DS}	V_{th}	V_{Dsat}	g_m
0	$20uA$	$0.8V$	$0.9V$	$0.7V$	$0.16V$	$200uS$
1	$20uA$	$0.9V$	$0.44V$	$0.67V$	$0.16V$	$196uS$
2	$20uA$	$0.9V$	$0.47V$	$0.78V$	$0.16V$	$195uS$
3	$20uA$	$1.36V$	$0.46V$	$0.66V$	$0.55V$	$46uS$
4	$20uA$	$0.9V$	$0.46V$	$0.77V$	$0.16V$	$200uS$

#	g_{ds}	g_{mb}	C_{db}	C_{gd}	C_{gs}	C_{sb}
0	$4.2uS$	$54uS$	$2.6e-16F$	$2e-17F$	$2.3e-15F$	$4e-16F$
1	$5.6uS$	$54uS$	$2.7e-16F$	$1.4e-17F$	$2.4e-15F$	$4e-16F$
2	$5.7uS$	$41uS$	$2e-16F$	$2.9e-17F$	$2.4e-15F$	$3e-16F$
3	$12uS$	$18uS$	$8e-15F$	$4.2e-15F$	$4.5e-14F$	$1e-14F$
4	$4.6uS$	$40uS$	$2e-16F$	$2.5e-17F$	$2.4e-15F$	$3e-16F$

- Check that all transistors operate in saturation. Does any transistor operate in triode? Why?

#	V_{DS}	$V_{DS,sat}$	$OP\ Region$
0	0.9	0.16	Sat
1	0.45	0.16	Sat
2	0.46	0.16	Sat
3	0.46	0.55	$Triode$
4	0.9	0.16	Sat

  - M3 is operating in triode, since it has $V_{OV} = V_B - V_{th} = 1.36 - 0.66 = 0.7V$, which is higher than $V_{DS} = 0.44V$.
- Do all transistors have the same vth? Why?
  - The CS transistor and the i/p transistor of the cascode have the same V_{th} as the source-body voltage for both devices is zero and thus no body effect, while the cascode transistor has non-zero V_{SB} and therefore the threshold is slightly higher.
- What is the relation ($\ll$,<,≈,>,$\gg$) between gm and gds?

$g_m >> g_{ds}$

- What is the relation ($\ll$,<,≈,>,$\gg$) between gm and gmb?

$$g_m > g_{mb}$$

- What is the relation (≪,<,≈,>,≫) between cgs and cgd?

$$C_{gs} > C_{gd}$$

- What is the relation (≪,<,≈,>,≫) between csb and cdb?

$$C_{sb} > C_{db}$$

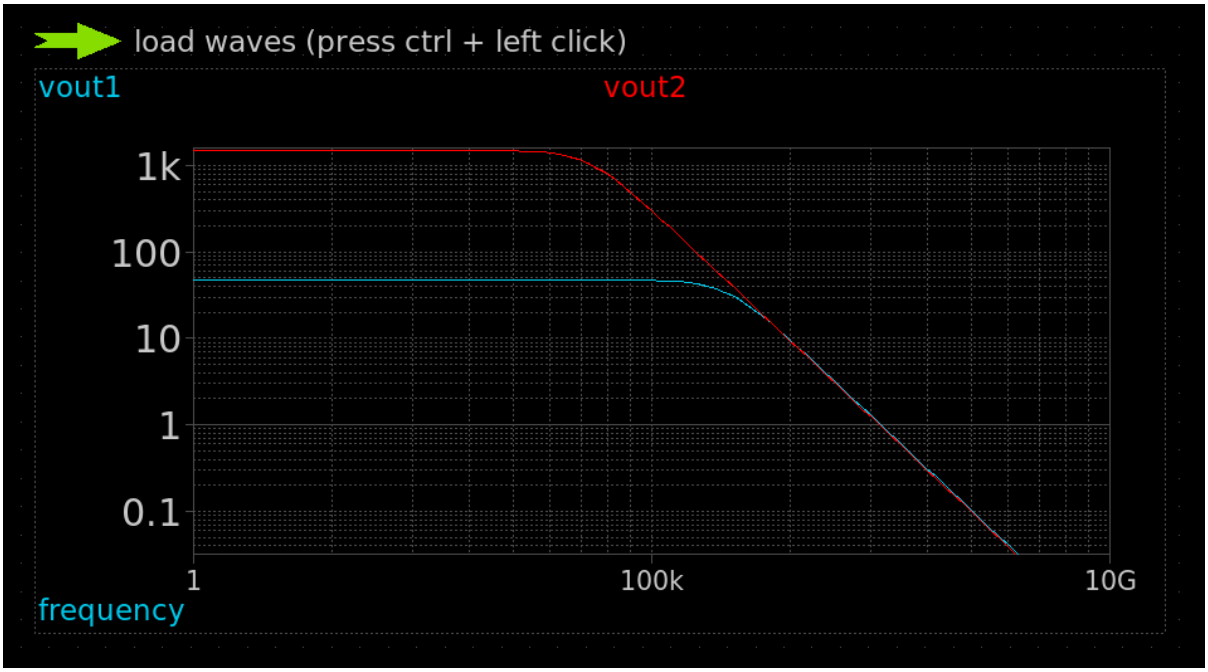
2. AC Analysis

- Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth. create expressions for circuit parameters (DC gain, BW, GBW, and UGF) and export them to interactive.

```
peak1               =  4.709049e+01 at=  1.000000e+00
f3db1               =  6.730899e+05
ugf1                =  3.159338e+07
gbw1 = 3.169613e+07
peak2               =  1.504826e+03 at=  1.000000e+00
f3db2               =  2.024958e+04
ugf2                =  3.064112e+07
gbw2 = 3.047209e+07
```

Required calculations

- Report the Bode plot (magnitude) of CS and cascode appended on the same plot.



Bode mag plot

- Using small signal parameters from OP simulation or SA, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.

$DC\ gain$
$CS\colon A_v = g_m r_o = 200u \times (4u)^{-1} = 50$
$Casc\colon A_v = g_{m,i/p} r_{o,casc} (g_{m,casc} + g_{mb,casc}) r_{o,i/p}$ $= 195u(5.6u)^{-1}(195u + 40u)(4.2u)^{-1} \approx 1950$

BW
$CS\colon BW = \frac{1}{2\pi R_o C_o} = \frac{4.2u}{2\pi(2.6e{-}16{+}1.9e{-}17(1{+}\frac{1}{47}){+}1p)} = 668k$
$Casc\colon BW = \frac{1}{2\pi R_o C_o} = \frac{1}{2\pi((5.6u)^{-1}(195u{+}40u)(4.2u)^{-1})(2e{-}16{+}2e{-}17{+}1p)}$ $\approx 19k$

GBW
CS: $GBW = 50 \times 668k = 33.4M$
$Casc$: $GBW = 1950 \times 19k = 37M$

- Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis.

CS		
$Parameter$	$Simulated$	$Calculated$
$DC\ gain$	47	50
BW	$670k$	$668k$
GBW	$31.5M$	$33.4M$

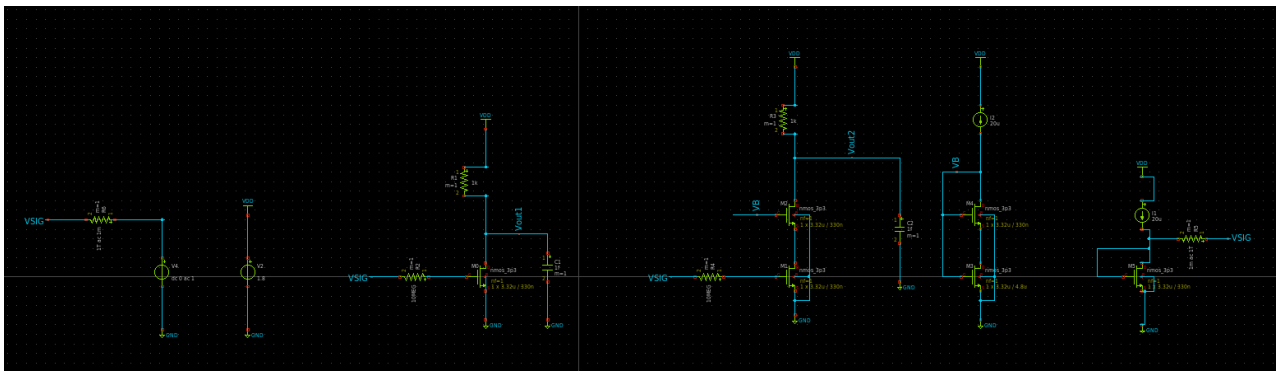
$Casc$		
$Parameter$	$Simulated$	$Calculated$
$DC\ gain$	$1.5k$	1950
BW	$20k$	$19k$
GBW	$30M$	$37M$

- Comment: It can be easily noticed that the cascode stage provides much larger gain than the CS stage, but has a lower bandwidth.

Part 3: Cascode for BW

1. OP Analysis

- Create a new schematic. Copy the old schematic instances to the new one. Make the following modifications: xxx



Required circuit

- Calculate R_D analytically such that the voltage drop on it is $\approx V_{DD}/2$ (the current remains roughly the same as in Part 2 because we are using the VGS generated by M5). Note that the DC voltage of the output node is set by the resistance (R_D); thus, we don't need a feedback loop as in the previous case.

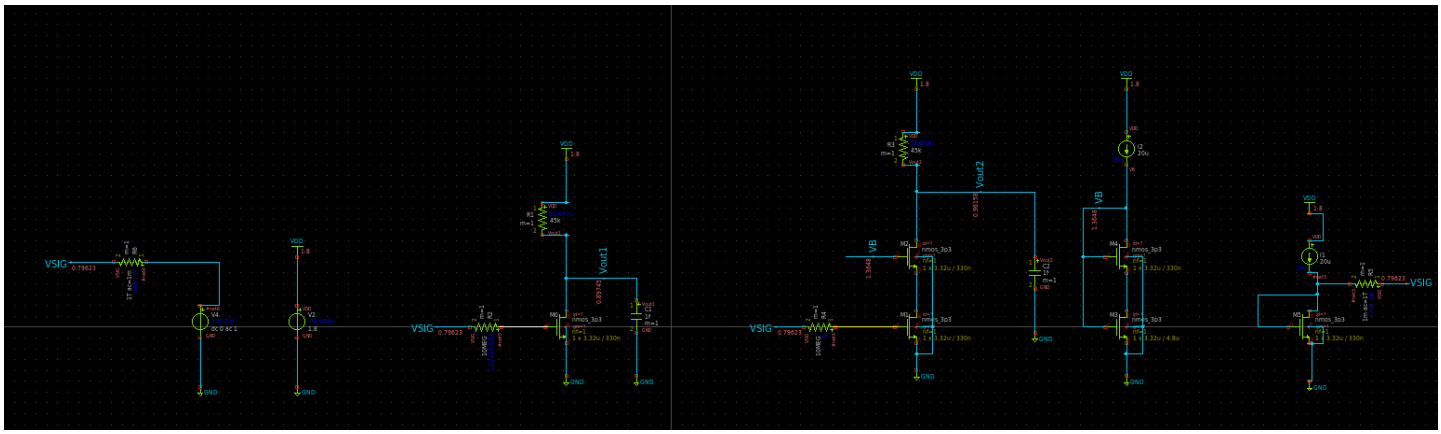
$$R_D = \frac{V_{DD}/2}{I_D} = \frac{0.9}{20u} = 45k\Omega.$$

- Simulate the DC OP point of the new CS and cascode amplifiers. Report a snapshot showing the following parameters for M0 to M5 in addition to DC node voltages clearly annotated.

```
BSIM4v5: Berkeley Short Channel IGFET Model-4
    device              m.xm3.m0              m.xm5.m0              m.xm4.m0
     model          nmos_3p3.10           nmos_3p3.8            nmos_3p3.8
        id                2e-05                 2e-05                 2e-05
       vgs              1.36484              0.796226              0.910802
       vds             0.454022              0.796219              0.910794
       vth             0.654459              0.668728              0.781517
     vdsat             0.550918              0.161512              0.164557
        gm          4.50895e-05          0.000198656          0.000198257
       gds           1.3775e-05           4.3479e-06           4.53717e-06
      gmbs           1.75277e-05          5.39979e-05          4.10728e-05
       cdb          -8.29324e-15         -2.62373e-16         -1.99924e-16
       cgd           -4.8947e-15          1.91849e-17          2.52409e-17
       cgs          -4.48635e-14         -2.31708e-15         -2.36946e-15
       csb          -1.08404e-14         -3.92855e-16         -2.99493e-16

BSIM4v5: Berkeley Short Channel IGFET Model-4
    device              m.xm2.m0              m.xm1.m0              m.xm0.m0
     model           nmos_3p3.8            nmos_3p3.8            nmos_3p3.8
        id          1.86315e-05           1.86315e-05           2.00566e-05
       vgs             0.914593              0.796227              0.796226
       vds              0.51132              0.450233               0.89744
       vth              0.78776              0.671309              0.669481
     vdsat             0.162861              0.159772              0.161026
        gm           0.00018822          0.000188475          0.000199326
       gds          5.15076e-06           5.19531e-06           4.23567e-06
      gmbs          3.93478e-05           5.14664e-05           5.4105e-05
       cdb          -2.02467e-16          -2.64884e-16          -2.61519e-16
       cgd           2.20772e-17           1.44378e-17           1.94153e-17
       cgs          -2.36636e-15           -2.3139e-15          -2.31281e-15
       csb          -3.02023e-16          -3.94284e-16          -3.91752e-16
```

Required parameters



DC node voltages annotated

- Check that all transistors operate in saturation. Does any transistor operate in triode? Why?

#	V_{DS}	$V_{DS,sat}$	$OP\ Region$
0	0.9	0.16	Sat
1	0.45	0.16	Sat
2	0.5	0.16	Sat
3	0.45	0.55	$Triode$
4	0.9	0.16	Sat
5	0.8	0.16	Sat

- M3 is operating in triode, since it has $V_{OV} = V_B - V_{th} = 1.36 - 0.66 = 0.7V$, which is higher than $V_{DS} = 0.45V$.

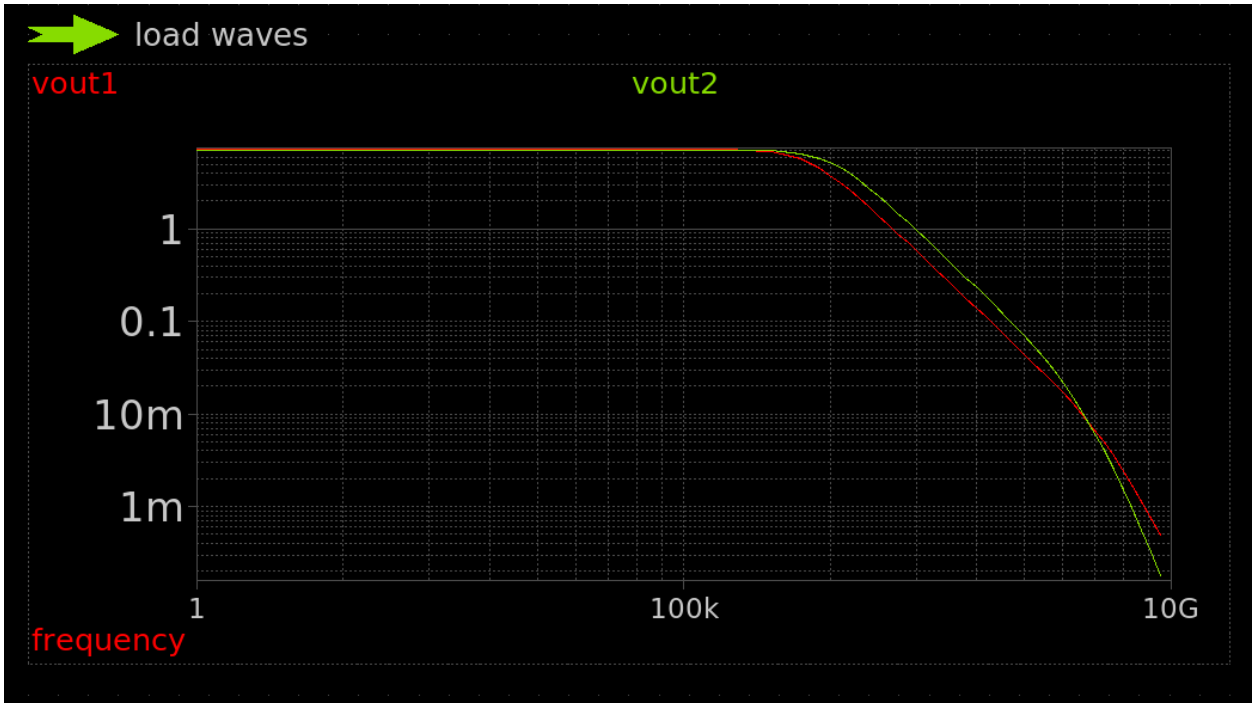
2. AC Analysis

- Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth. Use calculator to create expressions for circuit parameters (DC gain, BW, GBW, and UGF) and export them.

```
No. of Data Rows : 101
peak1                =  7.639994e+00 at=  1.000000e+00
f3db1                =  1.833668e+06
ugf1                 =  1.402092e+07
gbw1 = 1.400921e+07
peak2                =  8.892122e+00 at=  1.000000e+00
f3db2                =  3.210282e+06
ugf2                 =  2.866316e+07
gbw2 = 2.854622e+07
```

Required calculations

- Report the Bode plot (magnitude) of CS and cascode appended on the same plot.



Bode mag plot

- Using small signal parameters from OP simulation or SA, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.

$DC\ gain$
$CS\colon A_v \approx g_m R_D = 190u \times 45k = 8.6$
$Casc\colon A_v \approx g_{m,i/p} R_D = 190u \times 45k \approx 8.6$

BW
$CS\colon BW = \frac{1}{2\pi R_i C_i} = \frac{1}{2\pi(10M)(2.8e{-}15{+}540e{-}18(1{+}8.6){+}607e{-}18)} = 1.97M$ $Values\ from\ ADT\ *$

$Casc:\ BW = \frac{1}{2\pi R_o C_o} = \frac{1}{2\pi(10M)(3f+640a(1+1)+640a)} \approx 3.5M$ $Values\ from\ ADT\ *$

GBW
$CS:\ GBW = 8.6 \times 1.97M = 17M$
$Casc:\ GBW = 8.6 \times 3.5M = 30.1M$

- Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis. Comment on the results.

CS		
$Parameter$	$Simulated$	$Calculated$
$DC\ gain$	7.6	8.6
BW	$1.8M$	$1.97M$
GBW	$14M$	$17M$

$Casc$		
$Parameter$	$Simulated$	$Calculated$
$DC\ gain$	8.9	8.6
BW	$3.2M$	$3.5M$
GBW	$29M$	$30.1M$

- Comment: It can be noticed that the cascode stage provides almost the same gain as the CS stage due to the

severe reduction of o/p impedance, but has more bandwidth (around 2 times the BW of CS).