CMOS AIC design - ITI - Lab 2

Part 1: Sizing Charts

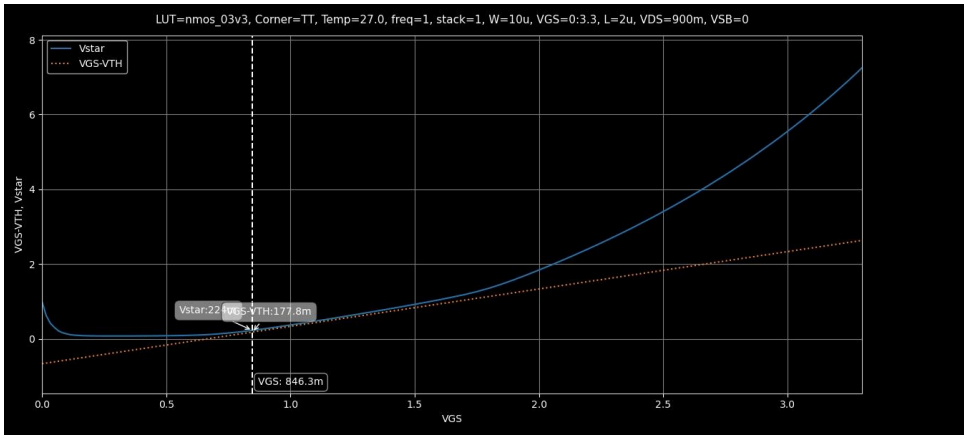
- Assuming CM output = $V_{R_D} = V_{DD}/2$ and given the DC bias current, determine the value of R_D.

$$R_D = \frac{V_{R_D}}{I_D} = \frac{0.9}{100u} = 9k\Omega.$$

- Given A_v and V_{R_D}, calculate the required V^* (again note that $V^* \neq V_{OV}$ for a real MOSFET). Let's name this value V_Q^*.

$$V_Q^* = \frac{2V_{R_D}}{|A_v|} = \frac{1.8}{8} = 225mV.$$

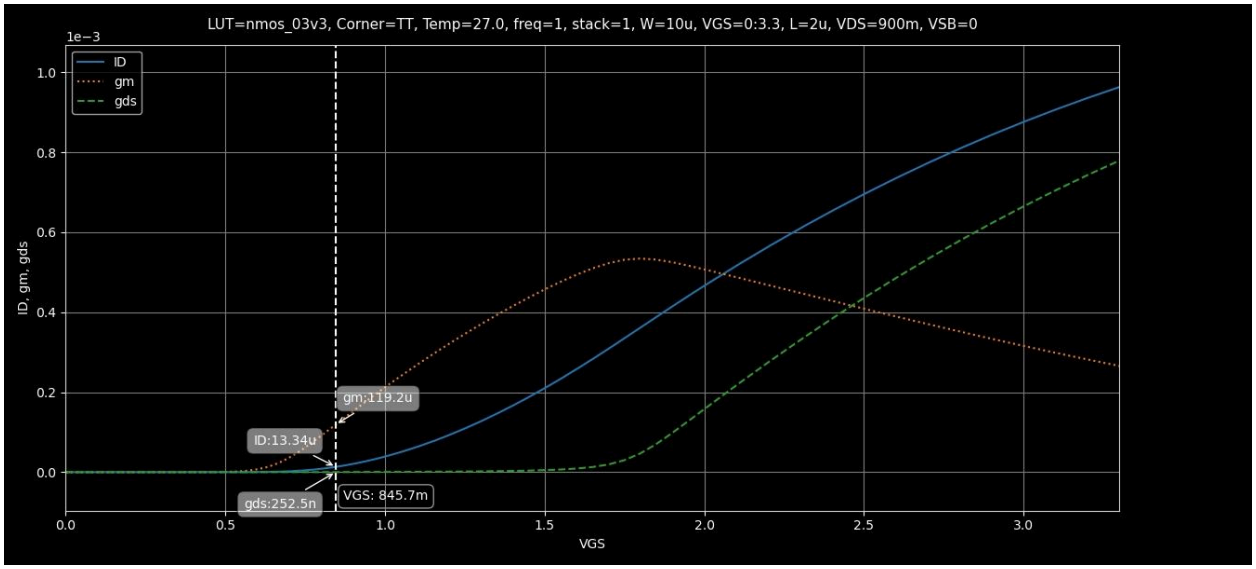
- On the V^* and V_{OV} chart locate the point at which $V^* = V_Q^*$. Find the corresponding V_{OVQ} and V_{GSQ}.



V and Vov VS VGS*

$$V_{OVQ} \approx 180mV, V_{GSQ} \approx 845mV$$

- Plot I_D, g_m, and g_{ds} vs V_{GS}. Find their values at V_{GSQ}. Let's name these values I_{DX}, g_{mX}, and g_{dsX}.



ID, gm, gds VS VGS

$$I_{DX} \approx 13uA,\ g_{mX} \approx 120uS,\ g_{dsX} \approx 250nS.$$

- Now back to the assumption that we made that $W = 10\mu m$. This is not the actual value that we will use for our design. But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be $I_{DQ} = 100\mu A$ as given in the specs. Calculate W.

$10um$	W_{actual}
$13uA$	$100uA$

$$W_{actual} = 77um.$$

- Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as V_{OV} is constant. On the other hand, $r_o = 1/g_{ds}$ is inversely proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross- multiplication) and double check that $A_v = -g_m(R_D||r_o)$ meet the required gain spec.

$10um$	$77um$
$120uS$	g_{mQ}

$$g_{mQ} = 925uS.$$

$13uA$	$100uA$
$250nS$	g_{dsQ}

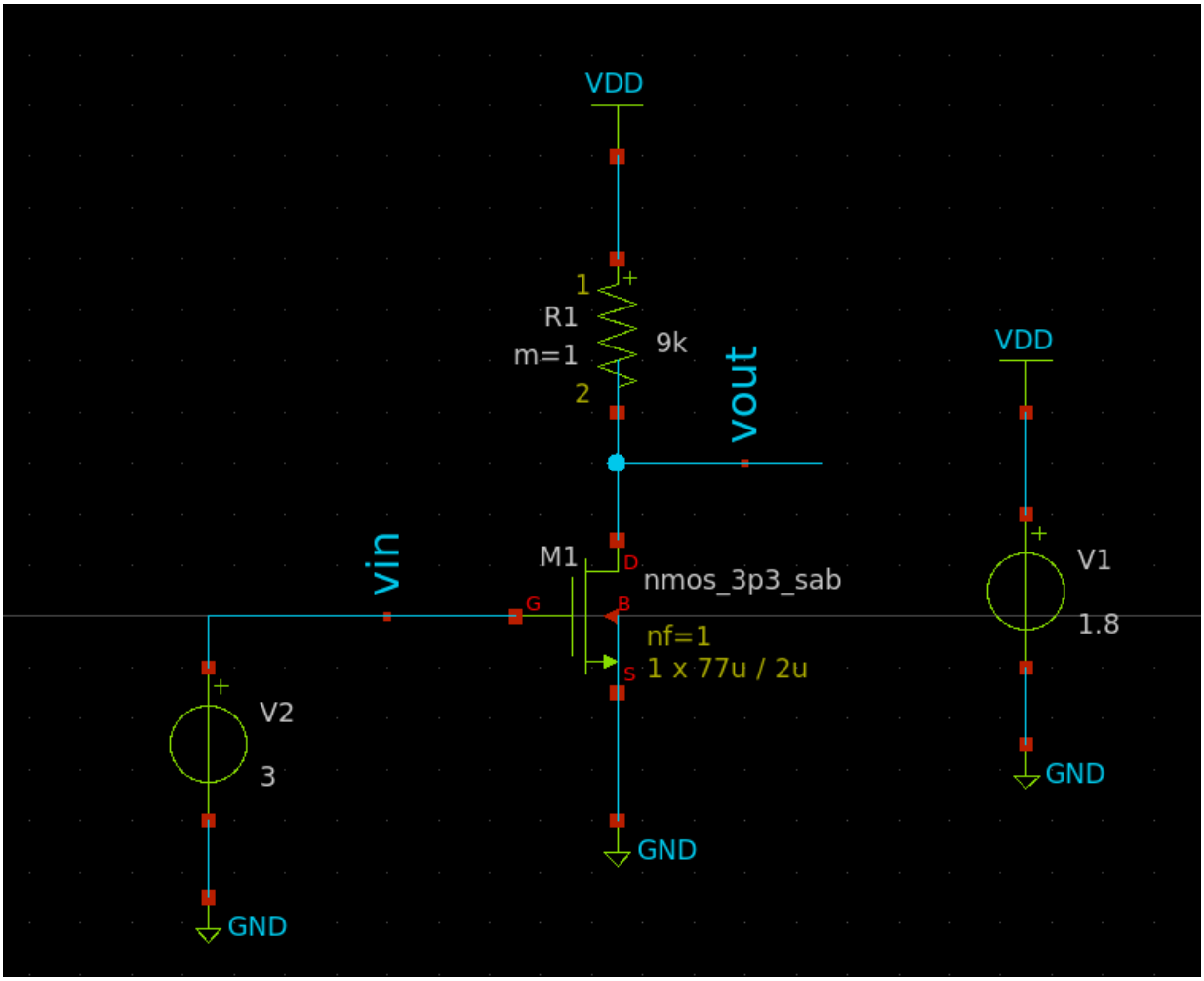
$$g_{dsQ} = 2uS.$$

$$A_v = 925u(9k \,||\, (2u)^{-1} = 8.2 \approx 8.$$

Part 2: CS Amplifier

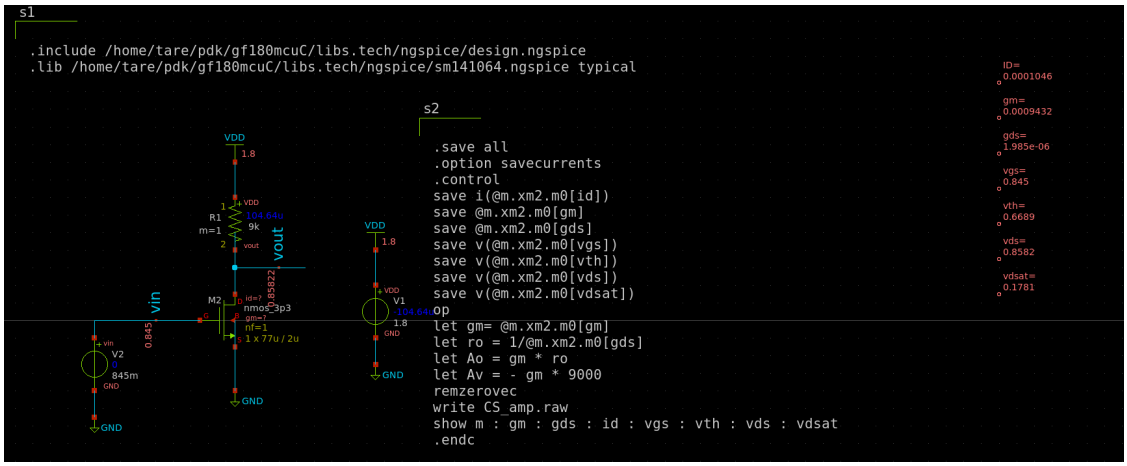
1. OP and AC Analysis

- Create a testbench for the resistive loaded CS amplifier using the V_{GSQ}, R_D, L, and W that you got from the previous part.



Required testbench

- Simulate the DC OP. Report a snapshot for the key operating point (OP) parameters. Compare the results with the results you obtained in Part1.



Required snapshot

  - As can be seen from the snapshot, the results from the simulation are very similar to those obtained in the previous part.
- Compare r_o and R_D. Is the assumption of ignoring r_o justified in this case? Do you expect the error to remain the same if we use min L?

r_o	R_D
$(g_{ds})^{-1} = (2u)^{-1} = 500k\Omega$	$9k\Omega$

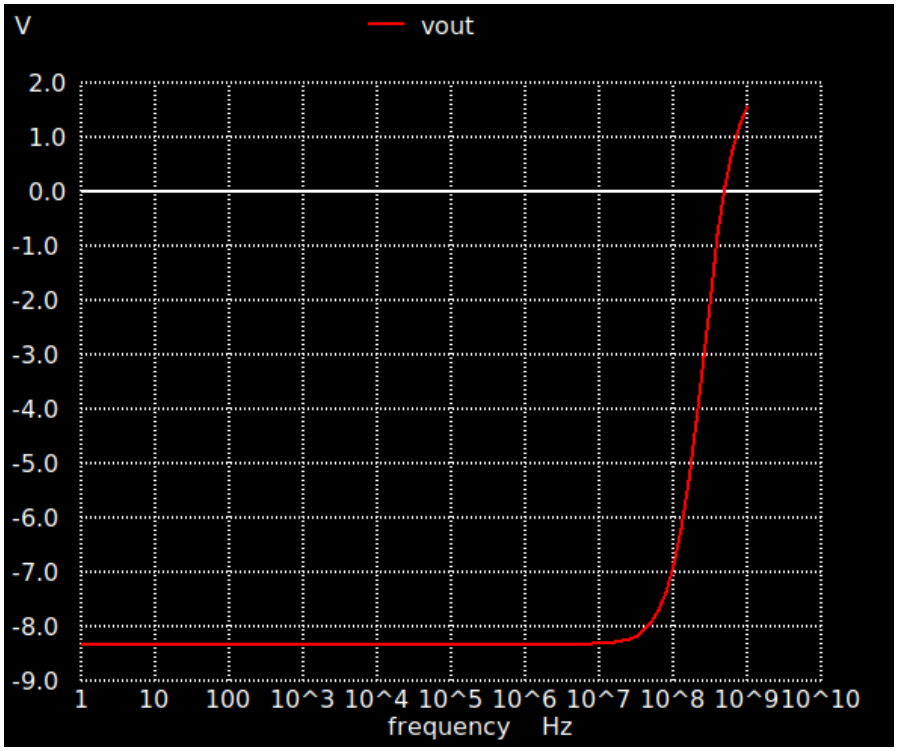
  - $r_o >> R_D$
  - Since the parallel combination is very close to R_D, ignoring r_o is justified.
  - $L_{min} \rightarrow \lambda_{max} \rightarrow V_{A,min} \rightarrow r_{o,min}$, so the error would be higher.
- Calculate the intrinsic gain of the transistor.

$$A_o = g_m r_o = 925u \times 500k \approx 460.$$

- Calculate the amplifier gain analytically. What is the relation ($\ll$,<,≈,>,$\gg$) between the amplifier gain and the intrinsic gain?

$$A_v = g_m(R_D||r_o) = 925u(9k||500k) \approx 8.2.$$

  - $A_o >> A_v$.
- Create a new simulation configuration and run AC analysis (from 1Hz to 1GHz). Report the gain vs frequency. Annotate the DC gain and make sure it meets the spec.

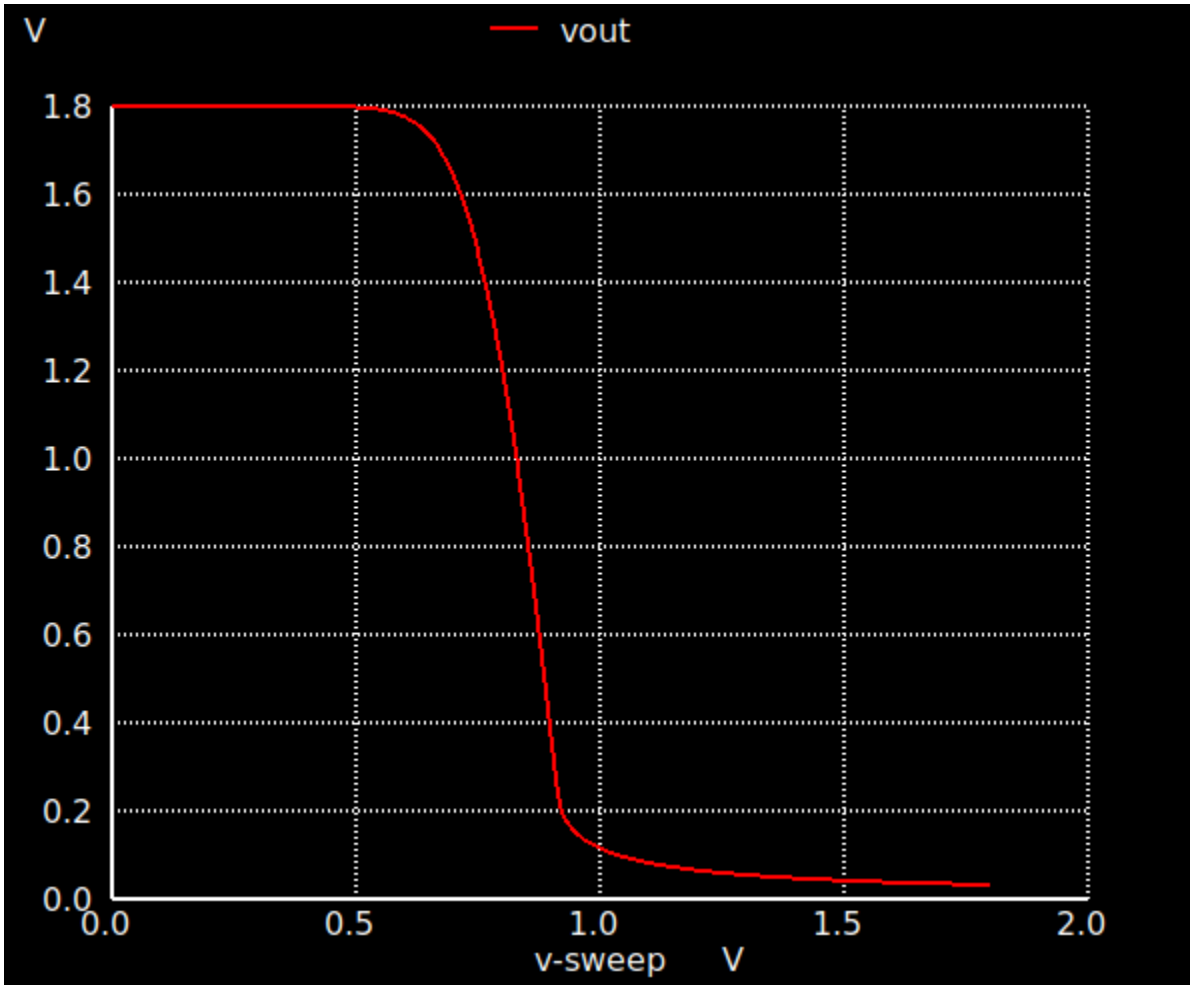


vout VS frequency

  - As seen in the plot, DC gain ≈ -8 as required in specs.

2. Gain Non-linearity

- Create a new simulation configuration. Perform a DC sweep for the input voltage from 0 to V_{DD} with 2mV step. Report VOUT vs VIN. Is the relation linear? Why?

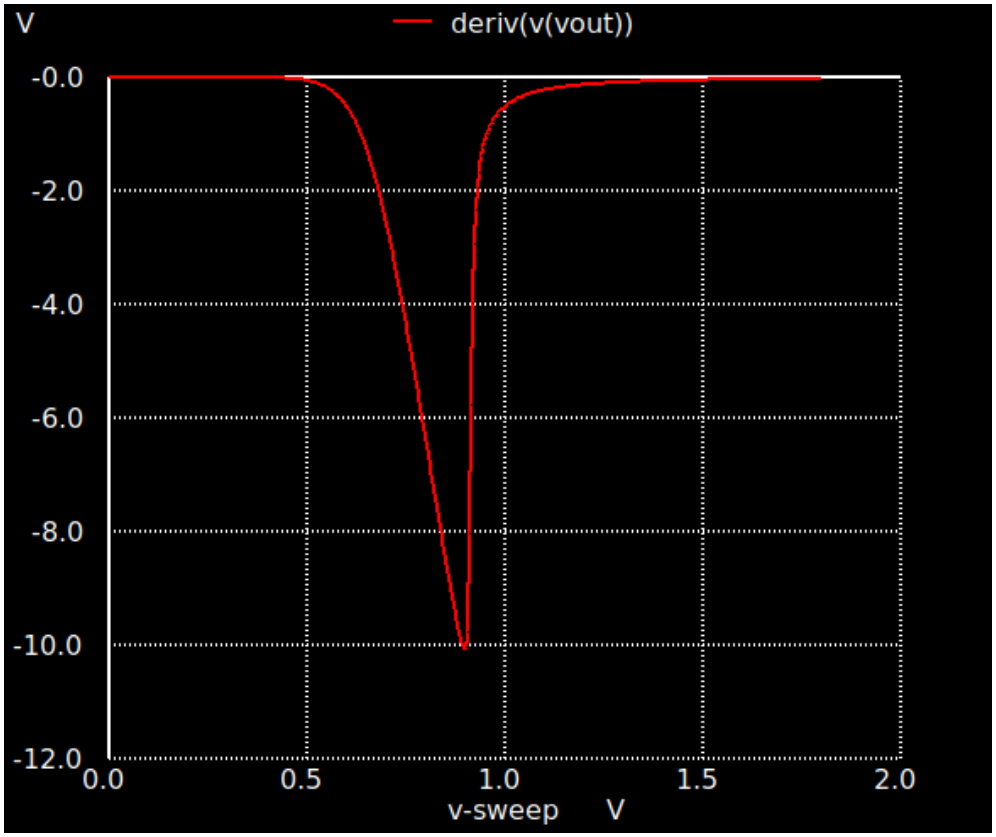


VOUT VS VIN plot

- No, the relation is not linear. At the beginning of the plot, V_{out} is constant due to the absence of drain current and thus no V_{DS} variation. This holds until V_{in} exceeds V_{th}, wherein the drain current begins to flow, inducing a voltage drop across R_D and therefore V_{DS} begins to fall in an almost linear fashion with a steep slope, then the slope begins to

be less steeper since the operating point has moved to triode region, which is characterized by small g_m's and r_o's (note that the slope of the curve is the gain of the circuit, which is a function of transconductance and o/p resistance).

- Calculate the derivative of VOUT using calculator. Plot the derivative vs VIN. The derivative is itself the small signal gain. Is the gain linear (independent of the input)? Why?

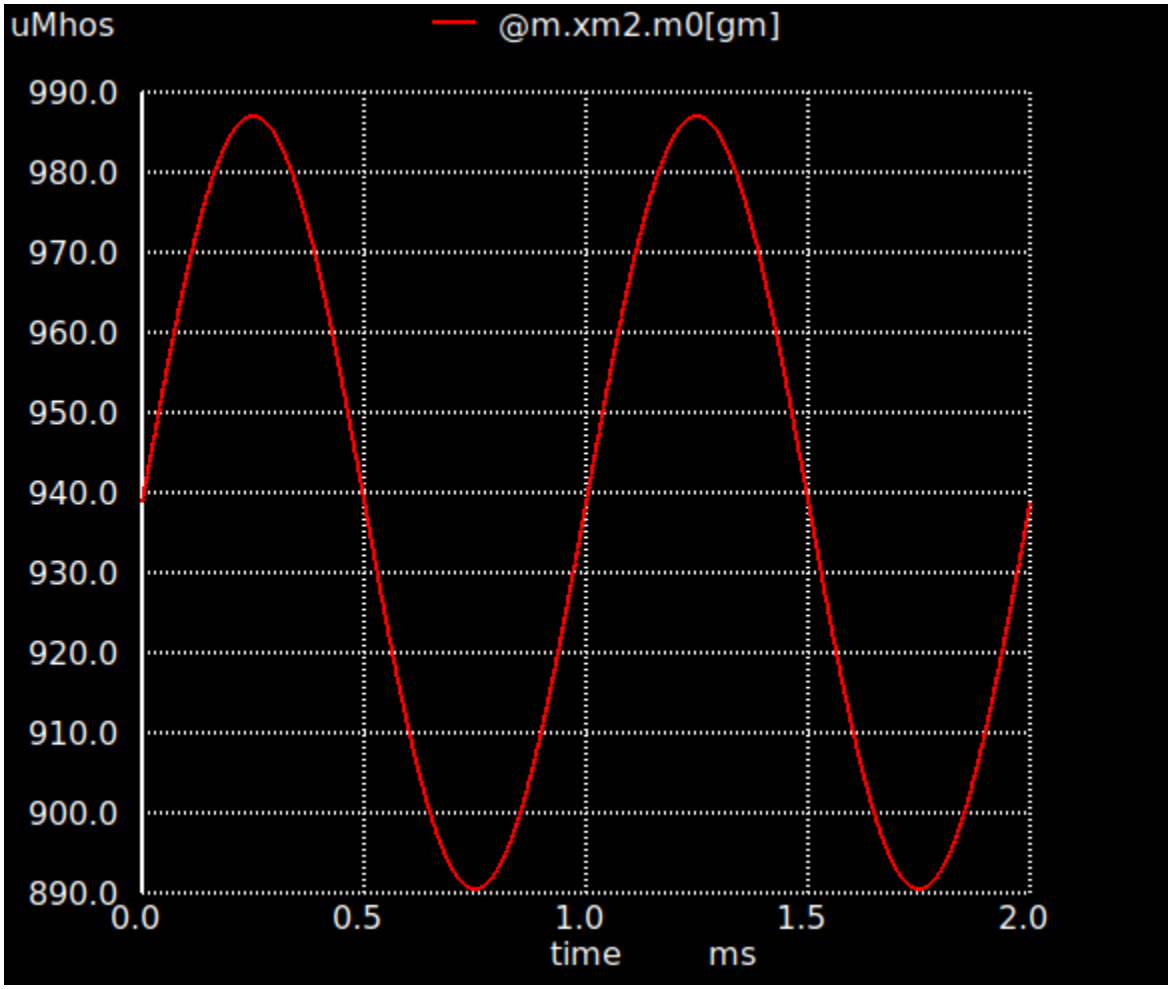


deriv(vout) VS vin

  - No, the gain depends on the i/p voltage. The gain of any CMOS amplifier is a function of G_m and R_o, which in turn are functions of the i/p voltage.

- Set the properties of the voltage source to apply a transient stimulus (sine wave of 1kHz frequency and 10mV amplitude superimposed on the DC input voltage). Create a new simulation

configuration. Run transient simulation for 2ms. Plot gm vs time. Does gm vary with the input signal? What does that mean?



gm VS time

- Yes, g_m varies with the i/p signal. This means that g_m is a function of gate-source voltage, which is emphasized by the formulae of g_m derived from the square law.

- Is this amplifier linear? Comment.
  - This amplifier is *not* linear. A linear amplifier is a system that has linear transfer characteristics (i.e. a linear relation between i/p and o/p), which is not satisfied in our case, as can be easily noticed from *VOUT VS VIN plot.*