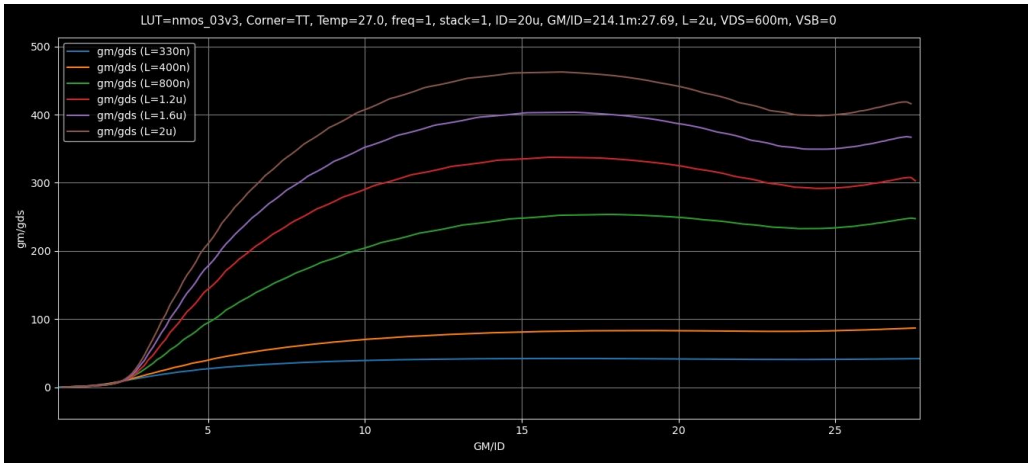
CMOS AIC design - ITI - Lab 7

Part 1: gm/ID Design Charts

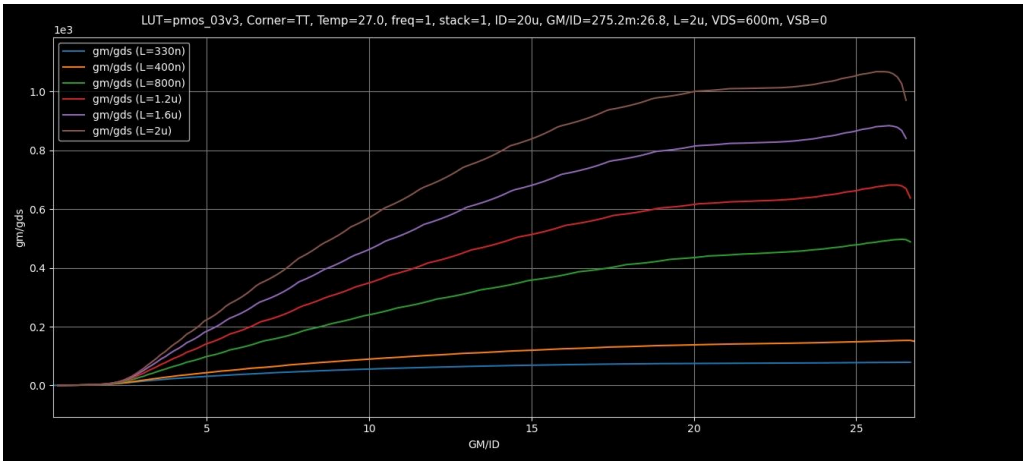
Subscript index: $i \rightarrow i/p\ pair,\ l \rightarrow load,\ tcs \rightarrow tail\ current\ source$**.**

- Using ADT Device Xplore, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS = VDD/3 and L = 0.33u,0.4u:0.4u:2u
  - Let $I_D = 20uA$.

  ➔ gm/gds

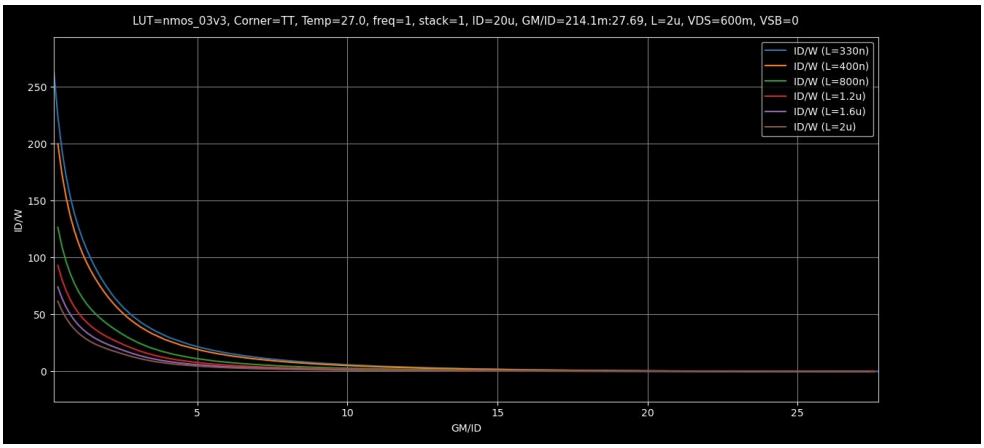


gm / gds vs gm / ID @ID = 20uA, VSB = 0 for ***NMOS***

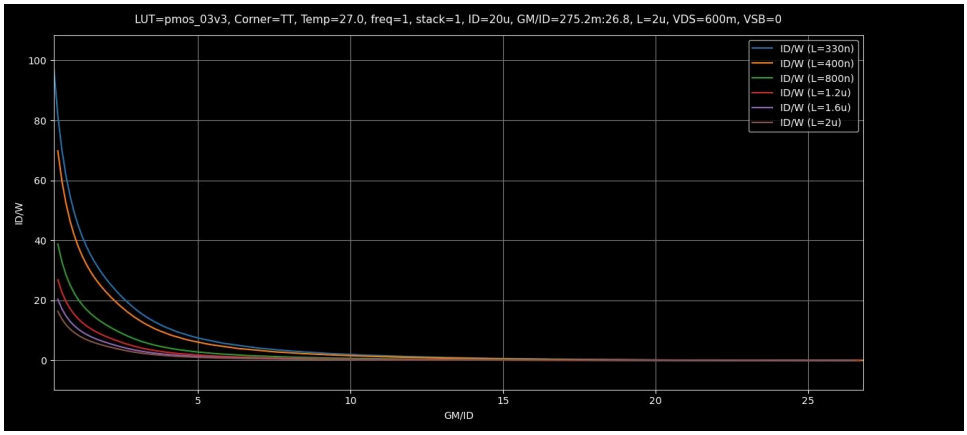


gm / gds vs gm / ID @ ID = 20uA, VSB = 0 for ***PMOS***

➔ ID/W

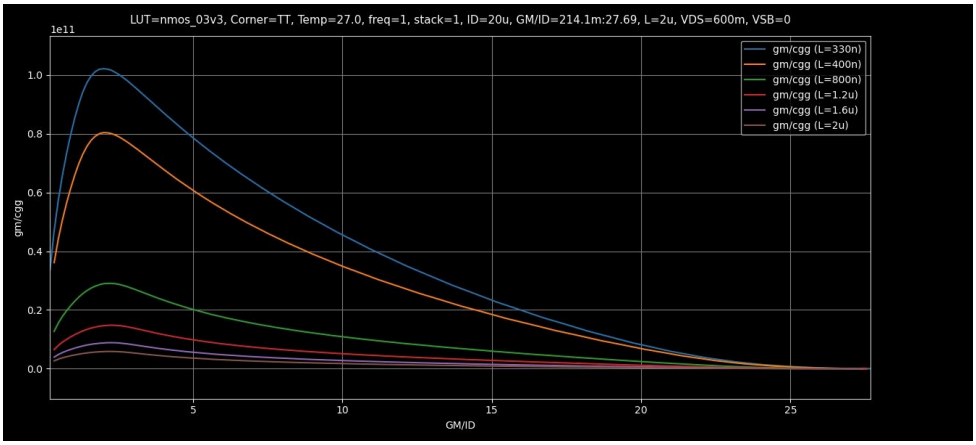


*ID / W vs gm / ID @ID = 20uA, VSB = 0 for **NMOS***

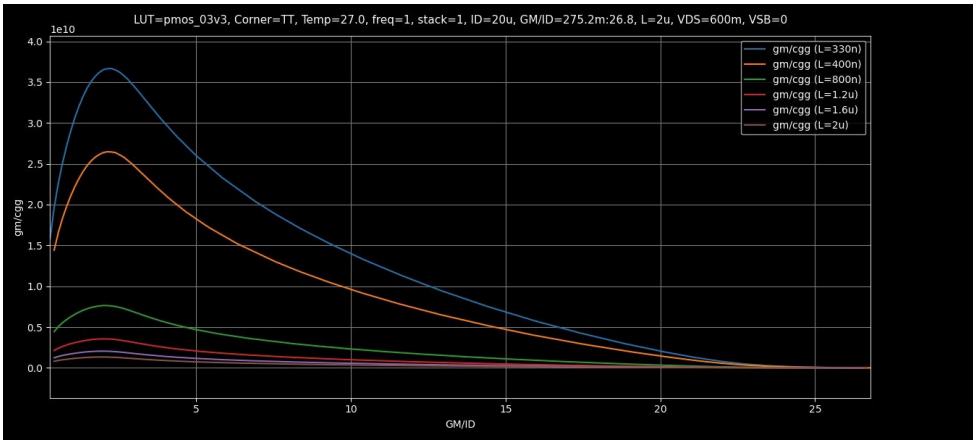


*ID / W vs gm / ID @ID = 20uA, VSB = 0 for **PMOS***

➔ gm/cgg

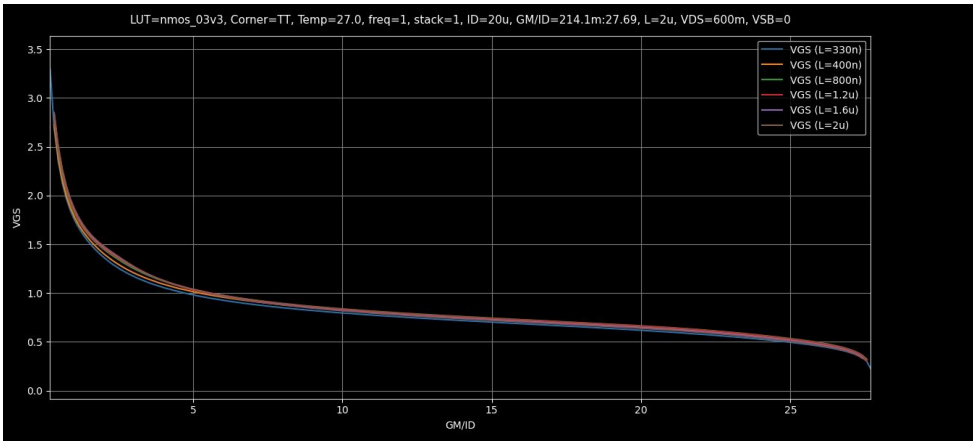


*gm / Cgg vs gm / ID @ID = 20uA, VSB = 0 for **NMOS***

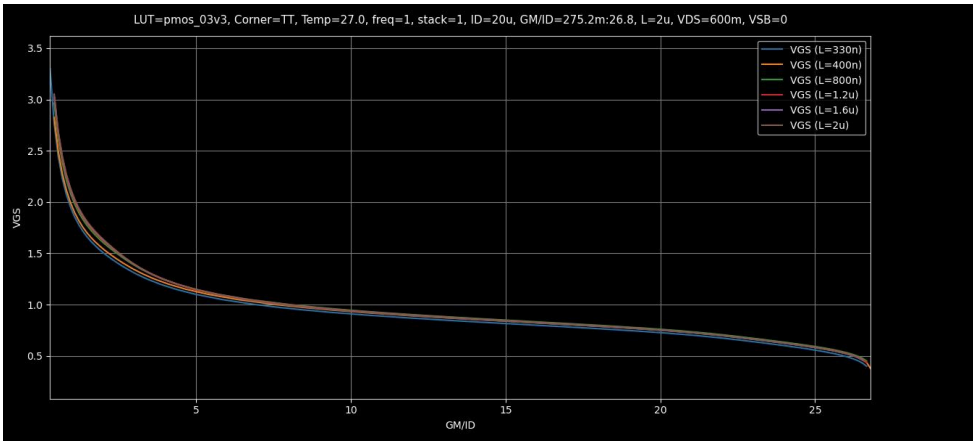


*gm / Cgg vs gm / ID @ID = 20uA, VSB = 0 for **PMOS***

➔ VGS



*VGS vs gm / ID @ID = 20uA, VSB = 0 for **NMOS***



*VGS vs gm / ID @ID = 20uA, VSB = 0 for **PMOS***

Part 2: OTA Design

- Use gm/ID methodology to design a diff input SE output operational transconductance amplifier (OTA) that achieves the following specs. Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec), but design your own current mirror.

1. Design of i/p pair

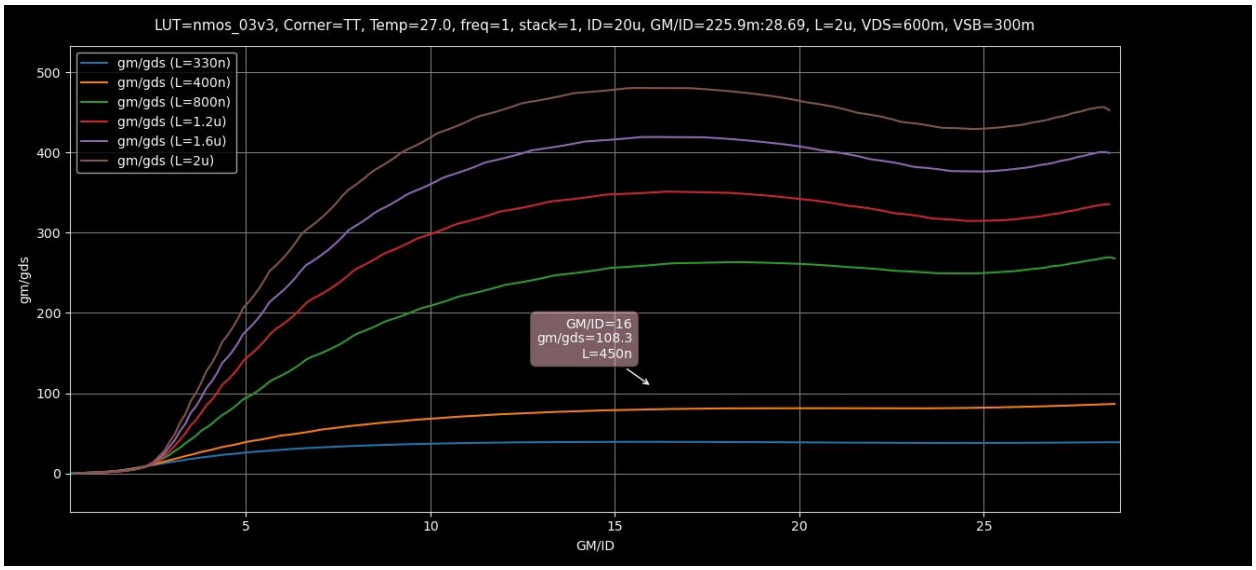
- From $CMIR$ spec, it can be noticed that its limits are closer to V_{DD}, thus an *NMOS* i/p pair is employed.
- From GBW spec: $GBW = \frac{g_{m,i}}{2\pi C_L} \Rightarrow g_{m,i} = 2\pi C_L \times GBW$.

$$g_{m,i} \approx 314uS.$$

- In part 1, it was assumed that $I_D = 20uA$. this value will be used in determining $\frac{g_m}{I_D}(i)$.

$$\frac{g_m}{I_D}(i) \approx 16S/A.$$

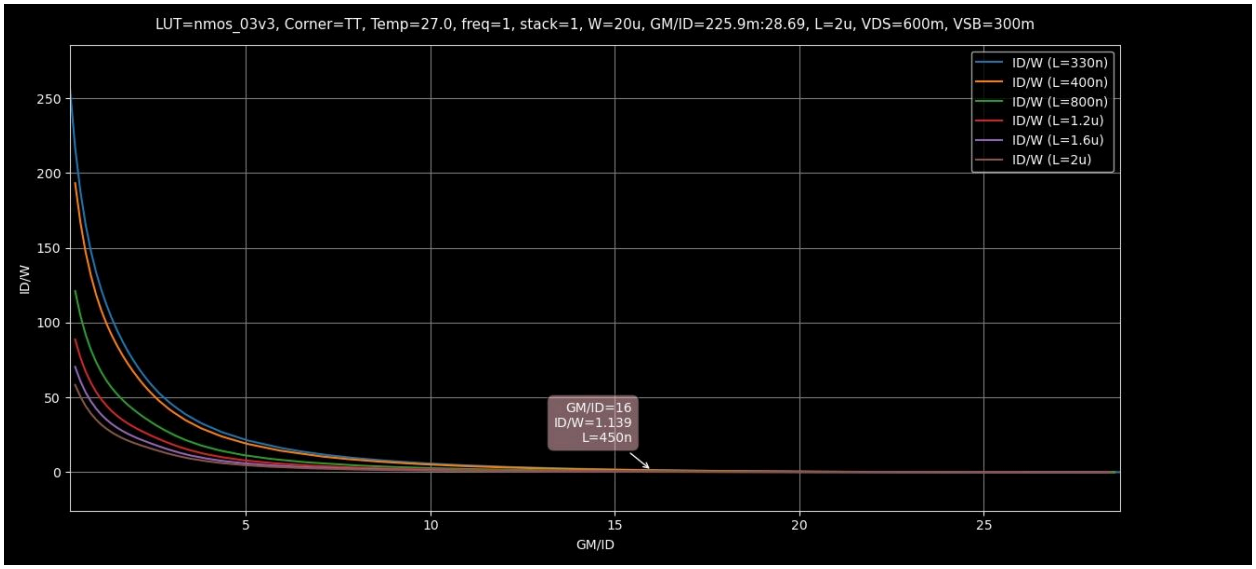
- $A_v = g_{m,i}(r_{o,i}||r_{o,l})$. for simplicity, let $r_{o,i} = r_{o,l} = r_{o,il}$, thus $A_v = \frac{g_{m,i} r_{o,il}}{2} > 43dB = 50 \Rightarrow \frac{g_{m,i}}{g_{ds,il}} > 100$.
- Note that in the plots shown in part 1, body effect was not taken into consideration, so new plots, that takes the body effect into account, will be used, assuming that $V_{SB} = 0.3V$.



gm / gds for i/p pair

$$L_i = 450nm.$$

- W can be selected from the current driving capability plot.



ID / W ≈ 1.14

$$W_i = 20u / 1.14 = 17.5um.$$

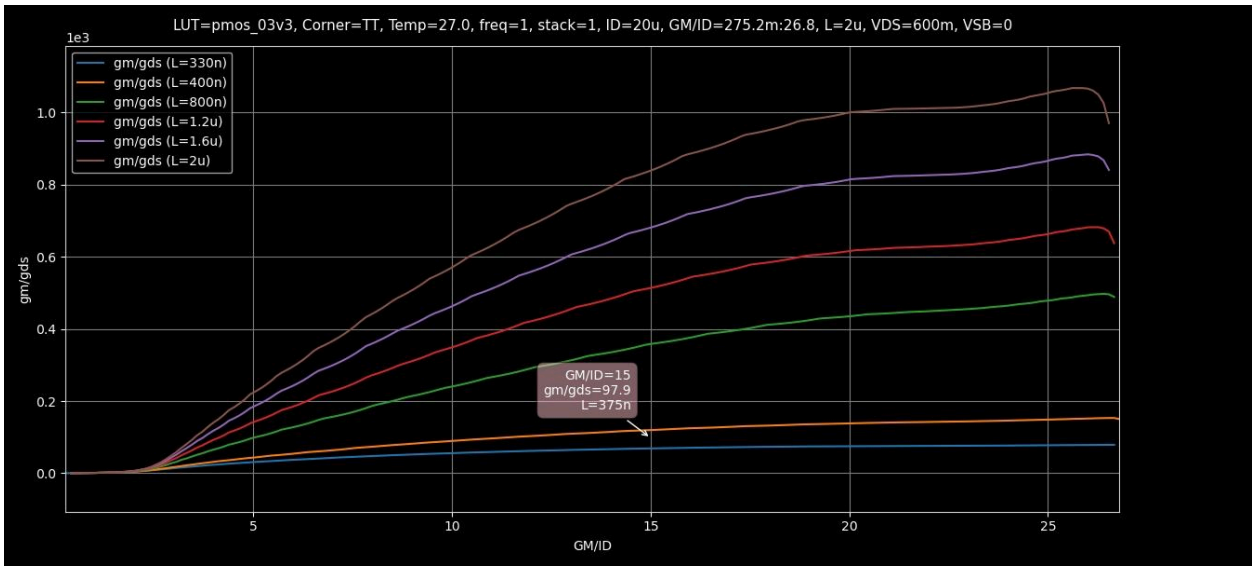
2. Design of Load Transistors

- Let $\frac{g_m}{I_D}(l) = 15$, and given that $I_D = 20uA$, thus

$$g_{m,l} = 300uS.$$

- In the process of designing the i/p pair, it was assumed that $r_{o,i} = r_{o,l} = r_{o,il}$, also a constraint was obtained: $\frac{g_{m,i}}{g_{ds,il}} > 100$, given that $g_{m,i} \approx 314uS$, thus

$$g_{ds,il} < 3.14uS, \quad \frac{g_{m,l}}{g_{ds,il}} = \frac{300}{3.14} > 95.5.$$



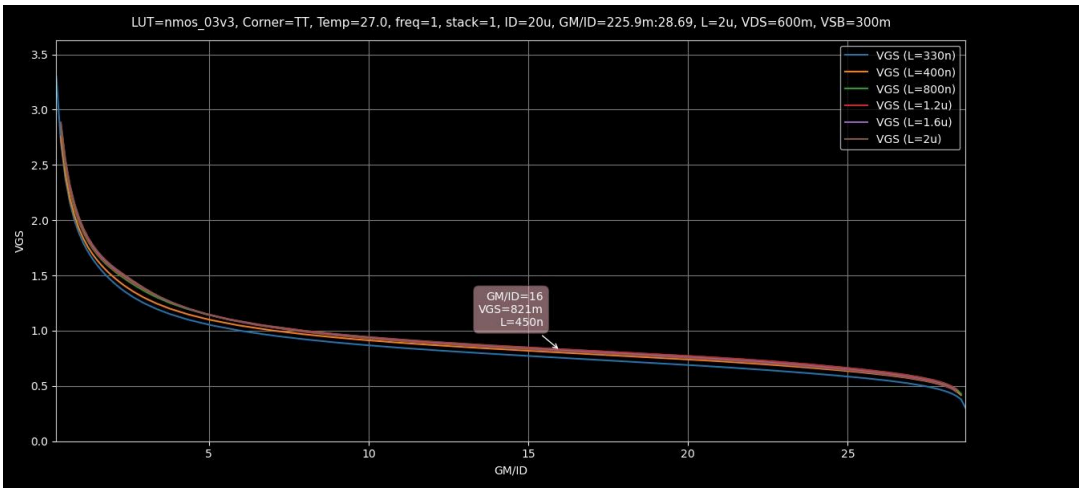
gm / gds for load transistors

$$L_l = 375nm.$$

- From $CMIR_{HIGH}$ spec, applying KVL:

$$CMIR_{HIGH} = V_{DD} + V_{GS,i} - V_{DS,i} - |V_{GS,l}|.$$

- $CMIR_{HIGH,min} = 1.5V,\ V_{DD} = 1.8V.$
- $V_{GS,i}$ can be obtained from VGS vs gm / ID plot.

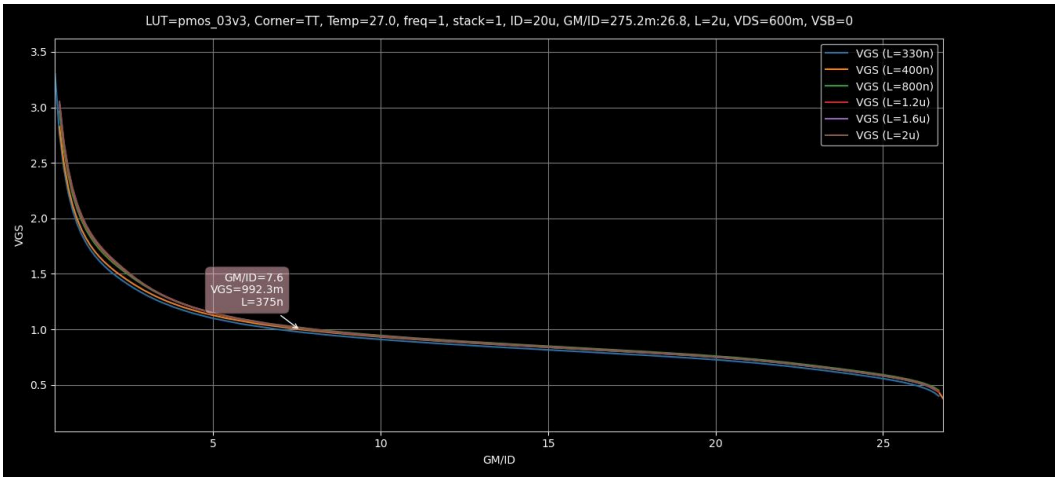


VGS,i = 0.82V

- Roughly talking, $V_{DS,i} = V_i^* = \frac{2}{g_m/I_D(i)} = 0.125V.$

$$|V_{GS,l,max}| = 0.995V.$$

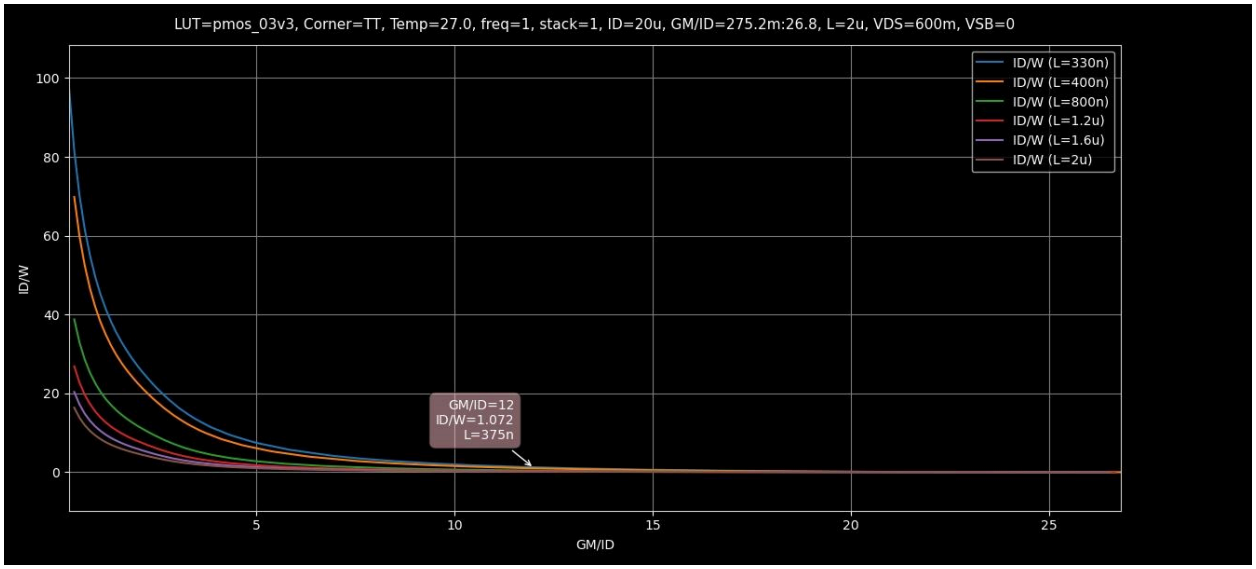
- From VGS vs gm/ID plot, a minima of $\frac{g_m}{I_D}(l)$ can be obtained.



VGS vs gm / ID for load transistors

$$\frac{g_m}{I_D}(l,\ min)\ =\ 6.7S/A.$$

- Let $\frac{g_m}{I_D}(l)\ =\ 12S/A.$
- W can be obtained from current driving capability plot.



ID / W ≈ 1

$$W_l\ =\ 20u\ /\ 1\ \approx\ 20um.$$

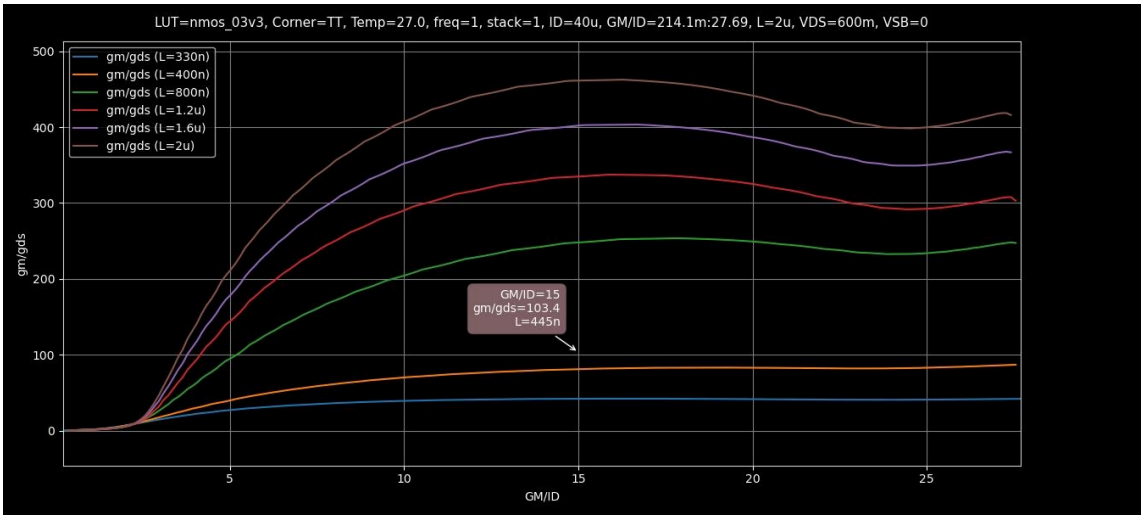
3. Design of Tail Current Source

- From $CMRR$ spec:
  $CMRR\ =\ A_{vd,dB}\ -\ A_{vCM,dB}\ \Leftrightarrow\ 34\ -\ A_{vCM,dB}\ =\ 74\ \Rightarrow\ A_{vCM,dB}\ =-\ 40dB.$
- $A_{vCM}\ =\ \frac{1}{2g_{m,l}r_{o,tcs}}\ =\ 0.01, g_{m,l}\ =\ 300uS$, thus

$$g_{ds,tcs}\ <\ 6uS.$$

- Let $\frac{g_m}{I_D}(tcs)\ =\ 15\ \Rightarrow\ g_{m,tcs}\ =\ 600uS$, thus

$$\frac{g_m}{g_{ds}}(tcs) > 100.$$

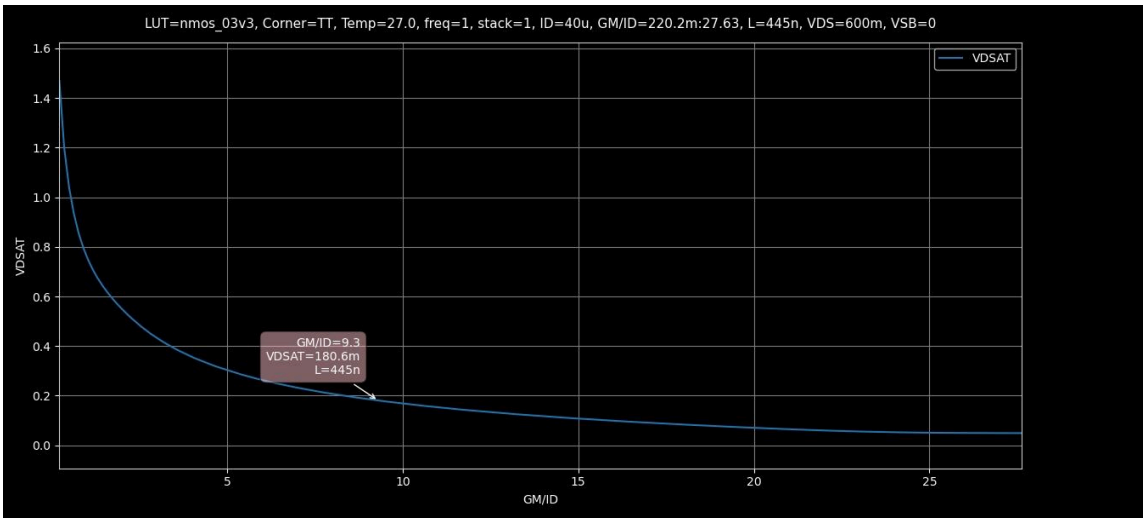


L is chosen to be 445nm

- From $CMIR_{LOW}$ spec, applying KVL: $CMIR_{LOW} = V_{GS,i} + V_{Dsat,tcs}$.
  - $CMIR_{LOW} = V$, $V_{GS,i} = 0.82V$, thus

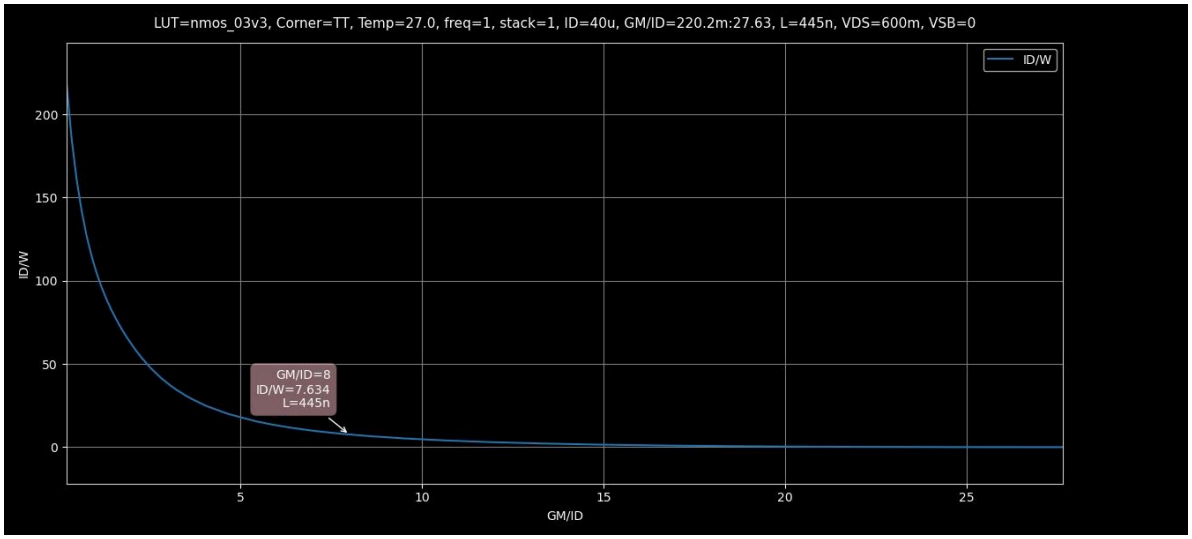
$$V_{Dsat,tcs,max} = 0.18V.$$

- From Vdsat vs gm / ID plot..



gm / ID (max) = 9.3 S/A

- To take some margin, let $\frac{g_m}{I_D}(tcs) = 8.$
- W can be obtained from the current driving capability plot



ID / W = 7.6

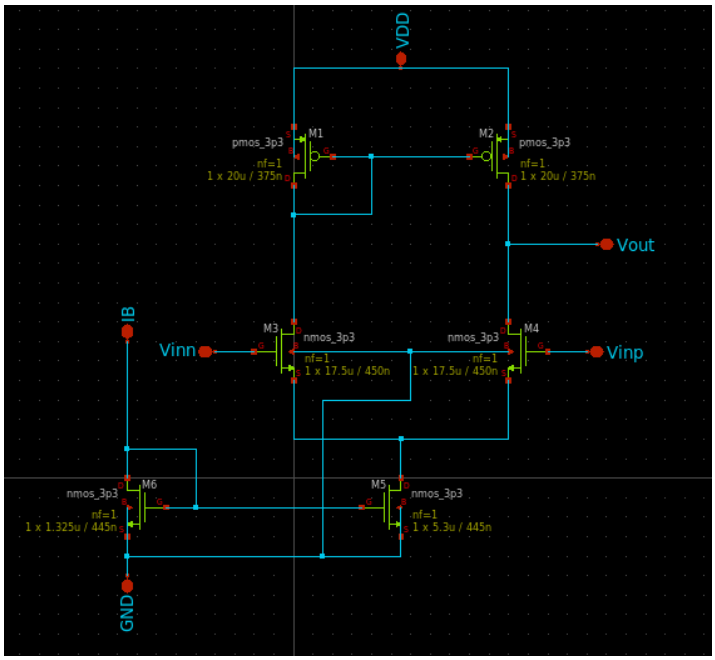
$$W_{tcs} = 40u / 7.6 = 5.3um.$$

- Report a table showing W, L, gm, Id , gm/Id , $Vdsat$, Vov= $Vgs-Vth$, and $V*$=2*gm/Id of all transistors (as calculated from gm/ID curves).

	W	L	g_m	I_D	g_m/I_D	$V_{dsat} \approx V^*$
i_1	$17.5u$	$450n$	$314u$	$20u$	16	0.125
i_2	$17.5u$	$450n$	$314u$	$20u$	16	0.125
l_1	$20u$	$375n$	$300u$	$20u$	12	0.167
l_2	$20u$	$375n$	$300u$	$20u$	12	0.167
tcs	$5.3u$	$445n$	$600u$	$40u$	8	0.25

Part 3: Open Loop OTA Simulation

- Create a testbench as shown above.Report the following:
  ➔ Schematic of the OTA showing sizing of the transistors.



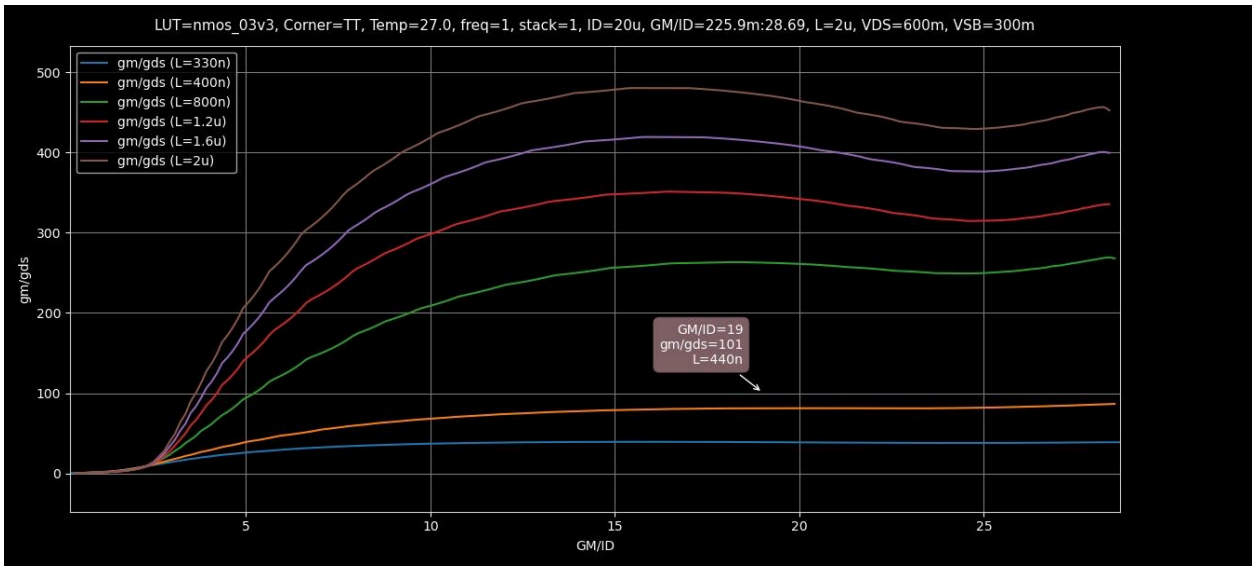
Required schematic

☐ Use VICM at the middle of the CMIR and show the operating points.

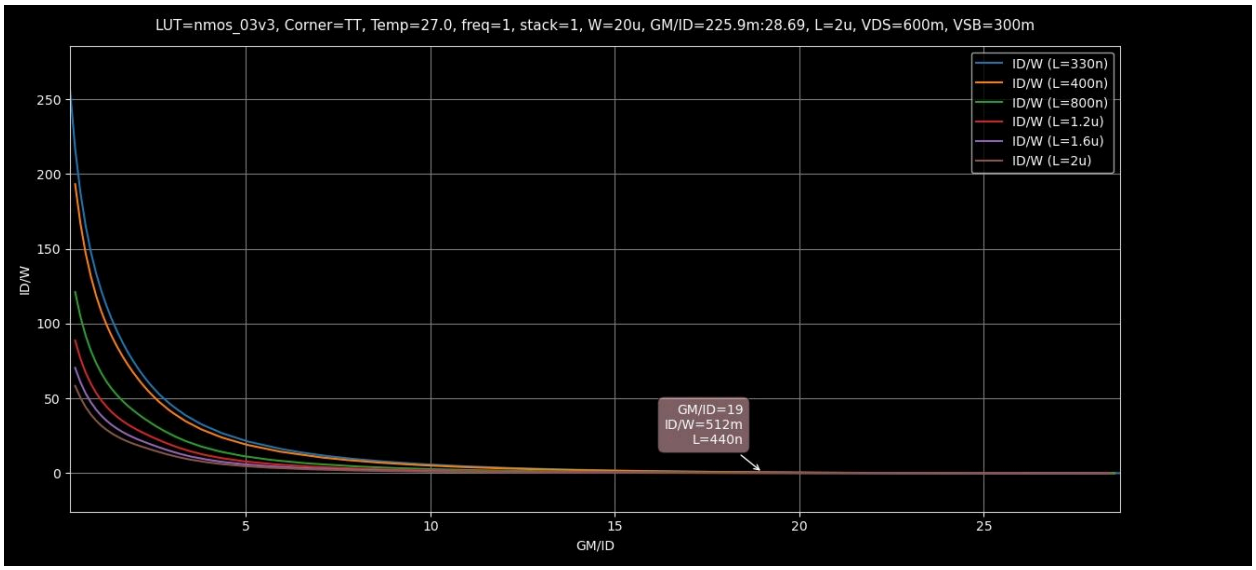
```
f2                =  1.911893e+05
peak = 5.930119e+01
f2 = 1.911893e+05
gbw = 1.133775e+07
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device         m.x1.m.xm6.m0         m.x1.m.xm5.m0         m.x1.m.xm4.m0
      model         x1:nmos_3p3.8         x1:nmos_3p3.8        x1:nmos_3p3.12
         gm           7.92652e-05           0.000314058            0.0003679
       gmbs            2.7031e-05           0.000106251          9.77933e-05
        gds          8.84883e-07           5.73422e-06          4.58001e-06
        vds                     0                     0                     0
      vdsat             0.213794              0.204533             0.0789614
        vgs                     0                     0                     0
        vth             0.693422              0.704402              0.834003
         id                1e-05           3.8872e-05           1.9436e-05

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device         m.x1.m.xm3.m0         m.x1.m.xm2.m0         m.x1.m.xm1.m0
      model        x1:nmos_3p3.12         x1:pmos_3p3.8         x1:pmos_3p3.8
         gm            0.0003679           0.000121362           0.000121362
       gmbs          9.77933e-05           4.90962e-05           4.90962e-05
        gds          4.58001e-06           1.58333e-06           1.58333e-06
        vds                     0                     0                     0
      vdsat             0.0789614              0.274487              0.274487
        vgs                     0                     0                     0
        vth              0.834003              0.770999              0.770999
         id           1.9436e-05            1.9436e-05           1.9436e-05
```

OP

- Note that this OP is obtained after performing fine tuning for the i/p pair, as the GBW spec was not satisfied. In order to increase GBW, G_m needs to be increased, i.e. using larger $\frac{g_m}{I_D}$. $\frac{g_m}{I_D} = 19$ is the new value used



gm / gds of the i/p pair after tuning

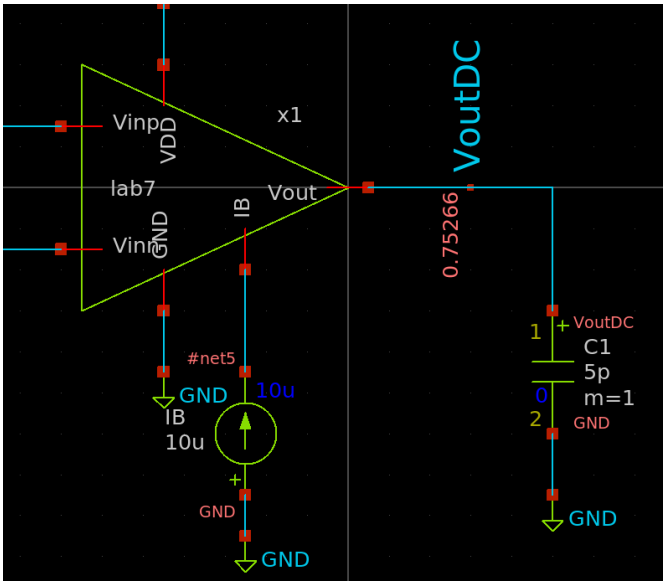


ID / W of the i/p pair after tuning, W ≈ 39um.

☐ Is the current (and gm) in the input pair exactly equal?

- Yes.

☐ What is DC voltage at VOUT? Why?

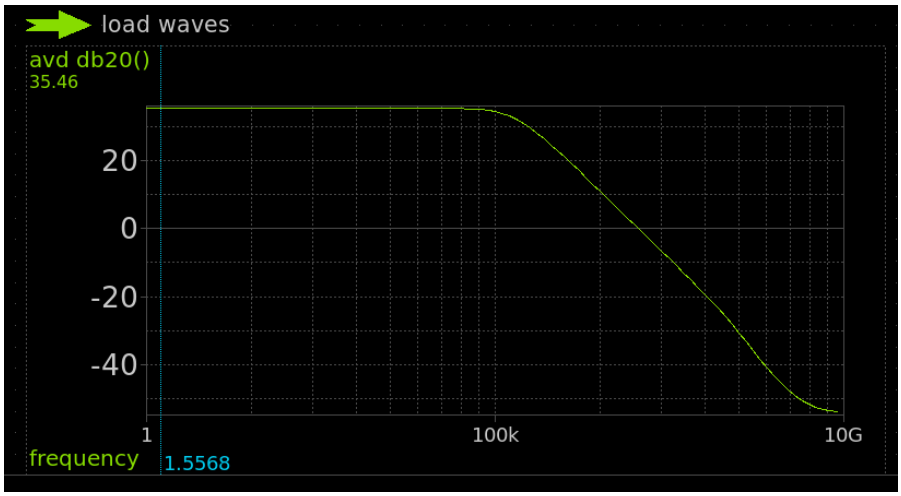


VoutDC

- It's less than the CM i/p due to CM rejection.

➔ Diff small signal ccs:

☐ Set VIDAC = 1 and VICMAC = 0. Use VICM at the middle of the CMIR. Plot diff gain (in dB) vs frequency.



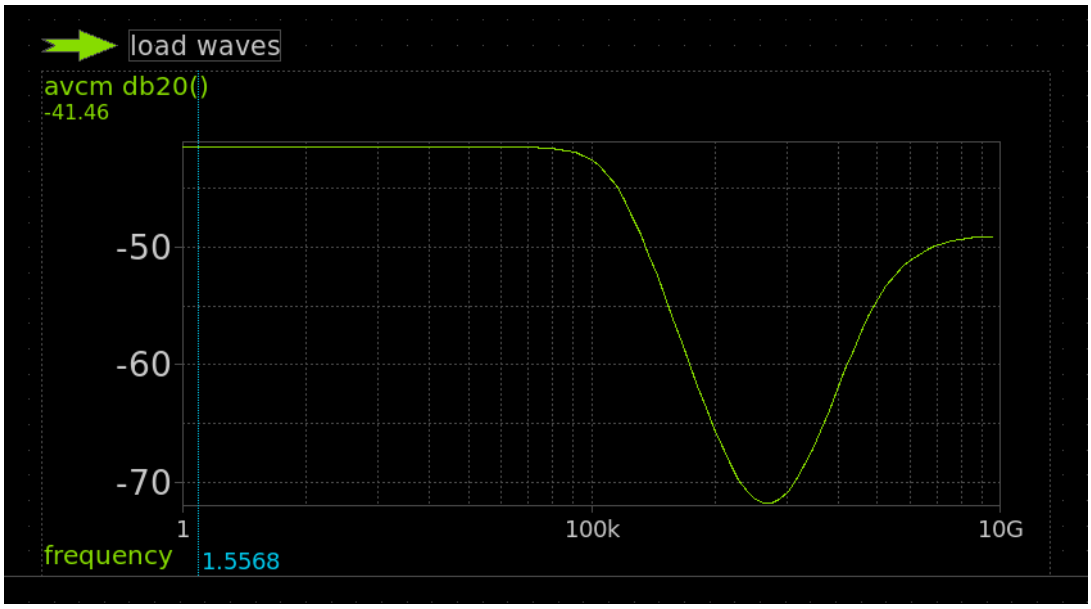
Differential gain vs frequency in dB

☐ Compare simulation results with hand calculations in a table.

Quantity	*Calculated*	*Simulated*
A_{vd}	$A_{vd} = g_{m,i}(r_{o,i} \| \| r_{o,l}) = 59.72 = 35.52dB$	$35.46dB$

➔ CM small signal ccs:

☐ Use AC analysis (1Hz:10GHz, logarithmic, 10 points/decade). Set VICMAC = 1 and VIDAC = 0. Use VICM at the middle of the CMIR. Plot CM gain in dB vs frequency.



CM gain vs frequency

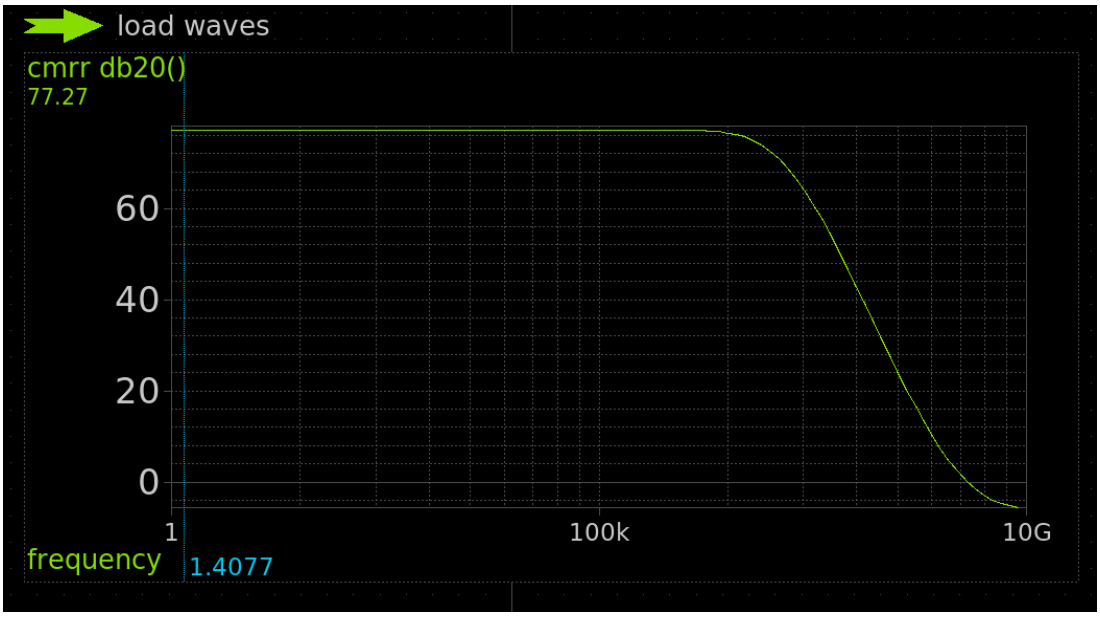
☐ Compare simulation results with hand calculations in a table.

Quantity	*Calculated*	*Simulated*
A_{vCM}	$A_{vCM} = \frac{1}{2g_{m,l}r_{o,tcs}}$ $= 0.01 = -39.2dB$	$-41.5dB$

- Note that this value was obtained after using $W_{tcs} = 470nm$ rather than the calculated one, that is, $W_{tcs,old} = 445nm$, as A_{vCM} that is needed to achieve $CMRR$ spec was not met, which indicated that longer channel is essential to rise $r_{o,tcs}$.

➔ CMRR:

☐ Use VICM at the middle of the CMIR. Plot CMRR in dB vs frequency at VICM at the middle of the CMIR.



CMRR in dB vs frequency

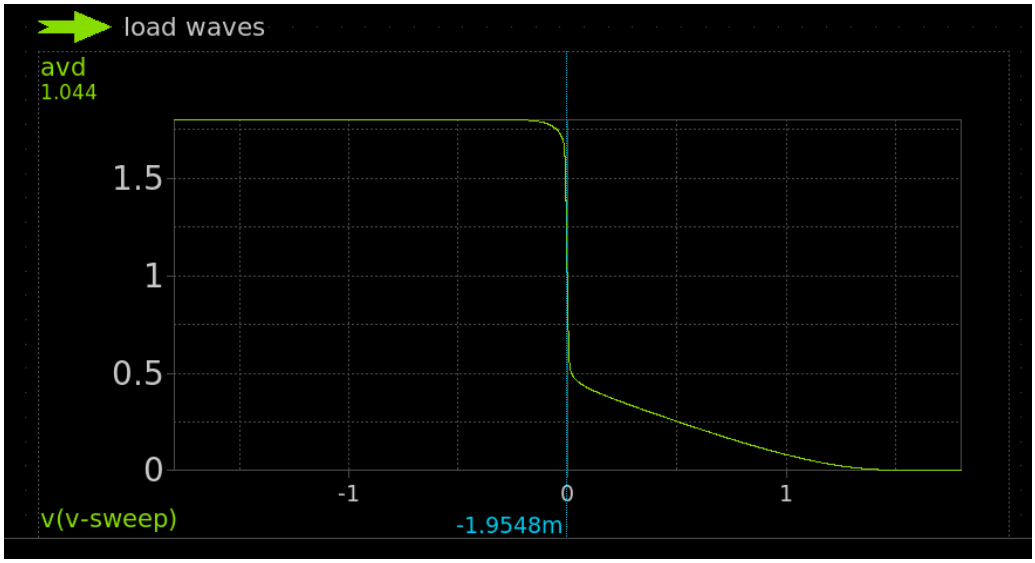
☐ Compare simulation results with hand calculations in a table.

Quantity	Calculated	Simulated
$CMRR$	$g_{m,i}(r_{o,i}\|\|r_{o,l}) \times 2g_{m,l}r_{o,tc}$ $= 2516 = 68dB$	$77dB$

- This large deviation is due to the fact that the parameter values used in hand calculations is before tuning.

➔ Diff large signal ccs:

☐ Use VICM at the middle of the CMIR. Use DC sweep (not parametric sweep) VID = -VDD:1m: VDD. You must use a small step (1mV) because the gain region is very small (steep slope). Plot VOUT vs VID.

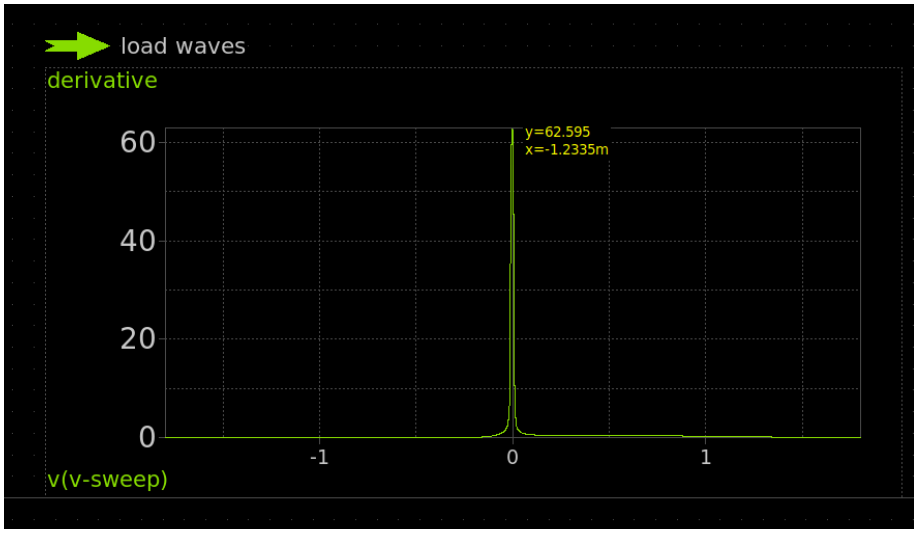


Vout vs VID

☐ From the plot, what is the value of Vout at VID = 0? Why?

- $V_{out}(0) = 1V$.
- To know why, values of V_{GS} and V_{DS} are required, which are not available due to SPICE code imperfections (they are shown as zeros after performing the simulation).

☐ Plot the derivative of VOUT vs VID. Compare the peak with Avd.

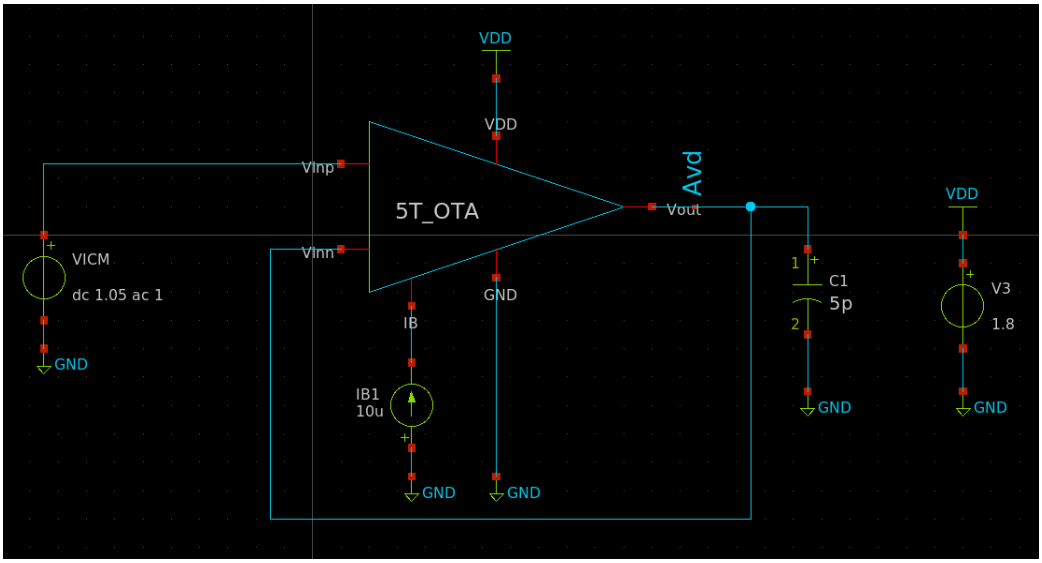


Deriv (Vout) vs VID

Quantity	*obtained from AC analysis*	*obtained from deriv plot*
A_{vd}	$35.46dB$	$62.6 = 35.93dB$

Part 4: Closed Loop OTA Simulation

- Create schematic of the OTA showing current and g_m operating point. Use VINCM = $CMIR_{LOW} + 50mV$.



Required schematic

```
No. of Data Rows : 1
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device          m.x1.xm12.m0          m.x1.xm11.m0          m.x1.xm10.m0
      model            nmos_3p3.8            nmos_3p3.8           pmos_3p3.12
         gm          7.74558e-05           0.000292939          0.000236479
       gmbs          2.72109e-05           0.000102059          9.49974e-05
        gds          7.91073e-07           1.38766e-05           2.2824e-06
        vds             0.898746              0.286374              0.751887
      vdsat             0.219915              0.209643              0.136693
        vgs             0.898756              0.898756              0.875788
        vth             0.696105              0.708302              0.775353
         id                1e-05           3.76205e-05          1.86726e-05

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device          m.x1.xm9.m0           m.x1.xm8.m0           m.x1.xm7.m0
      model          pmos_3p3.12           nmos_3p3.12           nmos_3p3.12
         gm          0.000239408           0.000356321          0.000360737
       gmbs          9.61091e-05           0.000101684          0.000102955
        gds          2.16744e-06           3.16264e-06          3.33855e-06
        vds             0.875787              0.761718              0.637818
      vdsat             0.137027             0.0762069             0.0767849
        vgs             0.875788              0.761718              0.763608
        vth             0.774881              0.791193              0.791552
         id          1.89479e-05           1.86726e-05          1.89479e-05

gm_mismatch = 4.415720e-06
id_mismatch = 2.753356e-07
```

Required calculations

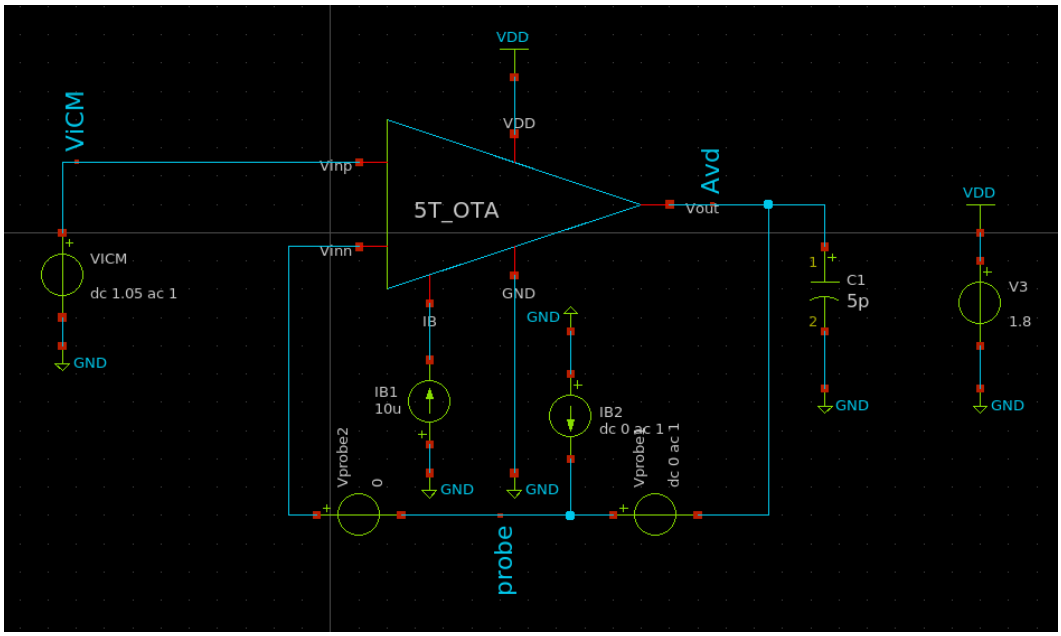
➔ Is the current (and gm) in the input pair exactly equal? Why?

- There is no exact equality in I_D and g_m due to the fact that the load of one i/p transistor is a diode-connected device, which probably leads to gate current leakage that creates a non-exact equality between currents and, therefore, the transconductances.

➔ Calculate the mismatch in I_D and g_m.

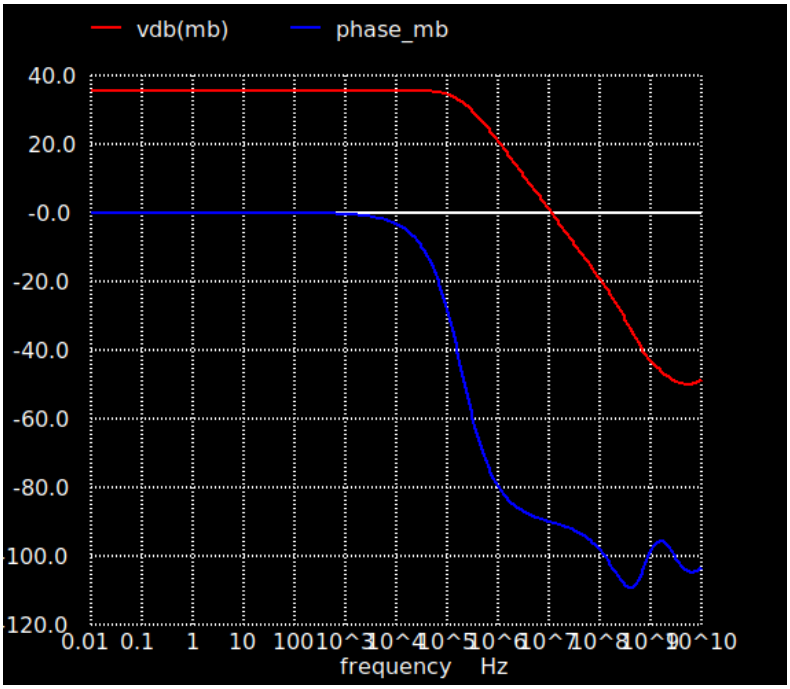
$$\sigma I_{out}/I_{out} = 2.75e - 7/20u = 1.375\%$$
$$\sigma g_m/g_m = 4.42e - 6/0.0003067 = 1.44\%$$

- Loop Gain:
  ➔ Put the OTA in a unity gain buffer configuration as shown in the schematic below.



Required configuration

➔ Use VICM at the middle of the CMIR. Plot loop gain in dB and phase vs frequency. Show the results in the console.



Loop gain & phase vs frequency

```
bw                =  1.828081e+05
pm_deg            =  -9.004003e+01
dominant_pole_f   =  1.122027e+07
loop_gain         =  3.577049e+01
gbw = 1.123362e+07
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 1
 BSIM4v5: Berkeley Short Channel IGFET Model-4
    device          m.x1.m.xm6.m0          m.x1.m.xm5.m0          m.x1.m.xm4.m0
     model          x1:nmos_3p3.8          x1:nmos_3p3.8         x1:nmos_3p3.12
        gm            7.74558e-05             0.000307758             0.00036236
      gmbs            2.72109e-05             0.000107105            9.62457e-05
       gds            7.91073e-07            5.34252e-06            3.19357e-06
       vds               0.898746                0.44013                0.804686
     vdsat               0.219915               0.209838               0.0772391
       vgs               0.898756               0.898756               0.804687
       vth               0.696105               0.708033                0.83266
        id                   1e-05            3.88705e-05            1.90418e-05

 BSIM4v5: Berkeley Short Channel IGFET Model-4
    device          m.x1.m.xm3.m0          m.x1.m.xm2.m0          m.x1.m.xm1.m0
     model         x1:nmos_3p3.12         x1:pmos_3p3.12         x1:pmos_3p3.12
        gm             0.00037462             0.000238164            0.000246589
      gmbs            9.95332e-05            9.5786e-05             9.9002e-05
       gds            3.79541e-06            2.67089e-06            2.2472e-06
       vds               0.480469               0.555162               0.879379
     vdsat              0.0788564                0.138713               0.139592
       vgs               0.809851               0.879381               0.879381
       vth               0.833653               0.776101               0.774868
        id            1.98288e-05            1.90417e-05            1.98288e-05
```

Results from console

➔ Compare DC gain and GBW with those obtained from open-loop simulation. Comment.

$Quantity$	OL	LG
$DC\ gain$	~ 59	$\sim 35.7dB \approx 60.9$
GBW	$11.3M$	$11.2M$

- Open loop gain and loop gain are the same as $\beta = 1$.

➔ Show the operating point at VICM in the middle of the CMIR.

```
No. of Data Rows : 1
 BSIM4v5: Berkeley Short Channel IGFET Model-4
    device         m.x1.m.xm6.m0         m.x1.m.xm5.m0         m.x1.m.xm4.m0
     model         x1:nmos_3p3.8         x1:nmos_3p3.8        x1:nmos_3p3.12
        gm          7.74558e-05           0.000307758           0.00036236
      gmbs          2.72109e-05           0.00010705           9.62457e-05
       gds          7.91073e-07           5.34252e-06           3.19357e-06
       vds             0.898746               0.44013              0.804686
     vdsat             0.219915              0.209838             0.0772391
       vgs             0.898756              0.898756              0.804687
       vth             0.696105              0.708033               0.83266
        id                 1e-05           3.88705e-05           1.90418e-05

 BSIM4v5: Berkeley Short Channel IGFET Model-4
    device         m.x1.m.xm3.m0         m.x1.m.xm2.m0         m.x1.m.xm1.m0
     model        x1:nmos_3p3.12        x1:pmos_3p3.12        x1:pmos_3p3.12
        gm           0.00037462           0.000238164           0.000246589
      gmbs          9.95332e-05           9.5786e-05           9.9002e-05
       gds          3.79541e-06          2.67089e-06          2.2472e-06
       vds             0.480469              0.555162              0.879379
     vdsat            0.0788564              0.138713              0.139592
       vgs             0.809851              0.879381              0.879381
       vth             0.833653              0.776101              0.774868
        id          1.98288e-05           1.90417e-05           1.98288e-05
```

OP @ middle of CMIR

➔ Compare simulation results (DC gain and GBW) with hand calculations in a table.

$Quantity$	$Calculated$	$Simulated$
$DC\ gain$	$LG = \beta A_{OL} = A_{OL} \approx 60$	$35.8dB = 60.9$
GBW	$GBW(LG) = GBW(A_{OL}) = 11.3M$	$11.2M$