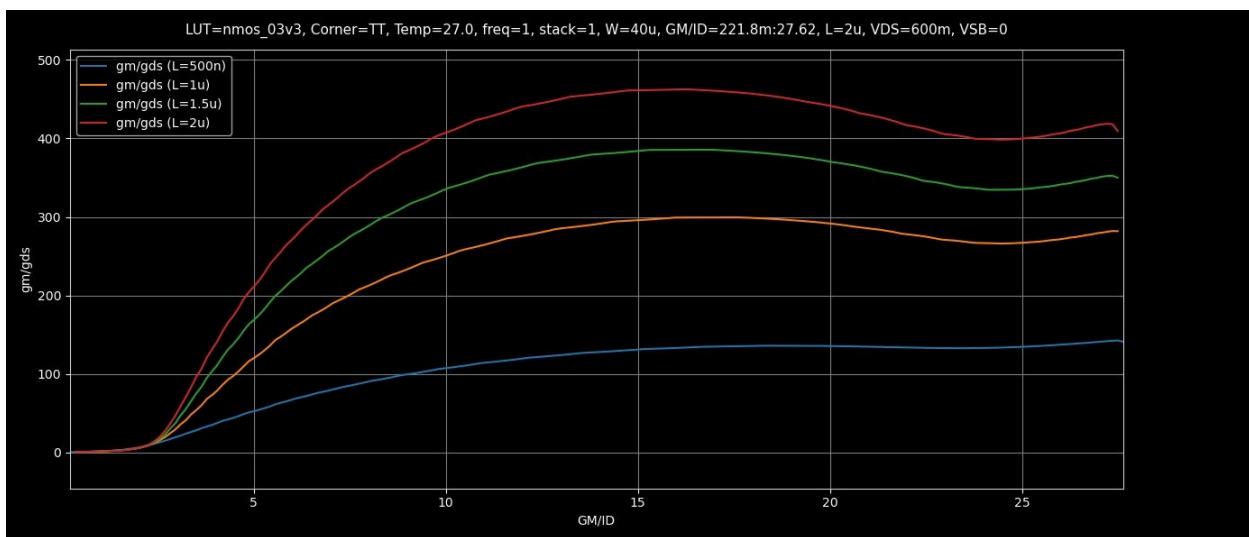


CMOS AIC design - ITI - Lab 9

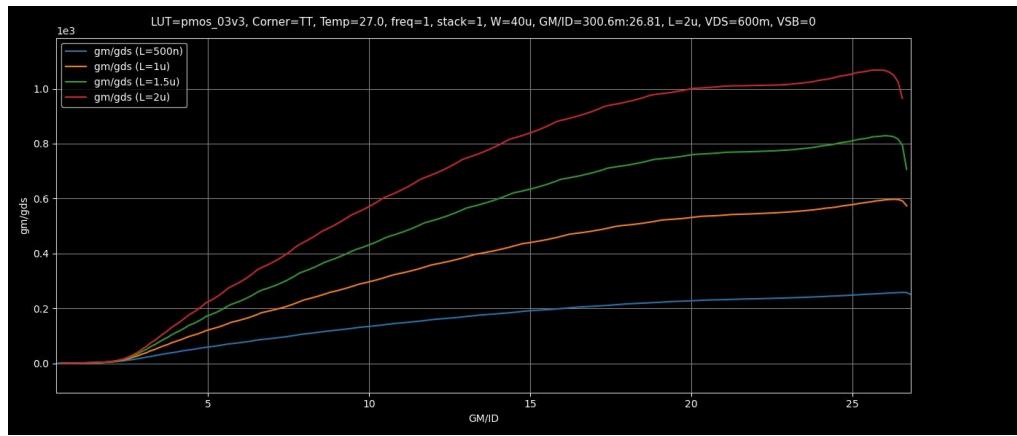
Part 1: gm/ID Design Charts

Suffix Index	
<i>tcs</i>	<i>Tail Current Source</i>
<i>cs</i>	<i>Current Source of 2nd Stage</i>
<i>i/p p</i>	<i>i/p pair</i>
<i>CML</i>	<i>Current Mirror Load</i>
<i>2nd i/p</i>	<i>i/p transistor od 2nd stage</i>
<i>CM</i>	<i>Current Mirror devices</i>

- Using ADT Device Xplore, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS = VDD/3 and L = 0.18u,0.5u:0.5u:2u.
→ gm/gds

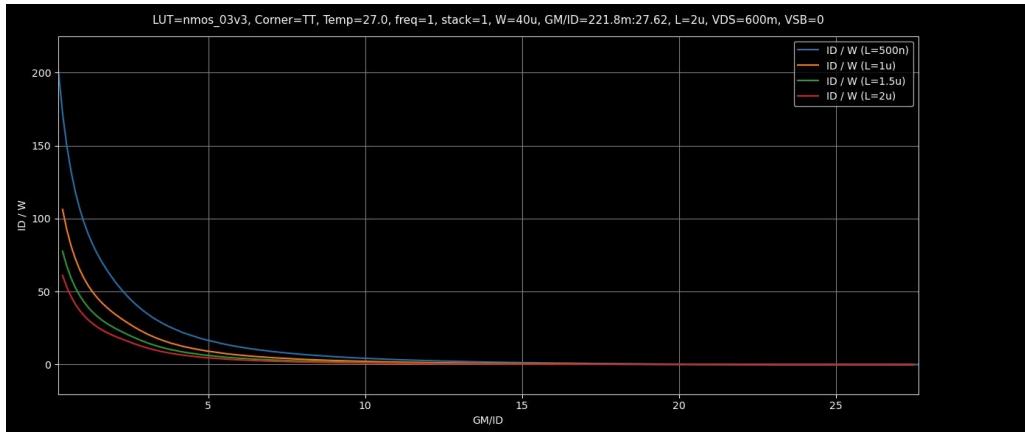


gm / gds vs gm / ID @ VSB = 0, W = 40um for NMOS

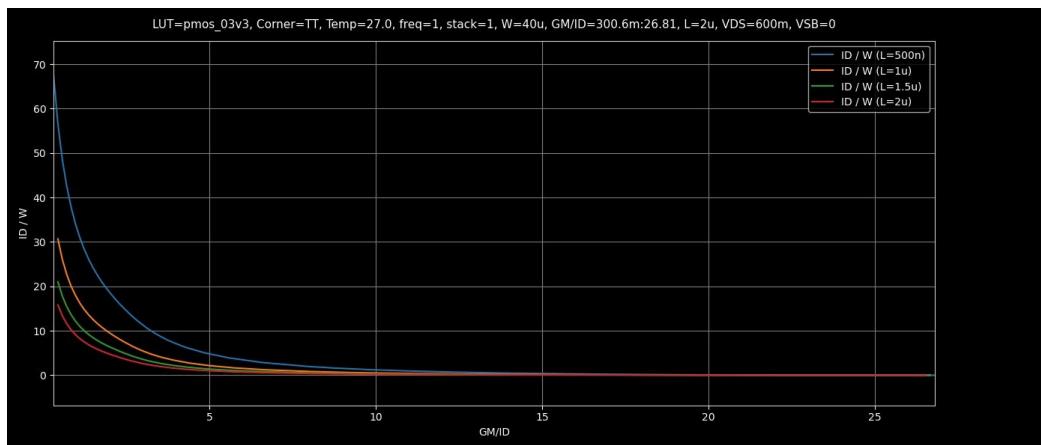


gm / gds vs gm / ID @ $V_{SB} = 0$, $W = 40\mu m$ for **PMOS**

→ ID/W

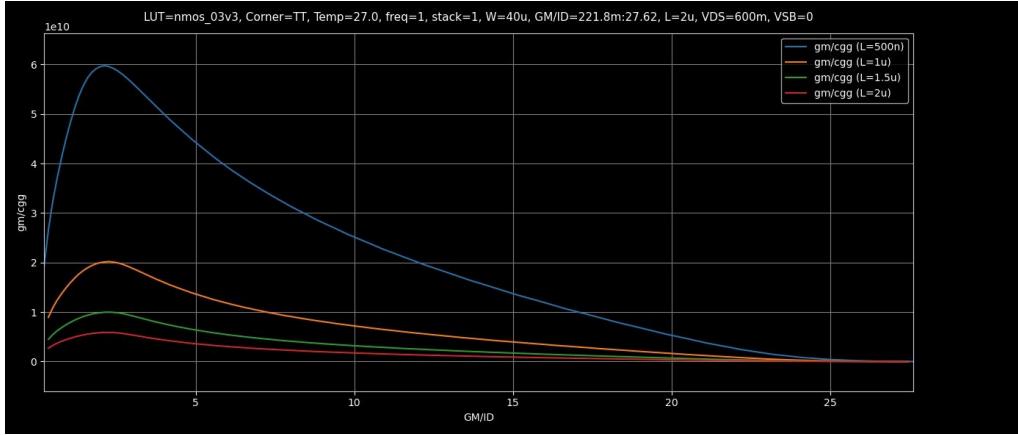


ID / W vs gm / ID @ $V_{SB} = 0$, $W = 40\mu m$ for **NMOS**

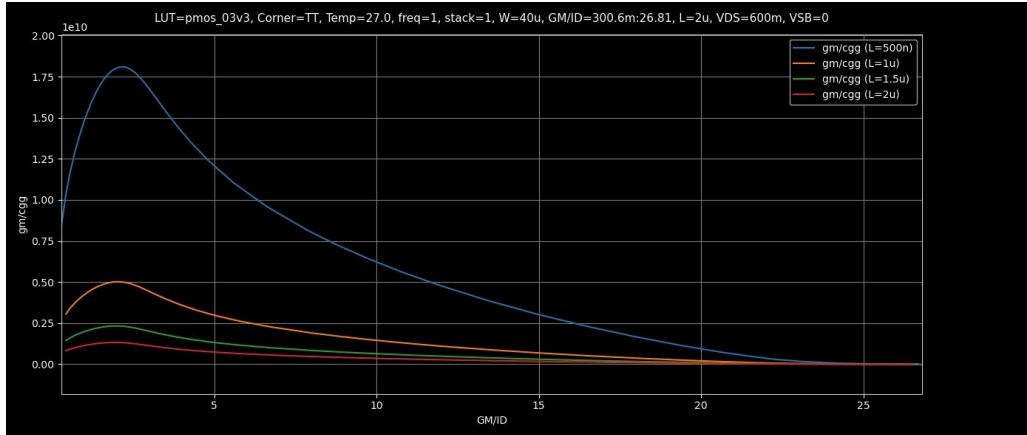


ID / W vs gm / ID @ $V_{SB} = 0$, $W = 40\mu m$ for **PMOS**

→ gm/Cgg

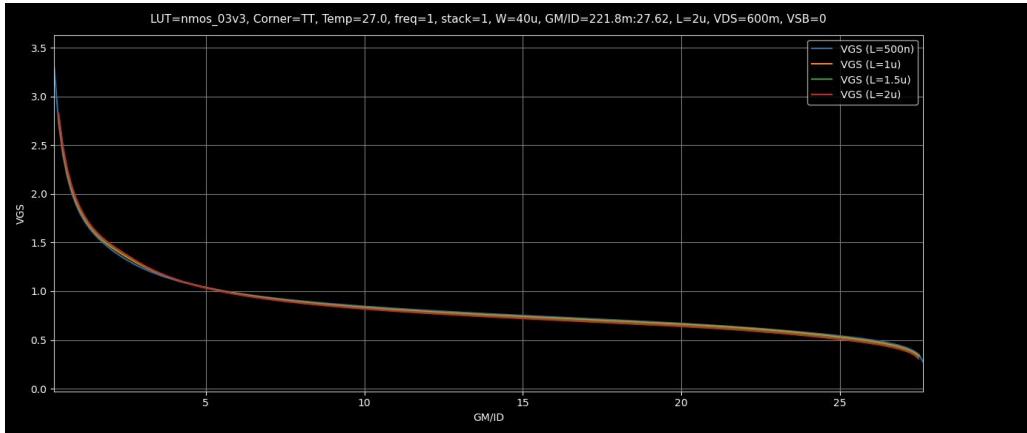


gm / Cgg vs gm / ID @ VSB = 0, W = 40um for NMOS

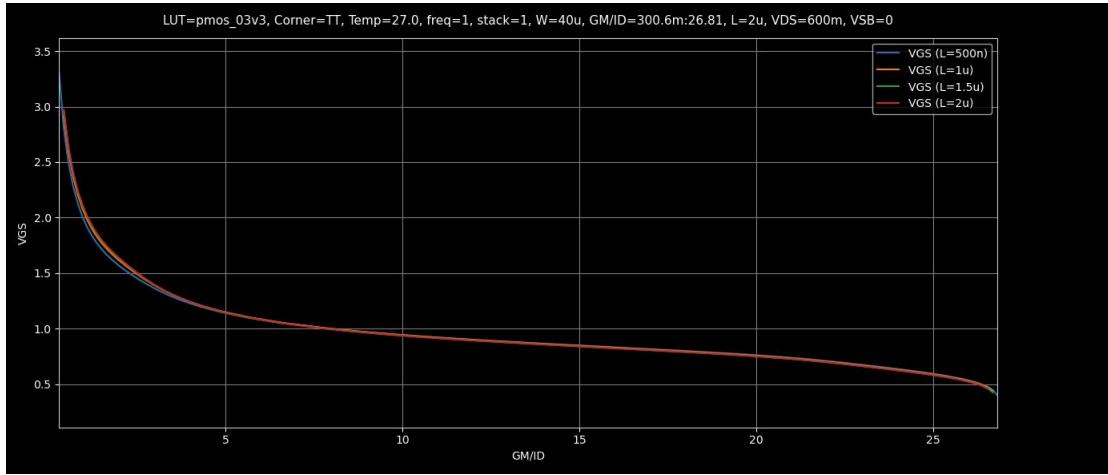


gm / Cgg vs gm / ID @ VSB = 0, W = 40um for PMOS

→ VGS



VGS vs gm / ID @ VSB = 0, W = 40um for NMOS



VGS vs gm / ID @ VSB = 0, W = 40um for PMOS

Part 2: OTA Design

- Use gm/ID methodology to design a differential input, single-ended output two-stage Miller-compensated OTA. The OTA is to be used as a buffer (unity gain feedback configuration) to probe sensitive internal signals in a complex mixed-signal design. The OTA should achieve the specs below (as listed). Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec), but design your own bias circuit (current mirrors). Create a schematic and an appropriate symbol for the OTA.

The design is finished using the suggested procedure

- From CMIR spec: the i/p pair should be of PMOS type, since the required CMIR is closer to GND.
- Calculate the unity gain frequency (UGF) from the rise time requirement ($t_{rise} = 2.2\tau$). Hence, calculate $g_{m, i/p p}$.

$$\tau_{CL} = \frac{t_{rise}}{2.2} \approx 31.8ns.$$

$$UGF = \frac{A_{CL}}{\tau_{CL}} \approx \frac{1}{31.8n} = 31.4M.$$

$$UGF = 31.4M = \frac{g_{m,i/p\ p}}{C_c} \Leftrightarrow g_{m,i/p\ p} = 31.4M \times 2.5p = 78.6uS.$$

- From the SR requirement, calculate the current required in the first stage. Given the total current budget, calculate the current of the second stage.

$$SR = \frac{I_{B1}}{C_c} \Leftrightarrow I_{B1} = 5M \times 2.5p = 12.5uA.$$

$$I_{B2} = 60 - 12.5 = 47.5uA.$$

- Calculate gm/ID of the first stage.

$$\frac{g_m}{I_D} (i/p\ p) = \frac{78.6}{6.25} = 12.6S/A.$$

- Given A_{vCL} gain error spec ($\%error = |\frac{actual-ideal}{ideal}| \times 100$), calculate the required DC gain in dB.

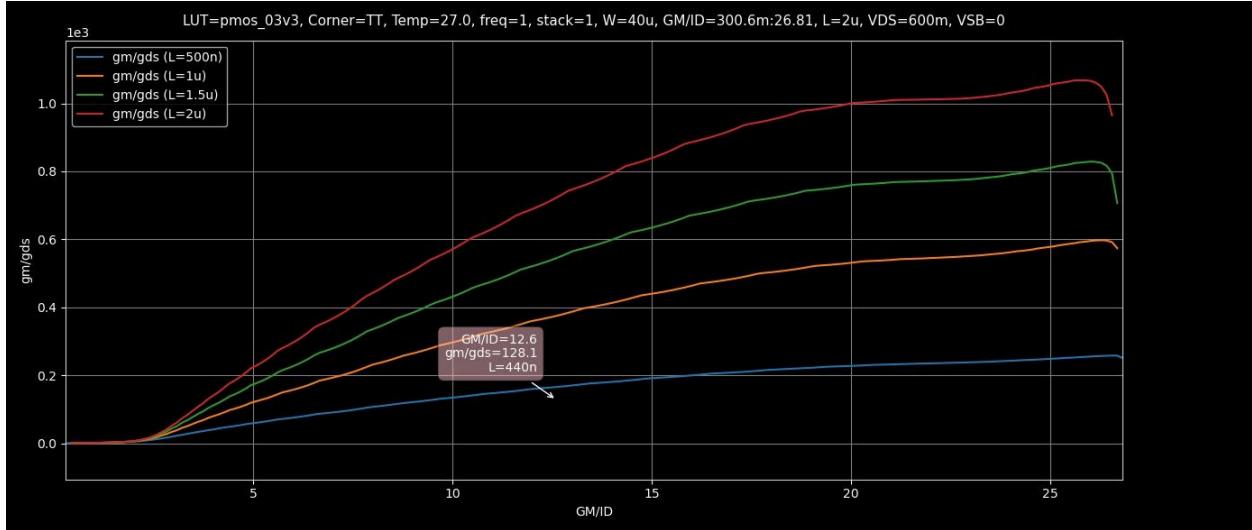
$$V_{err} = \frac{1}{LG}, \beta = 1 \Rightarrow V_{err} = 0.05/100 = \frac{1}{A_{OL}} \Rightarrow A_{OL} = 2000 = 66dB.$$

- Assign larger gain for the first stage. Do not split the gain equally between the two stages. You may assume the first stage gain is twice that of the second stage (6dB difference).

$$A_1 = 2A_2 \Leftrightarrow A_1 = 36dB, A_2 = 30dB.$$

- Given the 1st stage gain, calculate L (channel length) of the 1st stage input. You may assume input and load have the same gds.

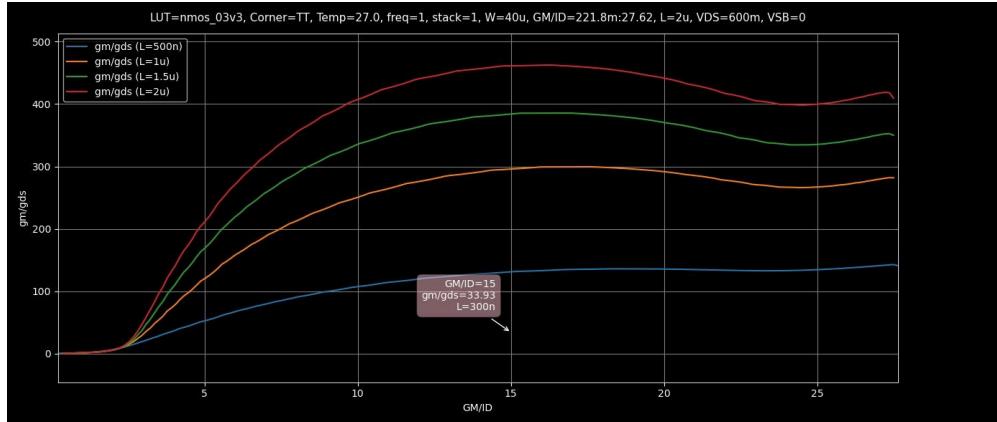
$$A_1 = 36dB = 63 = \frac{g_{m,i/p} r_{o,il}}{2} \Rightarrow \frac{g_m}{g_{ds}} (i/p p) = 126. Given \frac{g_m}{I_D} (i/p p) = 12.6S/A.$$



- Given VA of the first stage current mirror load, select L. Note that VA slightly decreases with gm/ID, which is not known yet. To get an estimate for L, you may ignore this dependence and assume a relatively large gm/ID for the load at this point (e.g., gm/ID = 15).

$$let \frac{g_m}{I_D} (CML) = 15, I_D = 6.25uA \Rightarrow g_{m,CML} \approx 94uS.$$

$$g_{ds,CML} = 3uS \Rightarrow \frac{g_m}{g_{ds}} (CML) = 31.3.$$



L is chosen to be 550nm

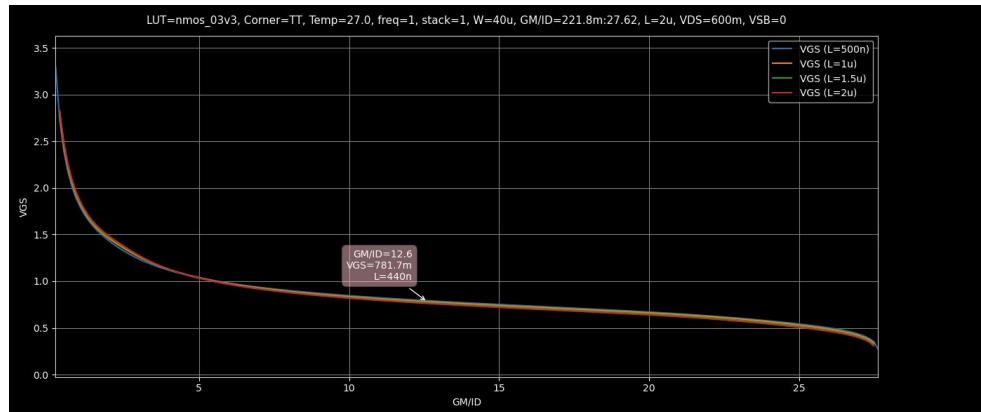
- Given the PM spec, calculate gm/ID of the second stage input transistor (Hint: assume $\omega_{P2} = 4\omega_u$).

$$\omega_{p2} = 125.6M = \frac{g_{m, 2nd\ i/p}}{C_L} \Rightarrow g_{m, 2nd\ i/p} = 628\mu S.$$

$$given I_D = 47.5\mu A \Rightarrow \frac{g_m}{I_D} (2nd\ i/p) = 13.2.$$

- Given the CMIR-high and Swing-high specs, calculate max vdsat for tail current source and output load.
 - Let CMIR-high = 0.8V..

Applying KVL: $|V_{GS,i}| + |V_{DS,tcs}| < 1$.



VGS of the i/p pair

$$|V_{DS,tcs}| = V_{tcs}^* < 220mV \Rightarrow \frac{g_m}{I_D}(CM) > 9$$

- Use the CMRR spec to find gds of the tail current source (note that the second stage does not affect the CMRR).

$$CMRR = A_{vd}(dB) - A_{vCM}(dB) \Rightarrow A_{vCM}(dB) = -38dB = 0.013.$$

$$A_{vCM} = \frac{1}{2g_{m,CML}r_{o,tcs}} = 0.013, \text{ let } \frac{g_m}{I_D}(CML) = 10, \text{ given } I_D = 6.25\mu A$$

$$g_{m,CML} = 62.5\mu S \Rightarrow g_{ds,tcs} = 1.625\mu S.$$

- Tail current source and 2nd stage load must have the same L (they form a current mirror). Thus, get gds of the 2nd stage load

$g_{ds,tcs} = 1.625\mu S$	$g_{ds,cs} = ??$
$I_{B1} = 12.5\mu A$	$I_{B2} = 47.5\mu A$

$$g_{ds,cs} = 6.175\mu S.$$

- Given the 2nd stage gain, calculate gds and L of the 2nd stage input transistor. This transistor is now fully specified; thus, calculate its VGS.

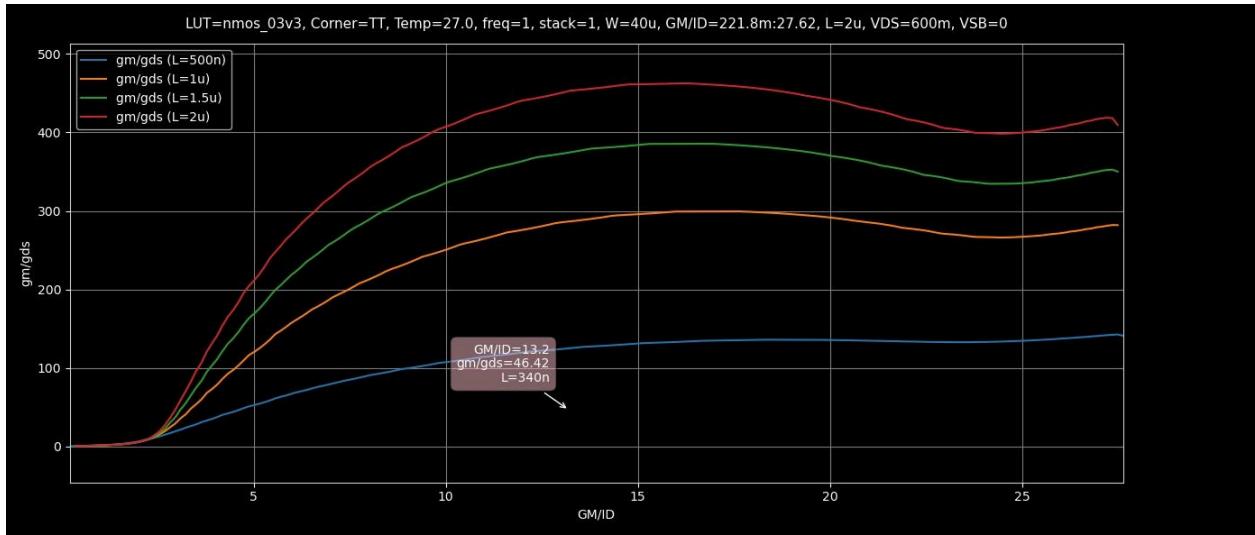
$$A_2 = 30dB = 31.6 = g_{m,2nd\ i/p}(r_{o,cs} || r_{o,2nd\ i/p})$$

$$\text{given } \frac{g_m}{I_D}(2nd\ i/p) = 13.2, I_D = 47.5\mu A$$

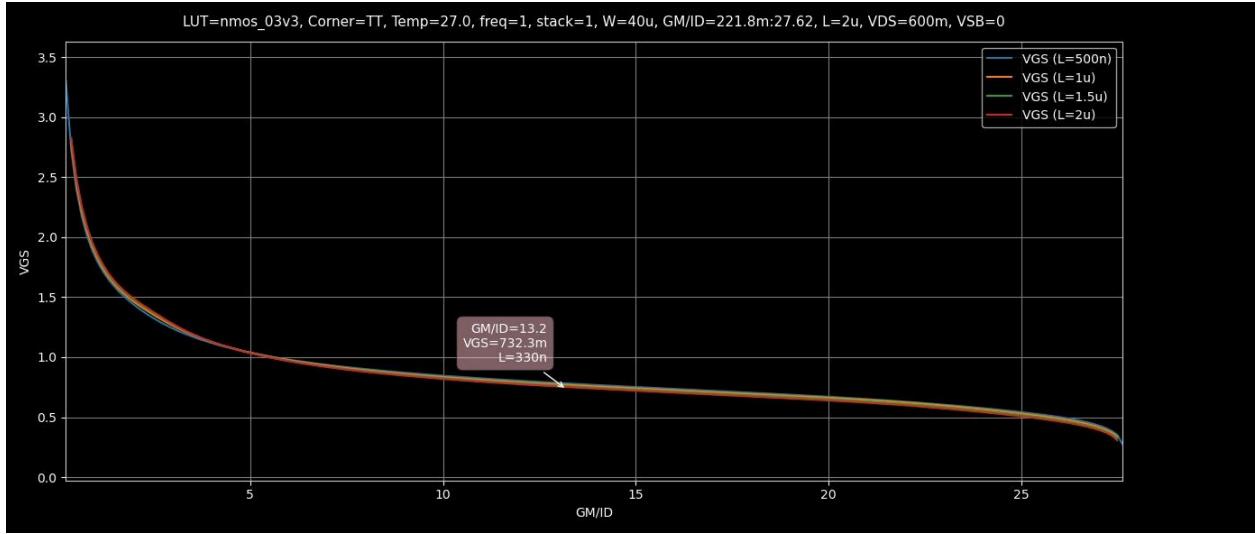
$$g_{m,2nd\ i/p} = 627\mu S.$$

$$\text{given } r_{o,cs} = 162k\Omega \Rightarrow g_{ds,2nd\ i/p} = 13.7\mu S.$$

$$\frac{g_m}{g_{ds}} \text{ (2nd } i/p) = 46, \text{ given } \frac{g_m}{I_D} (i/p p) = 13.2, \text{ thus}$$

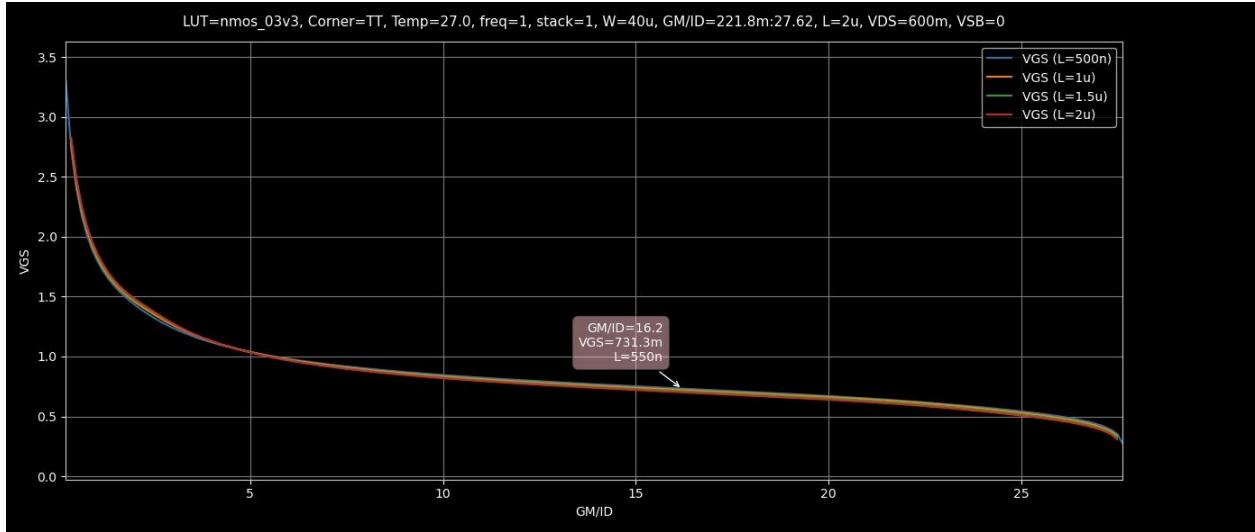


L is chosen to be 340nm



$VGS \approx 730mV$.

- Note that you need to avoid systematic offset. Use VGS charts to guarantee that 1st stage current mirror load and 2nd stage input transistor have the same VGS. Use this condition to determine the gm/ID of the current mirror load in the first stage.



$$gm / ID = 16.2$$

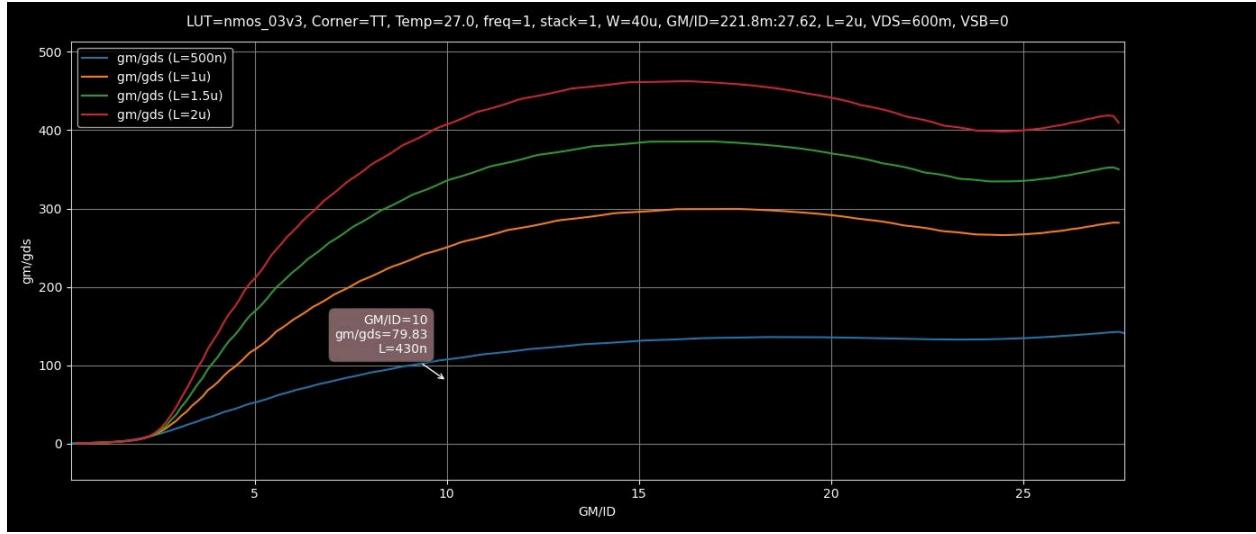
- Check that the calculated gm/ID is larger than the one you assumed before (to guarantee that the CMRR is satisfied).
 - It is larger than that assumed previously.
- Choose R_Z to place the zero at infinity (some designers may move the LHP zero to the vicinity of the non-dominant pole to improve the PM). Do NOT place the LHP zero at a frequency less than ω_{p2} .

$$R_Z = \frac{1}{g_{m, 2nd\ i/p}} = \frac{1}{627u} = 1.6k\Omega.$$

- Calculating L of tail current source

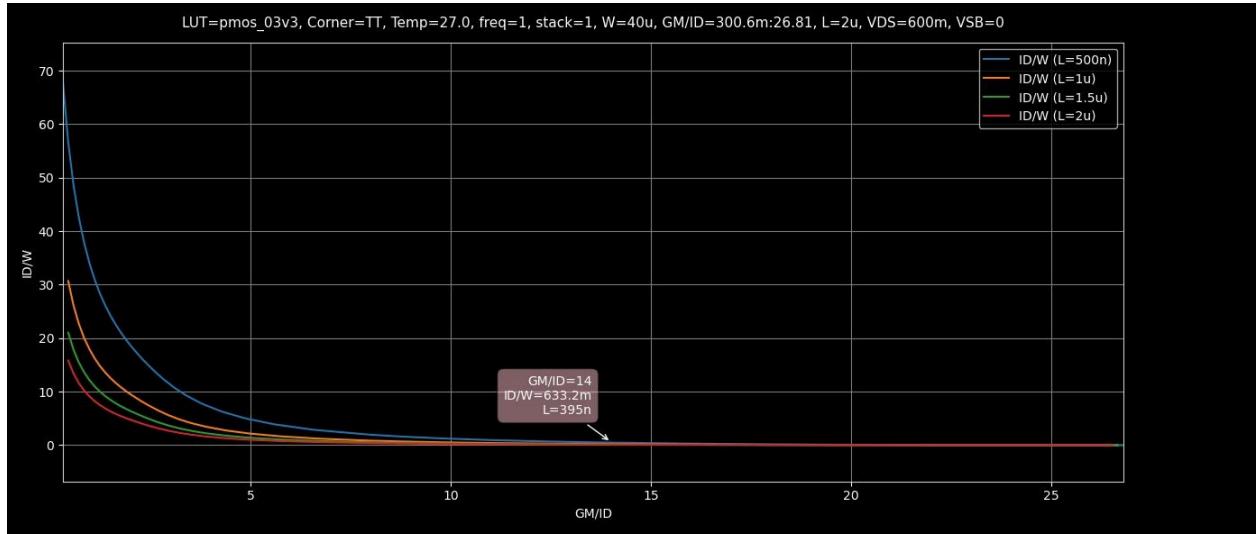
let $\frac{g_m}{I_D}(tcs) = 10$, given $I_D = 12.5uA \Rightarrow g_{m,tcs} = 125uS$.

$$\text{given } g_{ds,tcs} = 1.625uS \Rightarrow \frac{g_m}{g_{ds}}(tcs) = 77$$



L is chosen to be 430nm

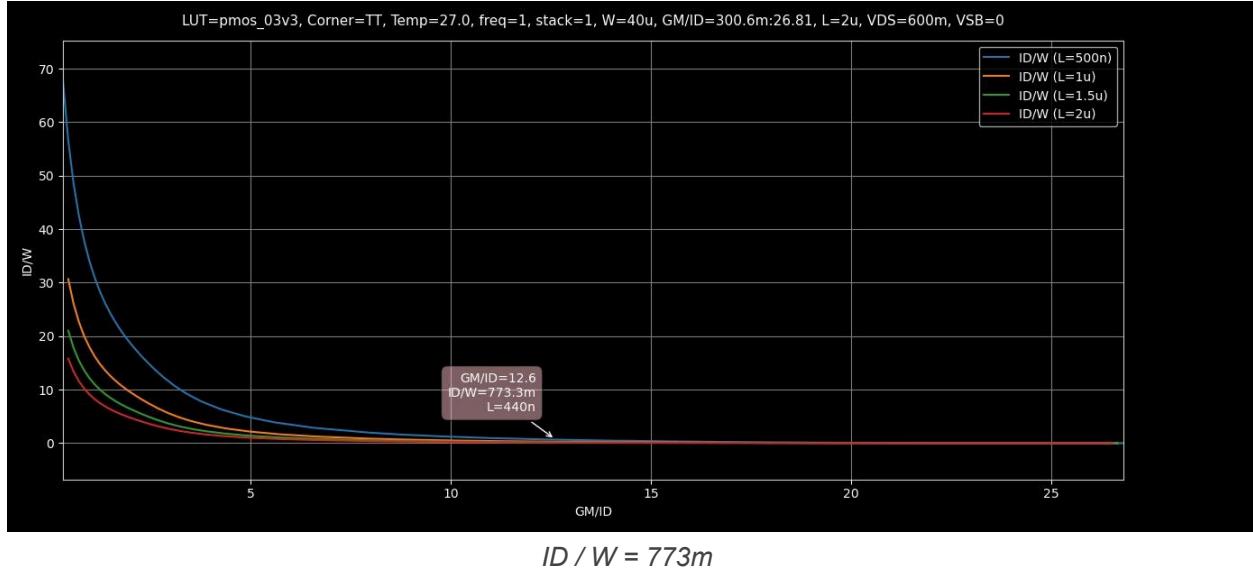
- L of 2nd stage current source = L of tcs.
- Calculating W of tail current source.



$ID / W \approx 760m$

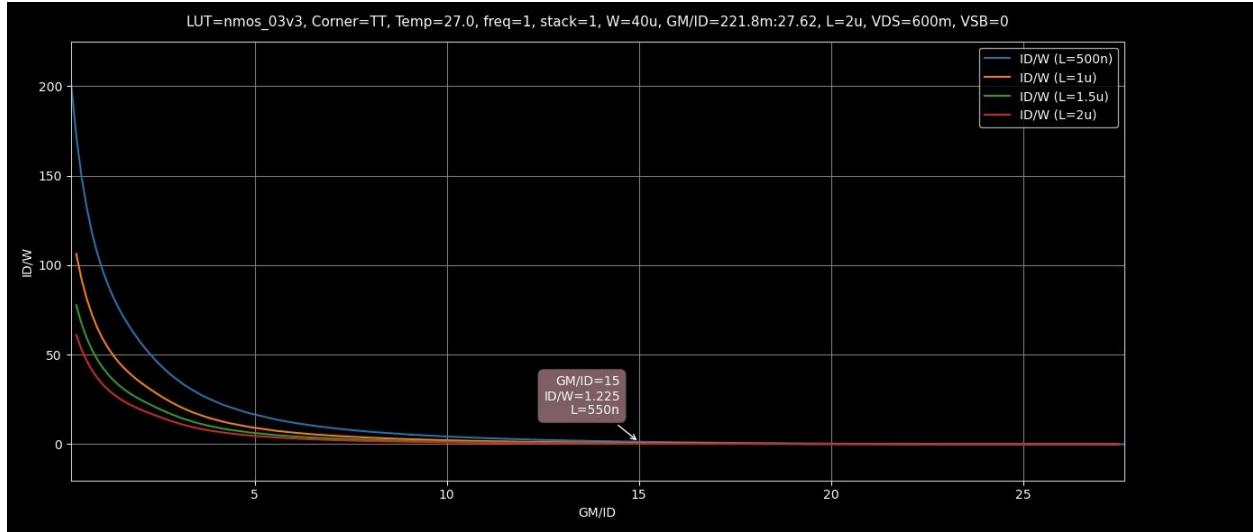
$$given I_D = 12.5\mu A \Rightarrow W = 19.8\mu m.$$

- Calculating W of i/p pair



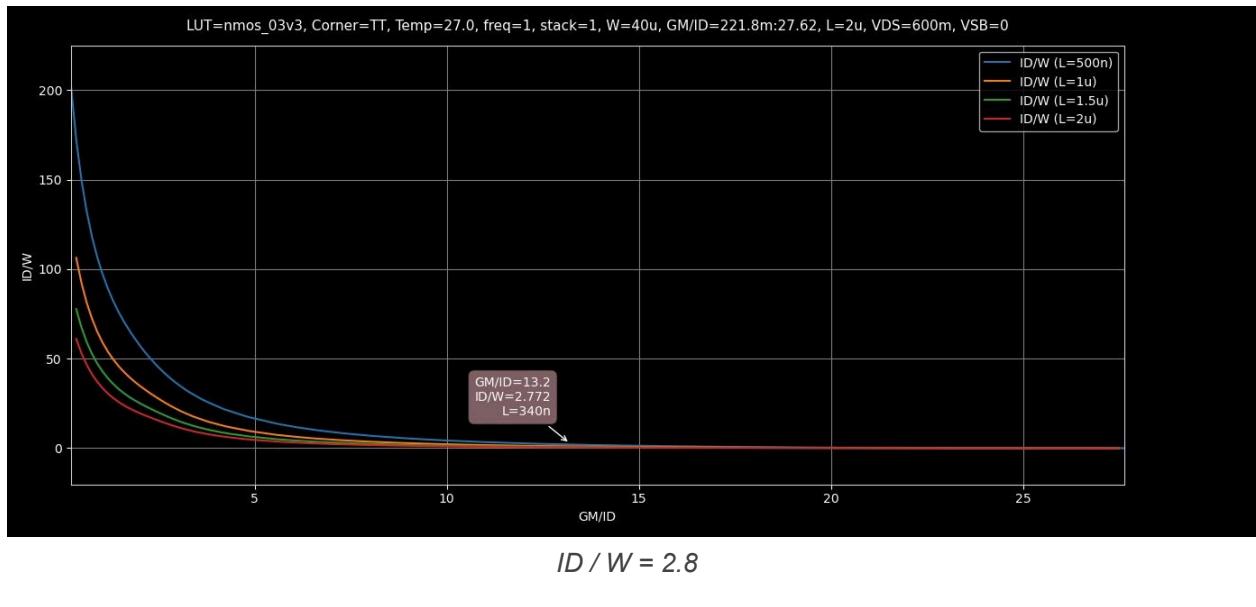
$$\text{given } I_D = 6.25\mu A \Rightarrow W \approx 8\mu m.$$

- Calculating W of current mirror load:



$$\text{given } I_D = 6.25\mu A \Rightarrow W = 5.1\mu m.$$

- Calculating W of 2nd stage i/p:



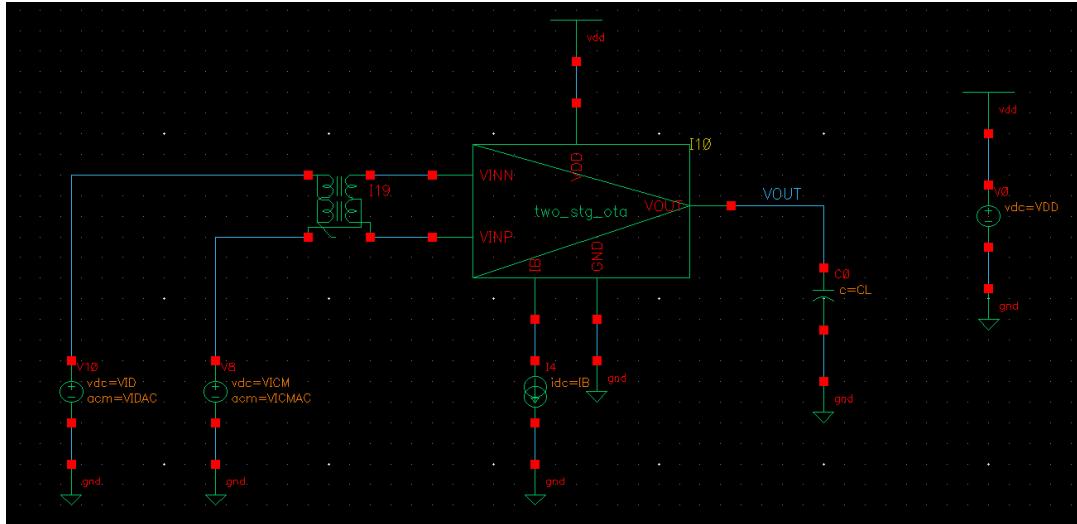
given $I_D = 47.5 \mu A \Rightarrow W = 17.1 \mu m.$

- The required table is as follows:

	W	L	g_m	I_D	g_m/I_D	$V_{Dsat} \approx V^*$
<i>tcs</i>	$19.8 \mu u$	$430n$	$125 \mu u$	$12.5 \mu u$	10	$200m$
<i>i/p p</i>	$8 \mu u$	$440n$	$78.6 \mu u$	$6.25 \mu u$	12.6	$160m$
<i>CML</i>	$5.1 \mu u$	$550n$	$94 \mu u$	$6.25 \mu u$	15	$133m$
<i>2nd i/p</i>	$17.1 \mu u$	$340n$	$628 \mu u$	$47.5 \mu u$	13.2	$150m$
<i>cs</i>	$75 \mu u$	$430n$	$475 \mu u$	$47.5 \mu u$	10	$200m$

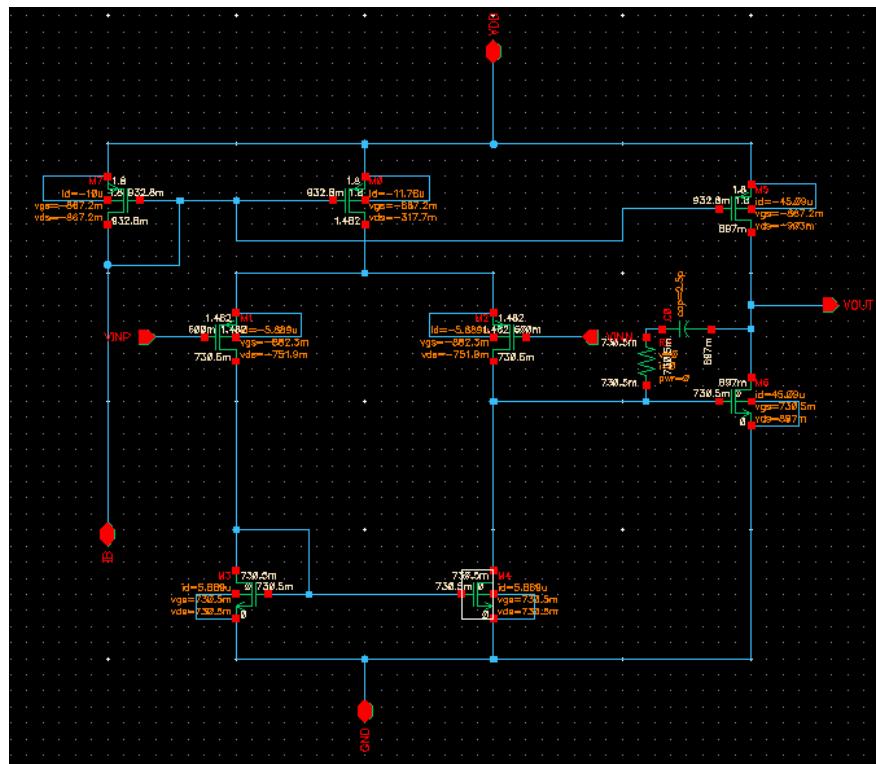
Part 3: Open Loop OTA Simulation

- Create a testbench similar to the one shown above



Required testbench

- Report the following:
 - Schematic of the OTA and bias circuit with DC node voltages clearly annotated.
 - Use $V_{CM} = V_{DD}/3$.



OTA sch with DC node voltages annotated

- Is the current (and gm) in the input pair exactly equal?
 - Yes.
- What is DC voltage at the output of the first stage? Why?
 - $V_{o,DC1} = 730.5mV$. When applying KVL such that $V_{o,DC1} = V_{DD} - |V_{DS,tcs}| - |V_{DS,i/p\ p}|$ this value would be obtained.
- What is DC voltage at the output of the second stage? Why?
 - $V_{o,DC2} = 897mV$. The width of current mirror load is swept and selected such that this particular value of dc o/p voltage is obtained.

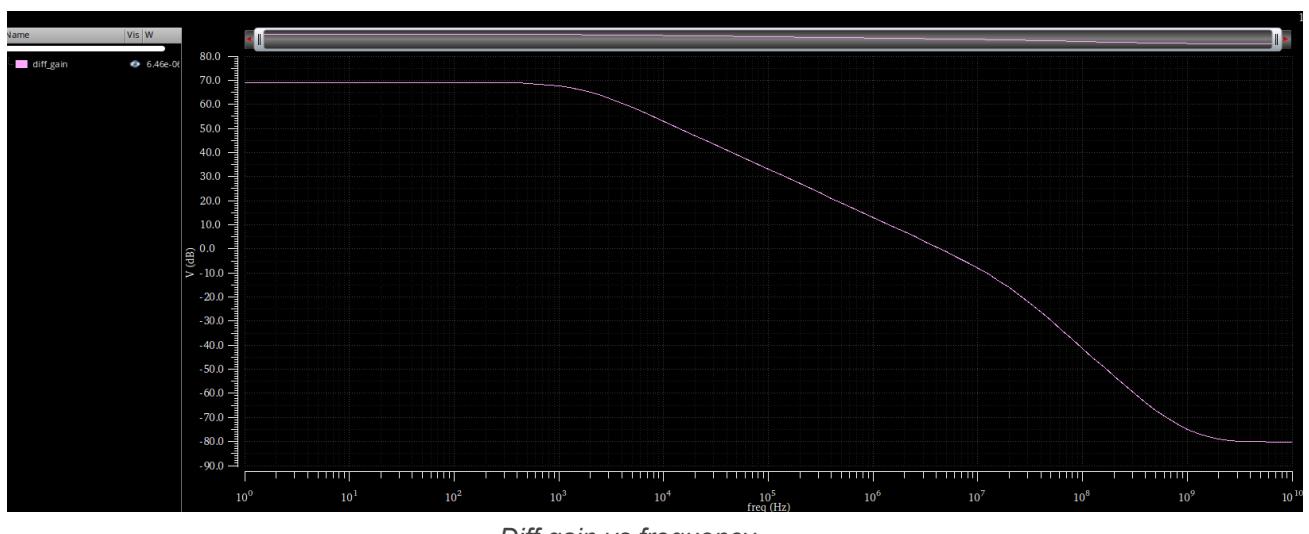
→ Diff small signal ccs:

- Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).

Set VIDAC = 1 and VICMAC = 0.

Use VICM = VDD/3.

Plot diff gain (in dB) vs frequency.



Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI_labs:two_stg_ota_tb:1	Ao	3.08k			
ITI_labs:two_stg_ota_tb:1	Ao_dB	69.77			
ITI_labs:two_stg_ota_tb:1	BW	1.895k			
ITI_labs:two_stg_ota_tb:1	UGF	5.685M			
ITI_labs:two_stg_ota_tb:1	GBW	5.85M			

Required calculations

- Compare simulation results with hand calculations in a table.

Quantity	Simulated	Calculated
A_{vd}	69.43dB	69.8dB
BW	1.895k	1.96k
$GBW \approx UGF$	5.85M	6.06M

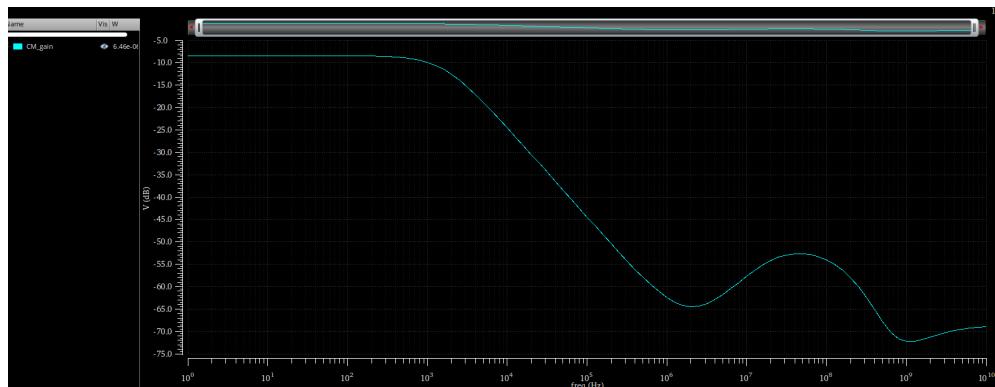
→ CM small signal ccs:

- Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).

Set VICMAC = 1 and VIDAC = 0.

Use VICM = VDD/3.

Plot CM gain in dB vs frequency.



CM gain vs frequency

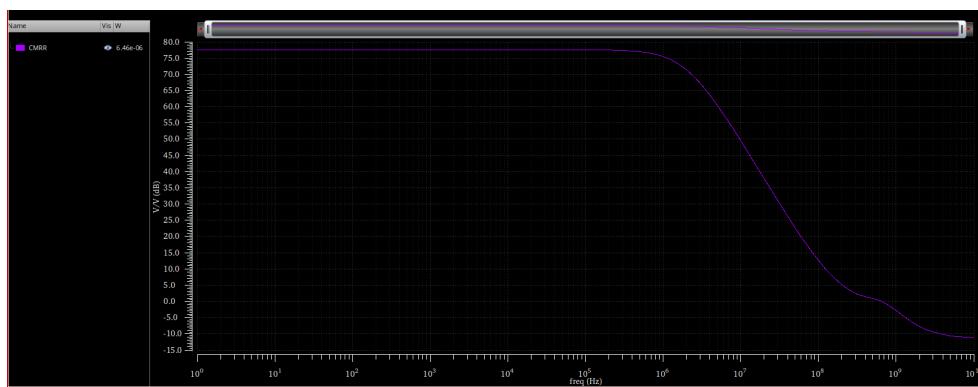
- Compare simulation results with hand calculations in a table.

Quantity	Simulated	Calculated
A_{vCM}	- 9.02dB	- 8.81dB

→ (Optional) CMRR:

- Use $VICM = VDD/3$.

Plot CMRR in dB vs frequency.



CMRR vs frequency

- Compare simulation results with hand calculations in a table.

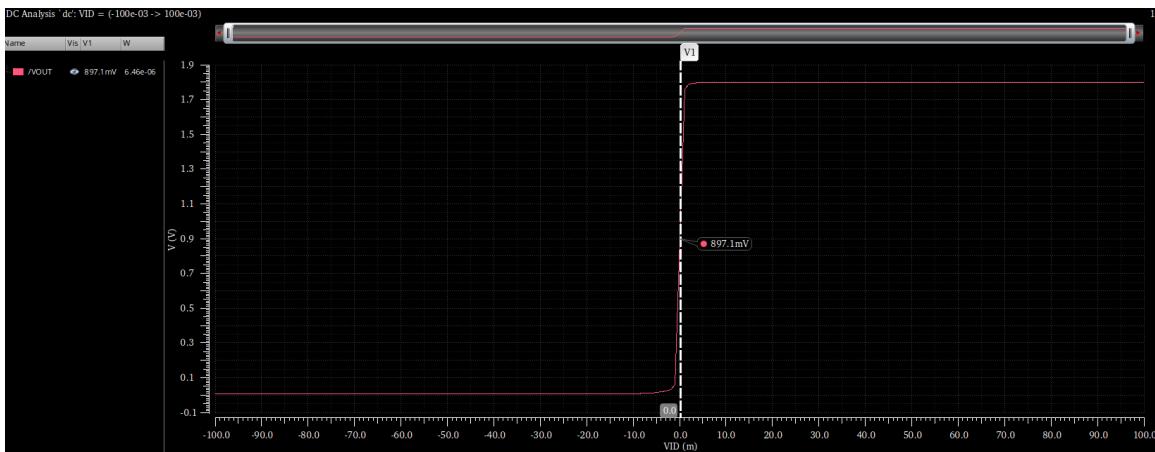
Quantity	Simulated	Calculated
CMRR	78.8dB	78.6dB

→ (Optional) Diff large signal ccs:

- Use $VICM = VDD/3$.

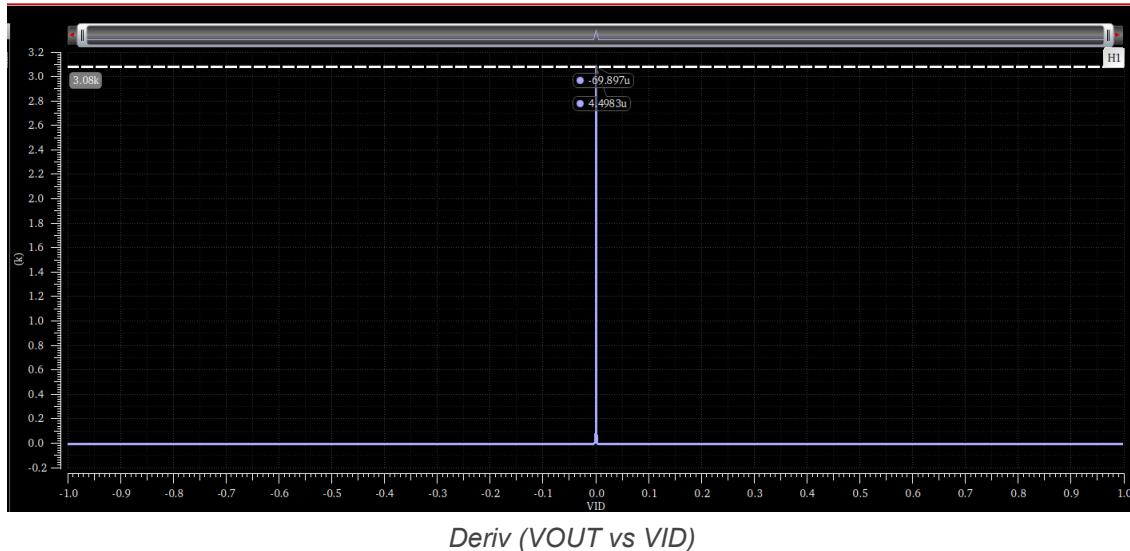
Use DC sweep (not parametric sweep) VID = -0.1:1m:0.1.
You must use a small step because the gain region is very small (steep slope).

From the plot, what is the value of Vout at VID = 0.
Compare it with the value you obtained in DC OP.



VOUT vs VID with vertical cursor added @ VID = 0

- It is exactly the same as VOUT obtained in OP analysis.
- Plot the derivative of VOUT vs VID. Is the peak less than the value of Avd obtained from ac analysis? Why?



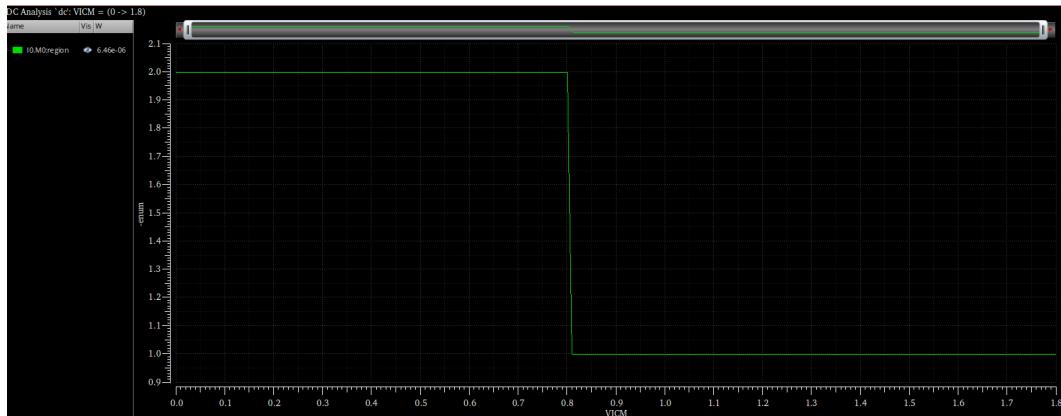
$$\text{Peak} = 3080 = 69.77 \text{dB} \approx A_{vd} = 69.43 \text{dB}.$$

- The peak of the deriv of large signal diff. Ccs. is exactly the same as the gain obtained from small signal analysis.

→ CM large signal ccs (region vs VICM):

Use DC sweep (not parametric sweep) VICM = 0:10m:VDD.

Plot “region” OP parameter vs VICM for the input pair and the tail current source (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown).



Find the CM input range (CMIR). Compare with hand analysis in a table.



Region of tcs and i/p pair vs VICM

- CMIR is located where both tcs and i/p pair are in sat (i.e. region 2), thus $0 < CMIR < 0.8V$.

Quantity	Simulated	Calculated
$CMIR$	$0 < CMIR < 0.8V$	$193.6m < CMIR < 791m$

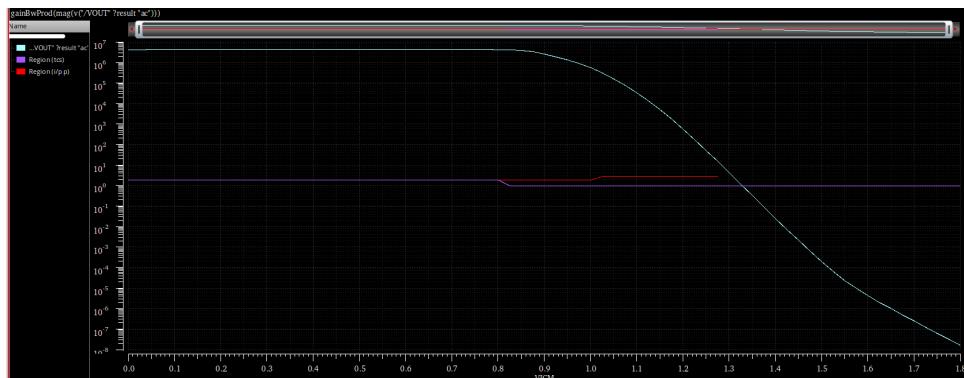
→ (Optional) CM large signal ccs (GBW vs VICM):

- Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).

Set VIDAC = 1 and VICMAC = 0.

Use parametric sweep (not DC sweep) VICM = 0:25m:VDD.

Plot GBW vs VICM. Plot the results overlaid on the results of the previous method (region parameter).

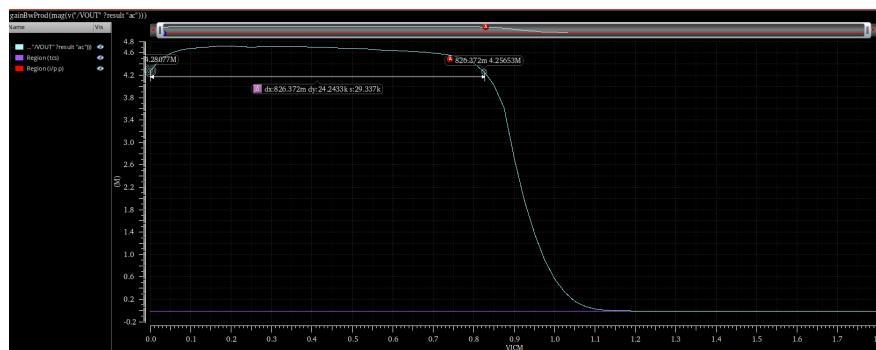


GBW, Region (tcs) and Region (i/p p) vs VICM

- Annotate the CM input range. Calculate the input range as the range over which the GBW is within 90% of the max GBW, i.e., 10% reduction in GBW.

Expression	Value
1 <code>ymax(gainBwPr...</code>	<code>4.725 E6</code>

Maximum value of GBW, 90% (GBW max) = 4.2525M

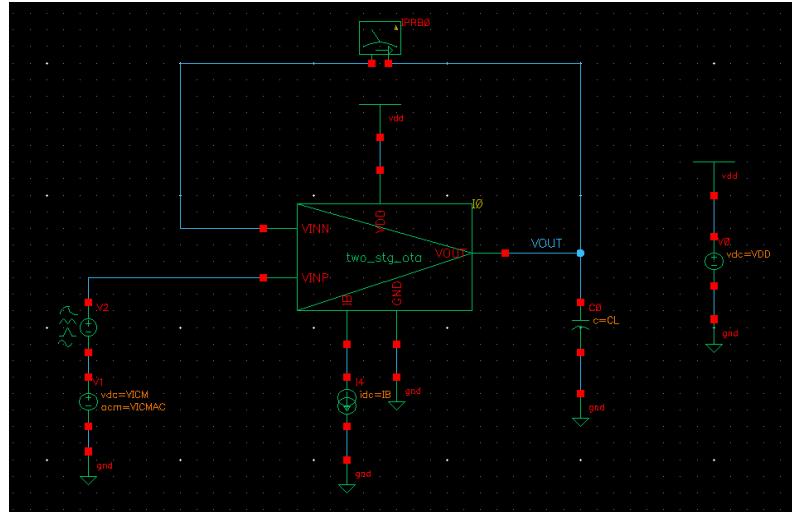


CMIR within which $GBW > 90\% (GBW \text{ max})$

Required CMIR $\in [0, 830mV]$.

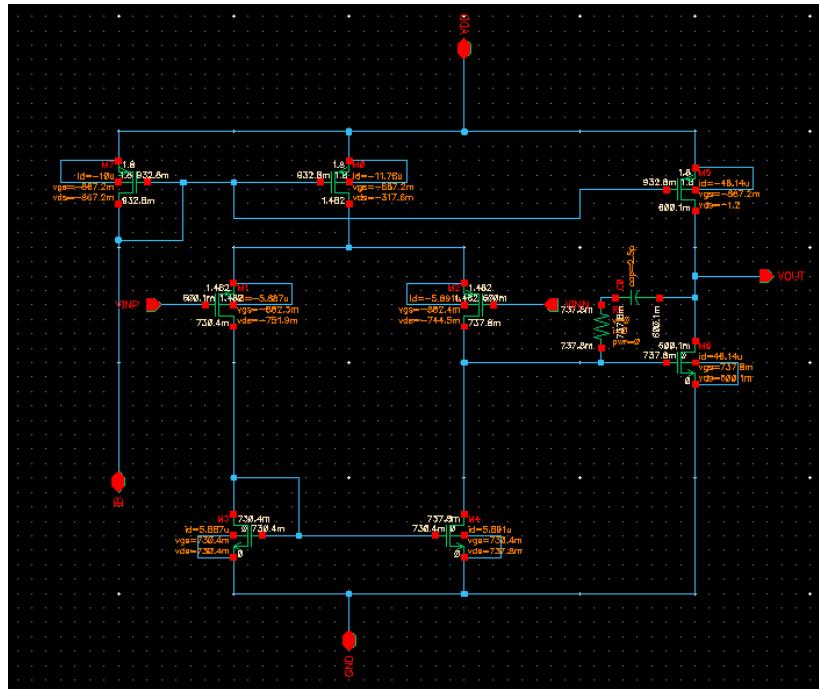
Part 4: Closed-Loop OTA Simulation

- Create a new testbench with the OTA connected in a unity gain buffer feedback configuration (the shown schematic is from the 5T OTA lab). Place a current probe (iprobe) or a zero voltage source in the feedback loop.



Required testbench

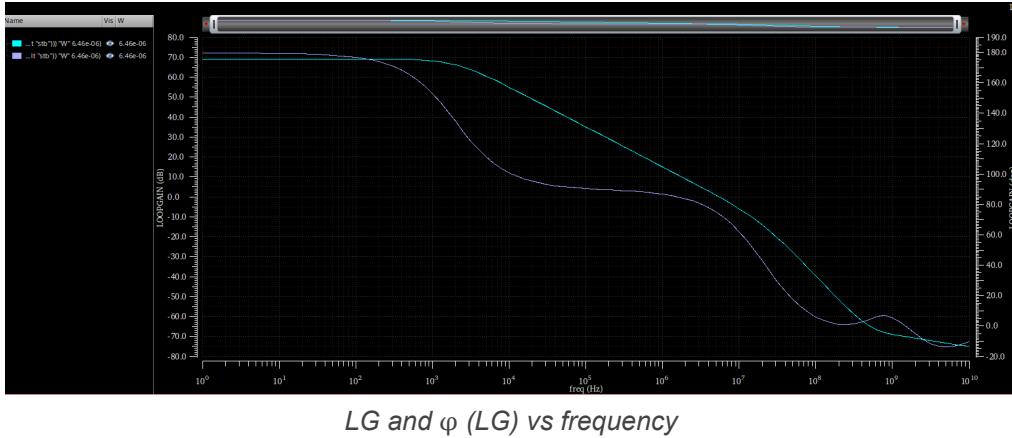
- Report the following:
 - Schematic of the OTA and the bias circuit with DC OP point clearly annotated in unity gain buffer configuration.
 - Use $VICM = VDD/3$.



DC OP annotated

- Are the DC voltages at the input terminals of the op-amp exactly equal? Why?

- They are nearly exactly equal, as the difference between them is the error voltage which a feedback loop by nature tries to minimize as much as possible.
 - Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?
 - It is almost the same as the i/p is the same as the OL case, which was 0.6V (i.e. the difference between the two inputs is very small (error elimination property of feedback loops), which means that the inputs is almost the same (0.6v), a case similar to what happened in OL simulation).
 - Is the current (and gm) in the input pair exactly equal? Why?
 - There is a slight difference due to mismatch.
- Loop gain:
- Use STB analysis (1Hz:10Gz, logarithmic, 10 points/decade) in unity gain buffer configuration.
- Use $V_{ICM} = VDD/3$.
- Plot loop gain in dB and phase vs frequency.



- Compare DC gain, f_u , and GBW with those obtained from open-loop simulation. Comment.

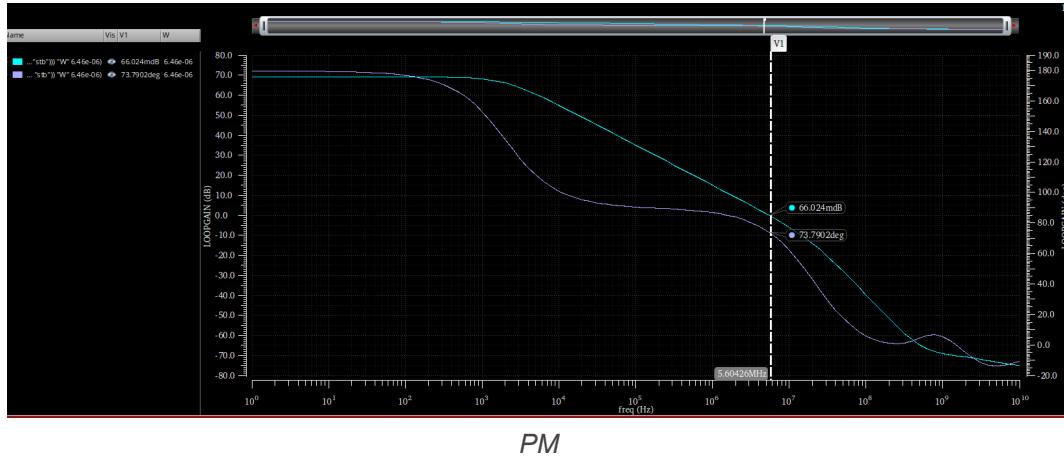
Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI_labs:two_stg_ota_tb:1	LG0_dB	69.42			
ITI_labs:two_stg_ota_tb:1	LG_UGF	5.684M			
ITI_labs:two_stg_ota_tb:1	LG_GBW	5.836M			

DC gain, UGF and GBW obtained from stb analysis

Quantity	OL	LG
DC gain	69.43dB	69.422dB
UGF	5.685M	5.684M
GBW	5.85M	5.836M

- The values are very close to each other, as $\beta = 1$.

Report PM. Compare with hand calculations. Comment.



PM

$$PM \approx 90 - \arctan\left(\frac{GX}{\omega_{p1}}\right), GX = 4.54M, \omega_{p1} = 1.869k \Rightarrow PM \approx 90$$

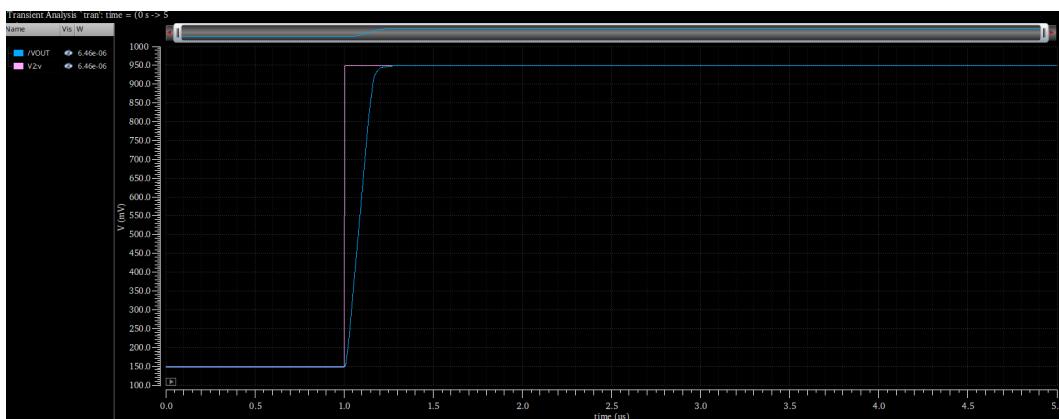
- There is slightly large deviation between sim and hand analysis results due to the fact that the equation used in hand analysis is approximate.
- The PM spec is achieved.

- Compare simulation results with hand calculations in a table.

Quantity	Simulated	Calculated
PM	73.79	90

→ Slew rate:

- Apply a step input with the following parameters (delay = 1us, initial value = CMIR-low + 50mV, final value = CMIR-high – 50mV, rise time = 1ns, period = 1s, width = 1s). Note that we want a single step input, which is why we selected very large period and width for the pulse.
Run transient analysis (stop = 5us and step = 0.1ns).
Report Vin and Vout overlaid.



VOUT and VIN vs time overlaid

Expression	Value
1 slewRate(value(...))	5.047E6

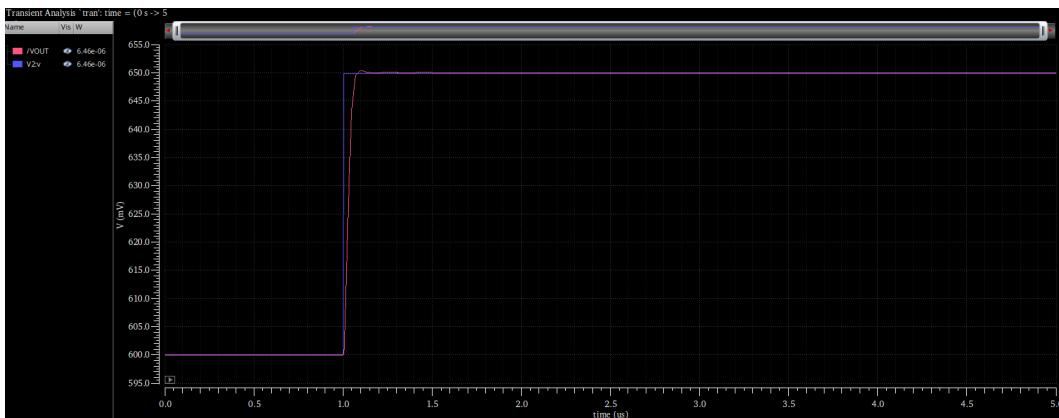
SR

- Compare simulation results with hand calculations in a table.

<i>Quantity</i>	<i>Simulated</i>	<i>Calculated</i>
SR	$5.047V/\mu s$	$\approx \frac{I_{B1}}{C_1 + C_c} \approx 4.7V/\mu s$

→ Settling time:

- Apply a small signal step input with the following parameters (delay = 1us, initial value = VDD/3, final value = VDD/3 + 5mV, rise time = 1ns, period = 1s, width = 1s). Note that we want a single step input, which is why we selected very large period and width for the pulse. Note that we apply a small signal pulse (5mV step) to measure the small signal settling time.



VOUT and VIN vs time overlaid

- Calculate the output rise time from simulation.

W	riseTime... "time")
1 6.460E-6	41.64E-9

Rise time

- Compare simulation results with hand calculations in a table.

<i>Quantity</i>	<i>Simulated</i>	<i>Calculated</i>
t_r	41. 64ns	31. 8ns

- Do you see any ringing? Why?
- A very slight peak is noticed due to the fact that the PM is less than 76 degrees, which corresponds to underdamped response.