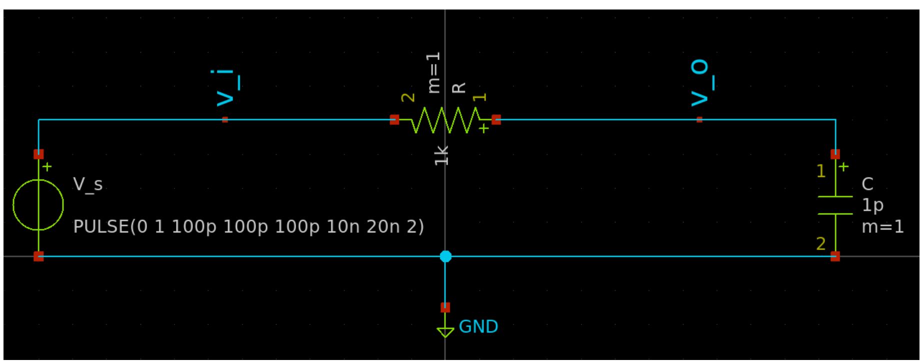
CMOS AIC design - ITI - Lab 1

PART 1: Low Pass Filter Simulation (LPF)

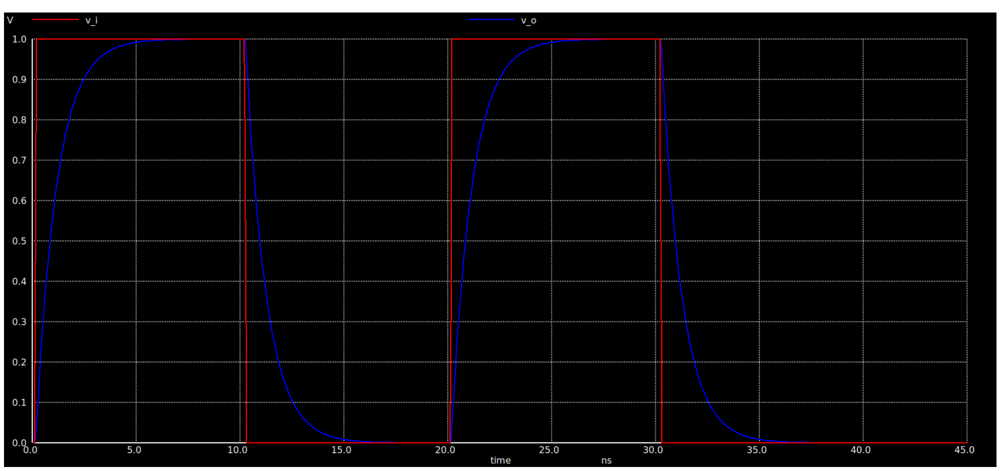
1. Transient Analysis

- Design a first order low pass filter that has $R = 1k\Omega$ and 1ns time constant. Apply a square wave input with $T_{high} = Pulse\,Width = 10ns,\ T_{clk} = Period = 20ns$ and $T_{rise} = T_{fall} = 100ps$.
    - $\tau = 1n = RC = 1k \times C \rightarrow C = 1pF$.



Required testbench

- Report transient analysis results for two periods.



Transient analysis results

- Calculate rise and fall time (10% to 90%).

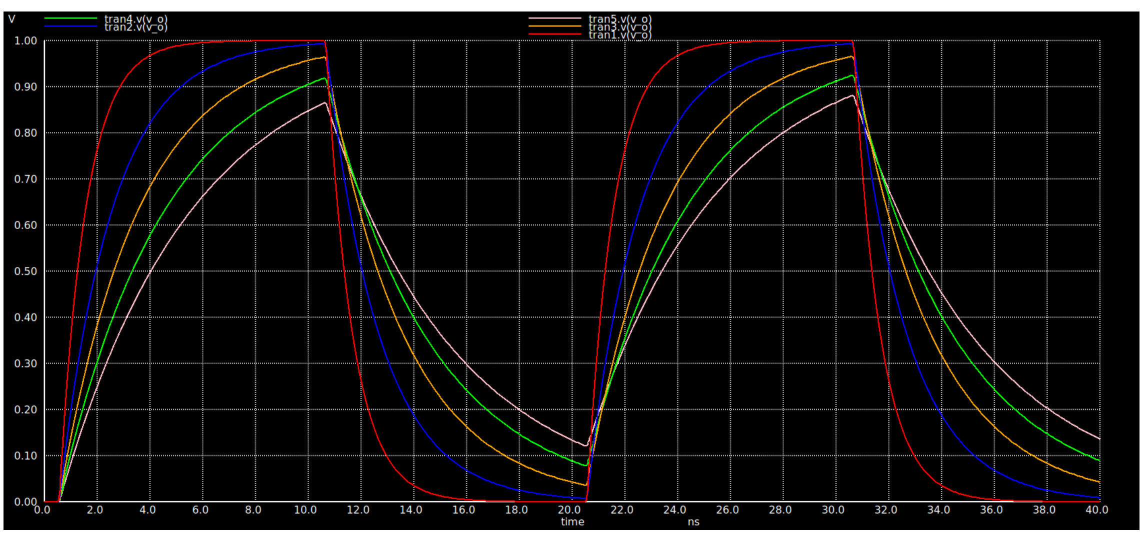
```
No. of Data Rows : 436
tr10                 =  2.558679e-10
tr90                 =  2.452309e-09
trise = 2.196441e-09
tf10                 =  1.255229e-08
tf90                 =  1.035577e-08
tfall = -2.19652e-09
```

Rise and fall time calculation results

- Compare simulation with analytical results in a table.

Simulation results	*Analytical results*
$t_r = t_f = 2.196ns$	$t_r = t_f = 2.2\tau = 2.2 \times 1n = 2.2ns$

- Do parametric sweep for $R = 1:1:5k\Omega$. Report overlaid results. Comment on the results.



Parametric sweep plots

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
v_o                                          0
v_i                                          0
v_s#branch                                   0


No. of Data Rows : 434
tr10                =  6.555992e-10
tr90                =  2.851133e-09
trise = 2.195534e-09
Reset re-loads circuit ** sch_path: /home/tare/iti_labs/lpf.sch
```

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
v_o                                          0
v_i                                          0
v_s#branch                                   0


No. of Data Rows : 434
tr10                =  7.605891e-10
tr90                =  5.154053e-09
trise = 4.393464e-09
Reset re-loads circuit ** sch_path: /home/tare/iti_labs/lpf.sch
```

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
v_o                                          0
v_i                                          0
v_s#branch                                   0


No. of Data Rows : 433
tr10                =  8.658120e-10
tr90                =  7.456885e-09
trise = 6.591073e-09
Reset re-loads circuit ** sch_path: /home/tare/iti_labs/lpf.sch
```

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
v_o                                          0
v_i                                          0
v_s#branch                                   0


No. of Data Rows : 433
tr10                =  9.712214e-10
tr90                =  9.759747e-09
trise = 8.788526e-09
Reset re-loads circuit ** sch_path: /home/tare/iti_labs/lpf.sch
```

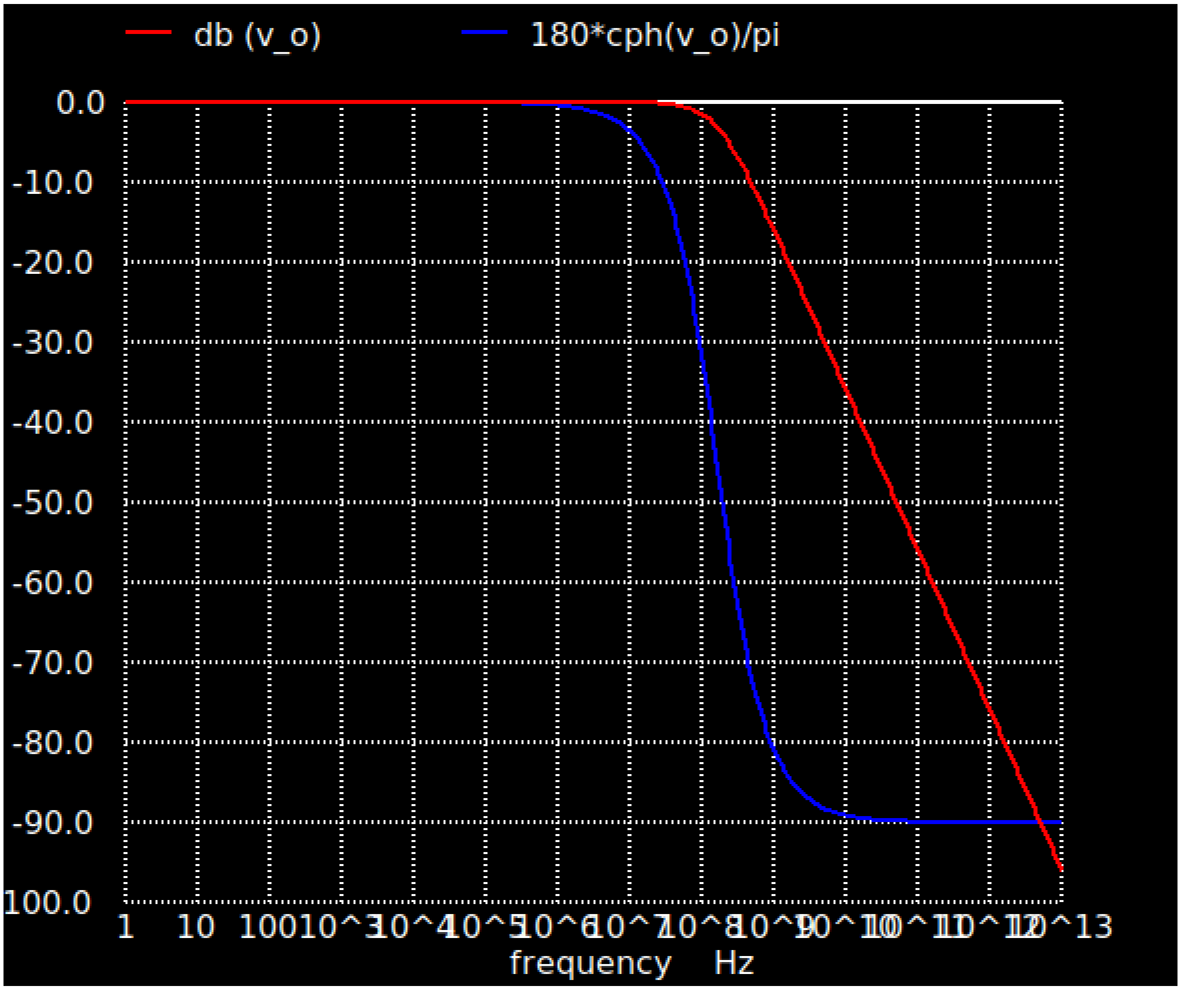
```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
v_o                                          0
v_i                                          0
v_s#branch                                   0


No. of Data Rows : 432
tr10                =  1.076581e-09

Error: measure  tr90  when(WHEN) : out of interval
 meas tran tr90 when v_o=0.9 rise=1 failed!

Warning from checkvalid: vector tr90 is not available or has zero length.
Error: RHS "tr90-tr10" invalid
Warning from checkvalid: vector trise is not available or has zero length.
Reset re-loads circuit ** sch_path: /home/tare/iti_labs/lpf.sch
```

Overlaid results

- Comment: As R increases, t_r decreases. They are linearly related.

2. AC Analysis

- Report Bode Plot (magnitude and phase) for the previous LPF. Also Calculate DC gain and 3dB bandwidth.



Bode plot

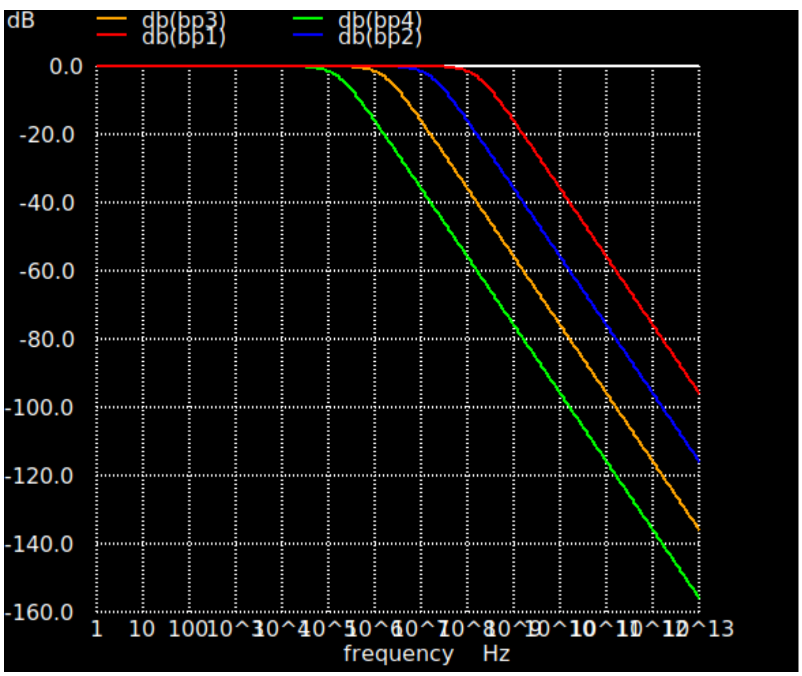
```
No. of Data Rows : 261
peak               =  1.000000e+00 at=  1.584893e+00
f3db               =  1.592255e+08
ngspice 1 ->
```

Required calculations

- Compare simulation with analytical results in a table.

Simulation results	*Analytical results*
DC gain = 1 3dB BW = 159 GHz	$H(s) = \frac{1}{RCs+1}$ General form of 1st order system: $H(s) = \frac{K}{\tau s+1}$ When compared to each other, DC gain = K = 1 3dB BW = $\frac{1}{2\pi RC} = \frac{1}{2\pi\times1k\times1p} = 159GHz$

- Do parametric sweep for $R = 1,\ 10,\ 100,\ 1000k\Omega$. Report overlaid results. Comment on the results.



Parametric sweep results

```
No. of Data Rows : 261
peak                = 1.000000e+00 at= 1.584893e+00
f3db                = 1.592255e+08
Reset re-loads circuit ** sch_path: /home/tare/iti_labs/lpf.sch

Circuit: ** sch_path: /home/tare/iti_labs/lpf.sch

binary raw file "RC_CKT.raw"
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 261
peak                = 1.000000e+00 at= 1.000000e+00
f3db                = 1.592255e+07
Reset re-loads circuit ** sch_path: /home/tare/iti_labs/lpf.sch

Circuit: ** sch_path: /home/tare/iti_labs/lpf.sch

binary raw file "RC_CKT.raw"
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 261
peak                = 1.000000e+00 at= 1.000000e+00
f3db                = 1.592255e+06
Reset re-loads circuit ** sch_path: /home/tare/iti_labs/lpf.sch

Circuit: ** sch_path: /home/tare/iti_labs/lpf.sch

binary raw file "RC_CKT.raw"
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 261
peak                = 1.000000e+00 at= 1.000000e+00
f3db                = 1.592255e+05
Reset re-loads circuit ** sch_path: /home/tare/iti_labs/lpf.sch

Circuit: ** sch_path: /home/tare/iti_labs/lpf.sch
```

Required calculations

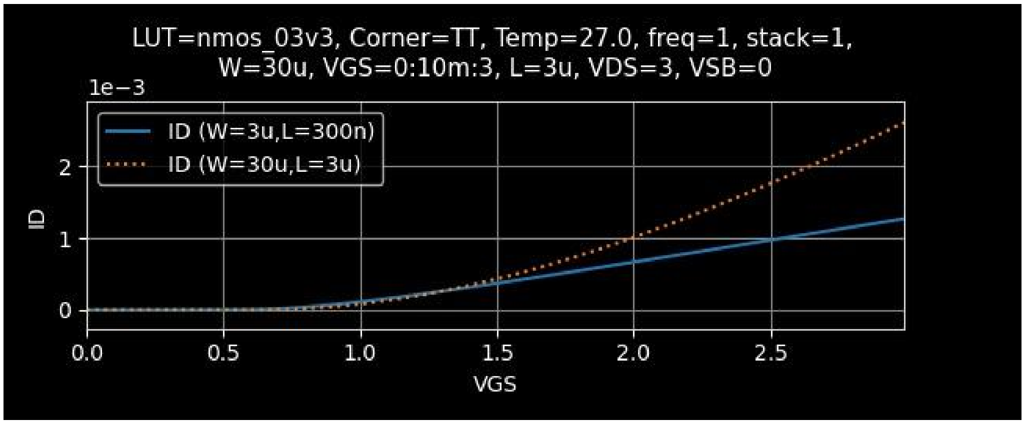
- Comment: As R increases, BW decreases. They are inversely related (i.e. $BW = \frac{1}{\tau} \alpha \frac{1}{R}$.

Part 2: MOSFET Characteristics

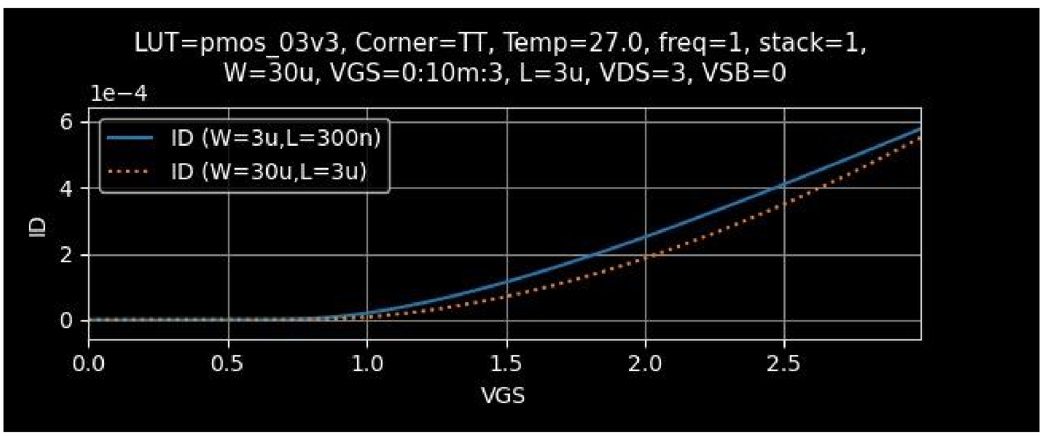
1. ID vs VGS

- Plot $I_D - V_{GS}$ characteristics for NMOS and PMOS devices. Set $V_{DS} = V_{DD}$, and $V_{GS} = 0{:}\,10m{:}\,V_{DD}$ Use $V_{DD} = 3V$. Plot the results overlaid for the following:

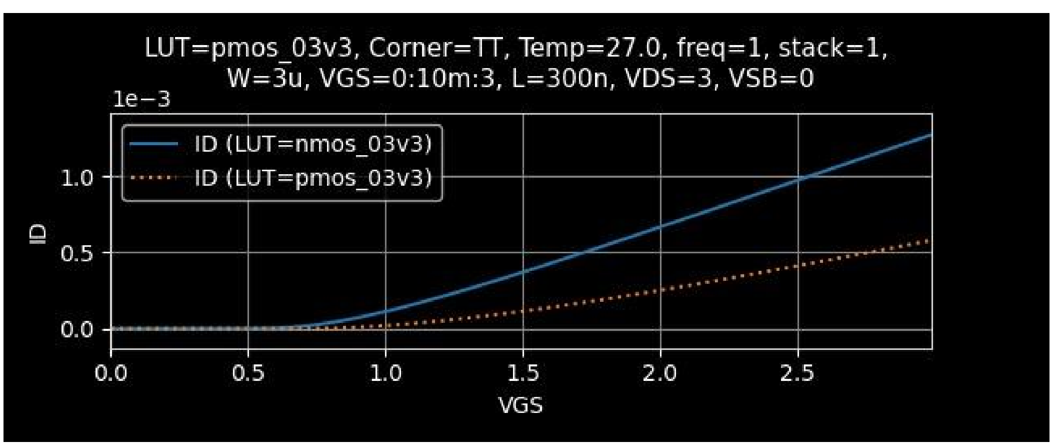
➔ Short channel device: $W = 3um$ and $L = 300nm$.
➔ Long channel device: $W = 30um$ and $L = 3um$.



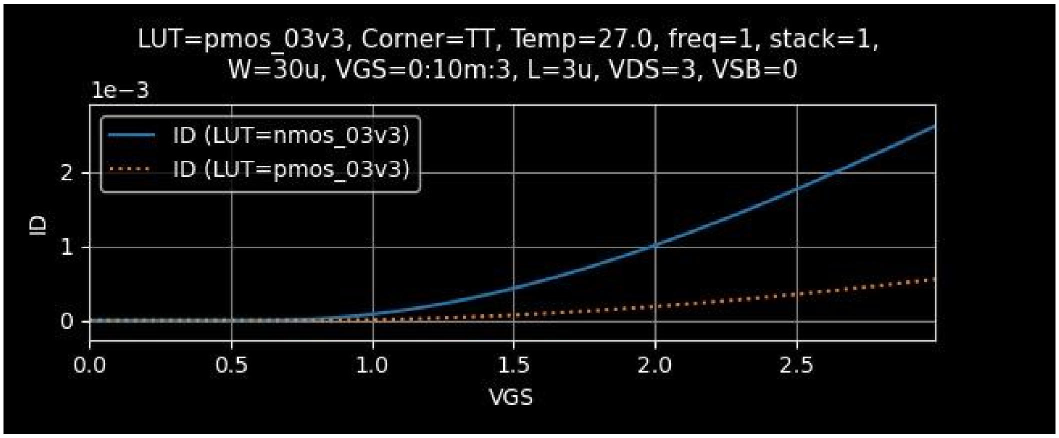
*ID VS VGS for short channel and long channel **NMOS***



*ID VS VGS for short channel and long channel **PMOS***



*ID VS VGS for **short** channel NMOS and PMOS*



*ID VS VGS for **long** channel NMOS and PMOS*

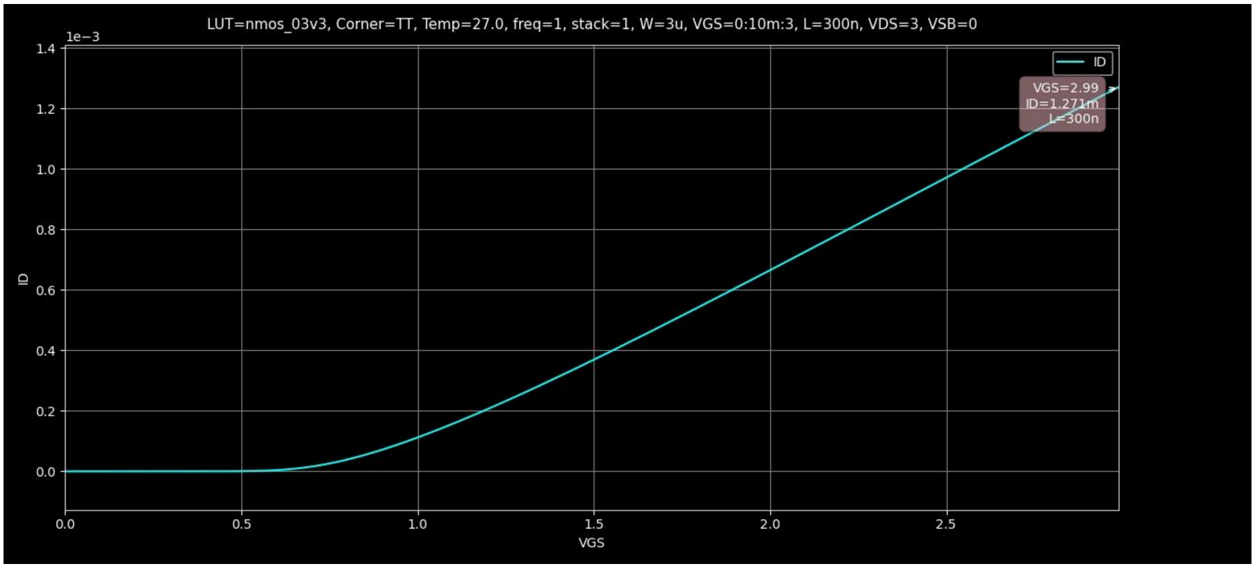
- Comment on the differences between short channel and long channel results.
    - ➔ Which one has higher current? Why?
    - ➔ Is the relation linear or quadratic? Why?

    - It can be noticed from the plots that the current of long channel devices is higher than that of short channel ones. Long channel devices have more current than short channel ones due to velocity saturation that has a higher effect on short channel devices.
    - In case of short channel, the relation is quadratic until V_{GS} reaches a value of $V_{TH} + V_{DS,sat}$, then it turns into a linear relation due to the strong effect of velocity saturation, while in the case of long channel, the relation is quadratic across all the values of V_{GS} that is higher than the threshold, since the effect of velocity saturation is much weaker.

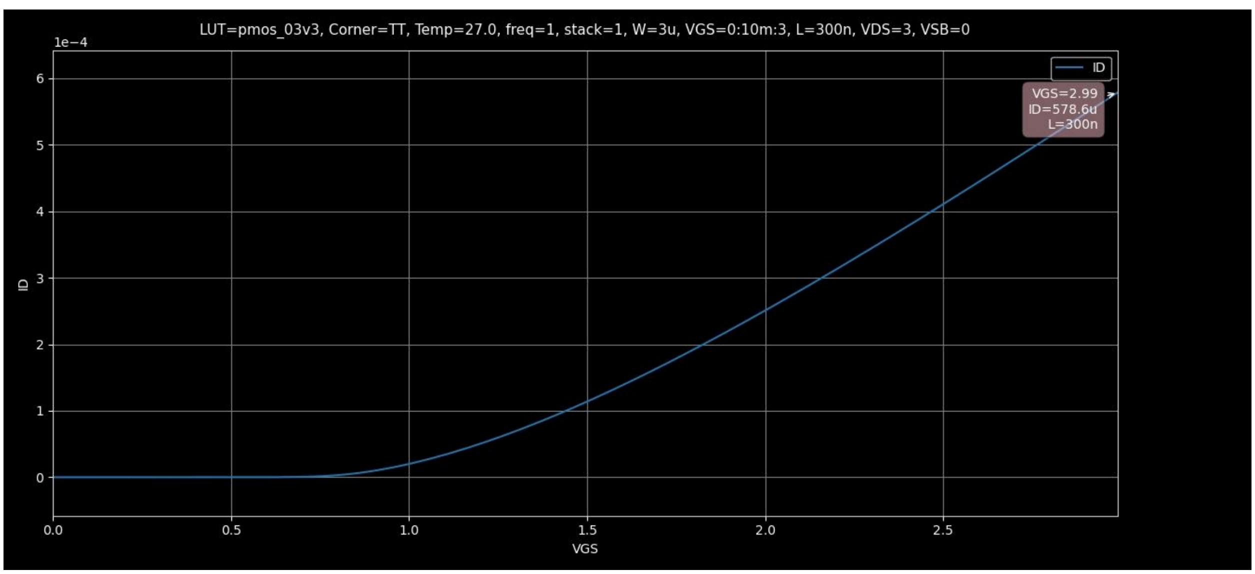
- Comment on the differences between NMOS and PMOS.
    - ➔ Which one has higher current? Why?
    - ➔ What is the ratio between NMOS and PMOS currents at VGS = VDD?

➔ Which one is more affected by short channel effects?

- NMOS has higher current than PMOS due to the higher carrier mobility.

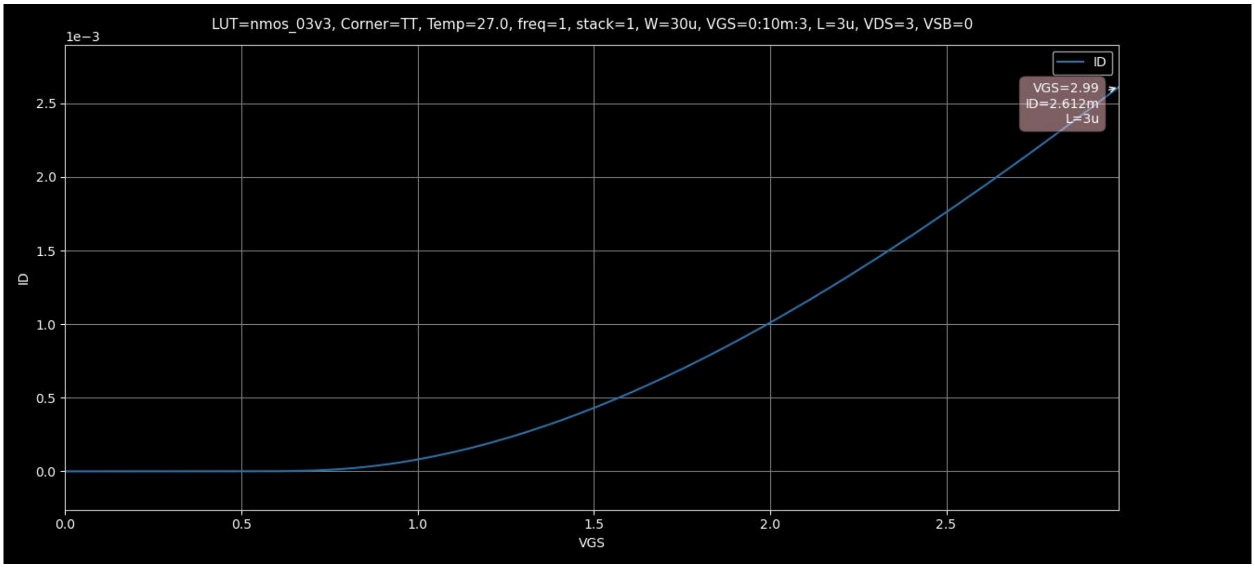


*ID @VGS = VDD for **short channel NMOS***

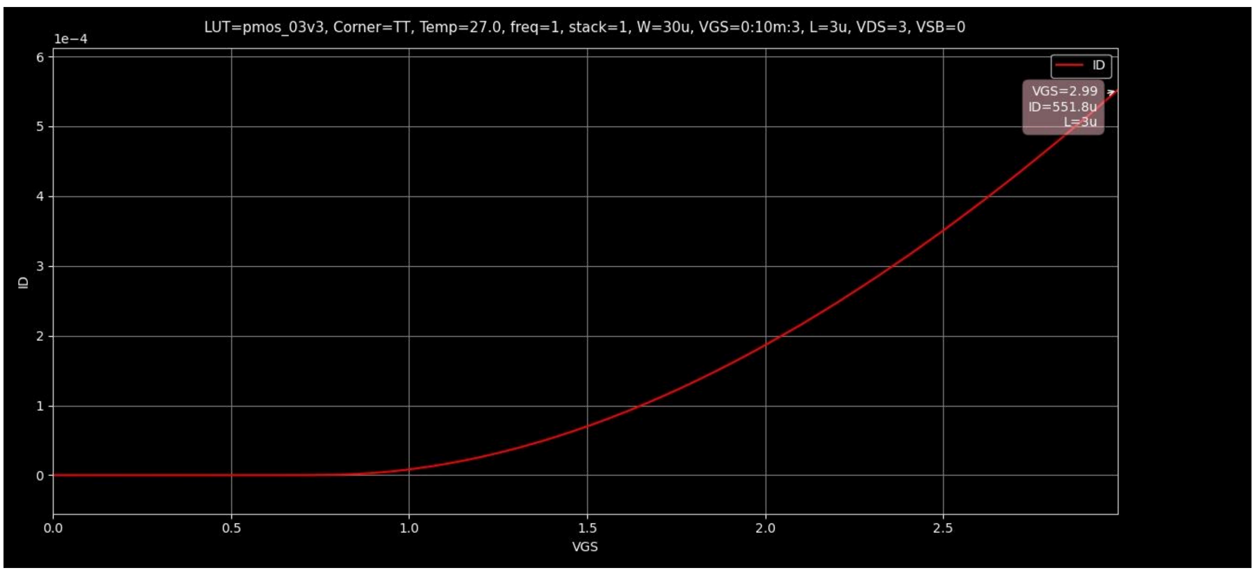


*ID @VGS = VDD for **short channel PMOS***

- $\frac{I_{DN}}{I_{DP}} = \frac{1.27m}{578.6u} \approx 2.2.$



ID @VGS = VDD for ***long channel NMOS***

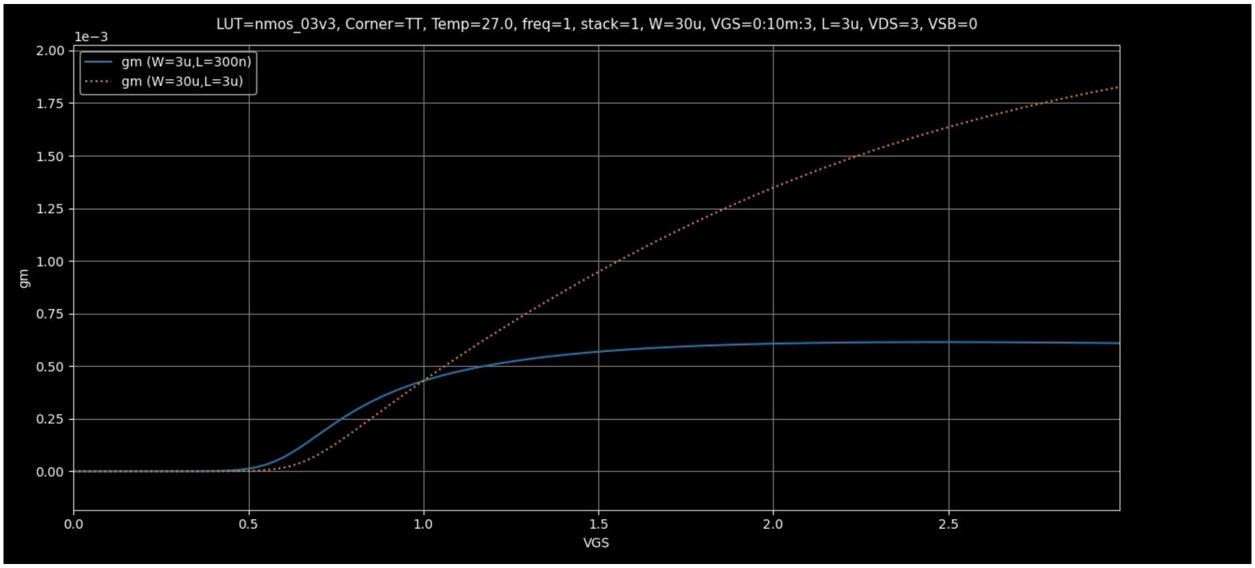


ID @VGS = VDD for ***long channel PMOS***

- $\frac{I_{DN}}{I_{DP}} = \frac{2.61m}{551.8u} \approx 4.7.$
- NMOS devices are more affected by short channel effects due to the higher mobility that leads to reaching velocity saturation more easily.

2. g_m vs VDS

- Plot g_m vs V_{GS} for NMOS device. Set $V_{DS} = V_{DD}$, and $V_{GS} = 0: 10m: V_{DD}$. Plot the results overlaid for the following:
  - ➔ Short channel device: $W = 3um$ and $L = 300nm$.
  - ➔ Long channel device: $W = 30um$ and $L = 3um$.



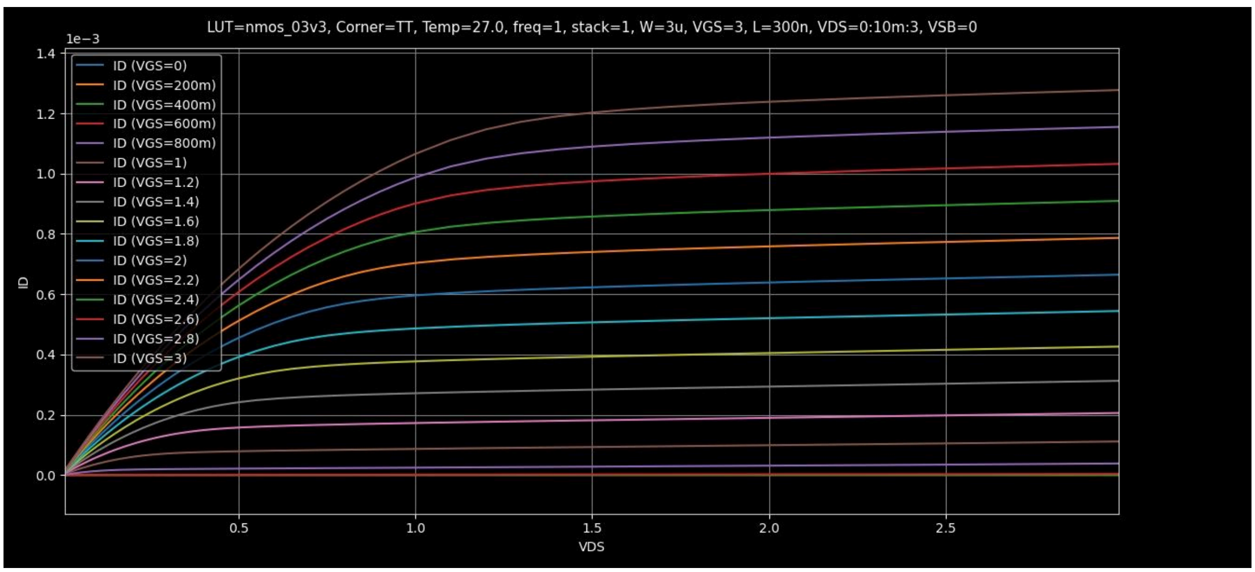
gm VS VGS plot for both long channel and short channel NMOS devices

- Comment on the differences between short channel and long channel results.
  - ➔ Does g_m increase linearly? Why?
  - ➔ Does g_m saturate? Why?
  - g_m is higher for long channel devices.
  - Yes, since g_m is the derivative of $I_D(V_{GS})$ plot, which is a quadratic relation in case of long channel. For short channel devices, the $I_D(V_{GS})$ plot is quadratic until V_{GS} reaches a value of $V_{TH} + V_{DS,sat}$, then it turns into a linear relation, meaning that $g_m(V_{GS})$ is a linear plot until

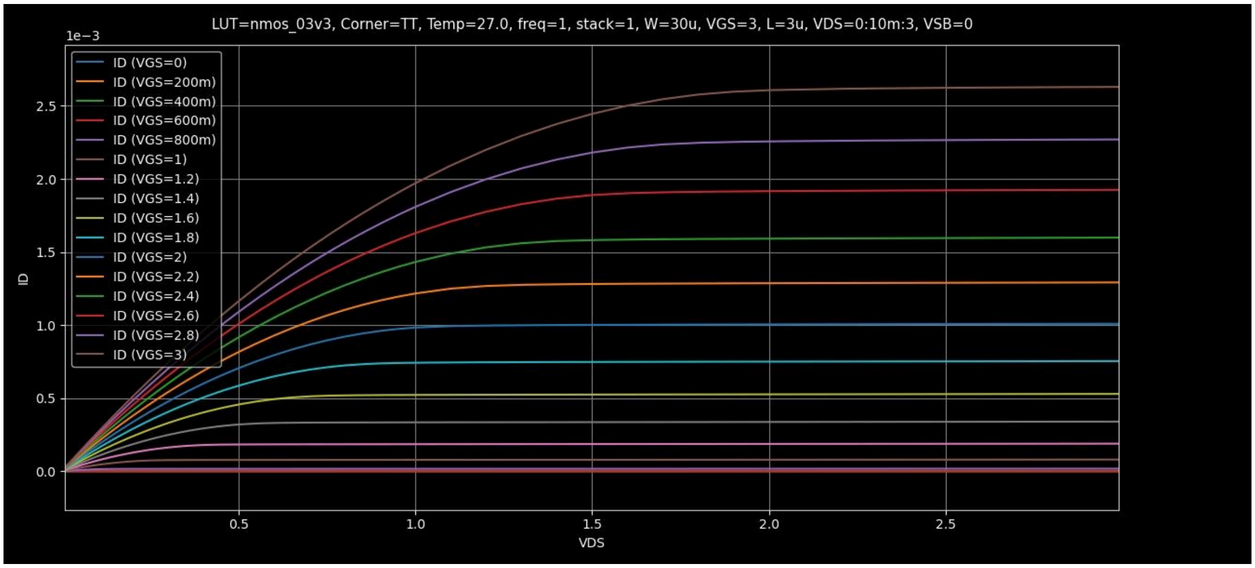
$V_{TH} + V_{DS,sat}$, then it turns into a constant, which justifies the saturation noticed in the red plot.

3. ID vs VDS

- Plot $I_D - V_{DS}$ characteristics for NMOS device. Set $V_{DS} = 0{:}\,10m{:}\,V_{DD}$, and $V_{GS} = 0{:}\,0.2{:}\,V_{DD}$ (nested sweep). Plot the results overlaid for the following:
  - ➔ Short channel device: $W = 3um$ and $L = 300nm$.
  - ➔ Long channel device: $W = 30um$ and $L = 3um$.



*ID VS VDS plot for **short** channel NMOS*



*ID VS VDS plot for **long** channel NMOS*

- Comment on the differences between short channel and long channel results.
  - ➔ Which one has higher current? Why?
  - ➔ Which one has higher slope in the saturation region? Why?

  - It can be concluded from the CCs that long channel devices have more current than short channel ones due to *the resultant effect of short channel effects* (e.g. DIBL, velocity saturation, …)*,* which leads generally to lower current levels.
  - Short channel devices have higher slope, since $\lambda \; \alpha \; \frac{1}{L}$, meaning that the shorter the channel, the higher the channel length modulation coefficient, and the less the Early voltage, which leads to a higher slope (i.e. less r_o).