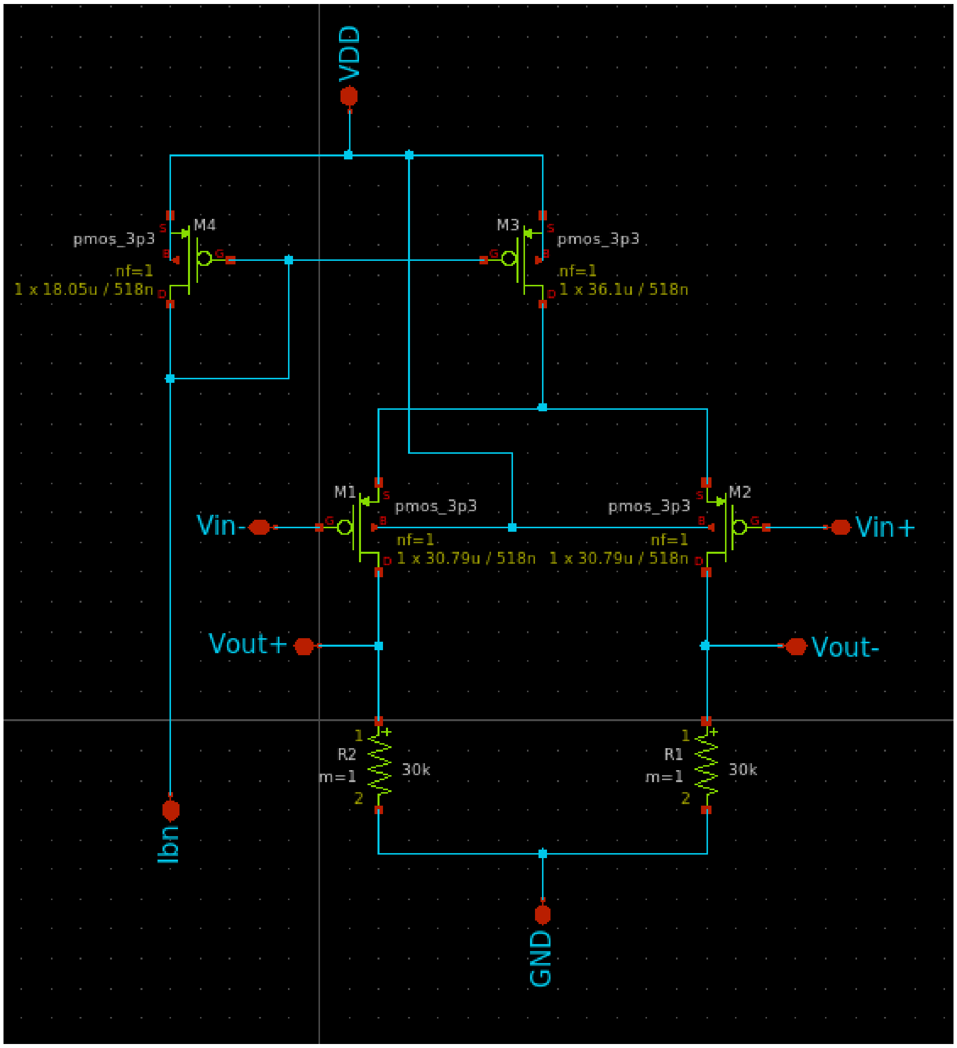
CMOS AIC design - ITI - Lab 6

Part 1: Differential Amplifier Design



Required schematic

- Choose R_D to meet the CM output level spec.

$$R_D = \frac{V_{DD}/3}{I_{SS}/2} = 30k\Omega.$$

- Choose V^* to meet the differential gain spec.

$$V^* = \frac{1.82V_{RD}}{|A_v|} \approx 135mV.$$

- Assume we will set V_{DS} of the tail current source to $300mV$ to allow more output swing. Report the input pair sizing using SA.

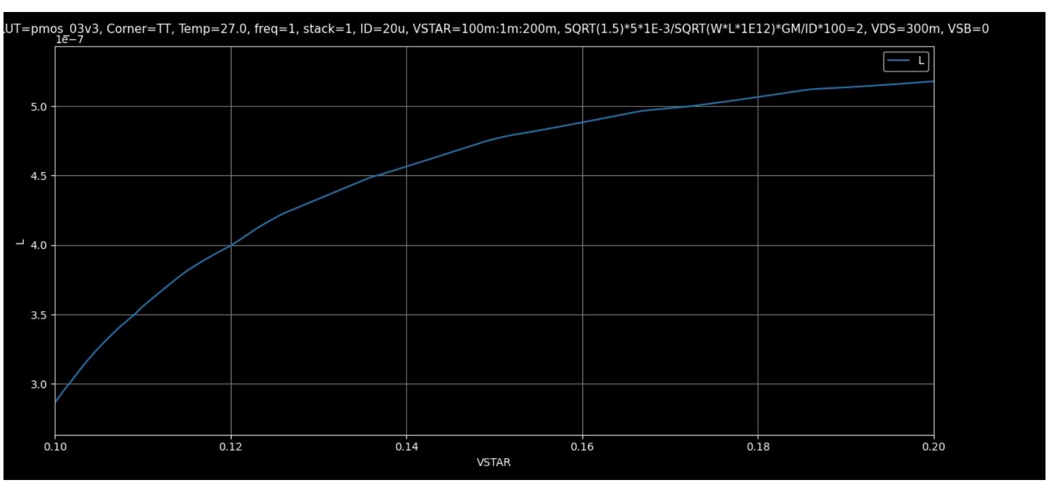
L	350n
W	30.79u

i/p pair sizing

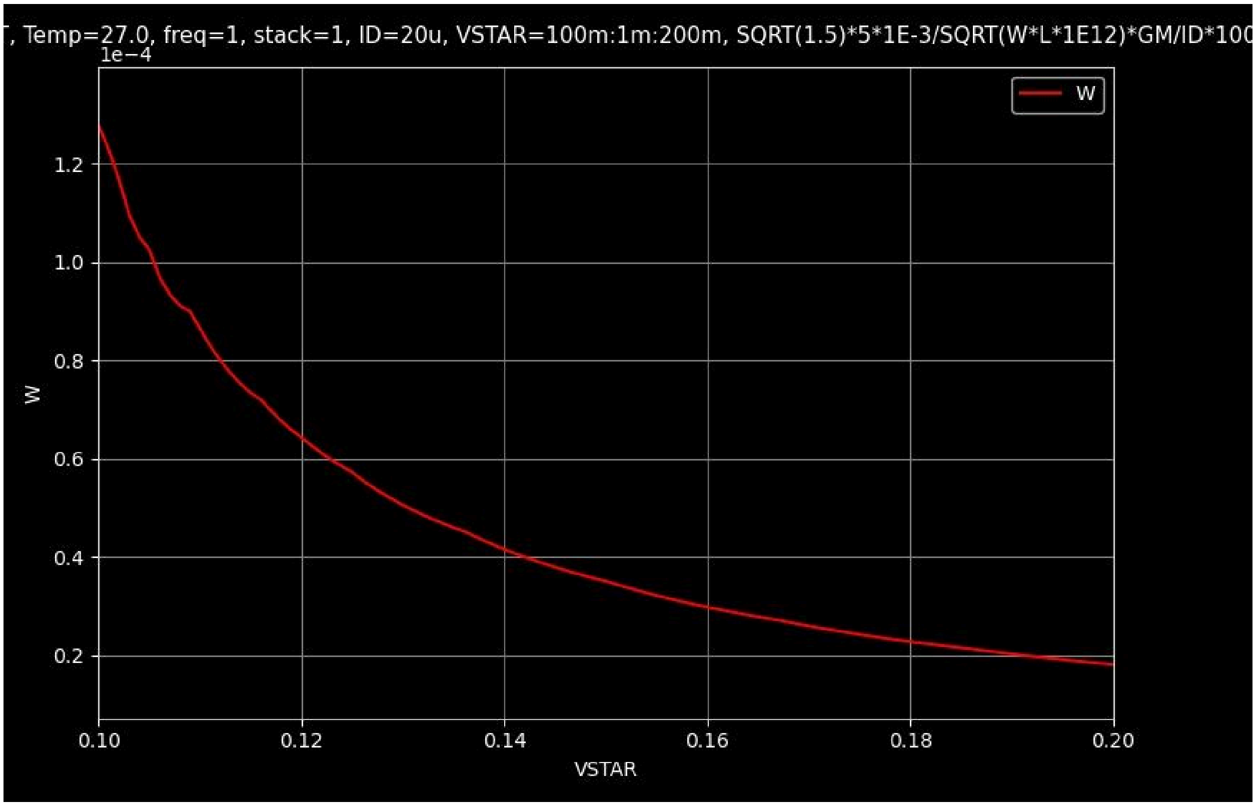
- Given the above assumption for V_{DS} of the tail current source, calculate the required CM input level.

$$V_{i,CM} = V_{DD} - V_{GS,i} - V_{DS,tcs} = 0.56V$$
$$Data\ from\ ADT\ *$$

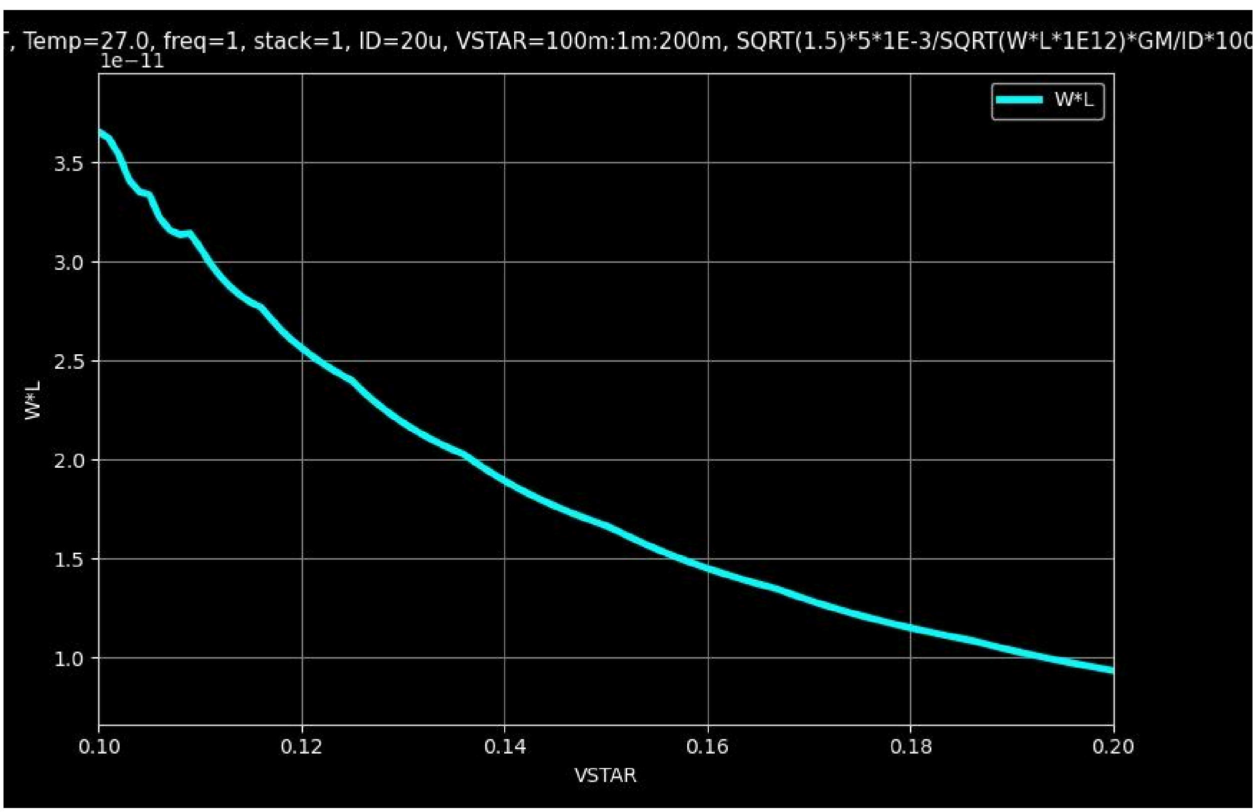
- Use SA to plot the sizing at a constant $\sigma I_{out}/I_{out}$.



*L vs V**

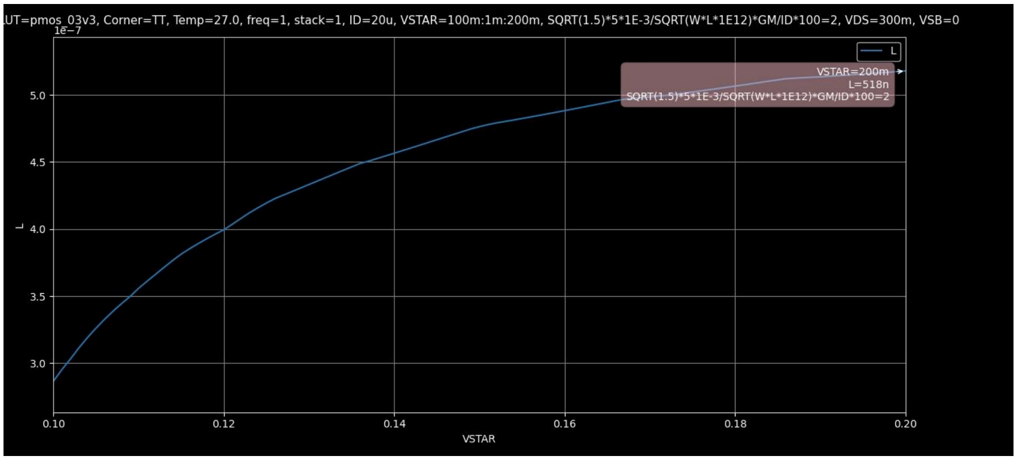


*W vs V**

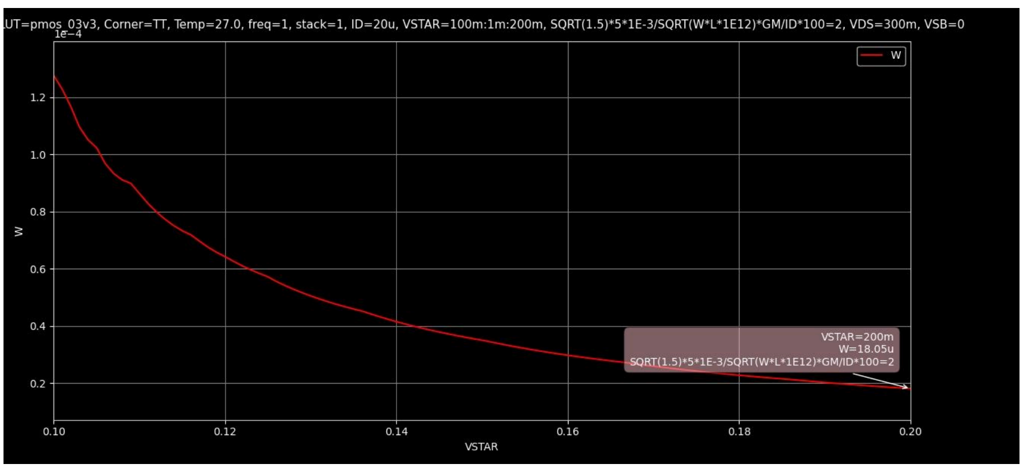


*Area vs V**

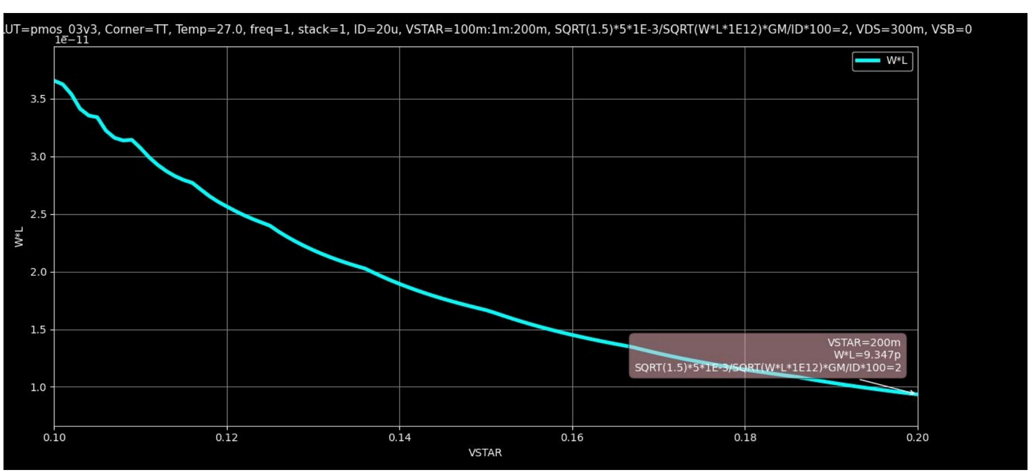
- Given the compliance voltage spec, report the above figure with a cursor added to the selected design point.



L @ selected design point



W @ selected design point



Area @ selected design point

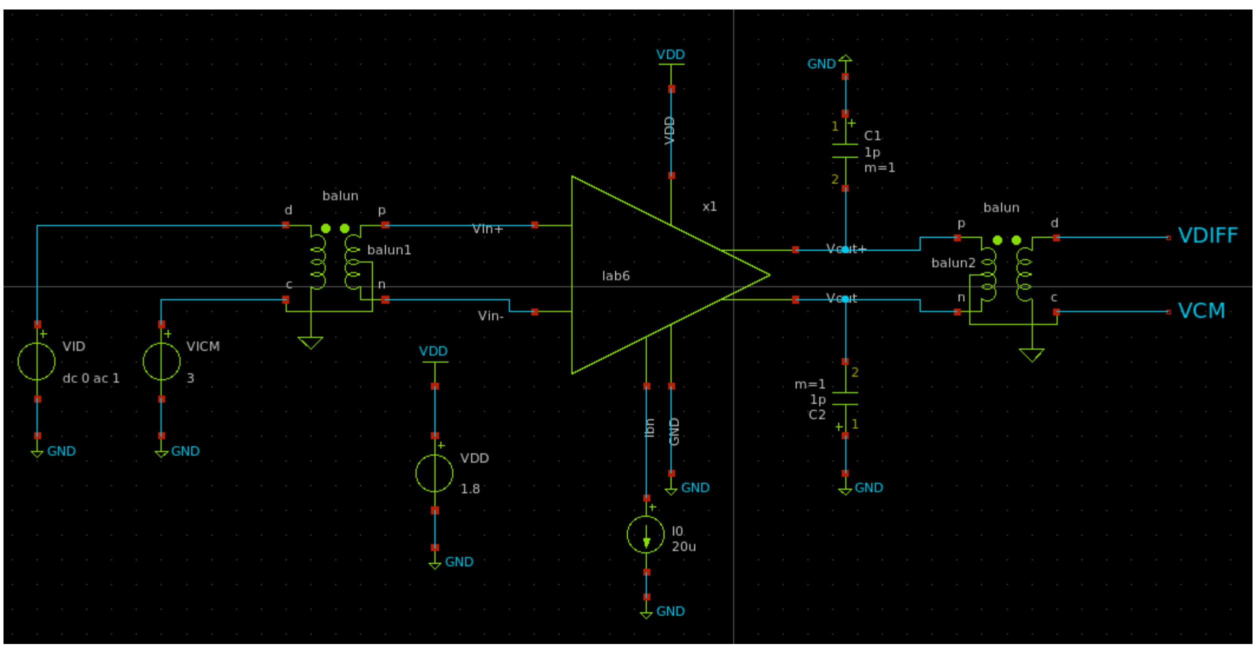
- Calculate the min and max CM input levels. Is the previously selected CM input level in the valid range?

$$V_{i,CM,min} = V_{th,i} + V_{O} = -\ 270mV.$$
$$V_{i,CM,max} = -\ V_{GS,i} - V^{*} + V_{DD} = 0.66V.$$

  - The selected CM i/p ***is*** in the valid range.

Part 2: Differential Amplifier Simulation

- Create the schematic of a differential amplifier “lab_06_diff_amp”. Create a symbol for the diff pair. Edit the symbol to look as shown below in the testbench schematic. Create a new cell for the testbench “lab_06_diff_amp_tb”. Create the testbench schematic as shown below.



Required schematic

- Report OP simulation

➔ Report a snapshot clearly showing the following parameters.

```
No. of Data Rows : 1
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device          m.x1.m.xm4.m0          m.x1.m.xm3.m0          m.x1.m.xm2.m0
      model        x1:pmos_3p3.13         x1:pmos_3p3.13         x1:pmos_3p3.13
         id                 2e-05            3.77022e-05            1.85842e-05
         gm           0.000205329            0.000394098            0.000238335
        gds           1.01639e-06            2.45003e-06            1.39868e-06
       gmbs           9.19315e-05            0.000176478            7.83489e-05
        vgs                0.9381                 0.9381                1.14067
        vth              0.787552                0.79174                1.04167
        vds              0.938098               0.659327               0.583145
      vdsat               0.16612               0.163028               0.140964

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device          m.x1.m.xm1.m0
      model        x1:pmos_3p3.13
         id            1.9118e-05
         gm           0.000242765
        gds           1.46266e-06
       gmbs           7.98073e-05
        vgs               1.14067
        vth               1.03944
        vds              0.567129
      vdsat              0.142613
```

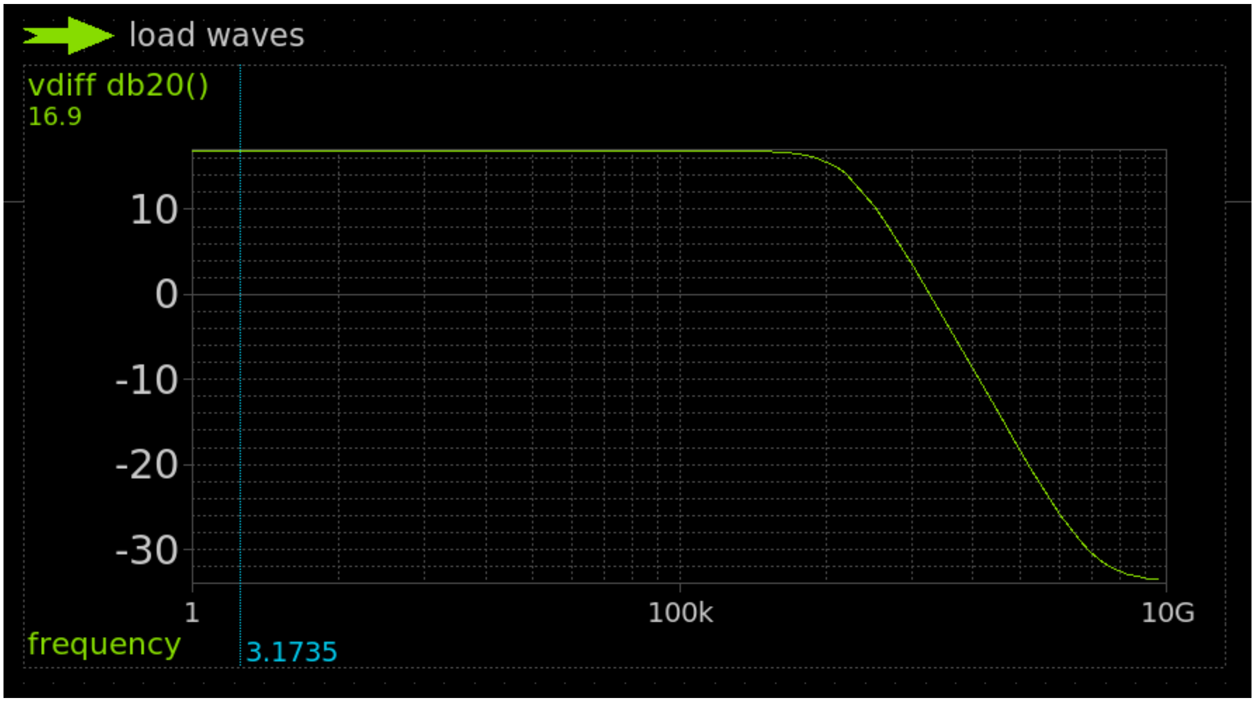
OP simulation results

➔ Check that all transistors operate in saturation.

$\#$	V_{DS}	V_{Dsat}	$Sat?$
1	0.6	0.14	Yes
2	0.6	0.14	Yes
3	0.66	0.16	Yes
4	0.94	0.17	Yes

- Diff small signal ccs:

   ➔ Report the Bode plot of small signal diff gain.



Bade mag plot of diff gain

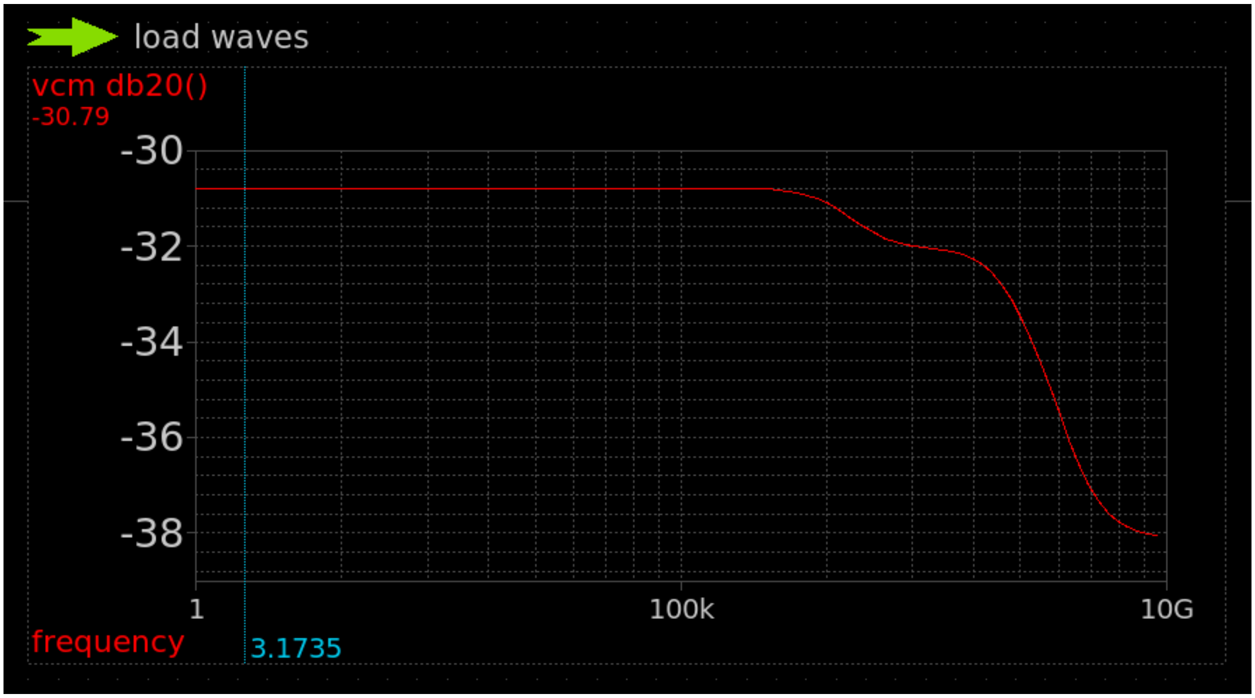
```
No. of Data Rows : 101
gain                  =  7.087708e+00 at=  1.000000e+00
bw                    =  5.351974e+06
```

Required calculations

➔ Compare the DC diff gain and BW with hand analysis in a table.

Quantity	*Calculated*	*Simulated*
Gain	$A_v = g_{m,i}(R_D \| r_o) \approx 7$	$A_v = 7.09$
BW	$BW = \frac{1}{R_o C_o} \approx 5.46\ MHz$	$BW = 5.35MHz$

- CM small signal ccs:
  ➔ Report the Bode plot of small signal CM gain.



Bode mag plot of small signal CM gain

```
No. of Data Rows : 101
cmgain               =  2.887720e-02 at=  1.000000e+00
```

CM gain

➔ Compare the DC CM gain with hand analysis in a table. Is it smaller than "1"? Why?

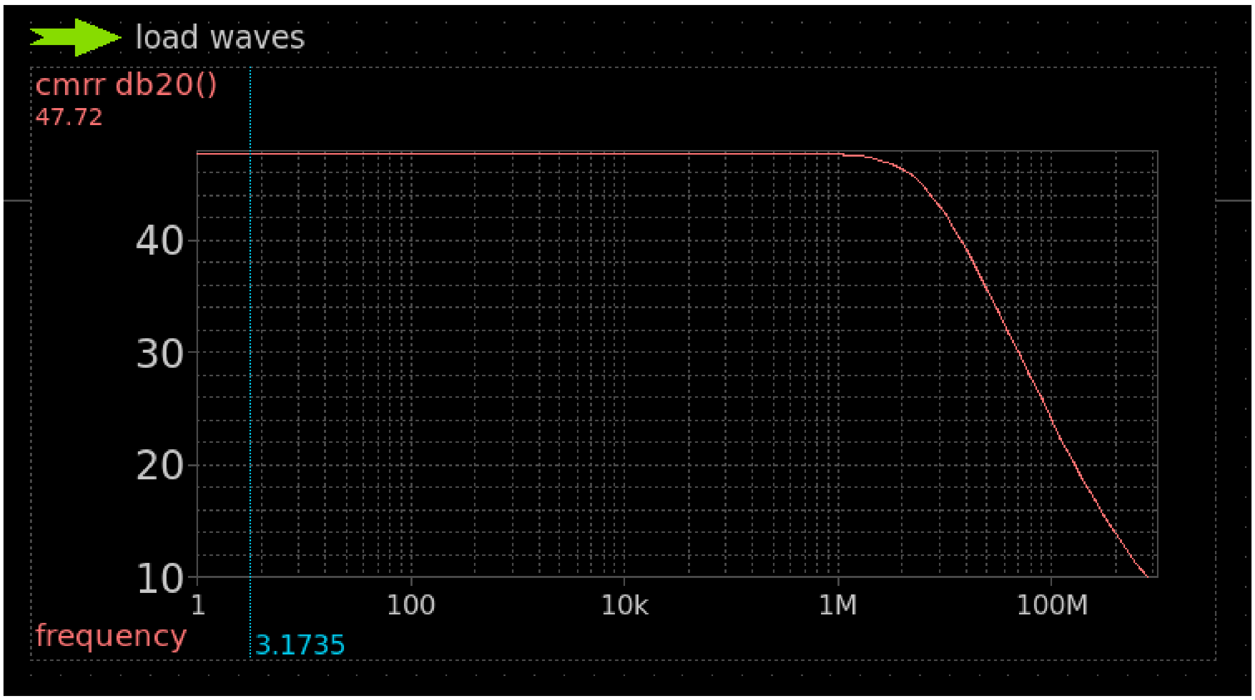
$Quantity$	$Calculated$	$Simulated$
$Gain$	$A_v = \frac{g_{m,i}}{1+2g_{m,i}r_{o,tcs}}(R_D \Vert r_o) \approx 26.4m$	$A_v = 28.8m$

- It's smaller than 1, as the value of the degeneration resistance "$2R_{ss} = 2r_{o,tcs} \approx 400k\Omega$" is very large.

➔ Justify the variation of Avcm vs frequency.

- A_{vCM} varies with frequency due to the fact that the capacitances of the tail current source shunt R_{ss} at high frequencies.

➔ Plot Avd/Avcm in dB. Compare Avd/Avcm @ DC with hand analysis in a table.



CMRR in dB vs frequency

```
No. of Data Rows : 91
cmgain                  =  2.973648e-02 at=  1.995262e+00
diffgain                =  7.228935e+00 at=  1.000000e+00
cmrr val = 2.430999e+02
```

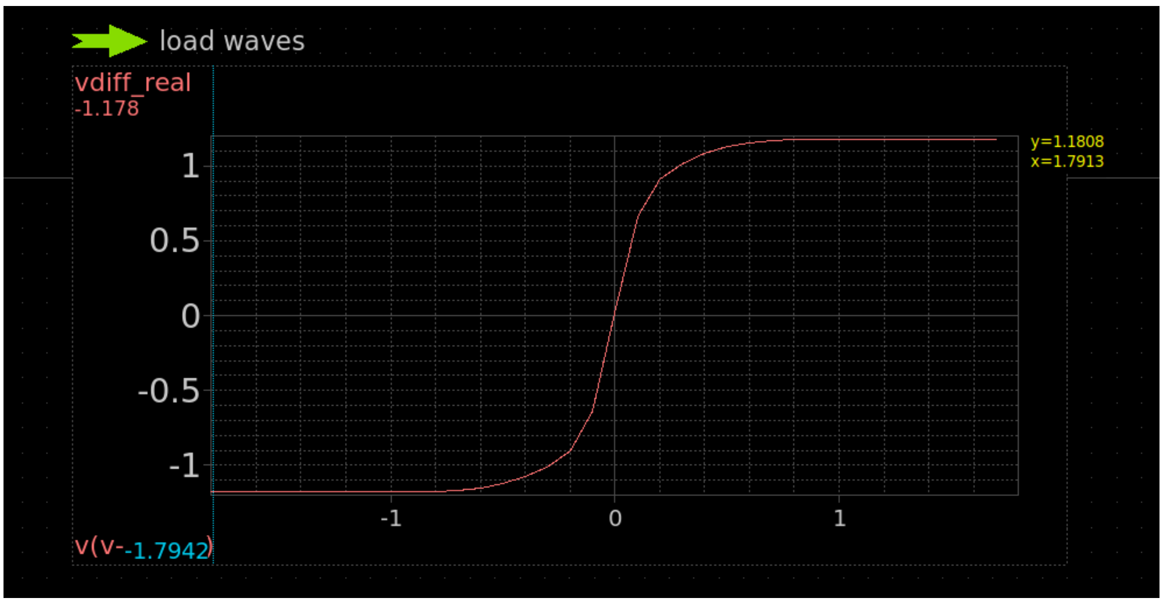
CMRR

$Quantity$	$Calculated$	$Simulated$
$CMRR$	$CMRR = 2(g_{m,i} + g_{mb,i})R_{ss} \approx 227$	$CMRR = 243$

➔ Justify the variation of Avd/Avcm with frequency.

- CMRR is proportional to R_{ss} and R_{ss} decreases with frequency due to C_p.

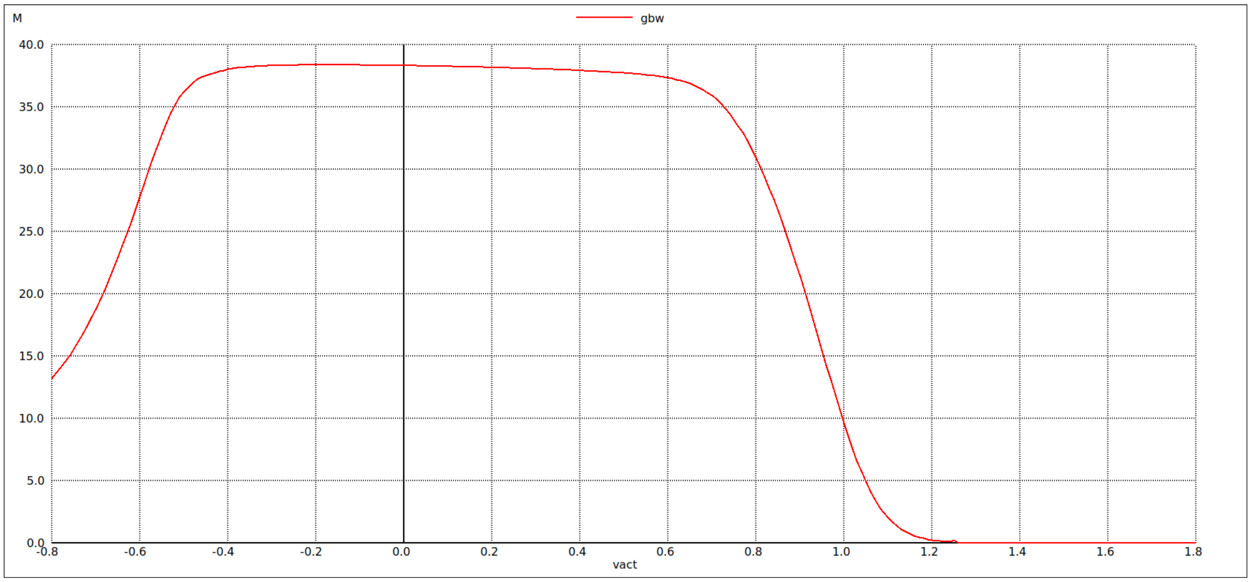
- Diff large signal ccs:
  ➔ Report diff large signal ccs (VODIFF vs VIDIFF). Compare the extreme values with hand analysis in a table.



Vod vs Vid

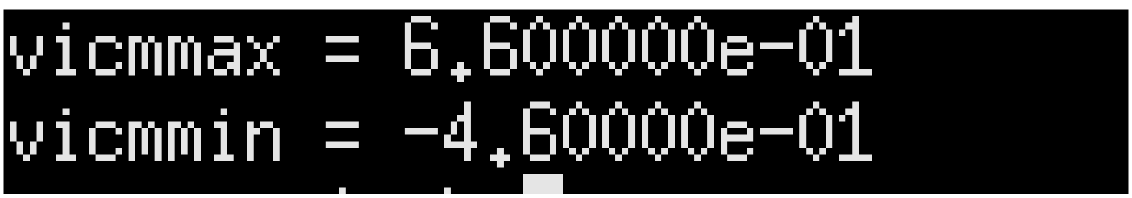
$Quantity$	$Calculated$	$Simulated$
$\lvert I_{ss} R_D \rvert$	1.131	1.18

- CM large signal ccs (GBW vs Vicm):
  ➔ Report CM large signal ccs (GBW vs VICM). Assume the valid range for Vicm (CMIR) is defined by the condition that Avd is within 90% of the max gain, i.e., 10% drop in gain.



GBW vs ViCM

➔ Find the CM input range (CMIR). Compare with hand analysis in a table.



CMIR

Quantity	*Calculated*	*Simulated*
CMIR	$-270m < V_{iCM} < 0.66$	$-460m < V_{iCM} < 660m$