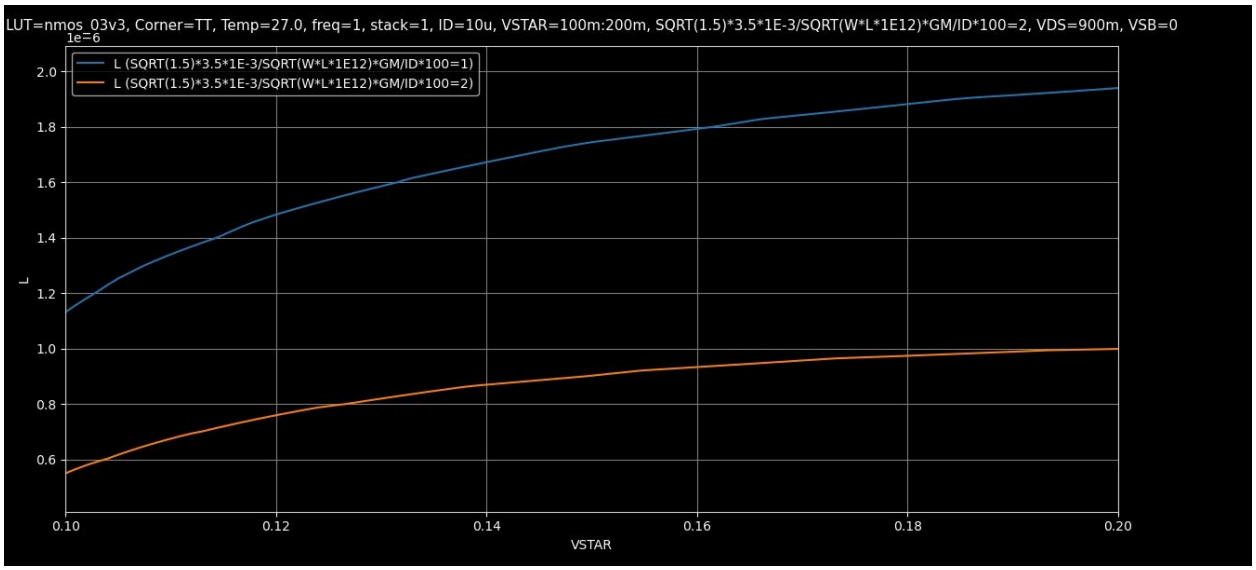
CMOS AIC design - ITI - Lab 5

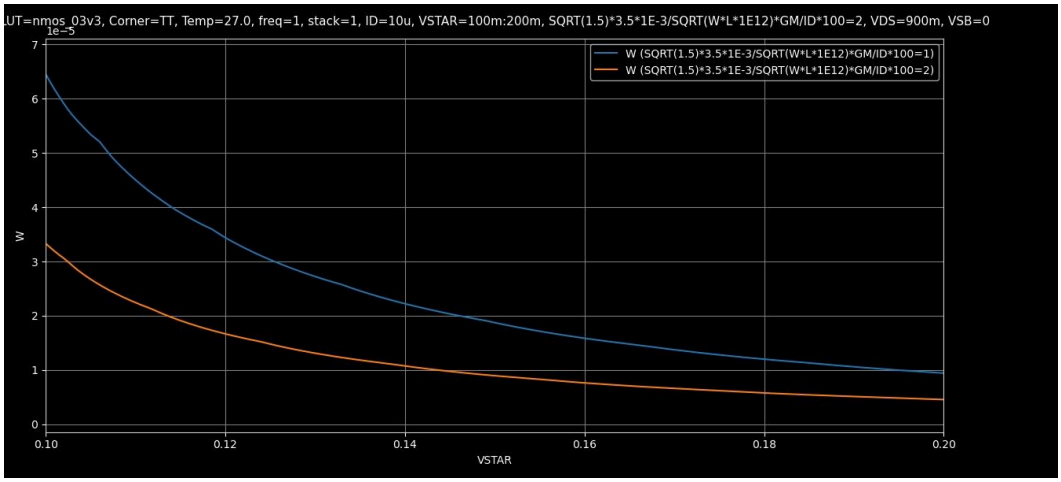
Part 1: Exploring Sizing Tradeoffs Using SA

- Sinking current means which device type? NMOS or PMOS?
  - Sinking current is performed using NMOS.
- The % Change in current translates to a spec on the $\lambda = 1/V_A$ of the device. How much is the required λ?

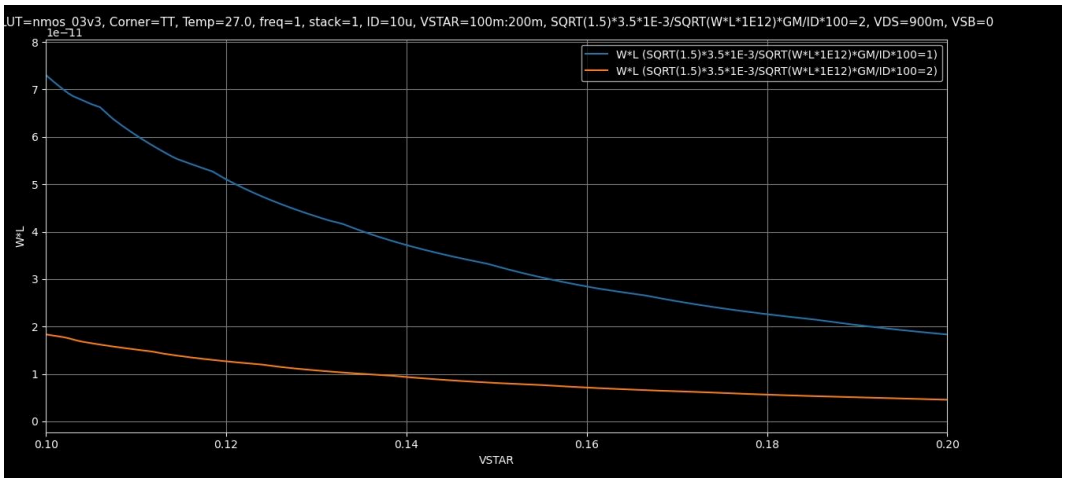
$$I_D = I_{DS}(1 + \lambda V_{DS}),\ \frac{\Delta I_D}{\Delta V_{DS}}\Big|_{V_{DS}=1} = \lambda \frac{I_D}{1+\lambda} \Rightarrow \lambda = 0.1$$



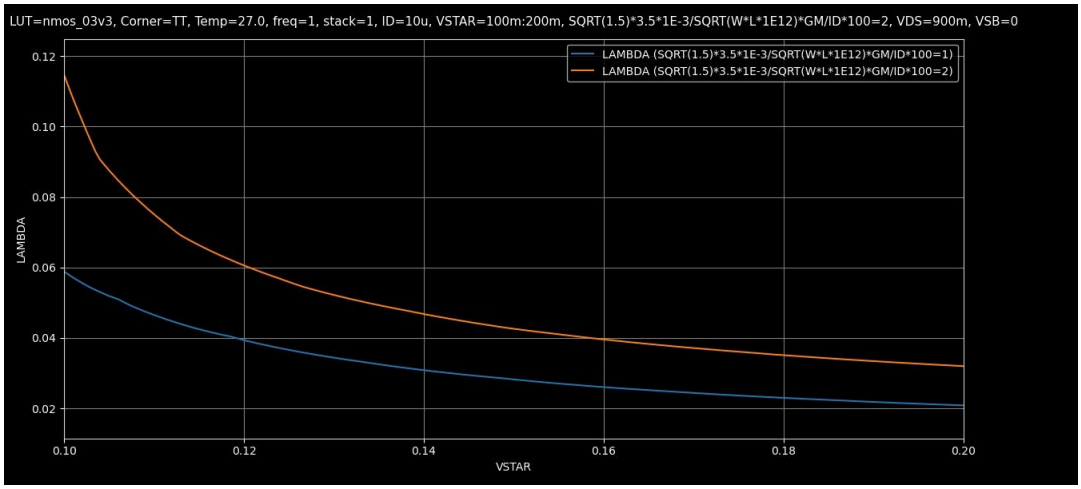
*L vs V**



*W vs V**



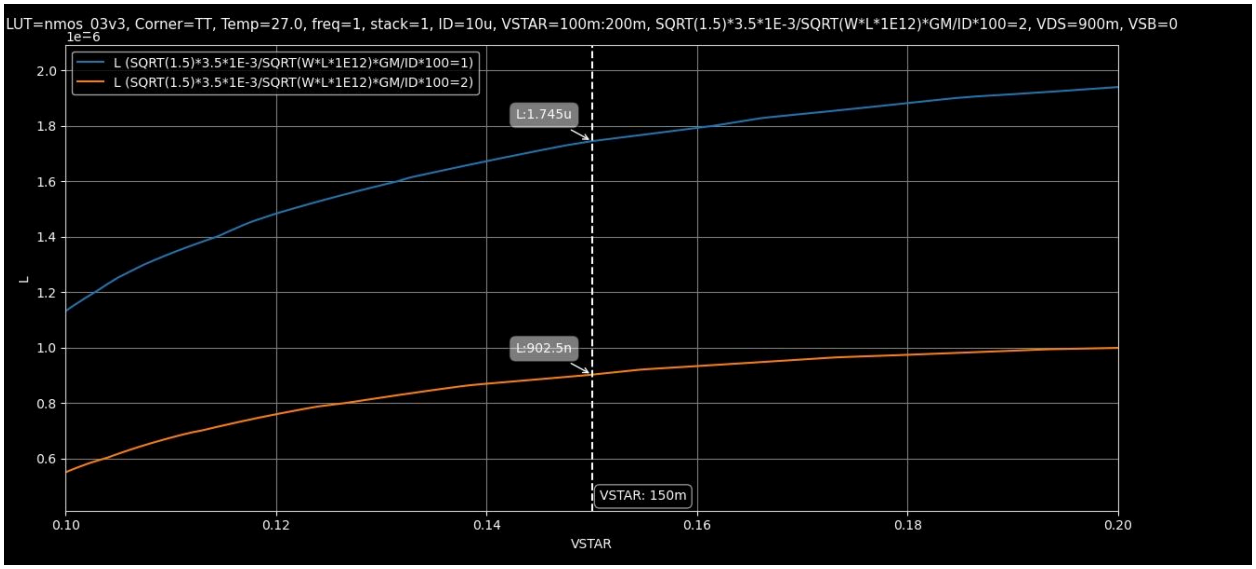
*Area vs V**



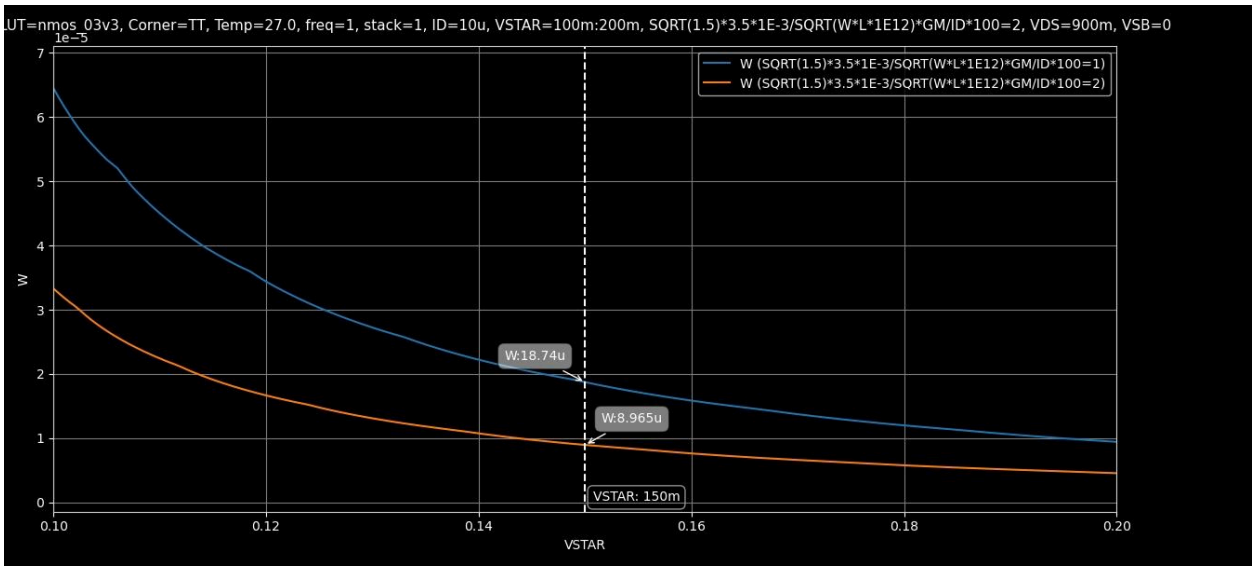
*Lambda vs V**

- Can we do the previous design trade-offs exploration sweeps using a standard SPICE simulator, i.e., sweep Vstar at a constant $\sigma(Iout)/Iout$? Why?
    - The mismatch is a statistical measure which the standard SPICE simulator has no control over.

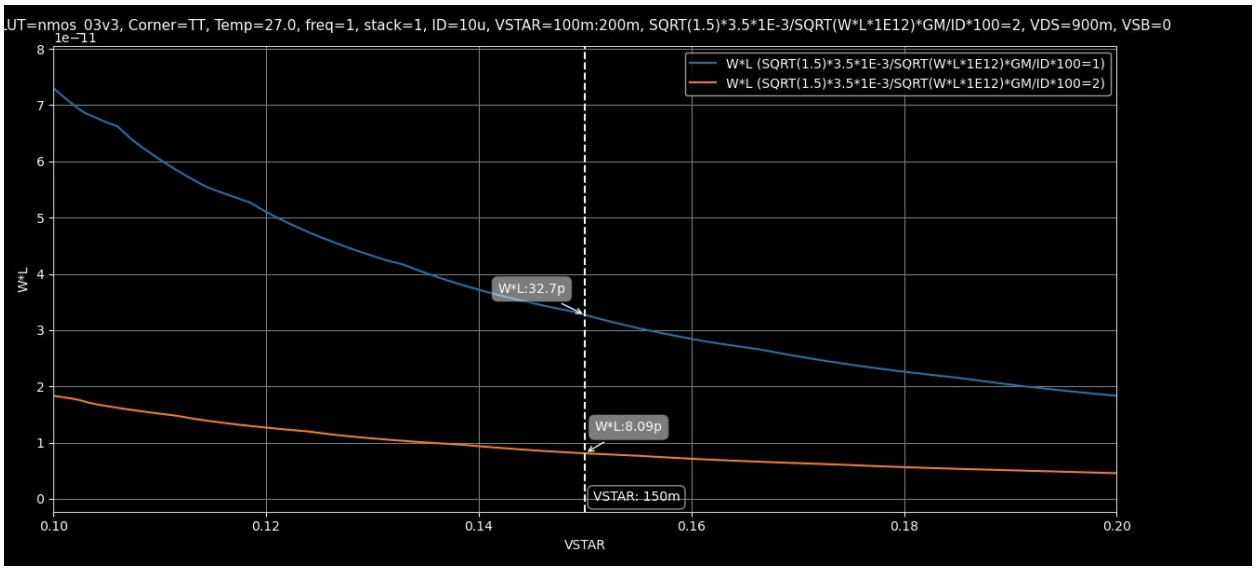
- Report the above plot with a cursor added at the required V^*. Does this point satisfy the mismatch and λ constraints?



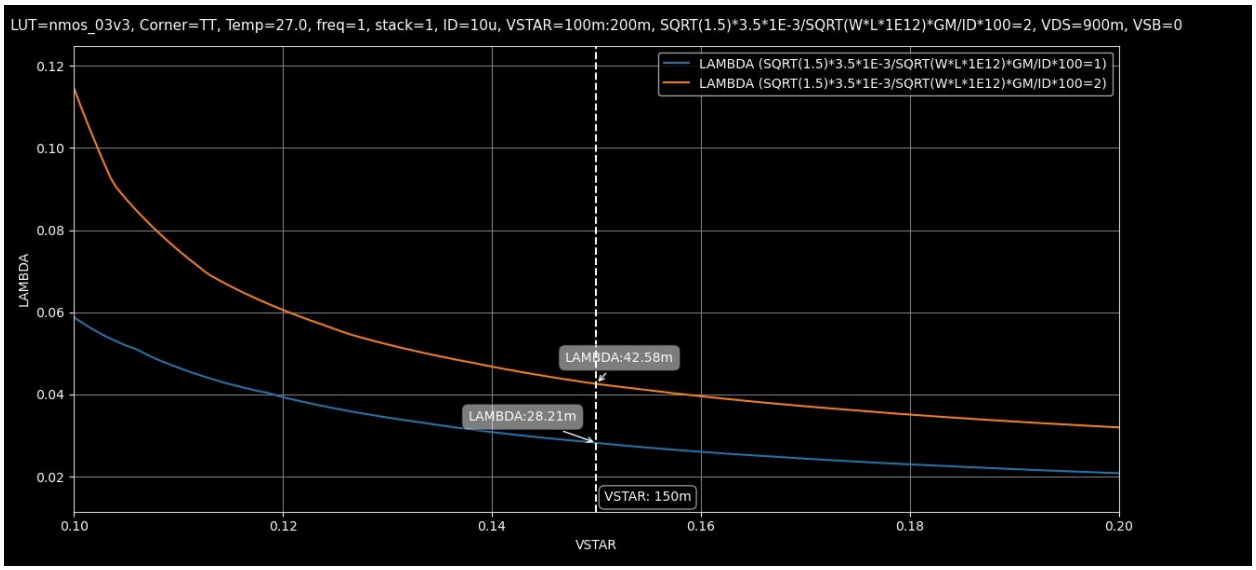
*L @ required V**



*W @ required V**



*Area @ required V**



*Lambda @ required V**

  - The constraints are satisfied.

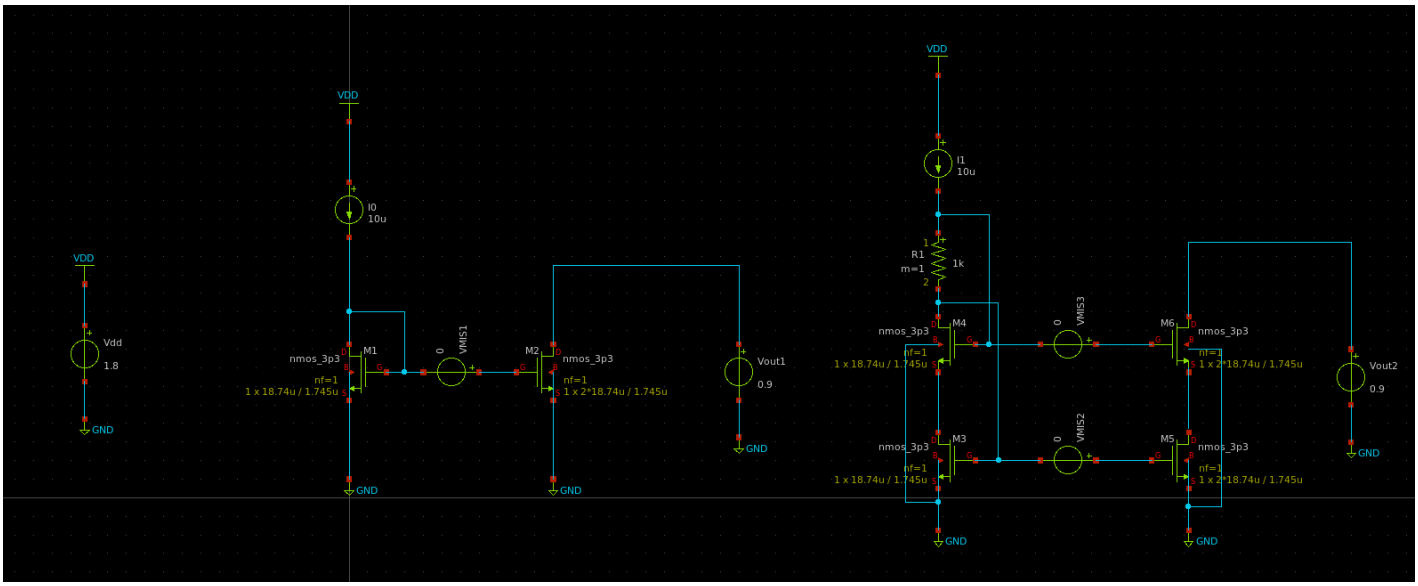
- If the λ constraint is not satisfied at $\sigma(Iout)/Iout$=2%, i.e., it needs a longer L, we can use SA to find the required design point as shown below. Report the device sizing and $\sigma(Iout)/Iout$ at the selected design point.

L	470n
W	4.79u

Device sizing after redesign

Part 2: Current Mirror Simulation

- Create a new schematic. Construct the circuit shown below.



Required schematic

1. Design and OP (Operating Point) Analysis

- Assume we want to set a $50mV$ saturation margin for M6 and M3, i.e., $V_{DS6} \approx V_{DS3} \approx V^{*} + 50mV$. Ignore the body effect and calculate a rough value for RB.

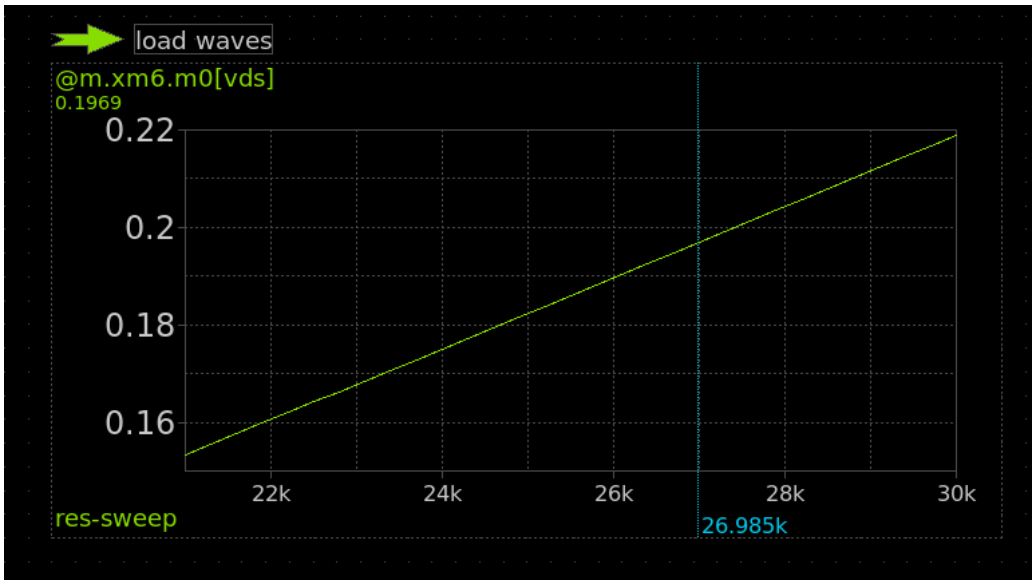
$$R_B = \frac{200m}{10u} = 20k\Omega.$$

- Perform DC sweep (not parametric sweep) for RB. Choose a reasonable sweep range given the rough value computed in the previous step. Report V_{DS6} vs R_B. Choose R_B to satisfy the $50mV$ saturation margin requirement. Is the selected R_B value larger or smaller than the rough analytical value? Why?

```
No. of Data Rows : 31
binary raw file "CM_TB_final.raw"
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device              m.xm5.m0              m.xm6.m0              m.xm2.m0
      model          nmos_3p3.14           nmos_3p3.14           nmos_3p3.14
         id          1.99541e-05           1.99541e-05                 1e-05
         gm          0.000269502           0.000267681             0.0001349
        gds          5.86337e-07           1.63754e-06          3.22657e-07
        vgs             0.831469              0.751969              0.831955
        vth             0.754193              0.672884              0.754132
        vds             0.679499              0.220499              0.531954

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device              m.xm3.m0              m.xm4.m0              m.xm1.m0
      model          nmos_3p3.14           nmos_3p3.14           nmos_3p3.14
         id                1e-05          2.05127e-05                 1e-05
         gm          0.000134025           0.000273983          0.000134595
        gds           8.2581e-07           5.67682e-07          2.92144e-07
        vgs             0.751969              0.751426              0.751426
        vth             0.672671              0.672136              0.673656
        vds             0.220013              0.899999              0.751425
```

Required calculations



Required RB ≈ 27kΩ

- The selected R_B has a larger value than the roughly-estimated one due to approximations implied in hand analysis.

- Simulate the OP point. Report a snapshot clearly showing the following parameters.

```
No. of Data Rows : 1
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device              m.xm5.m0              m.xm6.m0              m.xm2.m0
      model           nmos_3p3.14           nmos_3p3.14           nmos_3p3.14
         id           1.99268e-05           1.99268e-05                 1e-05
         gm           0.000269042           0.000262934           0.000134798
        gds           5.72584e-07           8.03127e-06           3.0815e-07
        vgs              0.805508              0.752625              0.807068
        vth               0.72841                0.6727               0.72932
        vds              0.752881              0.147116              0.607067
      vdsat              0.116533              0.116431              0.116917
       gmbs           9.82432e-05           0.000103149           4.92533e-05

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device              m.xm3.m0              m.xm4.m0              m.xm1.m0
      model           nmos_3p3.14           nmos_3p3.14           nmos_3p3.14
         id                 1e-05           1.97421e-05                 1e-05
         gm           0.000131593           0.000266887           0.000134613
        gds           4.30677e-06           5.52745e-07           2.92492e-07
        vgs              0.752625              0.748558              0.748558
        vth              0.672335              0.672118              0.670807
        vds              0.145556              0.899999              0.748557
      vdsat              0.116655              0.114304              0.115101
       gmbs           5.16262e-05           0.000104682           5.27906e-05
```

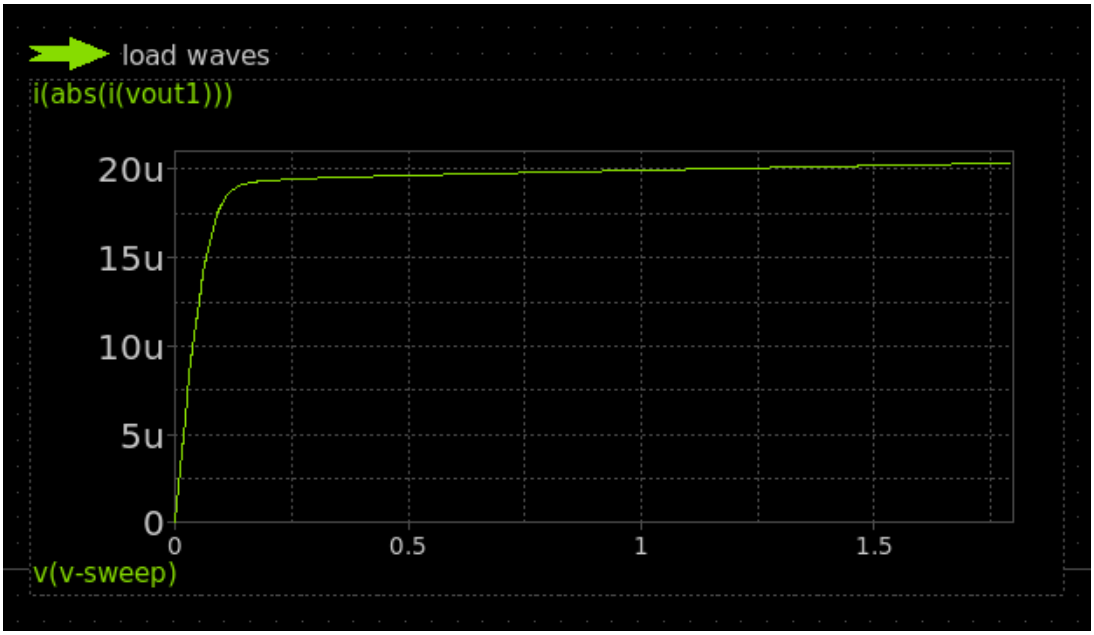
Required calculations

- Do all transistors operate in saturation?

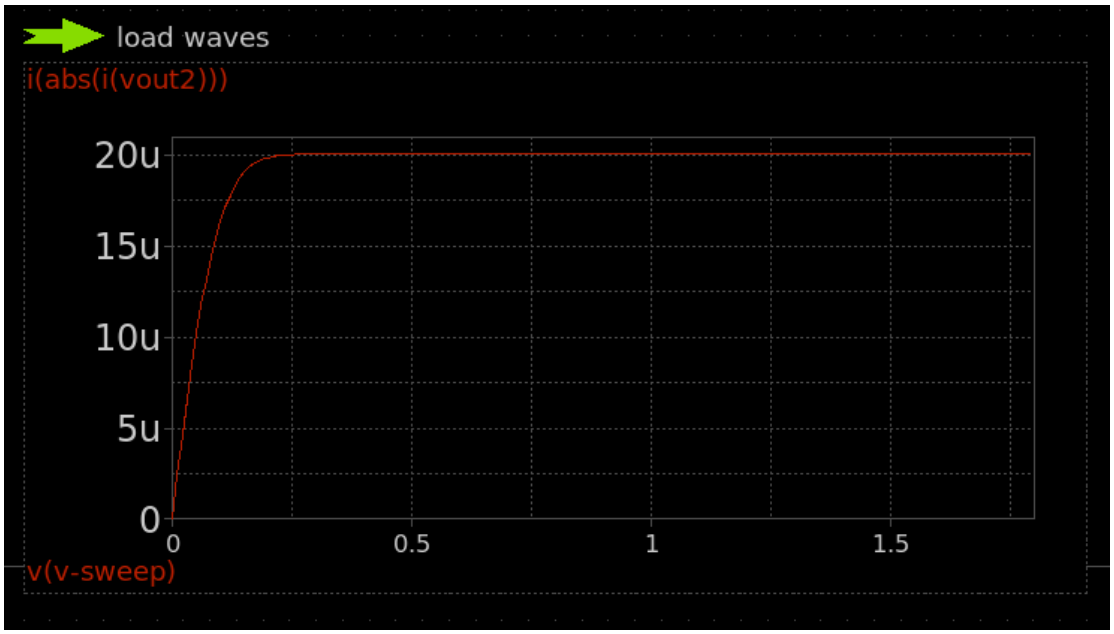
#	V_{DS}	$V_{DS,sat}$	$Sat?$
1	0.75	0.11	Yes
2	0.6	0.11	Yes
3	0.15	0.11	Yes
4	0.9	0.11	Yes
5	0.75	0.11	Yes
6	0.15	0.11	Yes

2. DC Sweep (I_{out} vs VOUT)

- Perform DC sweep (not parametric sweep) using VOUT = 0:10m:VDD. Report I_{out} vs VOUT for the two CMs overlaid in the same plot. Comment on the difference between the two circuits.



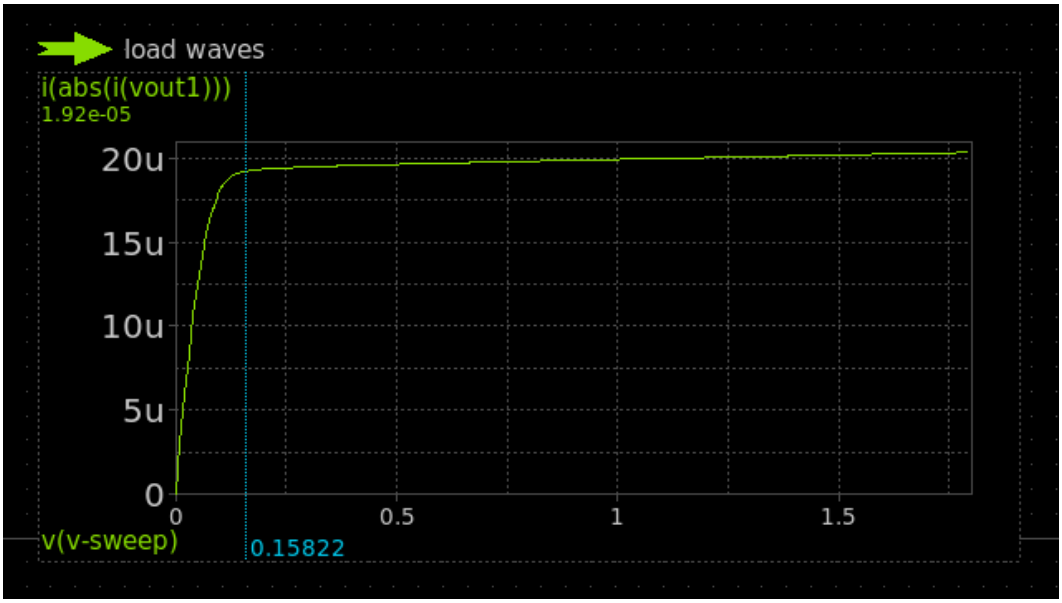
Iout1 vs Vout1



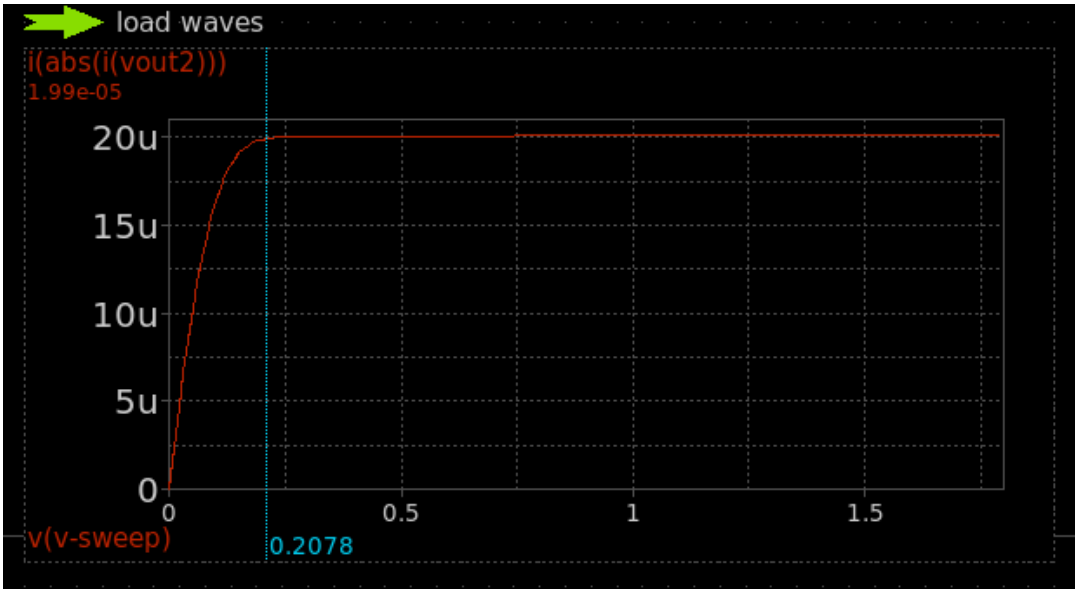
Iout2 vs Vout2

- It’s clear that the wide swing CM acts as a current source more ideal than the conventional CM due to the boosted o/p impedance.

- From the plot, find an estimate for the compliance voltage of each current mirror.

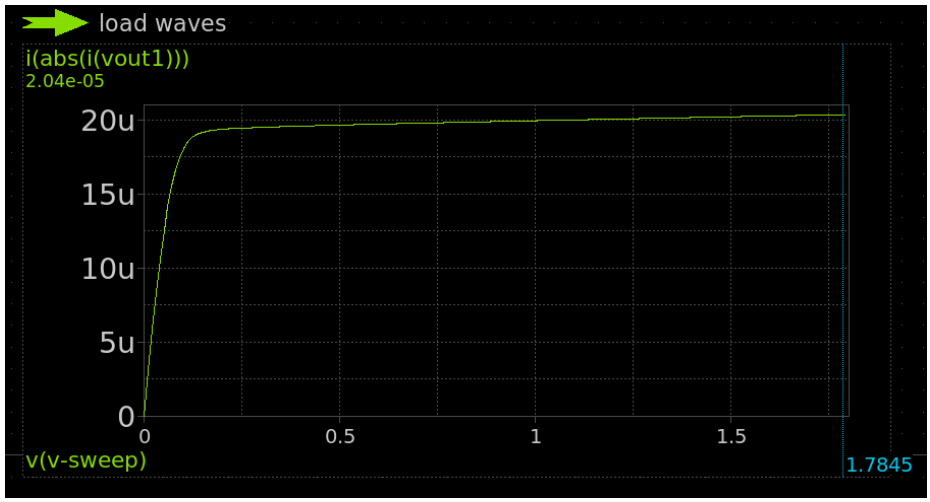


Compliance voltage of the conventional CM



Compliance voltage of the wide swing CM

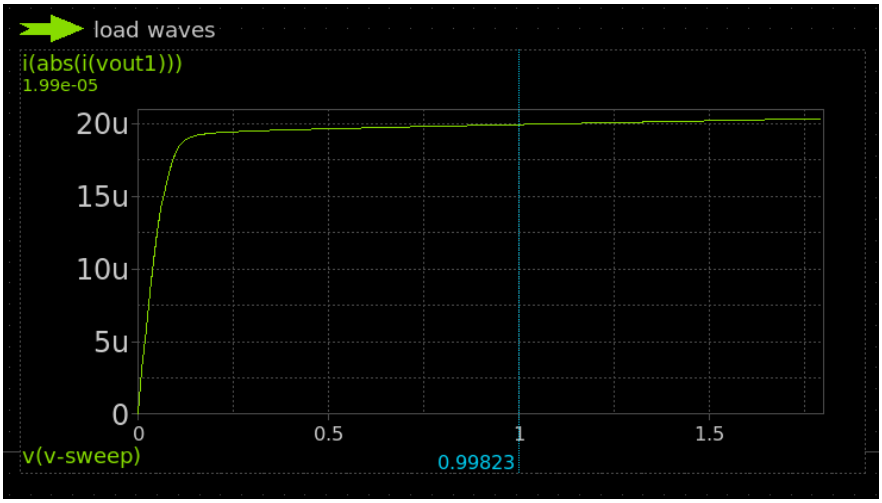
- I_{out} of the simple CM is exactly equal to IB*2 at a specific value of VOUT. Why?



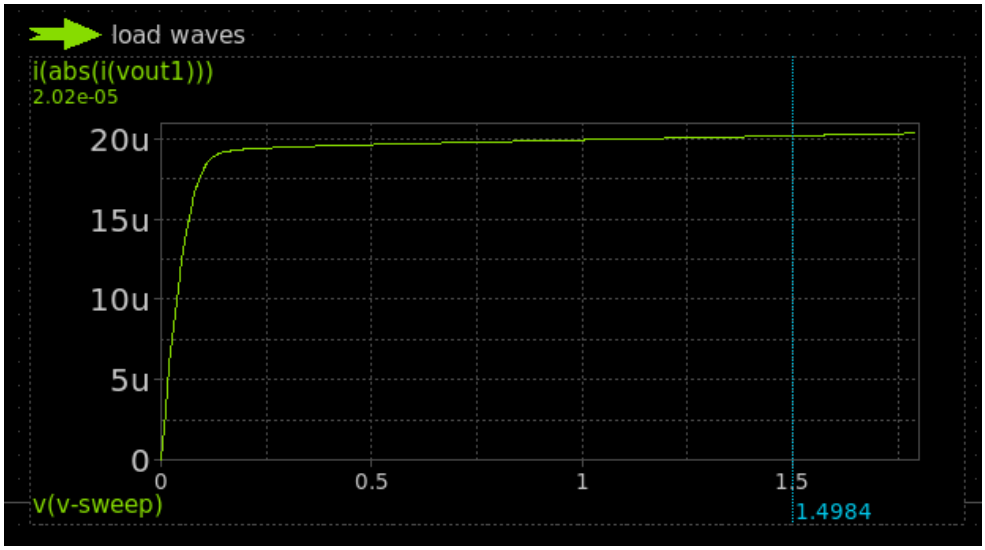
V @ which Iout ≈ 2IB

  - I_{out} nearly equals I_{ref} @ $V_{out} \approx 1.8V = V_{DD}$ which is the maximum V_{out} obtainable that achieves the almost-ideal current mirroring.

- For the simple current mirror, calculate the percent change in I_{out} when VOUT changes from 0.5V to 1.5V (i.e., 1V change). Compare the result to the value expected from Part 1.



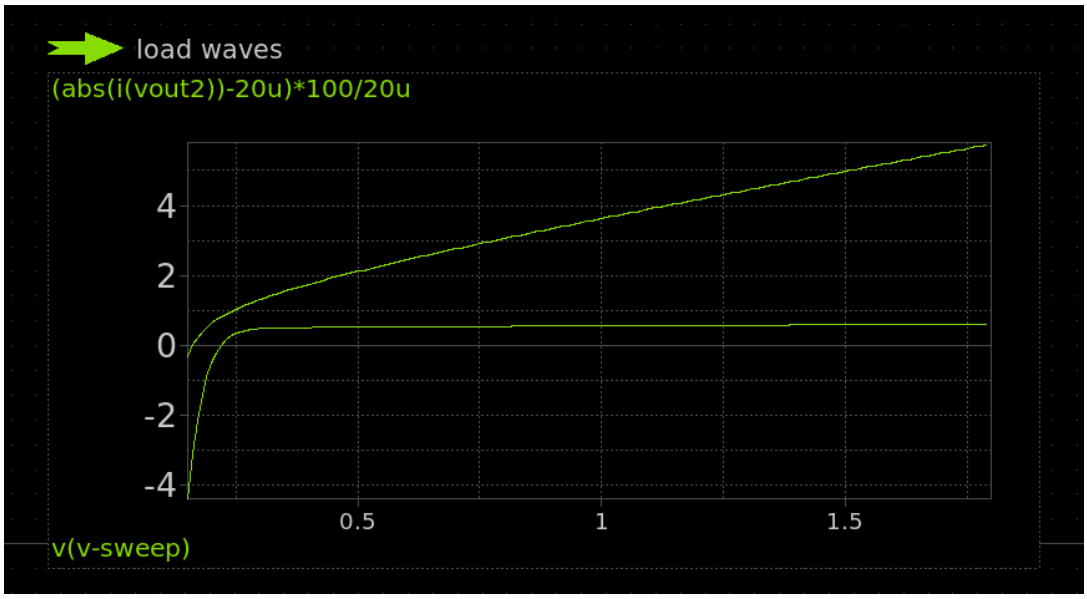
Iout @ Vout = 1V



Iout @ Vout = 1.5V

$$\frac{\Delta I_{out}}{\Delta V_{out}} = \frac{2.02u - 1.99u}{1.5 - 1} = 60n << 0.1$$

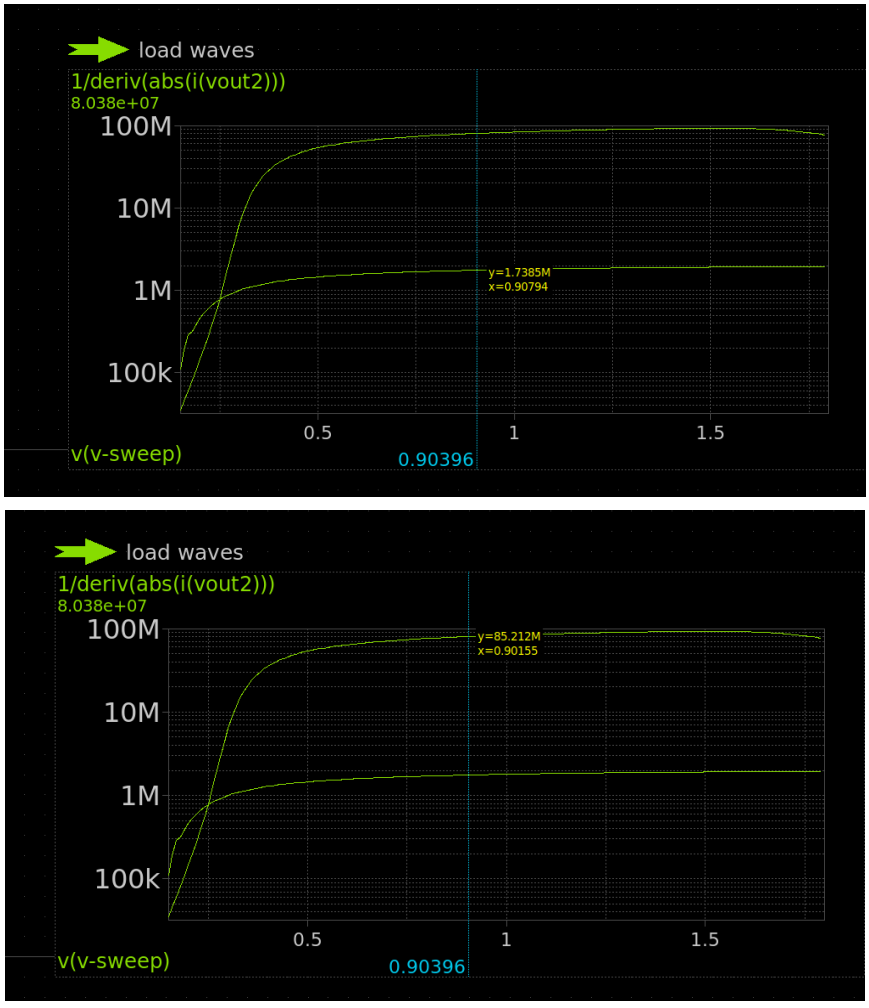
- Report the percent of error in I_{out} vs VOUT (ideal I_{out} should be IB*2) for the two CMs in the current mirror operating region (VOUT ≈ V^* to VDD) overlaid in the same plot. Comment on the difference between the two circuits.



Percent error in Iout vs Vout

- As V_{out} increases, the percent error in the conventional CM is getting very large compared to that of the wide swing CM.

- Report Rout vs VOUT (take the inverse of the derivative of I_{out} plot) for the two CMs in the current mirror operating region (VOUT ≈ V^* to VDD) overlaid in the same plot. Use log scale on the y-axis. Add a cursor at VOUT = VDD/2. Comment on the difference between the two circuits. Does Rout change with VOUT? Why?



Rout vs Vout

- The o/p impedance of the wide swing CM is much larger than that of the conventional CM.
- The variation of R_{out} with V_{out} is due to the fact that $R_{out} = \frac{\Delta V_{out}}{\Delta I_{out}} = f(V_{out})$.

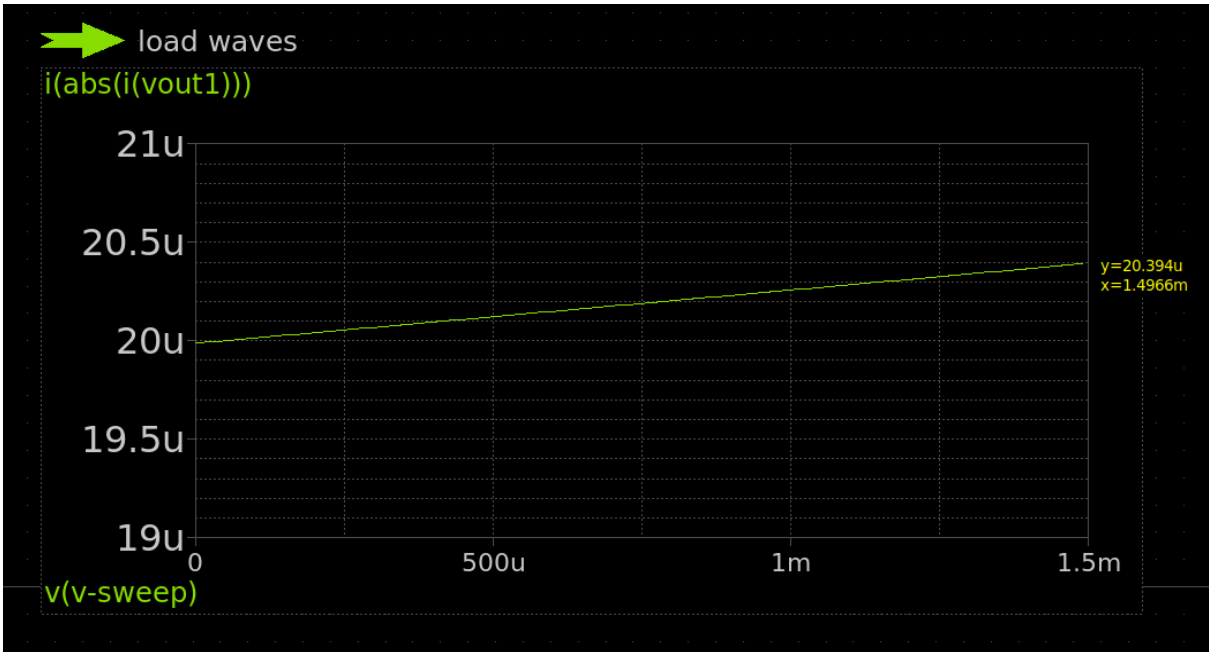
- Analytically calculate Rout of both circuits at VOUT = VDD/2. Compare with simulation results in a table.

$$Conventional: R_{out} = \frac{1}{g_{ds4}} \approx 1.8M\Omega$$
$$wide\ swing: R_{out} = r_{o5}(1 + (g_{m5} + g_{mb5})r_{o6}) \approx 64M\Omega$$

Circuit	Simulated	Calculated
Conventional	$1.7M$	$85M$
wide swing	$1.8M$	$64M$

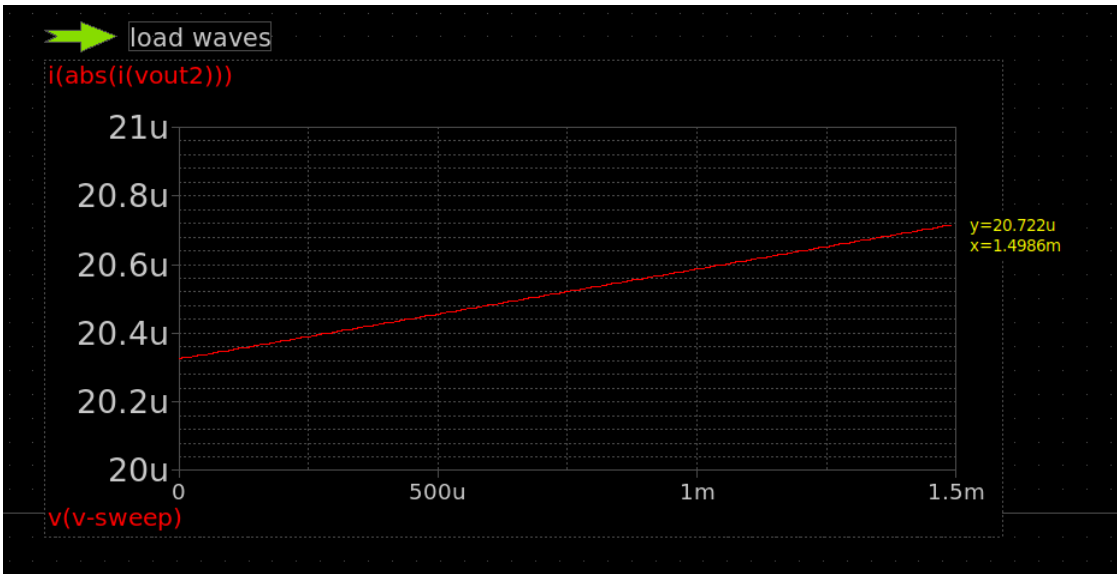
3. Mismatch

- Perform DC sweep for VMIS1 and VMIS2 from 0 to sqrt(1.5)*3.5m/sqrt(W*L*1e12) using the code below and set VMIS3 = 0. This models the standard deviation of the mismatch in V_{th} for the current mirror devices. Find the percent change in I_{out}.



Iout1 vs VMIS1

$$\frac{\sigma I_{out1}}{I_{out1}} = \frac{20.394-20}{20} \times 100 = 1.97\%$$



Iout2 vs VMIS2

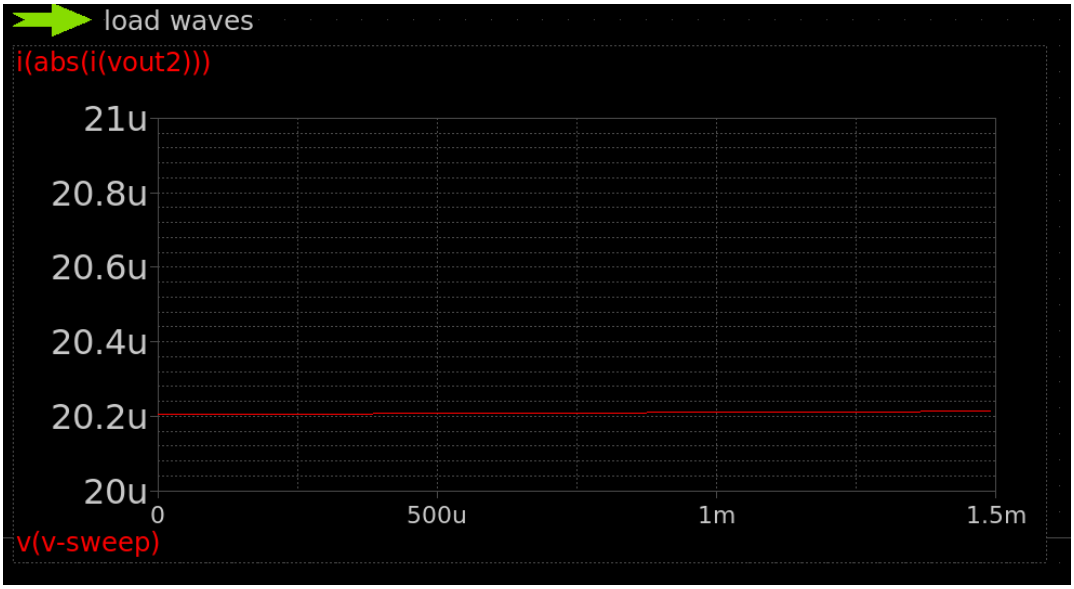
$$\frac{\sigma I_{out2}}{I_{out2}} = \frac{20.722-20}{20} \times 100 = 3.61\%$$

- Analytically calculate the percent change in I_{out} and compare it to the simulation result.
  Hint: The voltage change at the gate can be considered as a small signal. Thus, the change in the current can be calculated using the G_m of the circuit. In this case, the circuit can be considered as a cascode amplifier.

$$\frac{\sigma I_{out2}}{I_{out2}} = \frac{g_{m5} V_{mis2}}{I_{out2}} \approx 2.03\%$$

from simulation	*Analytically calculated*
3.61%	2.03%

- Set VMIS1 = VMIS2 = 0 and perform DC sweep for VMIS3 from 0 to sqrt(1.5)*3.5m/sqrt(W*L*1e12). This models the standard deviation of the mismatch in V_{th} for the cascode devices. Find the percent change in I_{out}.



Iout2 vs VMIS3

$$\frac{\sigma I_{out2}}{I_{out2}} \approx 0 \text{ "as can be seen from the graph"}$$

- Analytically calculate the percent change in I_{out} and compare it to the simulation result.
  Hint: The voltage change at the gate can be considered as a small signal. Thus, the change in the current can be calculated using the Gm of the circuit. In this case, the circuit can be considered as a degenerated common source amplifier.

$$\frac{\sigma I_{out2}}{I_{out2}} = \frac{g_{m5}}{1+g_{m5}r_{06}} V_{mis3} / I_{out2} \approx 0.06\%$$

from simulation	Analytically calculated
0	0.06%

- Which mismatch contribution is more pronounced? Why?
  - The contribution of V_{mis1} and V_{mis2} is much more pronounced due to the fact that they change the value of V_{GS} of mirror devices, which in turn have a one-to-one correspondence with I_D, while the change in V_{mis3} is absorbed by V_{DS} which has a much weaker effect on the current.

- Which design decision is better: setting the same W and L for the mirror and cascode devices? Or using larger W and L for the current mirror devices? Why?

- It can be deduced from the formula of calculating mismatch that larger L and W eventually leads to lower mismatch, so larger L and W is better.