**Faculty of computers and infromation,   
Cairo University**

**CS322: Computer Architecture and Organization  
Year 2019-2020**

**First Semester**

**Assignment 2 – Version 1.0**

**Course Instructors:**

Dr. Mohammad El-Ramly

**Revision History**

**Version 1.0** Dr Mohammed El-Ramly 10 October 2019 Version 1.0

**Objectives**

1. Review the basics of sequential logic circuits.
2. Learn digital design with Verilog and related tools.
3. Practice some simple designs with Verilog.

**Instructions**

1. **These instructions must be followed to get the full marks. يجب اتباع هذه التعليمات بكل دقة**
2. **Deadline is Tuesday 22 Oct. @ 11 am.**
3. **Weight is 6 marks** (4 for solving your part and 2 for group work)
4. Students will forms teams of 4 whose IDs **do not end with the same digit.** For example, 2017023, 20170433 and 20170124 cannot be in one team because two have IDs ending with 3.

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| --- |
| 1. **Please submit only work that you did yourself. If you copy work from a friend or book or the net you will fail the course. تسليم حلول منقولة من أى مصدر يؤدى إلى الرسوب فى هذا المقرر. لا تغش الحل أو تنقله من أى مصدر و اسألنى فى أى شئ لا تفهمه لكن لا تنقل الحلول من النت أو زملائك أو أى مكان و لو عثرت على حلول من أى مصدر أو زميل لا تنقل منها أى شئ وقد أعذر من أنذر ولن يتم التهاون مع الغش مطلقا** |

**Task 0 (0 marks)**

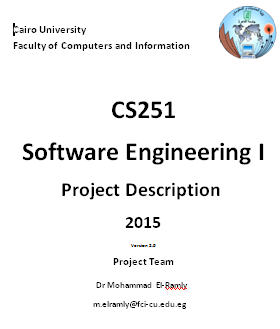
1. Watch Verilog tutorial (see links on acadox)
2. Read chapters 3 and 4 from the course textbook.
3. Install and learn these tools:

* Quartus II Web Edition for model synthesis (converting Verilog to schematic and vie versa) <https://www.intel.com/content/www/us/en/programmable/downloads/software/quartus-ii-we/120.html>
* ModelSim PE Student Edition for model simulation (simulating the behavior of the model) <https://www.mentor.com/company/higher_ed/modelsim-student-edition>

**Task 1 (4 marks)**

For chapters 3 and 4 from Digital Design and Computer Architecture by Harris and Harris, solve the **even** problems (from 1 to 34 in chapter 3 and 1 to 50 in chapter 4). Team member with LSDigit in his last digit in the ID solves problems 2, 10, 18, … and the next solves 4, 12, 20, …

Solve chap 3 by hand and for chap 4 deliver a print of the code and screen shot of the synthesis and simulation.



**Task 2 (2 marks)**

Team members should explain all solutions to each other and everyone should understand all solutions.

**Submission Instructions**

1. **Team will submit in acadox and in writing.**
2. Submit in acadox a report with a header and your Verilog files and ModelSim and Quartus screenshots.
3. Submit a handwritten report with **handwritten solutions of chap 3 and print of solutions of chap 4 (which you uploaded in acadox)**

* A cover page like the one in last page.
* Document should be organized and stabled.

1. Each team member will work individually on his part. **But the team must provide ONE integrated report.**
2. Team members are expected to help each other but not do work of others.
3. **All team members must understand the details** of all solutions and be able to explain them
4. TA can ask any team member about any of the programs developed and its code**.**

**Marking Criterion**

1. 4.0 for solving your problems, all of them
2. 2.0 for integrating the work and being able to understand it
3. -1.0 for any missing part that is not solved
4. Up to -4 if not able to explain solution and answer questions.