**Faculty of computers and infromation,   
Cairo University**

**CS322: Computer Architecture and Organization  
Year 2019-2020**

**First Semester**

**Assignment 3 – Version 2.0**

**Course Instructors:**

Dr. Mohammad El-Ramly

**Revision History**

**Version 1.0** Dr Mohammed El-Ramly 3 November 2019 Version 1.0

**Version 2.0** Dr Mohammed El-Ramly 25 Nov. 2019 -ve is bonus

**Objectives /**

1. Practice digital system design using Verilog
2. Building and testing a small ALU and Floating Point Adder.
3. Train on digital design synthesis and simulation tools.

**Instructions**

1. **These instructions must be followed to get the full marks. يجب اتباع هذه التعليمات بكل دقة**
2. **Deadline is Wednesday 13 Nov. 2019 @ 11 pm**
3. **Form groups of 2 students.**
4. **Weight is 6 marks.**

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| 1. **Please submit only work that you did yourself. If you copy work from a friend or book or the net you will fail the course. تسليم حلول منقولة من أى مصدر يؤدى إلى الرسوب فى هذا المقرر. لا تغش الحل أو تنقله من أى مصدر و اسألنى فى أى شئ لا تفهمه لكن لا تنقل الحلول من النت أو زملائك أو أى مكان و لو عثرت على حلول من أى مصدر أو زميل لا تنقل منها أى شئ وقد أعذر من أنذر ولن يتم التهاون مع الغش مطلقا** |

**Task 0 (0 marks)**

1. Watch Verilog tutorials and read some resources and train on writing code (see links on acadox)
2. Read chapters 4 and 5 from the course textbook.
3. Install and learn these tools: Quartus II Web Edition and ModelSim PE Student Edition.

**Task 1 (3 marks)**

Design and build an ALU in Verilog that receives a 4 bits selection code to decide which operation to perform. Use the abstractions available in SystemVerilog and Quartus if helpful and design a module for any function that does not have abstraction.

ALU should do the following operations:

**Integer Math Operations.** Add, Subtract, Multiply, Integer Division

**Shift Operations.** Logical Shift Left, Logical Shift Right, Mathematical Shift Right, Rotate Right.

**Logical Operations.** AND, OR, XOR, INVERT (The first input)

ALU has 6 flags **N**egative, **Z**ero, **C**arry, o**V**erflow, **E**qual and **L**ess than (a < b)

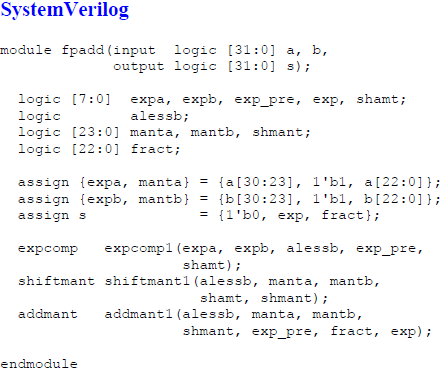
1. Design and Develop the circuit in Verilog.
2. Use the simulation tool to simulate the circuit and ensure it works well.
3. Deliver Verilog code, schematic design and simulation results.

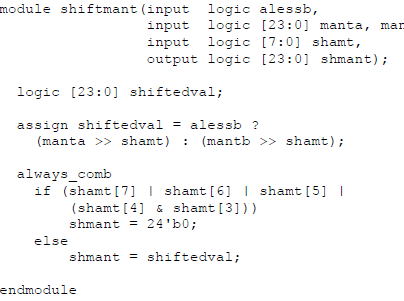
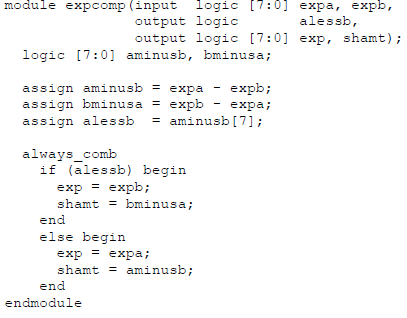
**Task 2 (3 marks)**

You are given a schematic and Verilog design for a floating-point adder.

Hint: Quartus does not synthesis floating point instructions or types **real** and **shortreal**.

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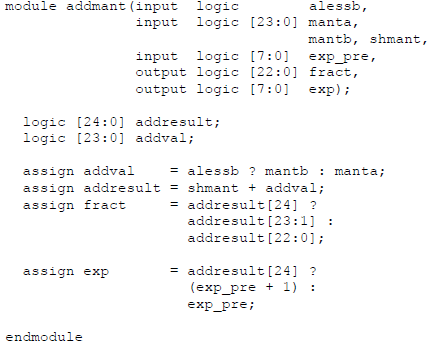


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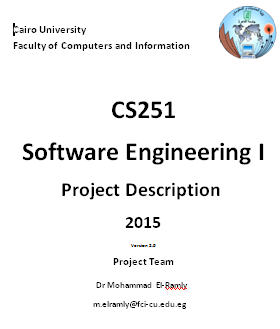
1. Ensure the given code works and compiles correctly.
2. Use better naming and improve coding style.
3. Extend the circuit design to handle the cases of

* Adding positive and negative numbers. (note that mantissa is NOT in two's complement format)
* Adding to +∞ or -∞
* Adding to NaN
* Adding a num + Zero
* If addition result is Zero.

1. Develop extended circuit design, Verilog & simulation.

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**Submission Instructions**



1. **Team will submit in acadox.**
2. Submit in acadox a zip file with the following:
3. PDF report with a header as shown in the figure that includes:

* Schematic and Verilog code of the adder
* Screenshots of simulation result
* Design of extended FP adder Verilog code
* Screen shots of the simulation results.

1. Verilog code files.
2. Name file should be named CS322-A3-ID1-ID2.pdf / .zip
3. **Do not submit huge files**
4. Team members are expected to help each other but not do work of others.
5. **All team members must understand the details** of all solutions and be able to explain them
6. TA can ask any team member about any of the programs developed and its code**.**

**Marking Criterion**

1. 0.0 for the Verilog code that does not compile and has errors.
2. 3.0 for the ALU: 0.75 mark for each set of instructions (0.75 x 3) and 0.75 for flags
3. 0.6 for perfecting the style and fixing errors in given design
4. 2.4 for dealing with special cases Nan, +∞, -∞ and Zero, (0.6 x 4)
5. 1.0 BONUS for dealing with special cases Negative
6. -6 for cheating any if not able to explain solution and answer questions.