Mahmoud Ashraf and Mohamed Said Team:

SWI		10	
B/BL		10	
Barrel Shifter	Immediate	10	
	Shifted Register – 5 bit Shift	10	Perfect
	Shifted Register – Bottom byte of another register	0	Not implemented
Conditional Execution		10	
Data Processing Instruction	ADD, ADDC…	9	Set Status Flags not implemented.
	TST, TEQ, CMP and CMN	8	No implementation of C, V flags updating
MUL and MULA		9	Excellent except you forget to update the status flags
Single Data Transfer		10	Elegant solution
These marks are not set to be summed up. i.e. larger sum doesn't indicate better implementation			The most elegant engineers, solving big problems with fewest possible keywords.