Hassan & Sameh Team:

SWI		10	
B/BL		10	
Barrel Shifter	Immediate	9	Rotate is incorrect
	Shifted Register – 5 bit Shift	9	Rotate Right Extended function not implemented
	Shifted Register – Bottom byte of another register	8	Least Significant byte not obtained
Conditional Execution		10	
Data Processing Instruction	ADD, ADDC…	9	Set Status Flags not checked correctly.
	TST, TEQ, CMP and CMN	8	No implementation of C, V flags updating
MUL and MULA		9	Excellent except you forget to update the status flags
Single Data Transfer		7	No distinguish between load word or byte. No little endian implementation. No Barrel shifter on the Base address.
These marks are not set to be summed up. i.e. larger sum doesn't indicate better implementation			Genius solutions, and smart coding all around.