Alaa Nabil:

SWI		10	
B/BL		10	
Barrel Shifter	Immediate	10	
	Shifted Register – 5 bit Shift	0	Not implemented
	Shifted Register – Bottom byte of another register	0	Not implemented
Conditional Execution		0	Not implemented
Data Processing Instruction	ADD, ADDC…	9	Not all instruction are implemented, Set Status Flags not checked correctly.
	TST, TEQ, CMP and CMN	0	Not implemented
MUL and MULA		9	Excellent special when you implemented “ensuring operands restrictions”, except updating the Z and N flags are in correct.
Single Data Transfer		9	STRB, LDRB not implemented therefor little endian not implemented shifted register addressing mode not implemented
These marks are not set to be summed up. i.e. larger sum doesn’t indicate better implementation			Such perfection and caring even for the tiniest details.