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SWI		10	
B/BL		10	
Barrel Shifter	Immediate	10	
	Shifted Register – 5 bit Shift	10	
	Shifted Register – Bottom byte of another register	10	Incorrect Sign checking in case of ASR
Conditional Execution		0	Not implemented
Data Processing Instruction	ADD, ADDC…	10	Not all instruction are implemented, however updating the N,Z,V,C status flags are implemented in case of Set Status flag is 1
	TST, TEQ, CMP and CMN	0	Not implemented
MUL and MULA		10	Perfect
Single Data Transfer		10	However this part of the code not well organized
These marks are not set to be summed up. i.e. larger sum doesn't indicate better implementation			You can't be compared by any other than Linus, Ritchie and Stroustrup. Just keep working hard don't settle.