Abdelrahman Soliman & Abdallah Azayem Team:

SWI		10	
B/BL		10	
Barrel Shifter	Immediate	10	
	Shifted Register – 5 bit Shift	10	
	Shifted Register – Bottom byte of another register	10	
Conditional Execution		10	
Data Processing Instruction	ADD, ADDC…	10	
	TST, TEQ, CMP and CMN	10	
MUL and MULA		10	
Single Data Transfer		10	
These marks are not set to be summed up. i.e. larger sum doesn't indicate better implementation			It's your hard work, passion and curiosity that drives you towards perfection. Always "stay hungry stay foolish".