Cairo University
Faculty of Engineering
Electronics & Comm. Dept.

جامعة القاهرة

Third Year
Electronics Project
ELC3060

Submission Notes:

- This project can be done in groups of 4 students or less.

- Project grade will be based on the submitted report and cadence files; any copied reports will be given Zero.

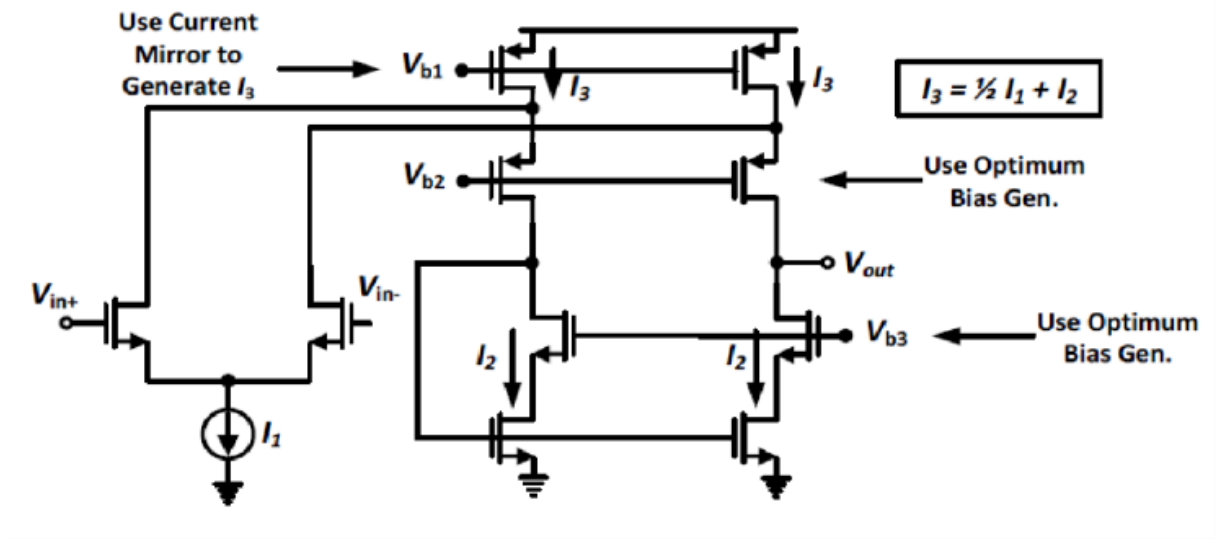
- The report is limited to 15 pages without the cover, half a point will be lost for each extra page.

- The cover page must contain the group names in Arabic and their ID's.

- All graphs and figures should be clear with readable axes and traces, and all schematics of the operating points and sizing should be included.

Dead line 1 May 2025 at 11:59 PM

Q1.Using the Vm of 65nm tsmc technology, design the following amplifier to achieve the following specs:



1- VDD= 3.3V
2- VinCM= 0.5*VDD
3- ADC (DC gain) > 58dB
4- GBW>150MHz for a load capacitance of 1pF
5- Slew rate > 100 V/usec
6- Output swing > 1.5 VPP
7- Input refered noise density < $30nv\ /\ \sqrt{Hz}$ (include thermal and flicker only)
8- PM > 60deg
9- GM > 12dB
10- Minimal power consumption and area.

• Do not use ideal current sources (assume that you have only one ideal current source of 25 µA coming from VDD). Use biasing circuit to generate I1 and optimum bias for Vb1, Vb2, and Vb3.

• Design all current mirrors to provide close to optimum compliance voltage (to obtain maximum output swing). BUT Adjust VDS of any transistor in the current mirror (or current source) to (Veff + 100 mV) in order to improve ro of this transistor.

Simulations

• Simulate the circuit (DC analysis - save operating point, AC analysis)
  – Print all transistor operating point information (DC)
  – Plot the gain and phase versus frequency (AC). Show open-loop gain and PM
  – Plot the common-mode rejection ratio (CMRR)
  – Plot the power supply rejection ratio (PSRR)

• Place the op-amp in a unity feedback (**Buffer**) configuration:
  – Simulate stability using STB analysis and IPROBE
  – Plot STB gain and phase versus frequency (AC) and calculate open-loop gain and PM – What is the difference between those results and previous open-loop AC results?
  – Plot the DC-gain versus Vout (report when DC-gain drops by 10dB to verify specifications) –
  – Plot closed-loop (CL) frequency response. What is the ACL and BWCL (comment)?
  – Simulate input-referred noise and tabulate top 4 contributors @10MHz (comment).
  – Simulate the slew rate and verify the specifications.
  – Apply a sine input signal of 1Vpp @ **10 MHz** and plot Vout (Add proper input DC value). Plot DFT (in dB) and calculate harmonic distortion (HD2, HD3, and THD) in dB.
  – Plot Vout for a small step input of 100mV (Add proper input DC value). Calculate the fractional gain error (FGE) and 1% settling time (compare with hand analysis).

You are required to deliver a report that contains:
1- **Schematic diagrams** (snapshots from Cadence showing dimensions and values)
2- **Design procedure** (hand calculations)
3- **Simulation results** (snapshots from Cadence)
4- **Discussion** of your results and conclusions