

1. Power

File: [1] Power.kicad_sch

2. Zynq Power and Decoupling

File: [2] Zynq Power and Decoupling.kicad_sch

3. Zynq Config, JTAG, Debug

File: [3] Zynq Config, JTAG, Debug.kicad_sch

4. Zynq Processing System (PS)

File: [4] Zynq Processing System (PS).kicad_sch

5. Zynq Programmable Logic (PL)

File: [5] Zynq Programmable Logic (PL).kicad_sch

6. Zynq DDR Interface & Termination

File: [6] Zynq DDR Interface & Termination.kicad_sch

7. 1GB DDR3L Modules

File: [7] 1GB DDR3L Modules.kicad_sch

8. Gigabit Ethernet

File: [8] Gigabit Ethernet.kicad_sch

9. USB 2.0 High-Speed (OTG)

File: [9] USB 2.0 High-Speed (OTG).kicad_sch

10. Mezzanine Connectors

File: [10] Mezzanine Connectors.kicad_sch

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File: MA_Inventronics.kicad_sch

Title: Xilinx-FPGA-10-Layer

Size: A3 Date: 2023-12-19

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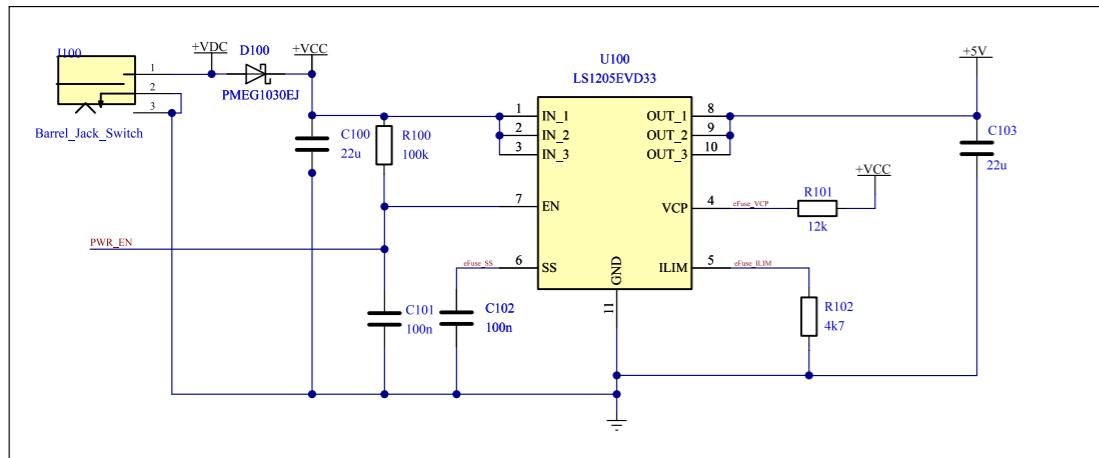
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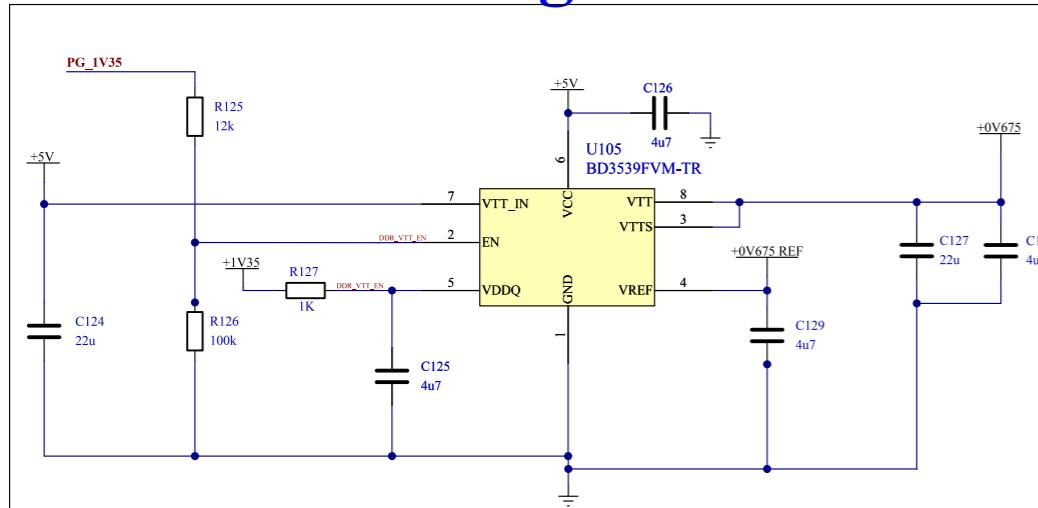


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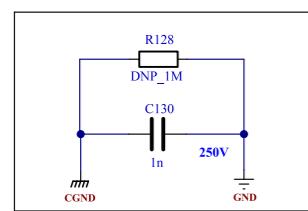
Input Power



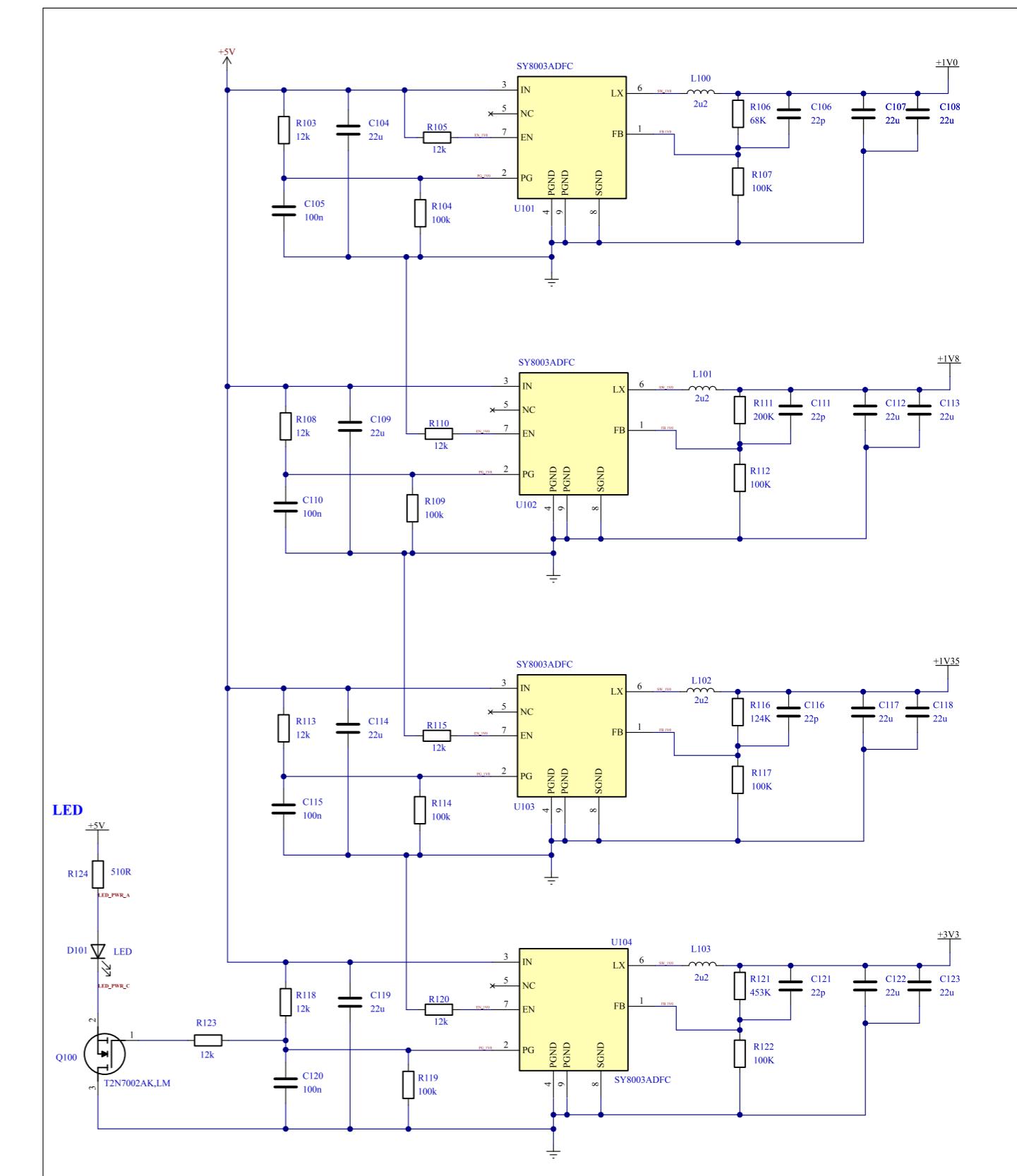
DDR3L VTT Regulator



Chassis GND Connection



Buck Convertors



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Title: [1] Power
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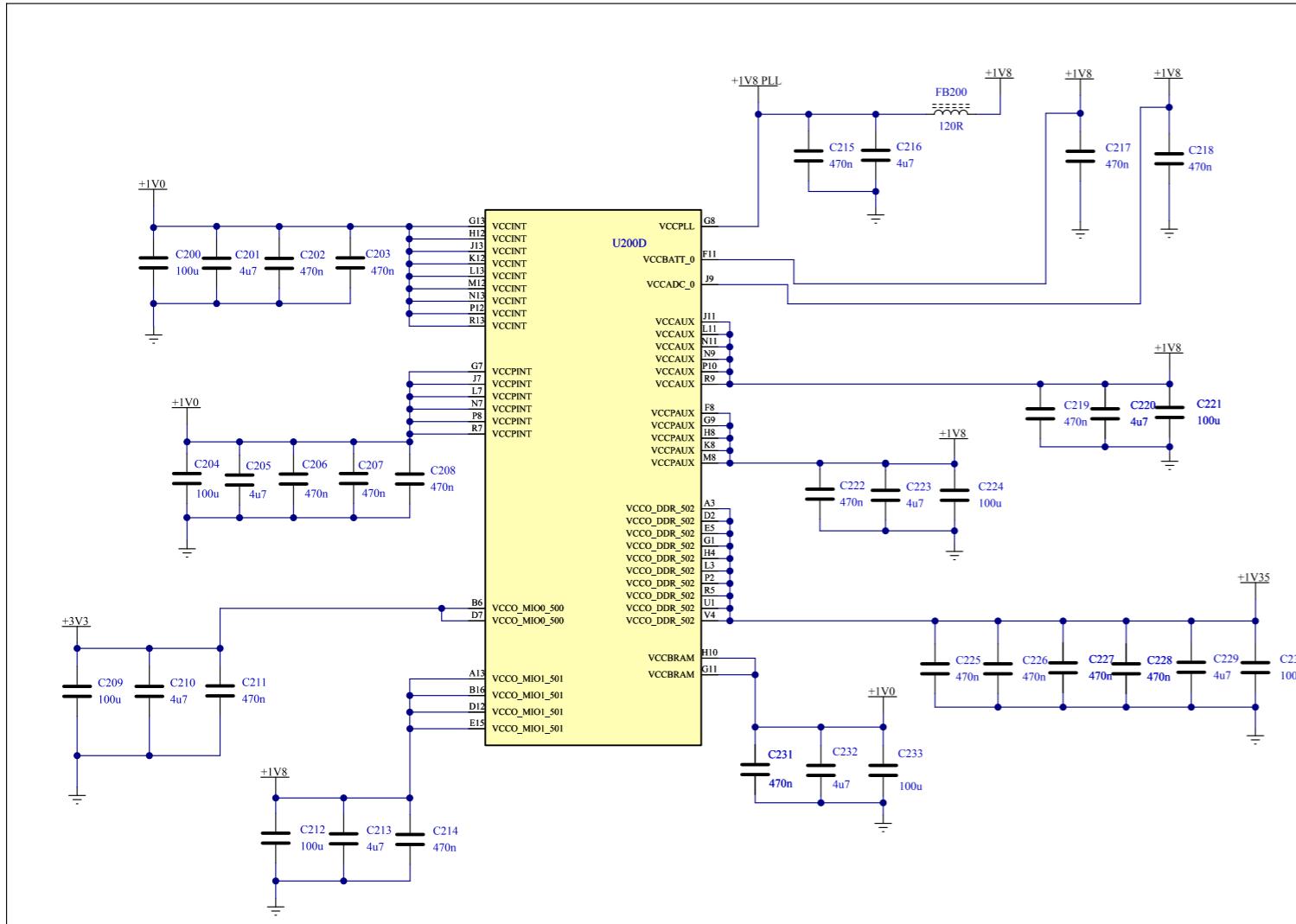
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2. Zynq Power and Decoupling

Bank Supplies



Xilinx Recommend Decoupling Caps

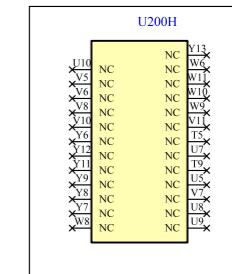
Table 3-2: Required PCB Capacitor Quantities per Device (PS)

Package	Device	V_{CCPINT} 100 μF	$V_{CCPAUX}^{(1)}$ 4.7 μF	V_{CCO_DDR} 100 μF	V_{CCO_MIO0} 4.7 μF	V_{CCO_MIO1} 4.7 μF	$V_{CCPLL}^{(2)(3)}$ 4.7 μF
CLG225	Z-7007S	1	1	3	1	1	1
CLG400	Z-7007S	1	1	3	1	1	1
CLG225	Z-7010	1	1	3	1	1	1
CLG400	Z-7010	1	1	3	1	1	1

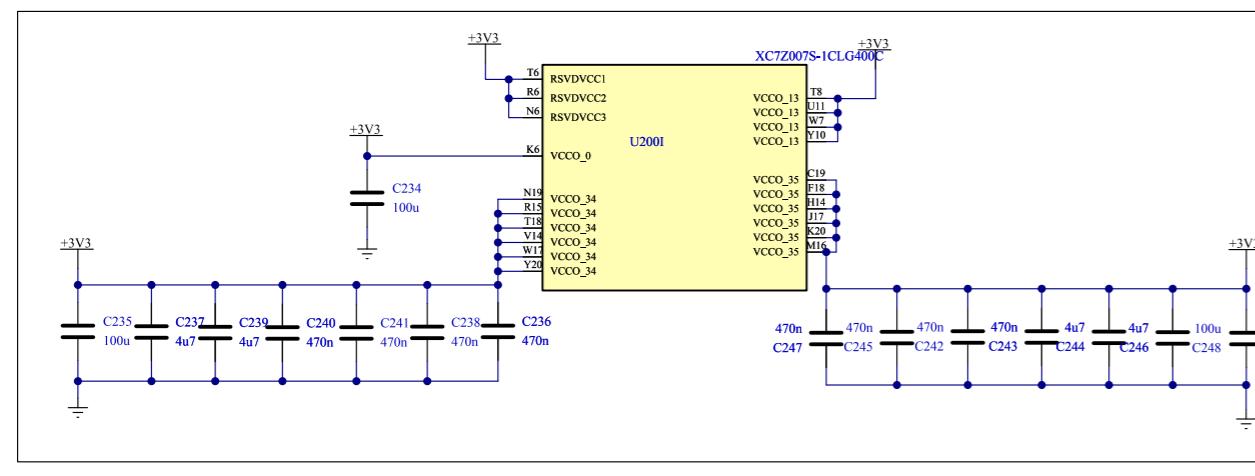
Table 3-1: Required PCB Capacitor Quantities per Device (PL)

Package	Device	V_{CCINT} 680 μF	V_{CCBRAM} 330 μF	V_{CCAUX} 100 μF	V_{CCAUX_ID} 4.7 μF	$V_{CCO\ per\ Bank}^{(4)(5)}$ 4.7 μF or 100 μF	Bank 0
CLG225	Z-7007S	0	0	1	1	2	NA
CLG400	Z-7007S	0	0	1	1	2	0
CLG225	Z-7010	0	0	1	1	2	NA
CLG400	Z-7010	0	0	1	1	2	NA

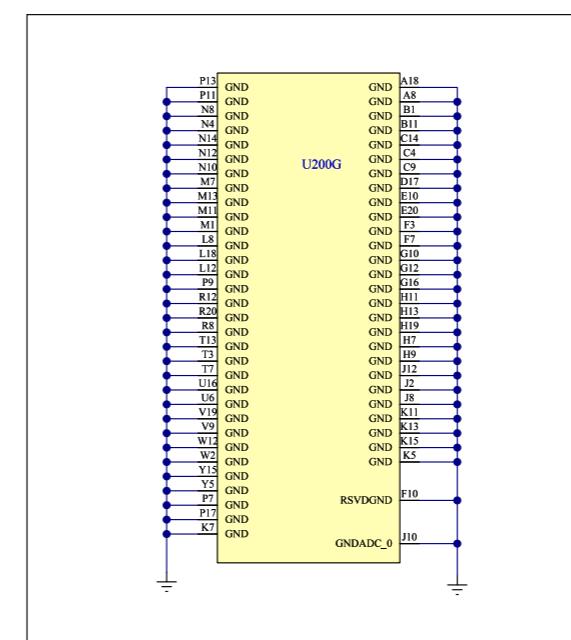
Unused Pins



Bank Supplies



GND Connections



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Sheet: 2. Zynq Power and Decoupling/
File: [2] Zynq Power and Decoupling.kicad_sch

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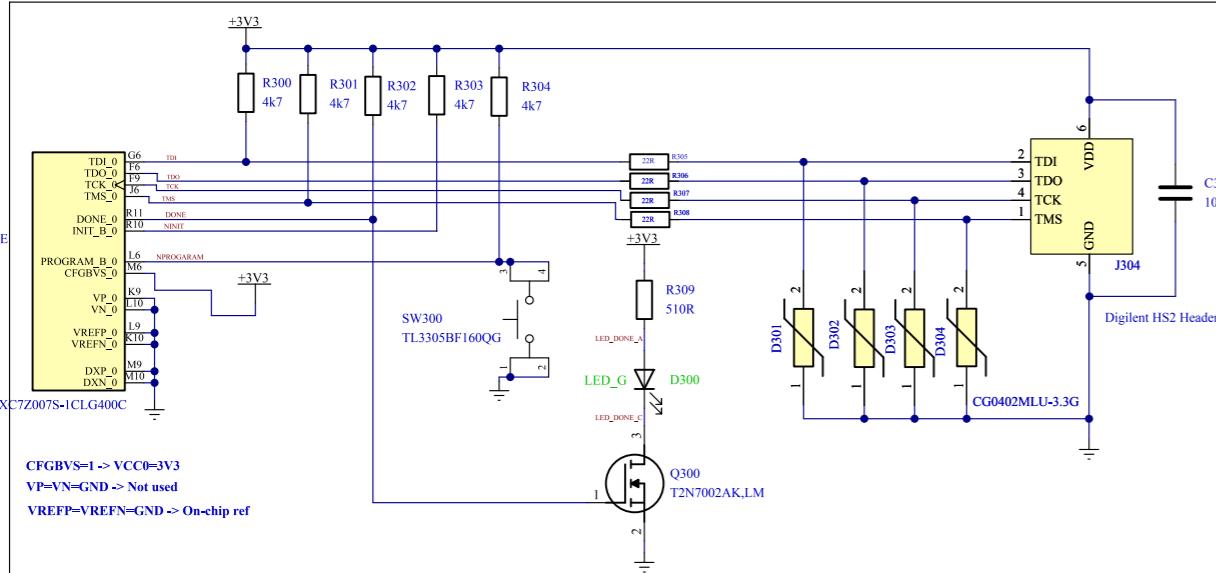
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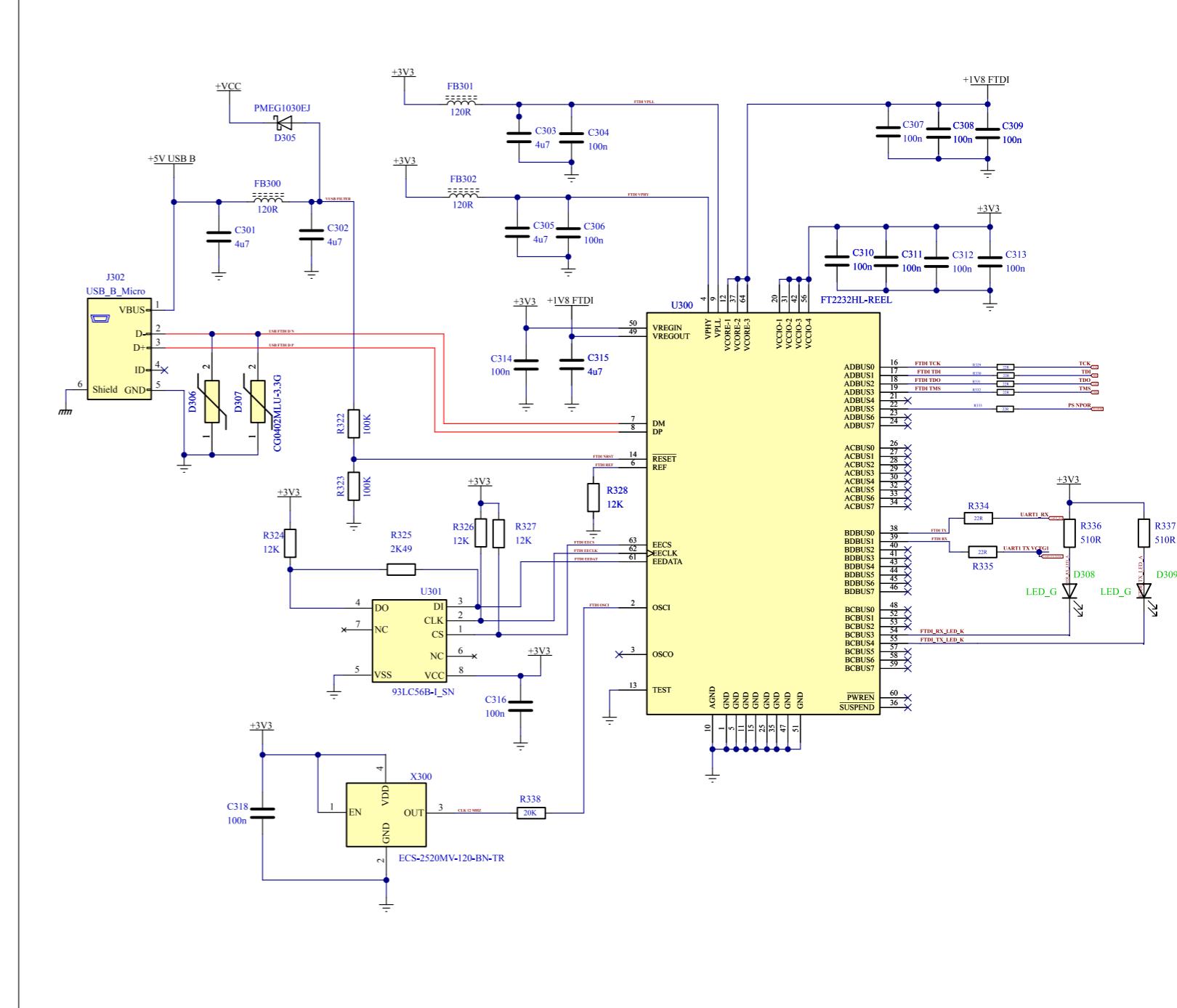
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3. Zynq Config, JTAG, Debug

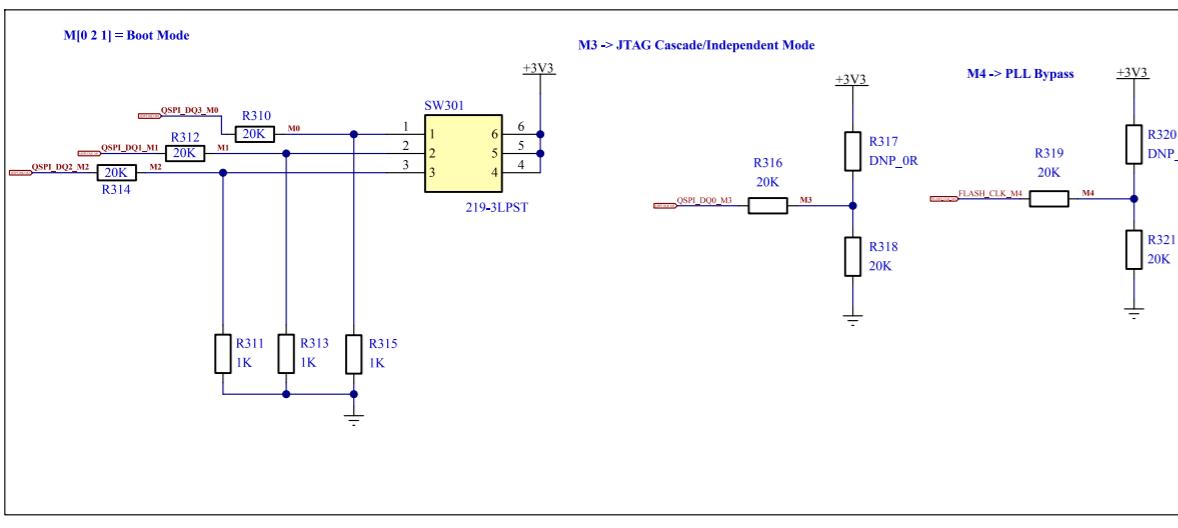
Zynq Config, JTAG



FTDI JTAG Programmer and USB-to-UART



Boot Mode MIO Strapping Pins (Zynq TRM p167)



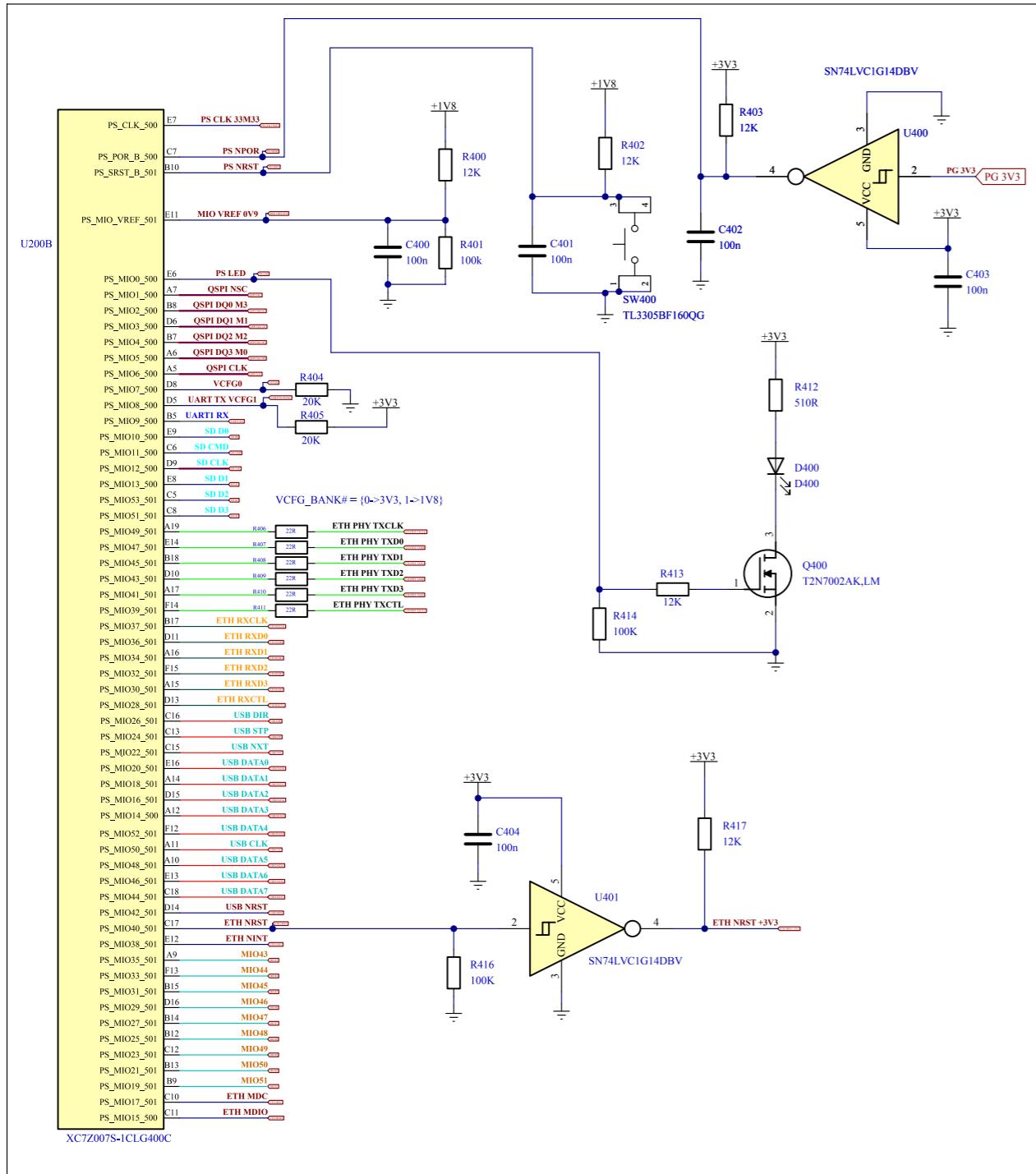
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Sheet: [3] Zynq Config, JTAG, Debug/
File: [3] Zynq Config, JTAG, Debug.kicad_sch

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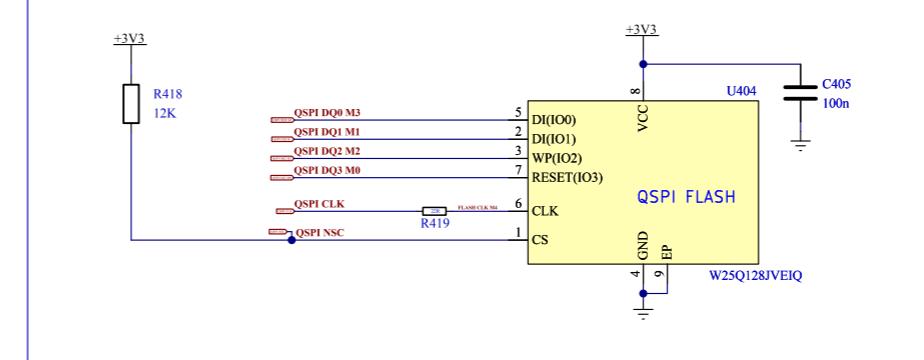
4. Zynq Processing System (PS)

Zynq PS (Bank 500 & 501)

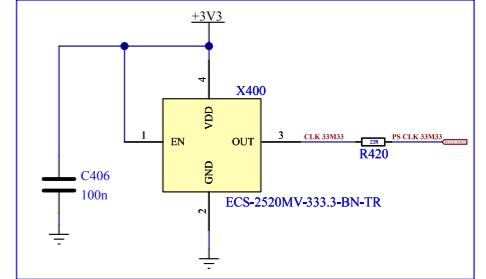


Bank 1 I/O Voltage = 1.8V due to HSTL requirement (high-speed for USB + Ethernet)

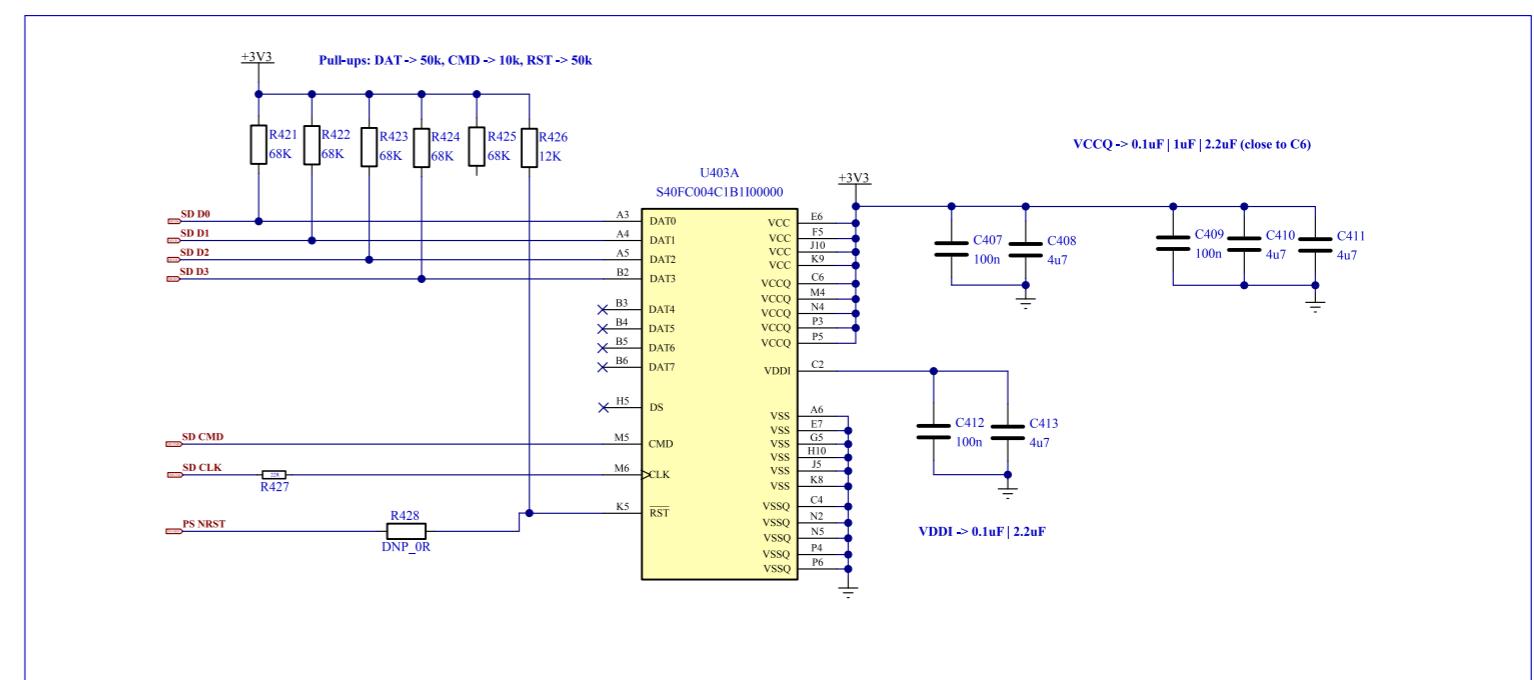
QSPI Flash Memory (128MBit)



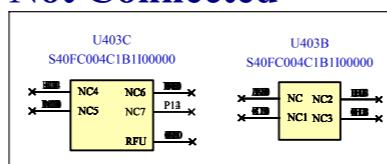
PS Clock (33.33 MHz)



EMMC Memory



Not Connected



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Sheet: 4. Zynq Processing System (PS)/
File: [4] Zynq Processing System (PS).kicad_sch

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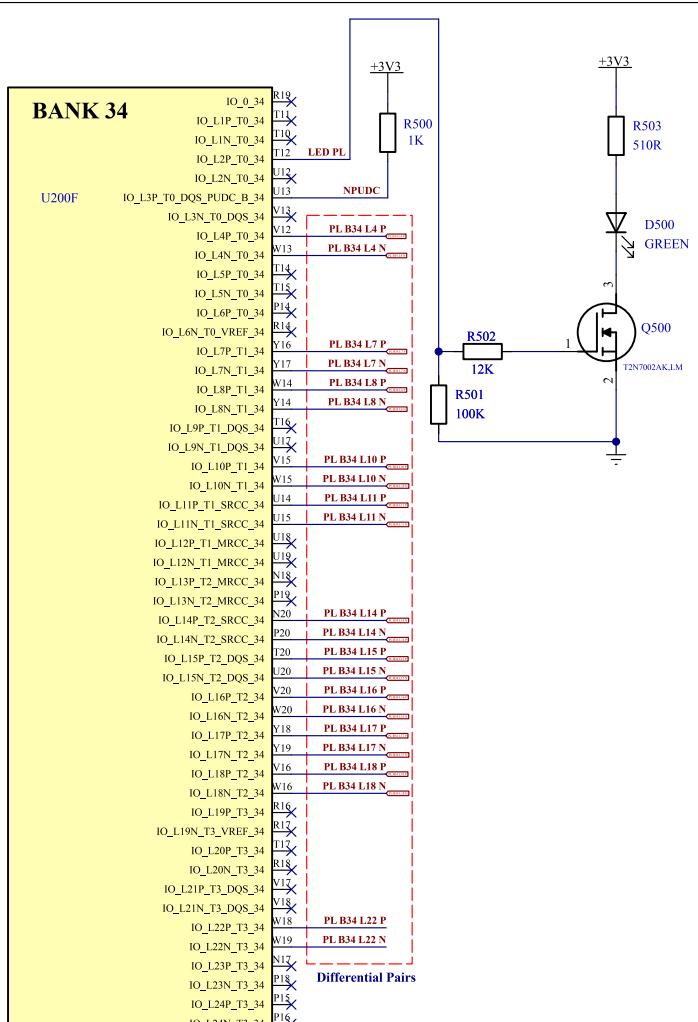
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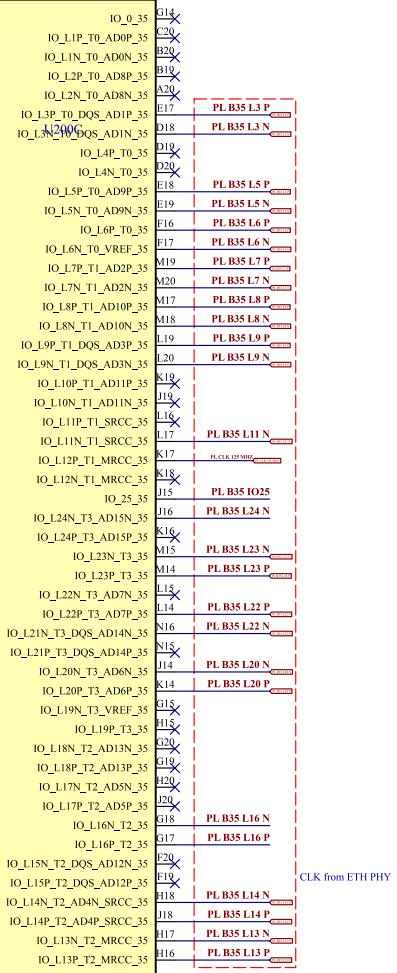


5. Zynq Programmable Logic (PL)

Bank 34



Bank 35



XC7Z007S-1CLG400C

XC7Z007S-1CLG400C

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Sheet: /5. Zynq Programmable Logic (PL)/
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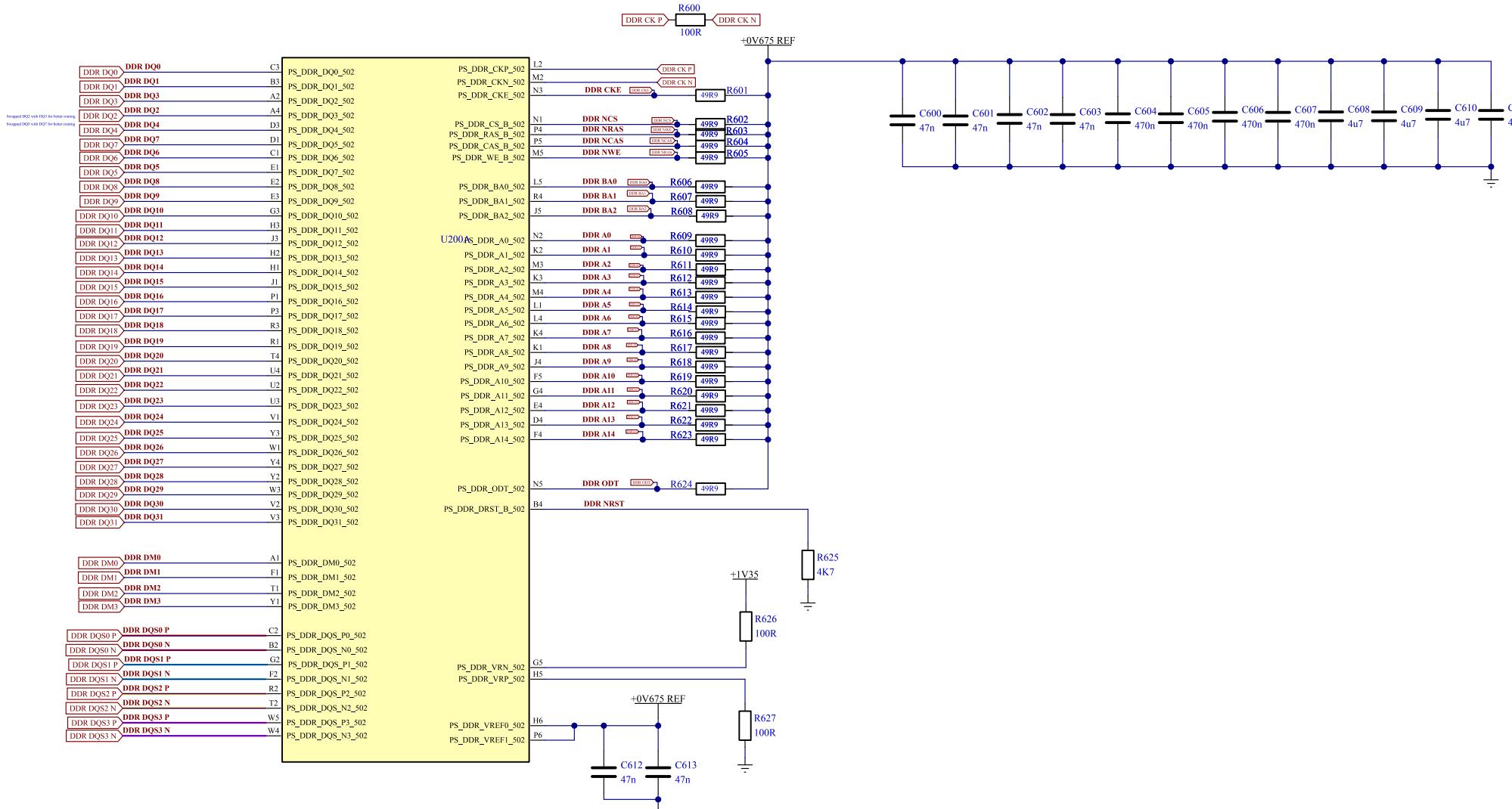
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6. Zynq DDR Interface & Termination

A



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 File: [6] Zynq DDR Interface & Termination.kicad_sch

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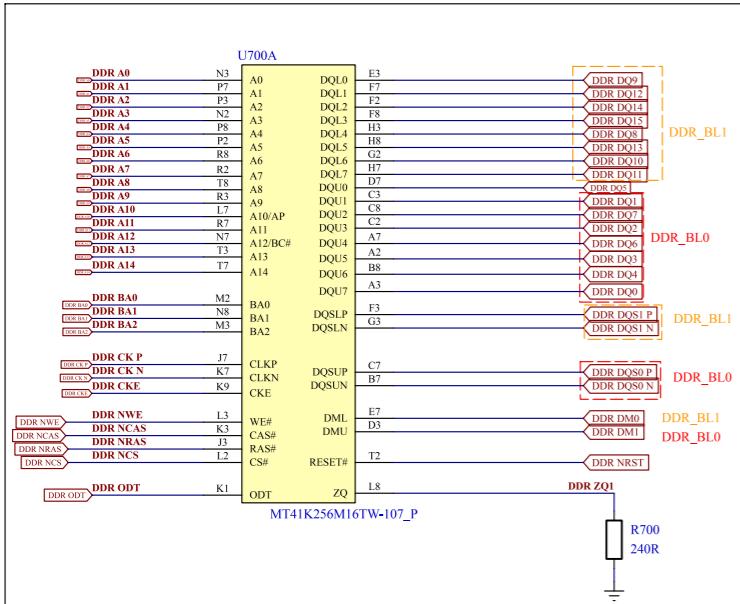
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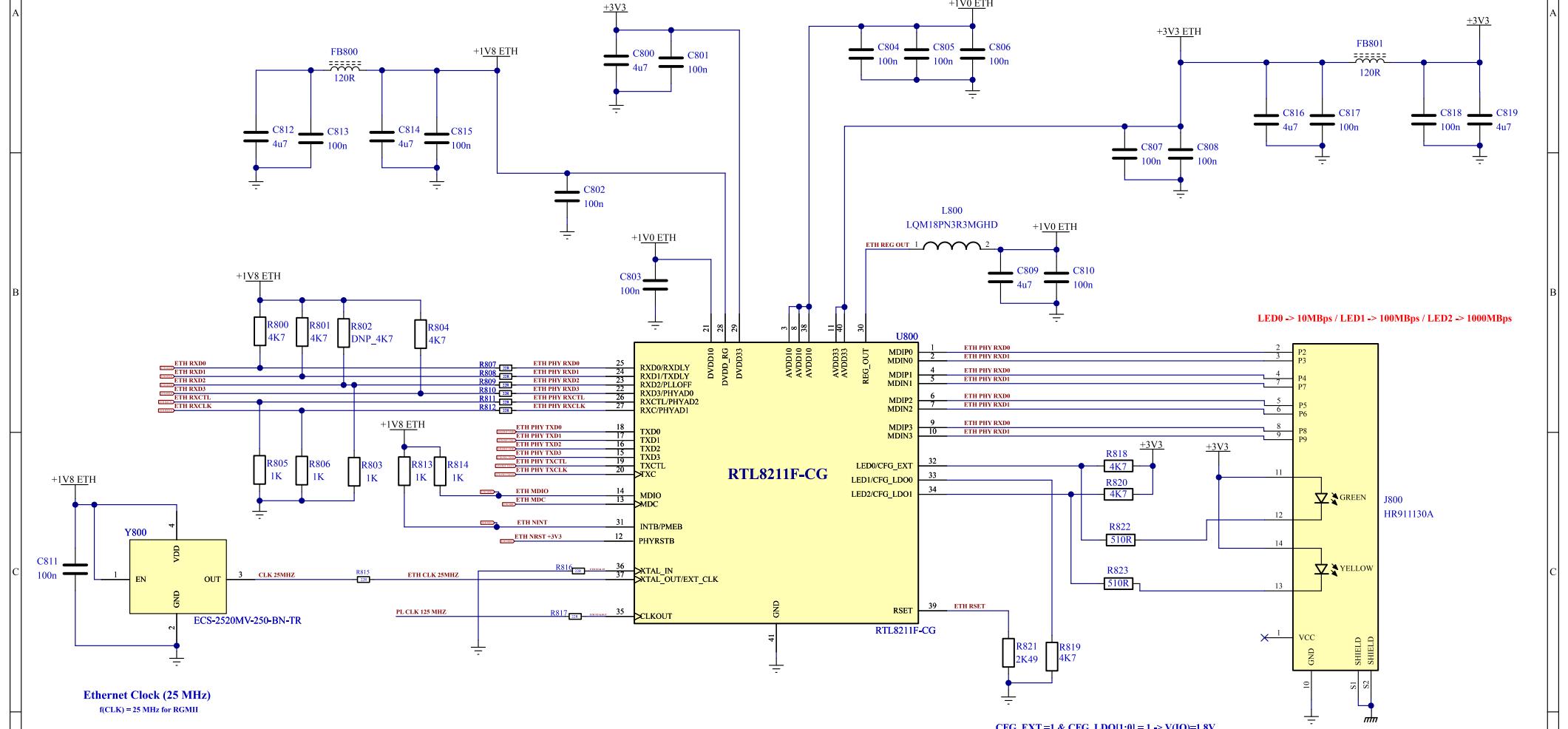
D

7. 1GB DDR3L Modules

ACC & DAT Connections



8. Gigabit Ethernet



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Sheet: /8. Gigabit Ethernet/
 File: [8] Gigabit Ethernet.kicad_sch

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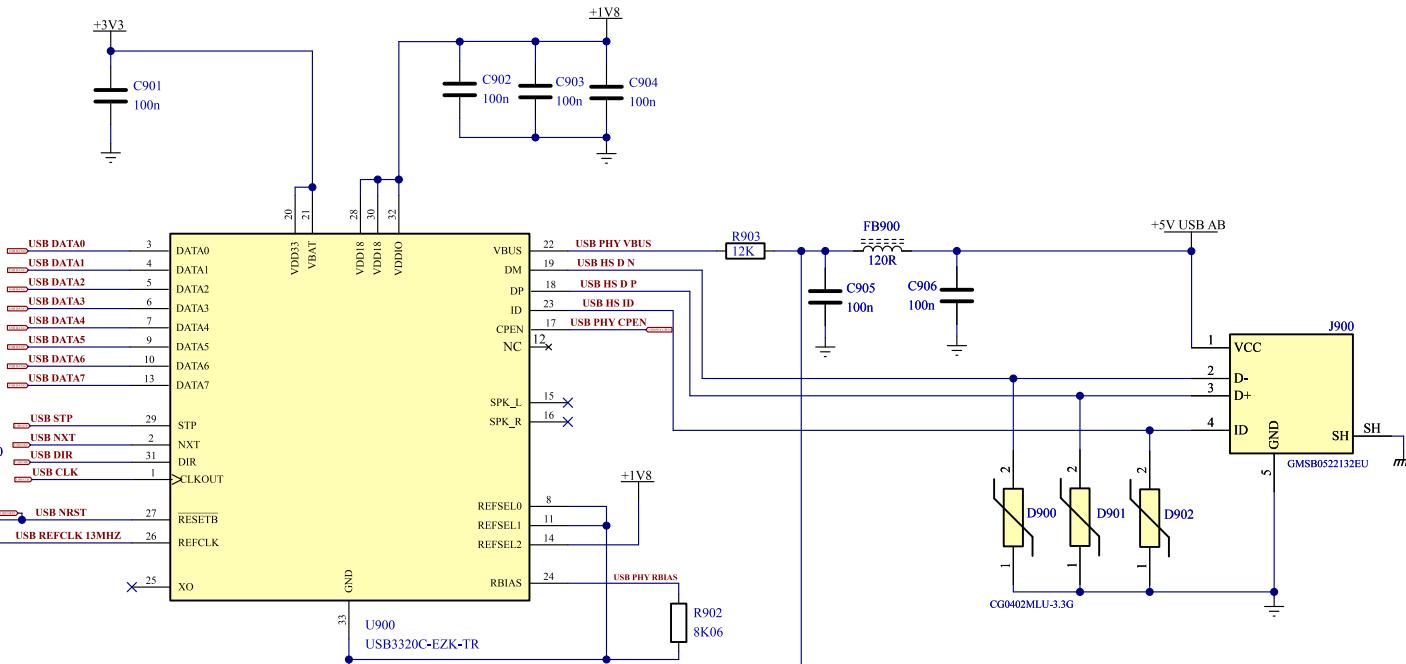
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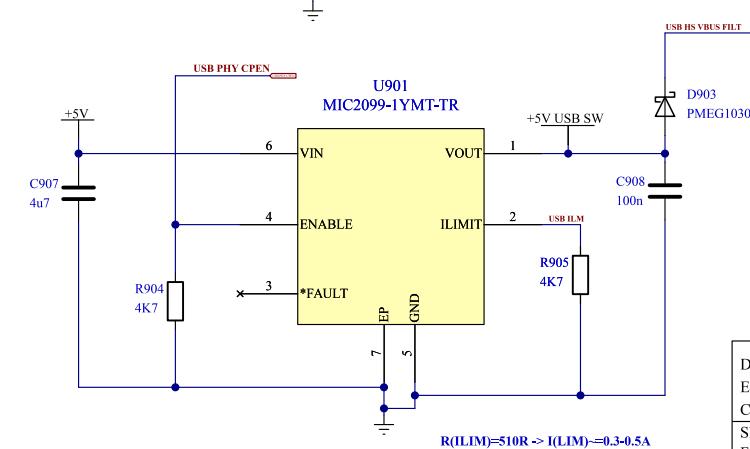
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9. USB 2.0 High-Speed (OTG)

A



B



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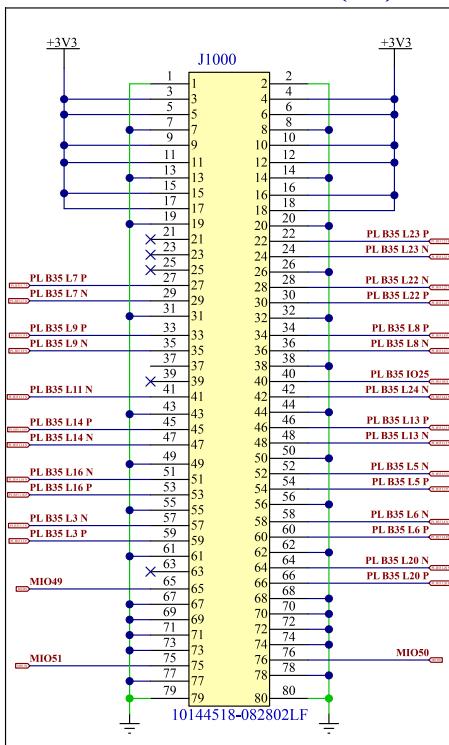
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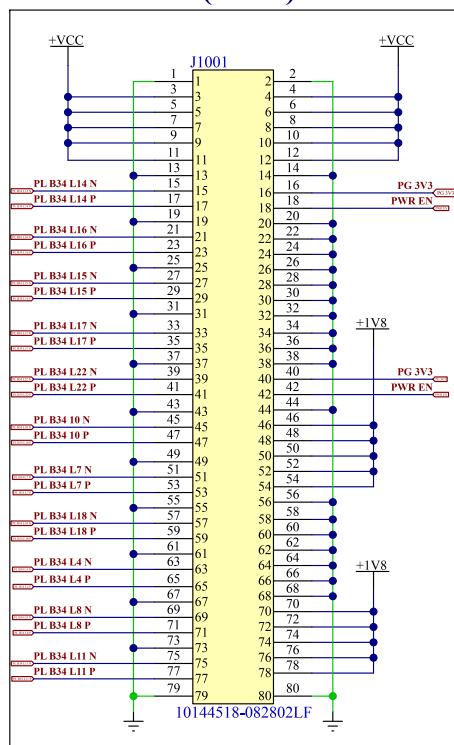


10. Mezzanine Connectors

PS MIO & PL Bank 35 (SE)



PL Bank 34 (DIFF)



- H901 MountingHole
- H902 MountingHole
- H903 MountingHole
- H904 MountingHole

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