

MA Xilinx-FPGA-10-Layer

1. Power

2. Zynq Power and Decoupling

3. Zynq Config, JTAG, Debug

File: [1] Power.kicad_sch

File: [2] Zynq Power and Decoupling.kicad_sch

File: [3] Zynq Config, JTAG, Debug.kicad_sch

4. Zynq Processing System (PS)

5. Zynq Programmable Logic (PL)

6. Zynq DDR Interface & Termination

File: [4] Zynq Processing System (PS).kicad_sch

File: [5] Zynq Programmable Logic (PL).kicad_sch

File: [6] Zynq DDR Interface & Termination.kicad_sch

7. 1GB DDR3L Modules

8. Gigabit Ethernet

9. USB 2.0 High-Speed (OTG)

File: [7] 1GB DDR3L Modules.kicad_sch

File: [8] Gigabit Ethernet.kicad_sch

File: [9] USB 2.0 High-Speed (OTG).kicad_sch

10. Mezzanine Connectors

File: [10] Mezzanine Connectors.kicad_sch

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COMPANY: INVENTIVETRONICS
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File: MA_Inventronics.kicad_sch

Title: Xilinx-FPGA-10-Layer

Size: A3 Date: 2023-12-19

KiCad E.D.A. kicad 7.0.2-0

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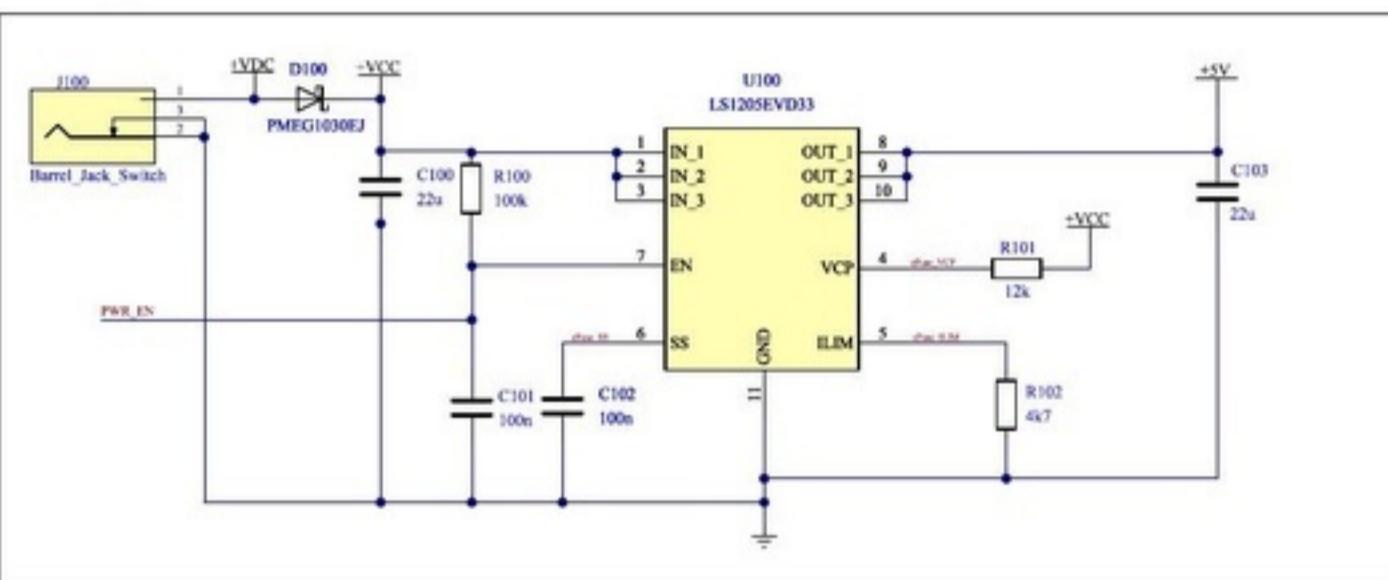
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Id: 1/11

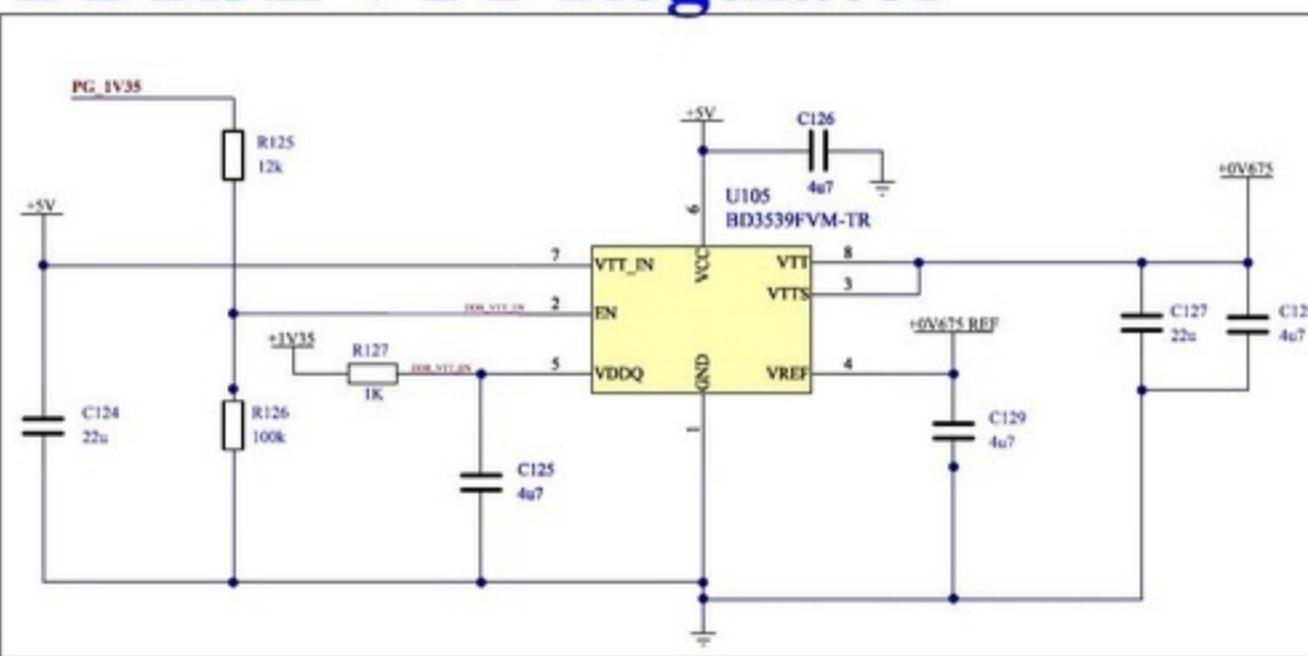
1. Power

Buck Convertors

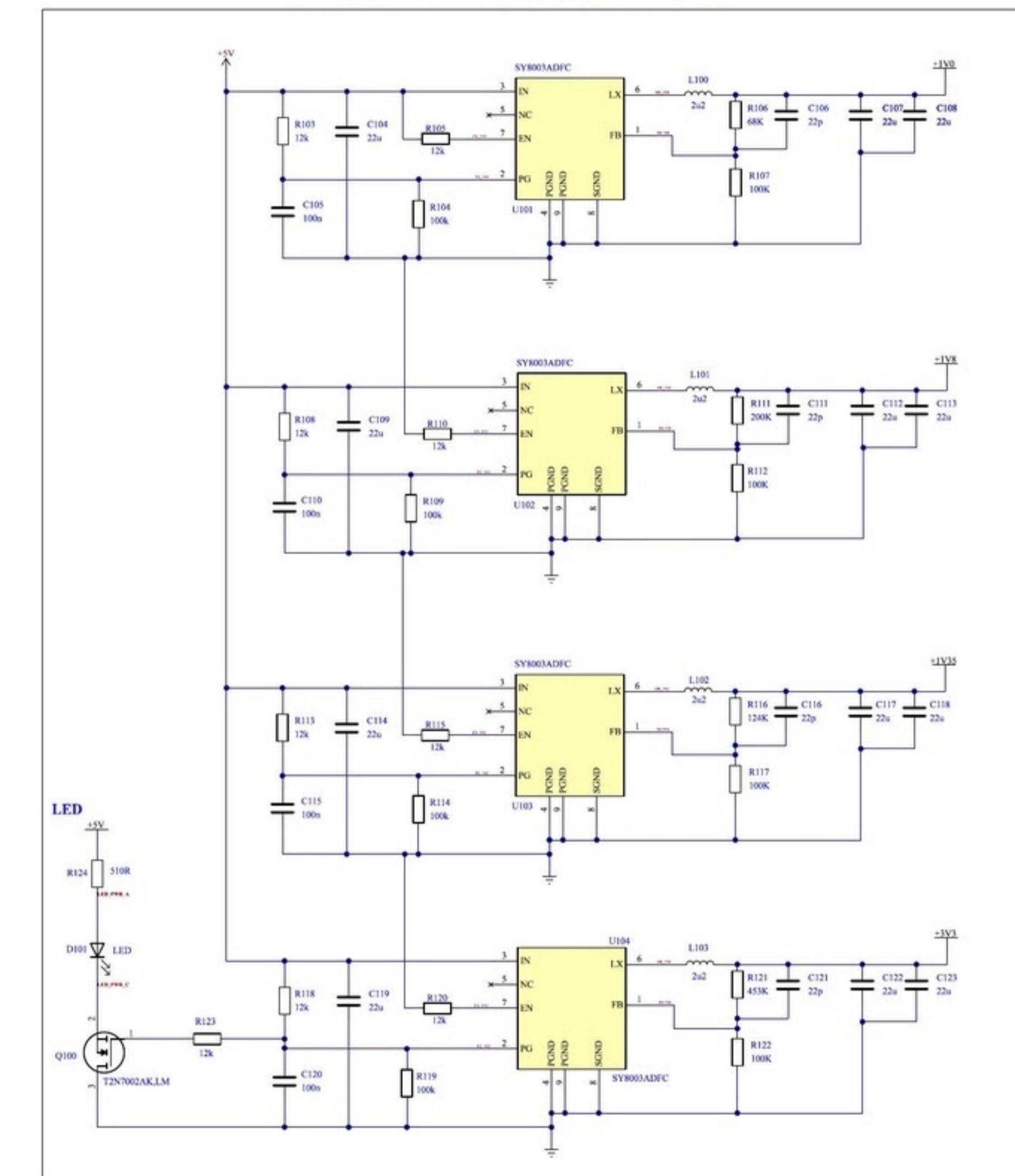
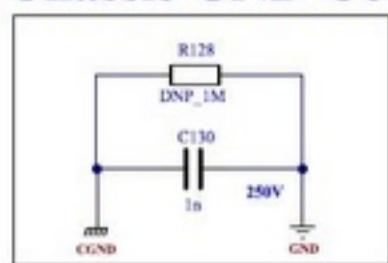
Input Power



DDR3L VTT Regulator



Chassis GND Connection



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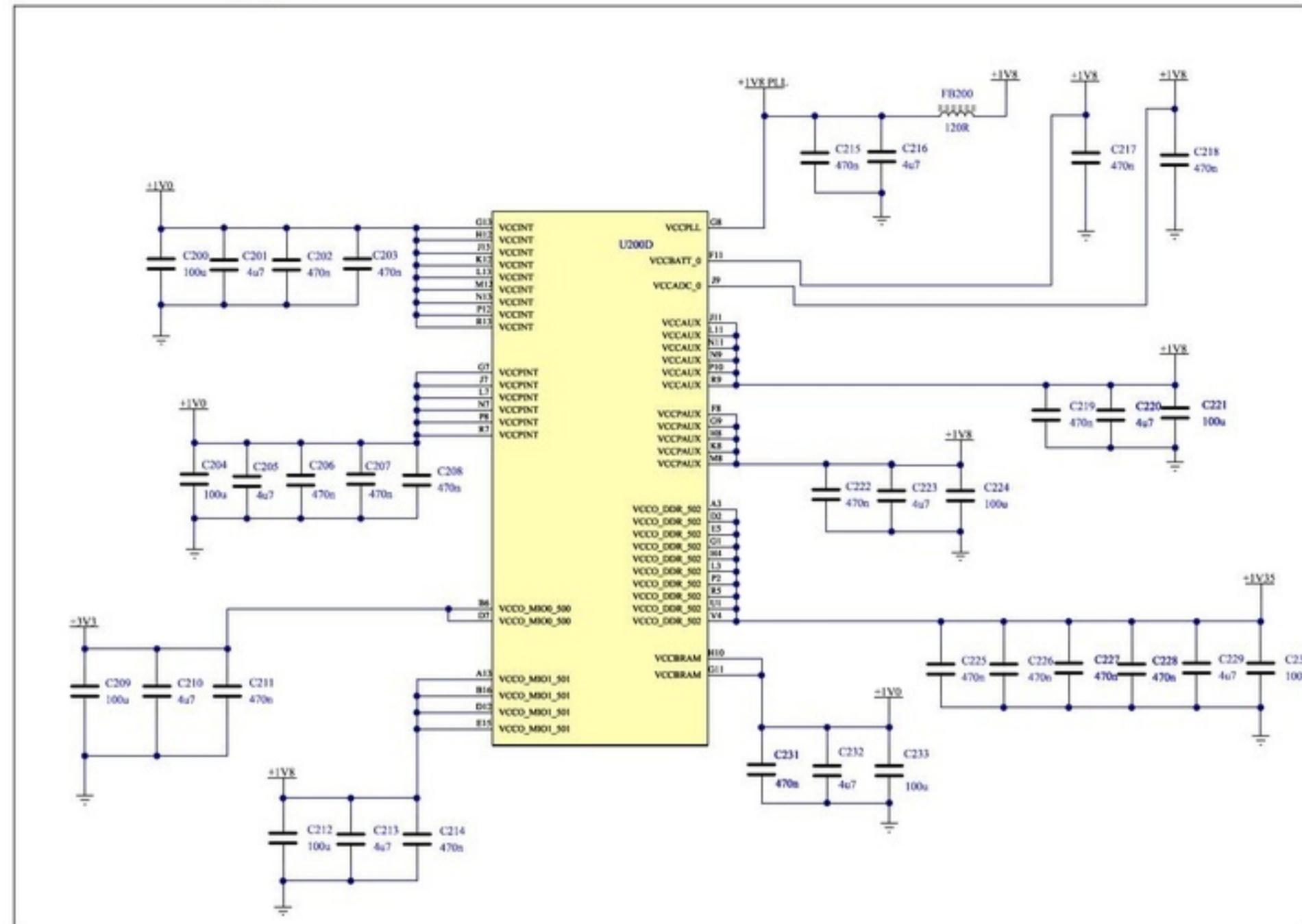
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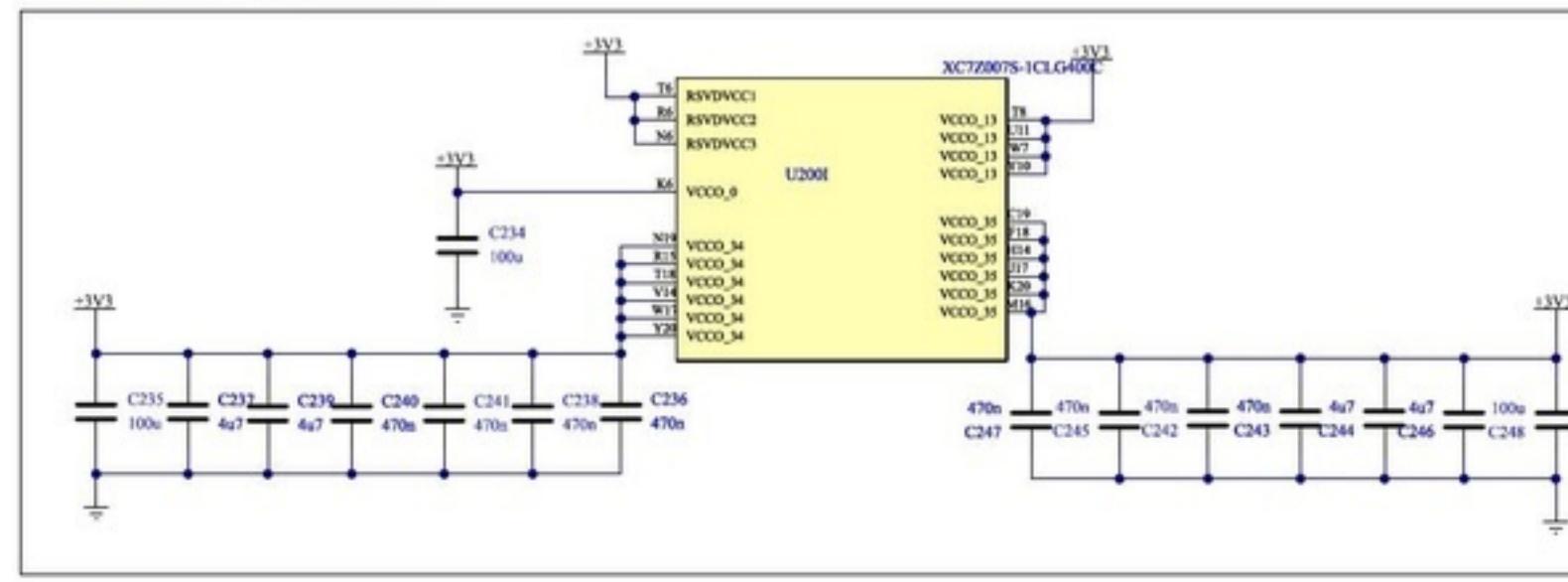
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Id: 6/11

Bank Supplies



Bank Supplies



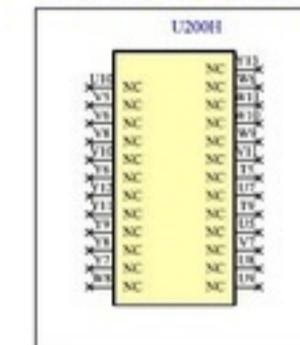
Xilinx Recommend Decoupling Caps

Table 3-2: Required PCB Capacitor Quantities per Device (PS)

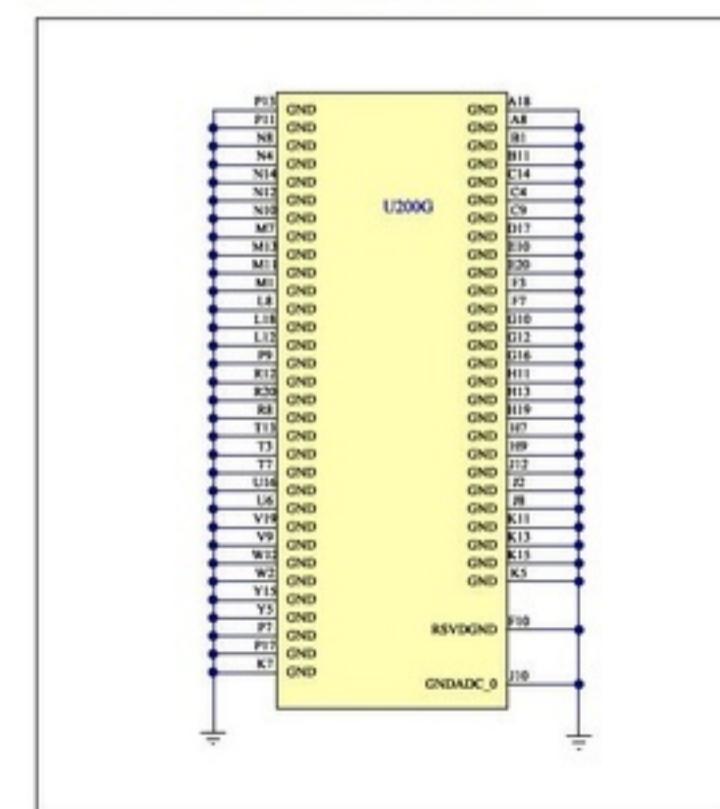
Table 3-1: Required PCB Capacitor Quantities per Device (PL)

Package	Device	Required PCB Capacitor Quantities per Device (Ref)												Bank					
		V _{DQINT}			V _{DQDRAM}			V _{DQAI}			V _{DQHIO}			V _{DQ0} per Bank					
680 μF/ μF	330 μF/ μF	100 μF/ μF	4.7 μF/ μF	0.47 μF/ μF	100 μF/ μF	47 μF/ μF	4.7 μF/ μF	0.47 μF/ μF	47 μF/ μF	4.7 μF/ μF	0.47 μF/ μF	47 μF/ μF	4.7 μF/ μF	0.47 μF/ μF	47 μF/ μF or 100 μF/ μF	4.7 μF/ μF	0.47 μF/ μF	47 μF/ μF	
CUG225	Z-70075	0	0	1	1	2	N/A	N/A	N/A	1	1	1	N/A	N/A	N/A	1	2	4	1
CUG400	Z-70075	0	0	1	1	2	0	1	1	1	1	1	N/A	N/A	N/A	1	2	4	1
CUG225	Z-7010	0	0	1	1	2	N/A	N/A	N/A	1	1	1	N/A	N/A	N/A	1	2	4	1
CUG400	Z-7010	0	0	1	1	2	0	1	1	1	1	1	N/A	N/A	N/A	1	2	4	1

Unused Pins



GND Connections



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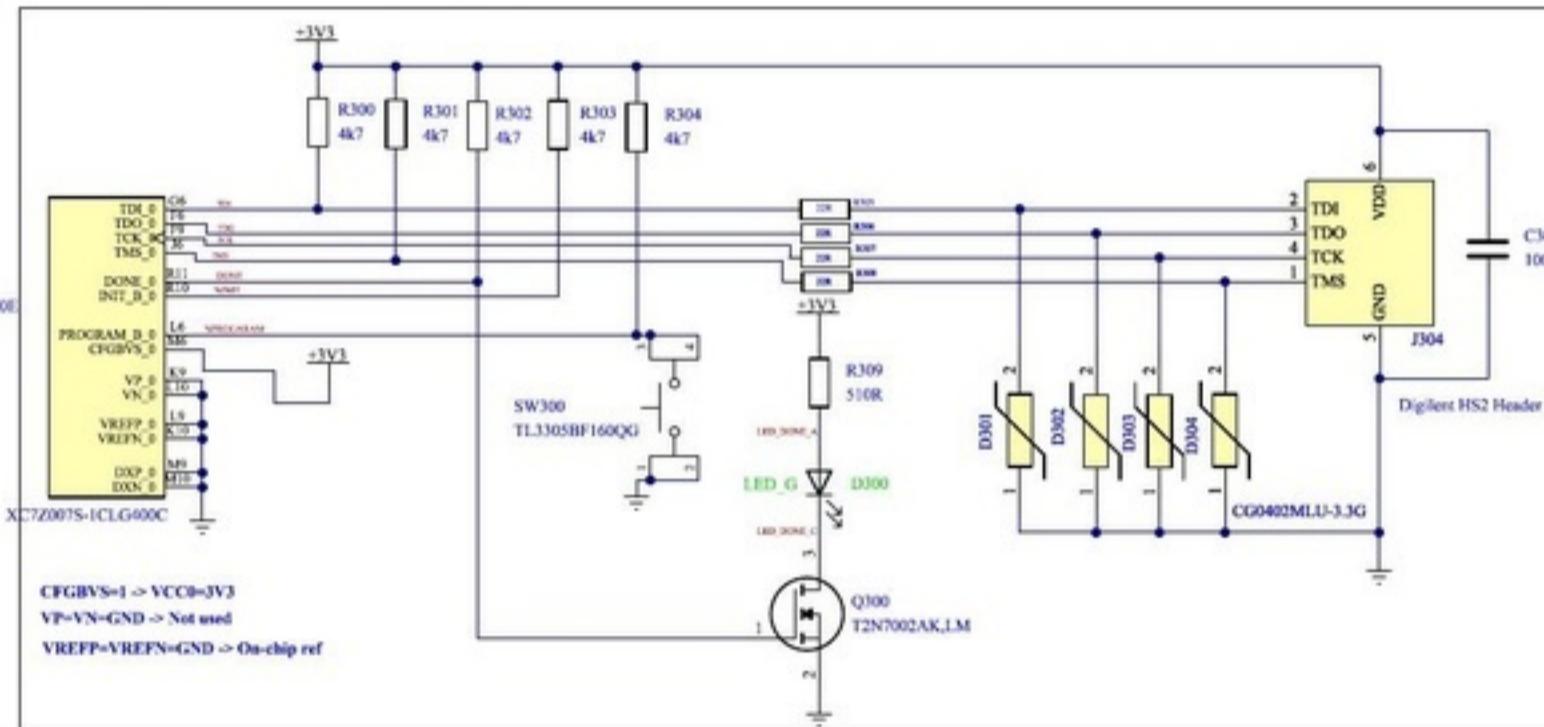
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10

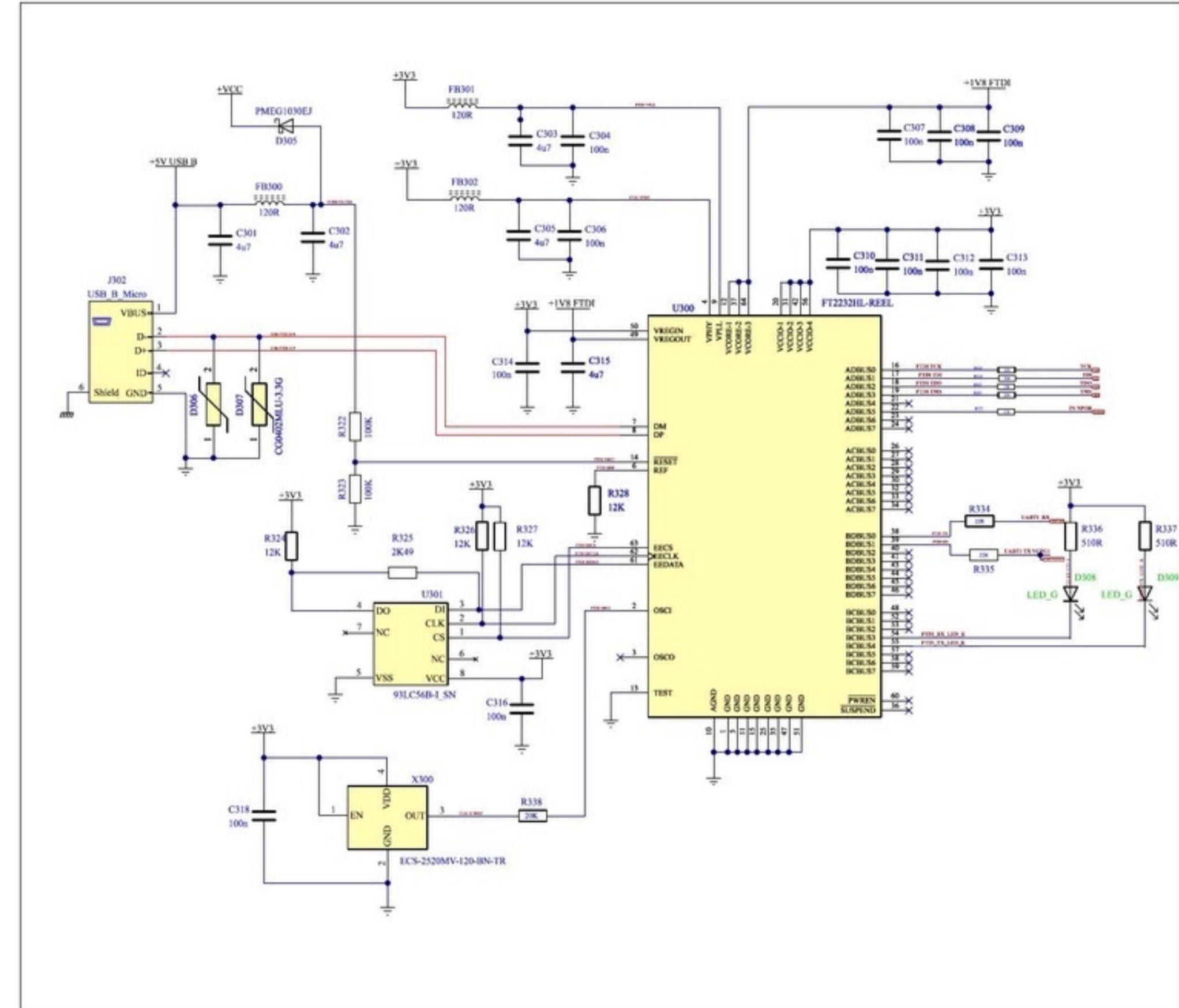
REV:
14-11/11

3. Zynq Config, JTAG, Debug

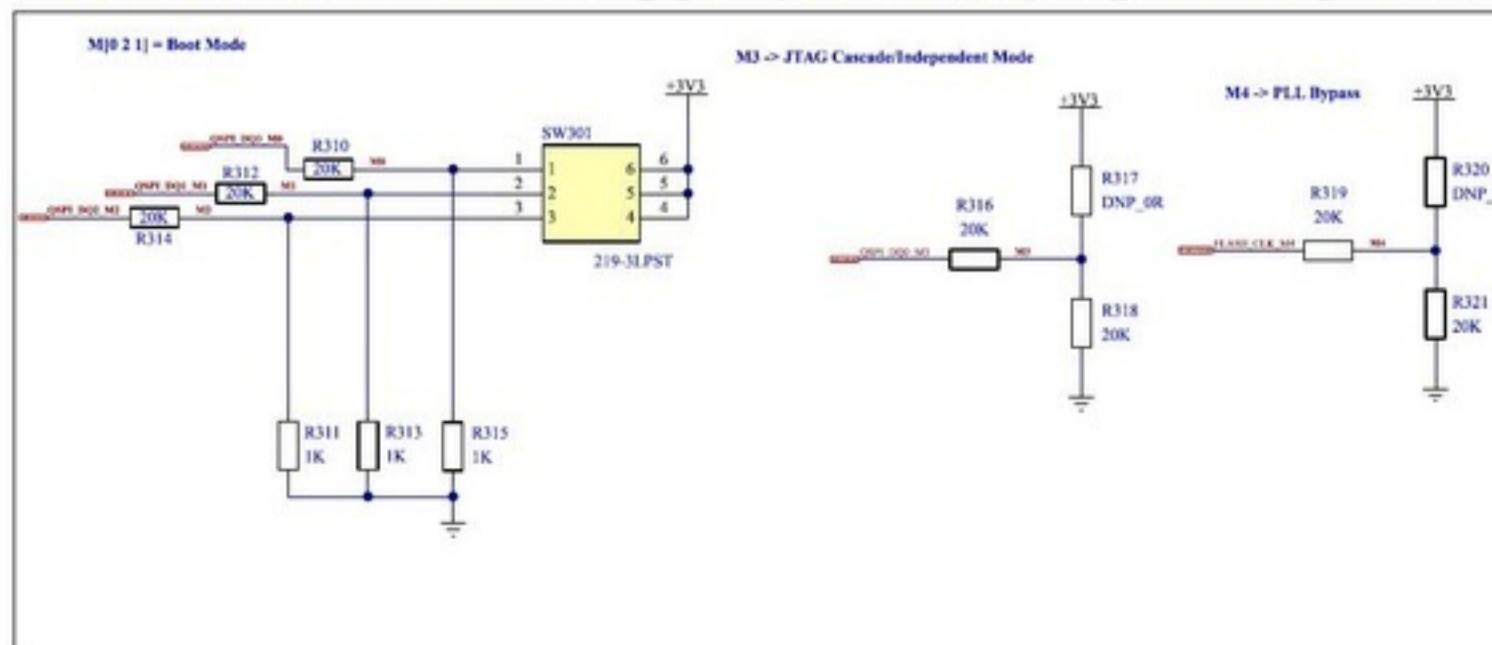
Zynq Config, JTAG



FTDI JTAG Programmer and USB-to-UART



Boot Mode MIO Strapping Pins (Zynq TRM p167)



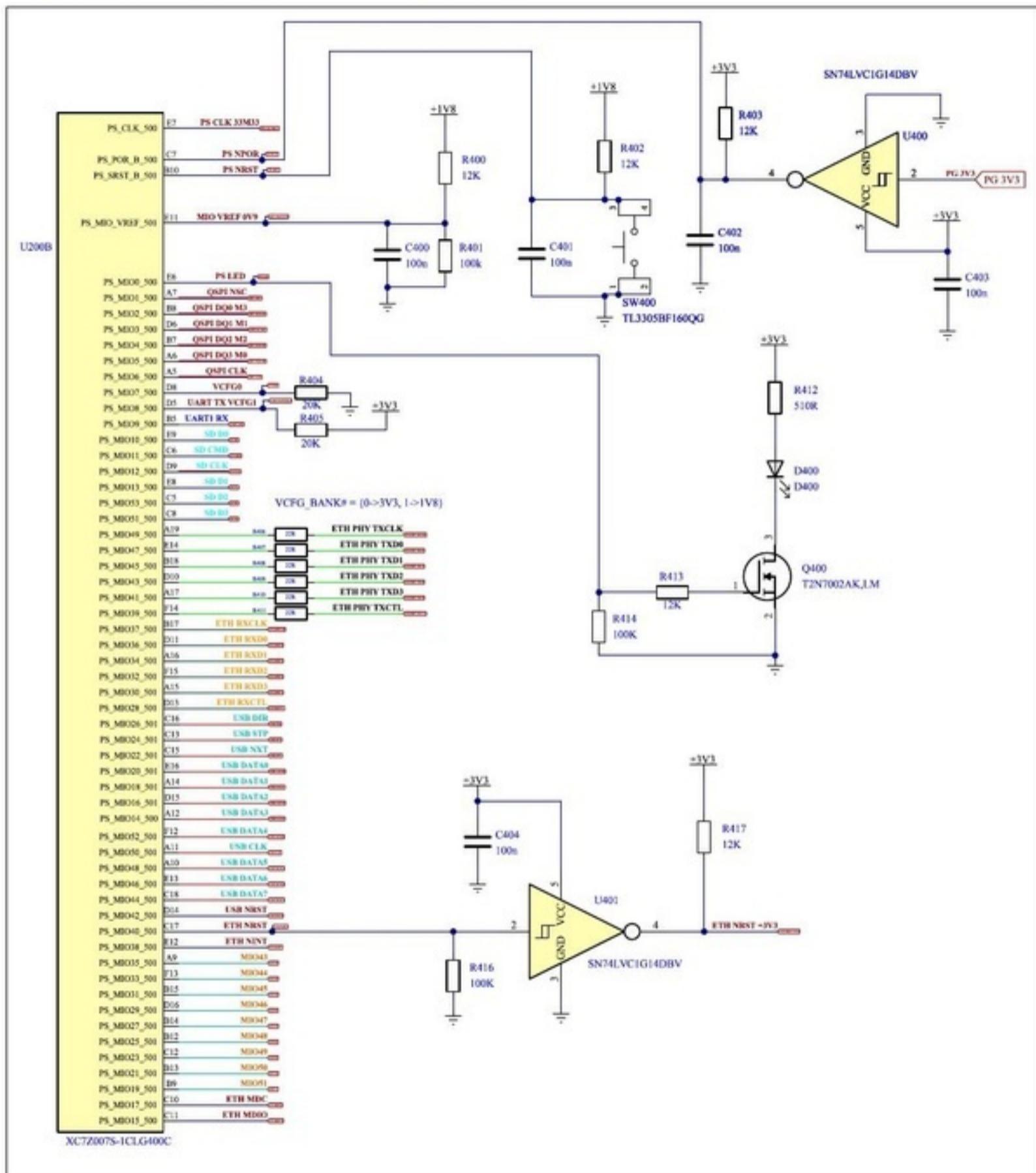
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Sheet: 3. Zynq Config, JTAG, Debug/
File: [3] Zynq Config, JTAG, Debug.kicad_sch

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Size: A3 Date: 2023-12-27
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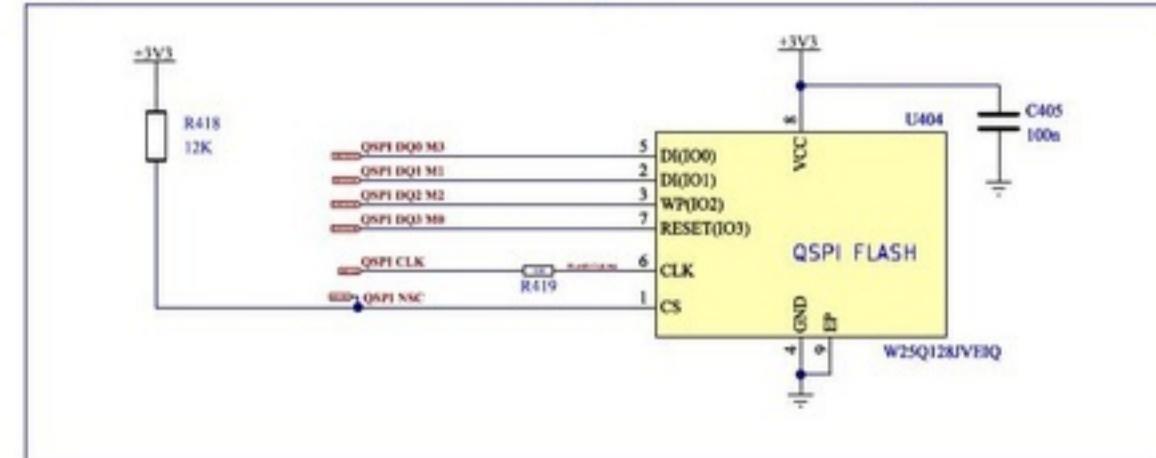
4. Zynq Processing System (PS)

Zynq PS (Bank 500 & 501)

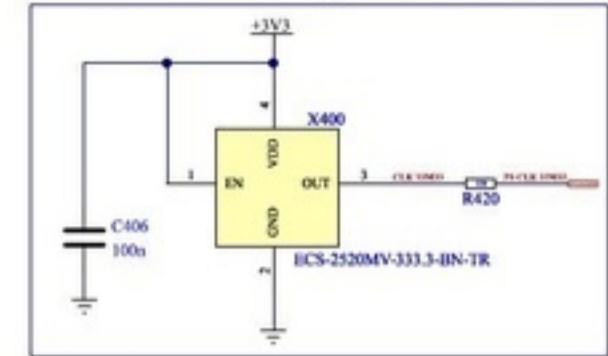


Bank 1 I/O Voltage = 1.8V due to HSTL requirement (high-speed for USB + Ethernet)

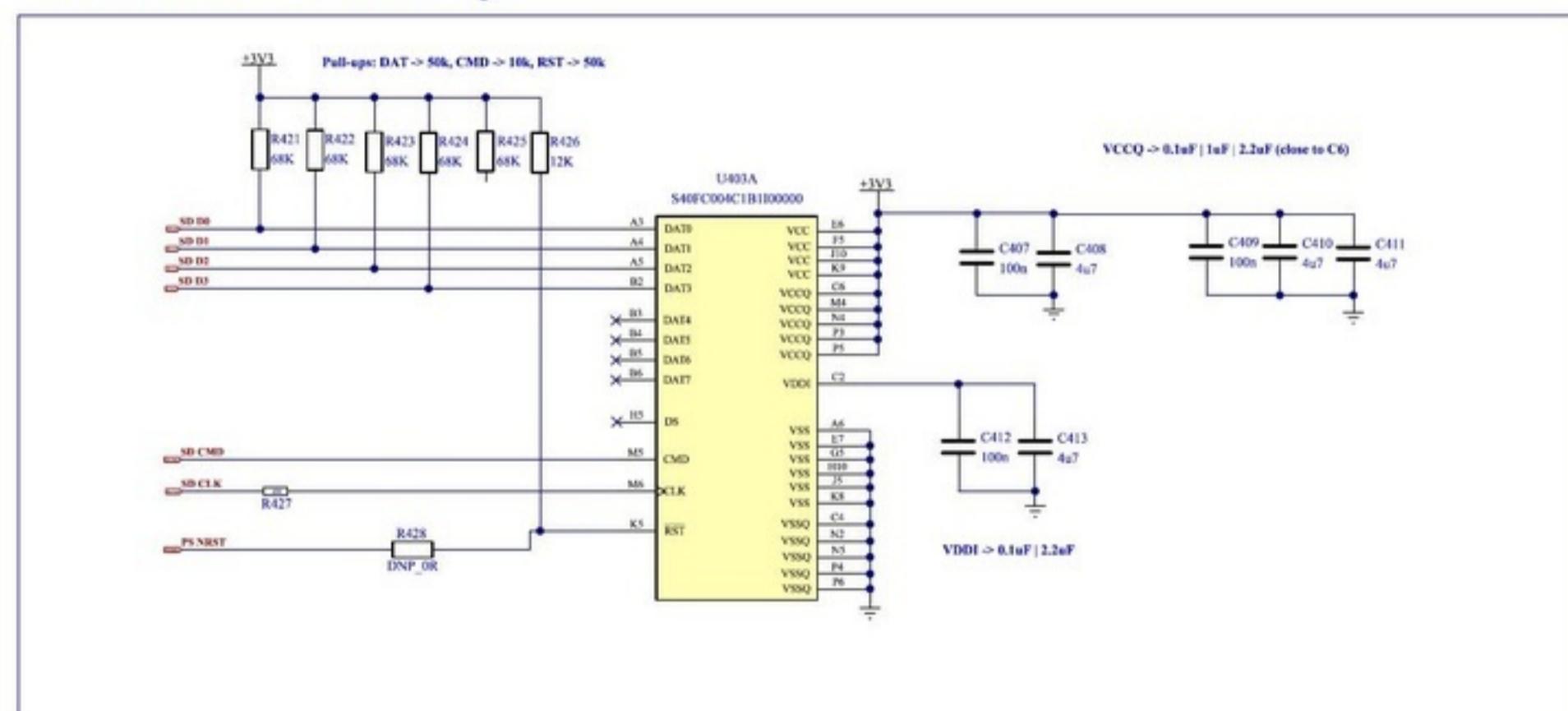
QSPI Flash Memory (128MBit)



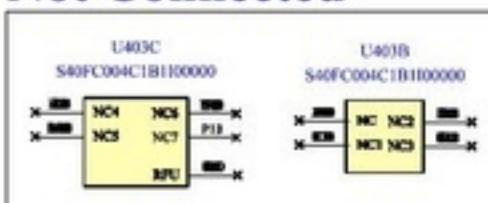
PS Clock (33.33 MHz)



EMMC Memory



Not Connected



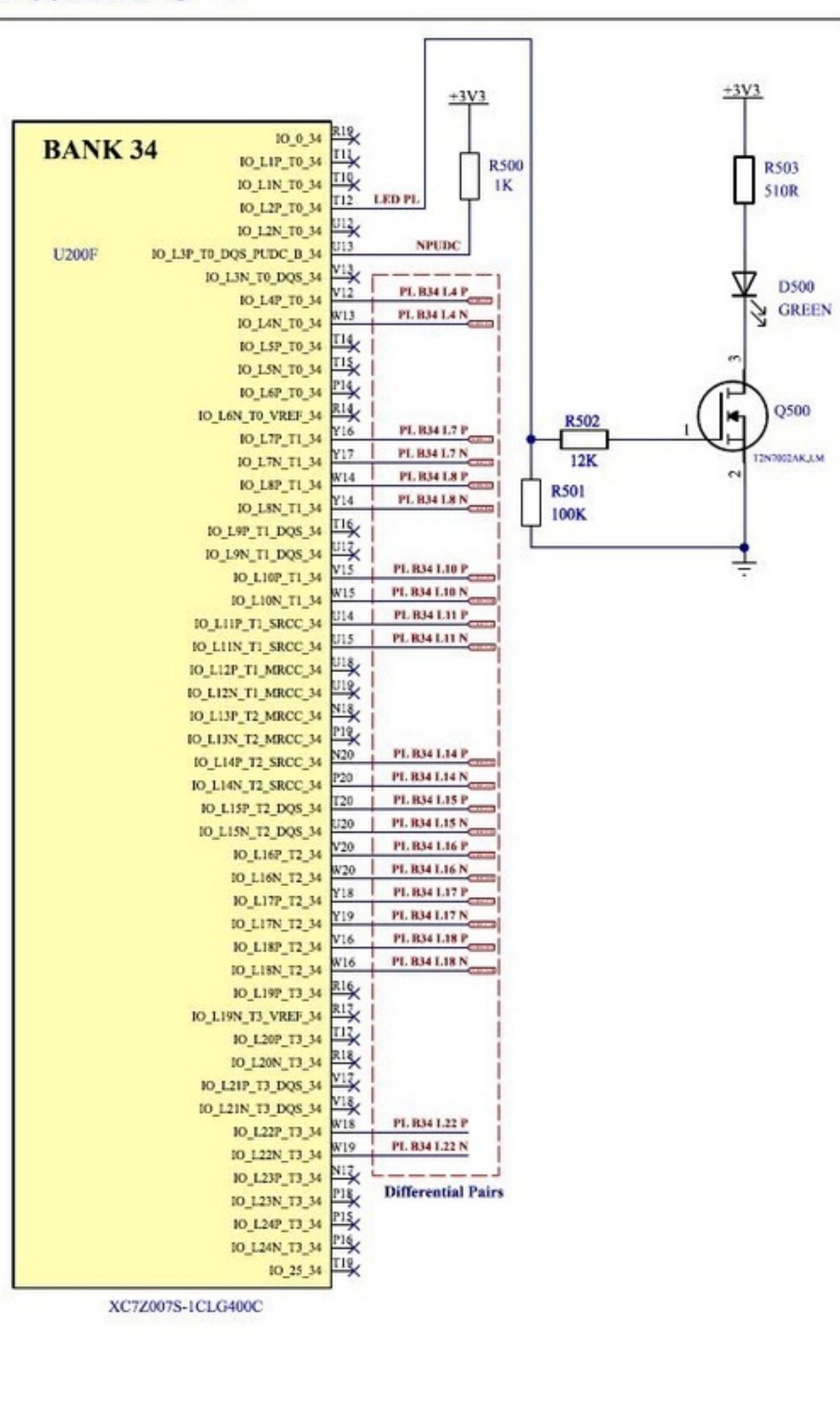
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Sheet: [4] Zynq Processing System (PS)
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[2024-01-11]

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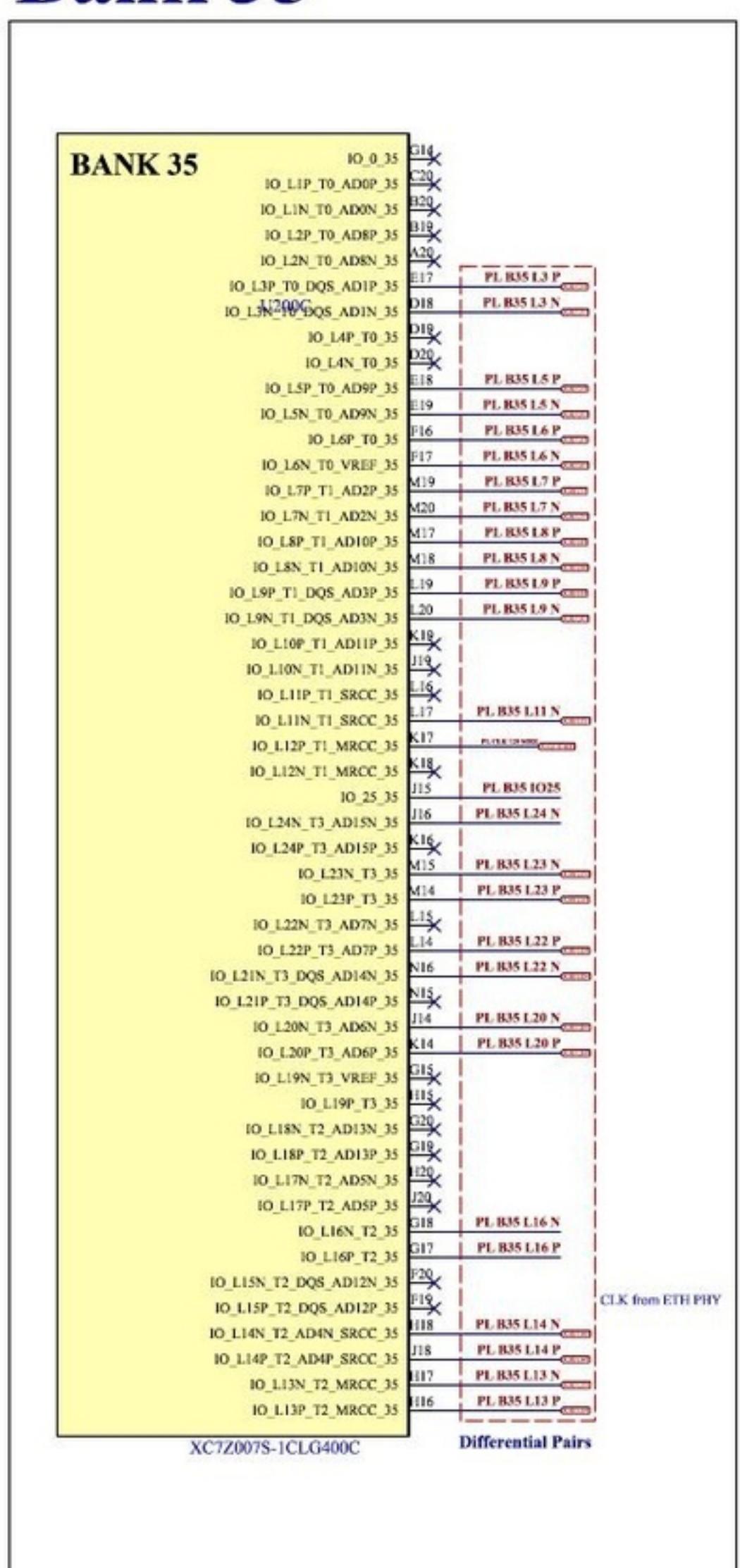
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5. Zynq Programmable Logic (PL)

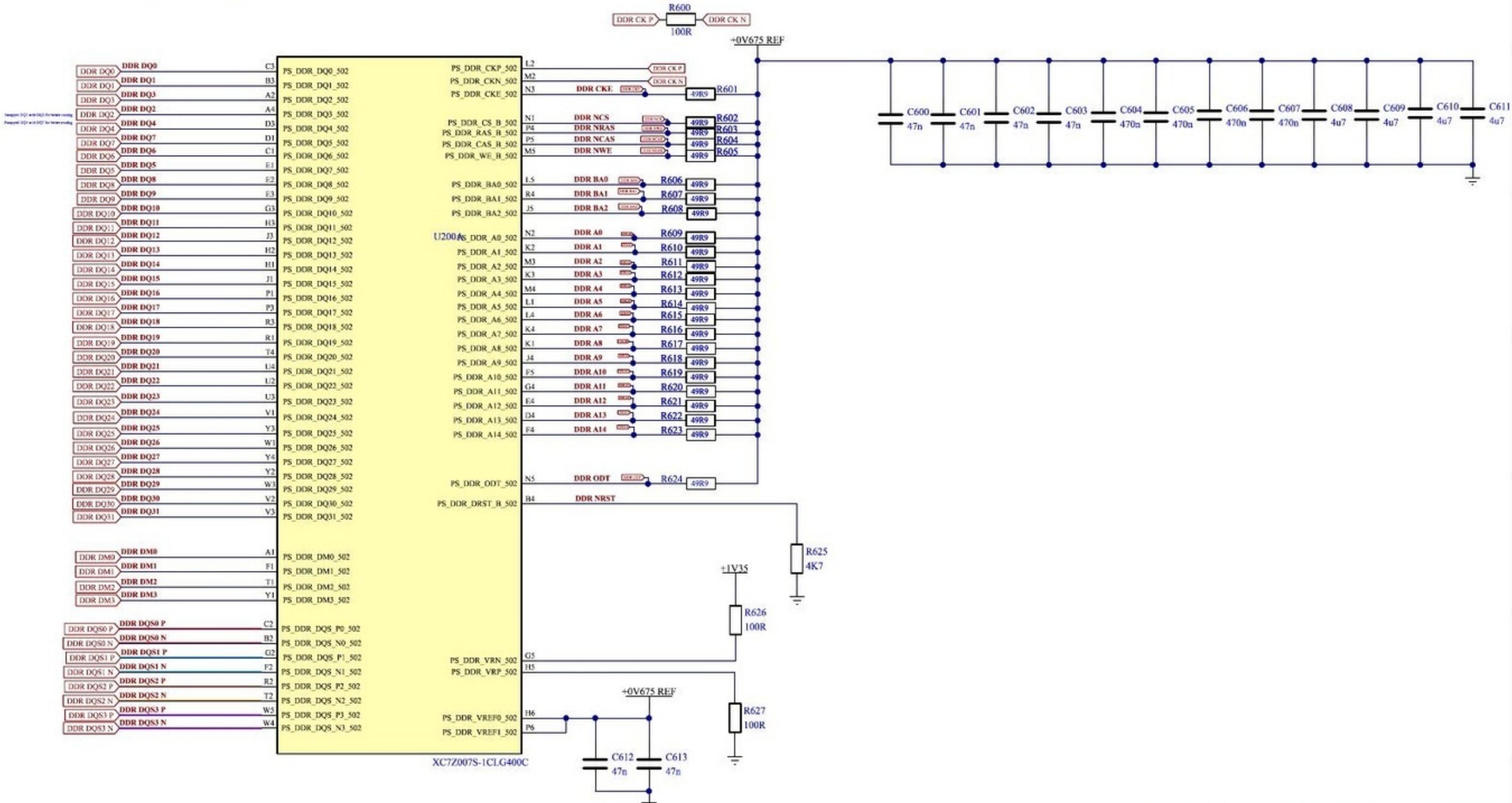
Bank 34



Bank 35



6. Zynq DDR Interface & Termination



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 File: [6] Zynq DDR Interface & Termination.kicad_sch

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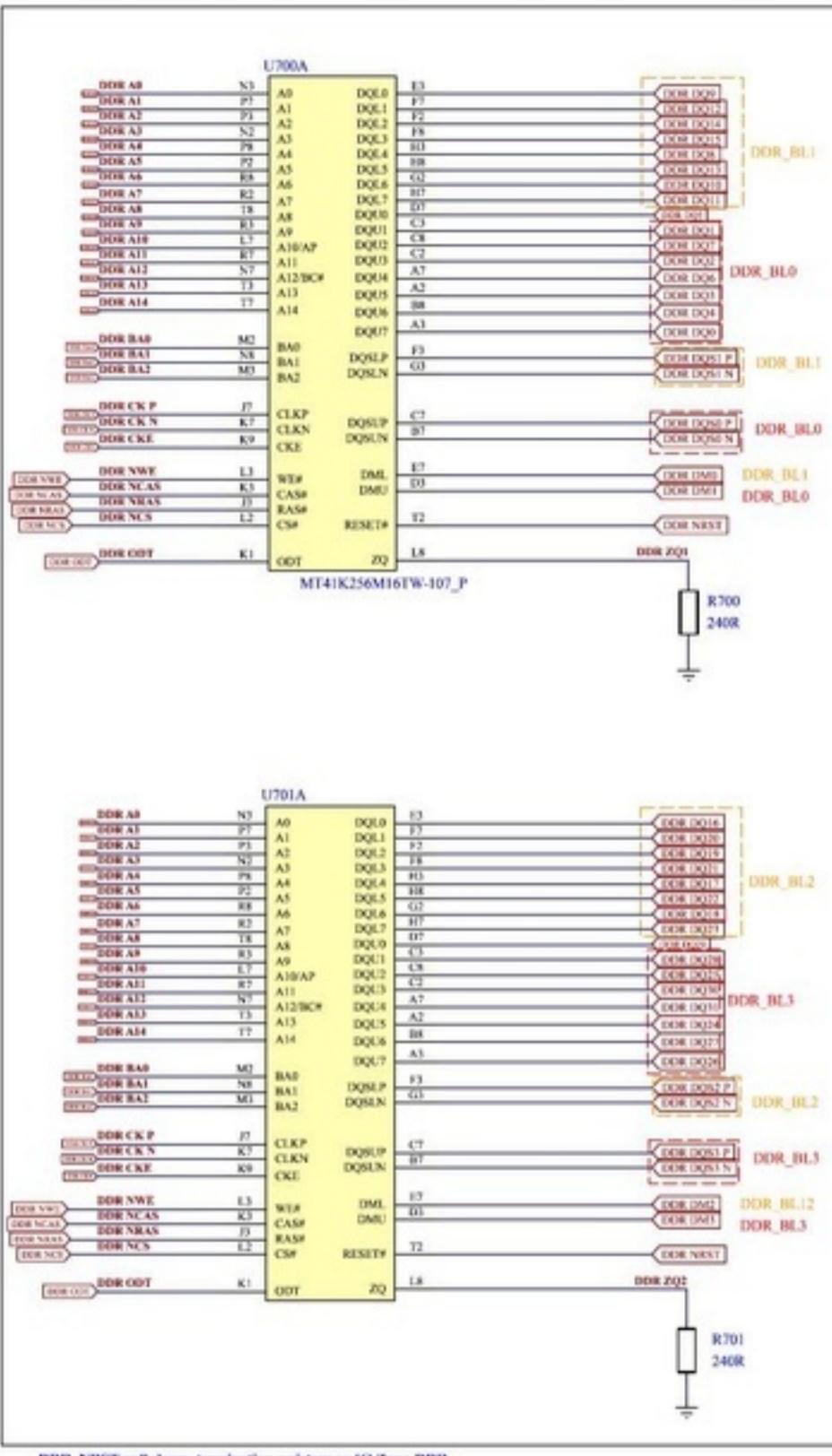
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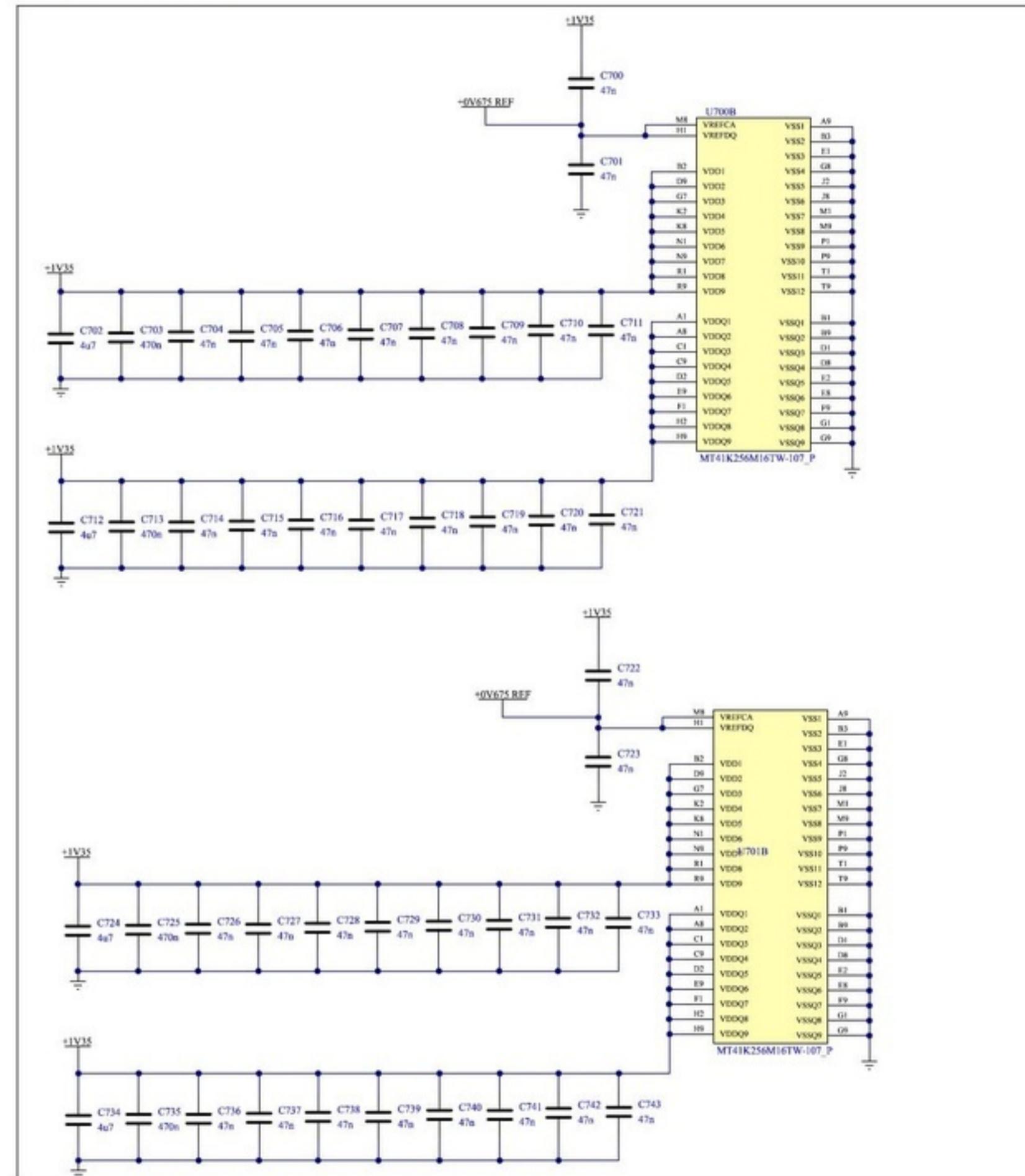


7. 1GB DDR3L Modules

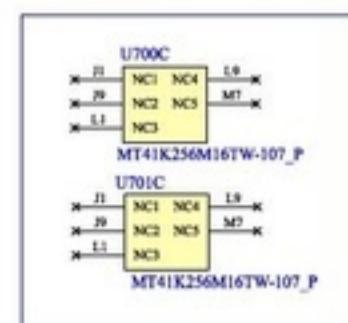
ACC & DAT Connections



POWER



Unused Pins



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Sheet: 7. 1GB DDR3L Modules/
File: [7] 1GB DDR3L Modules.kicad_sch

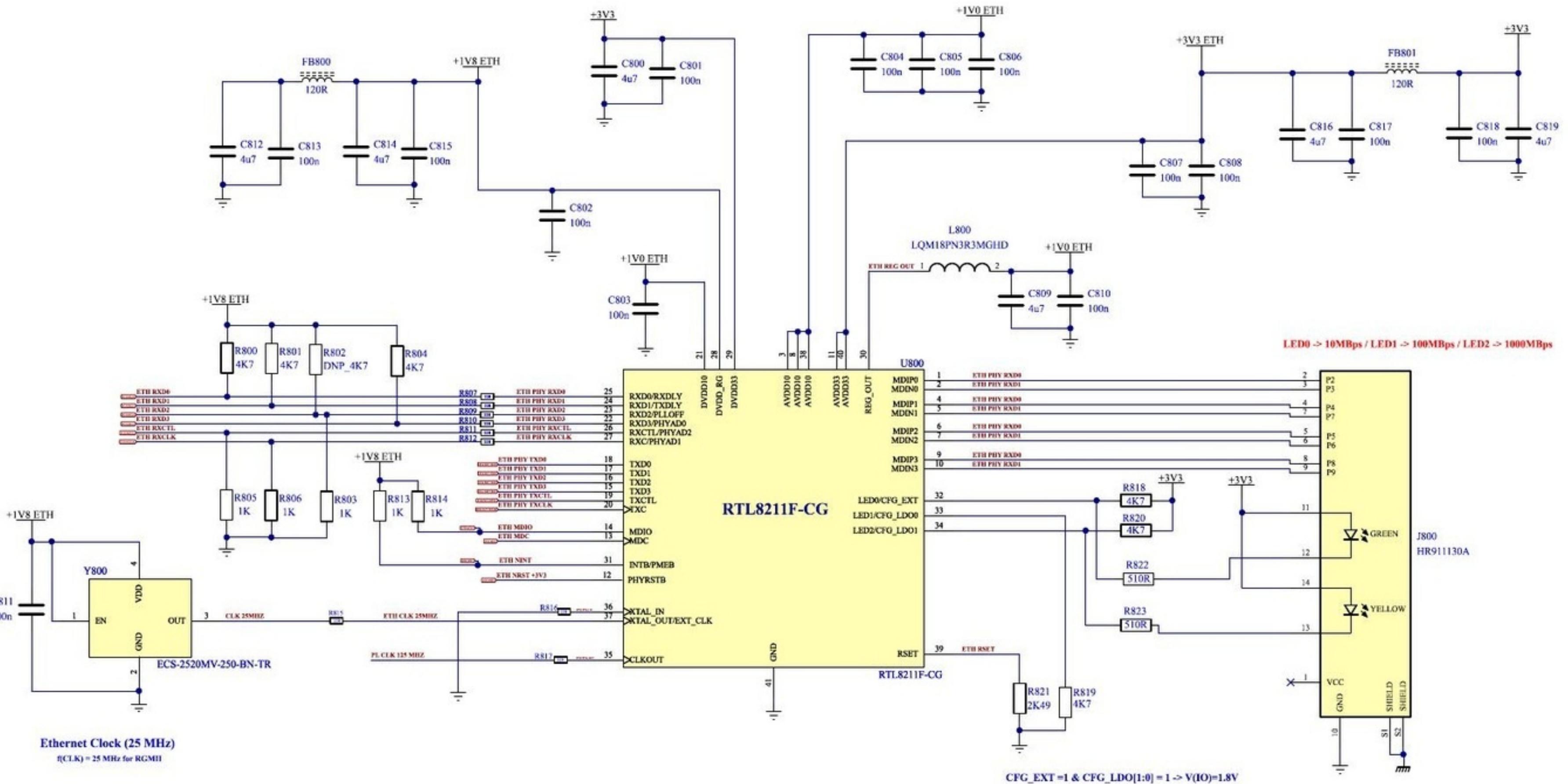
Title: DDR3L Modules

Size: A3 Date:
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8. Gigabit Ethernet



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Sheet: /8. Gigabit Ethernet/
File: [8] Gigabit Ethernet.kicad_sch

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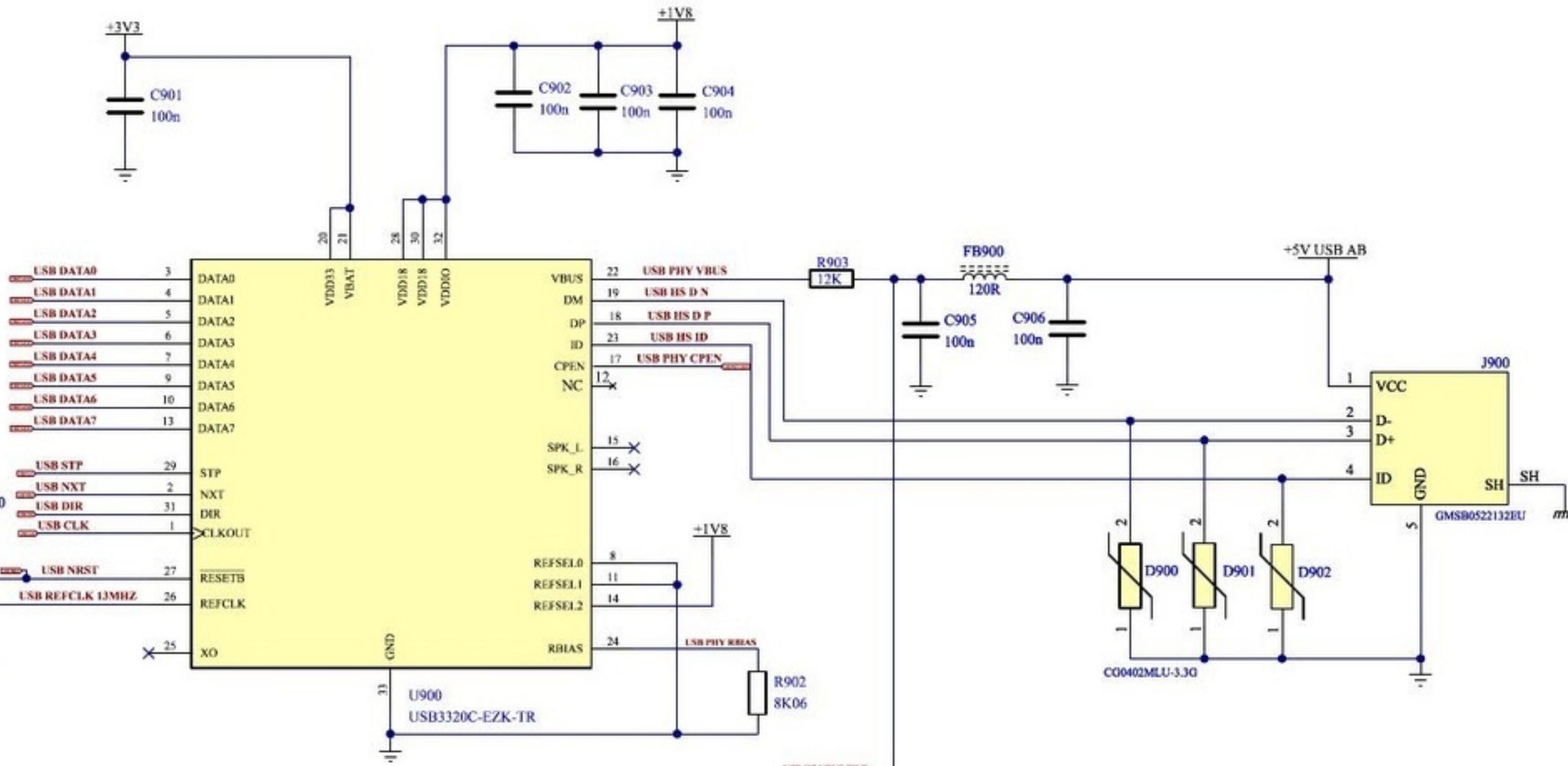
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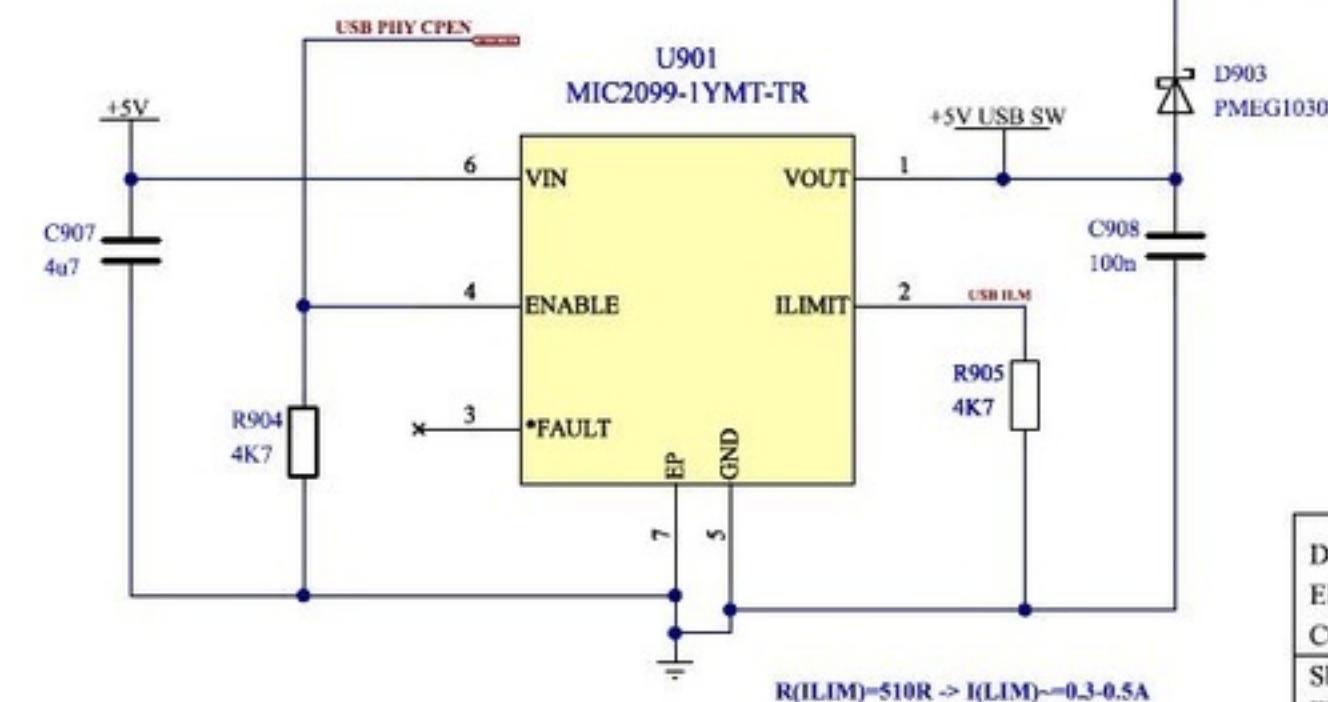
9. USB 2.0 High-Speed (OTG)

A



USB PHY Reference Clock (13MHz)

C



D

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Sheet: /9. USB 2.0 High-Speed (OTG)/
File: [9] USB 2.0 High-Speed (OTG).kicad_sch

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Size: A4 Date:
KiCad E.D.A. kicad 7.0.2-0

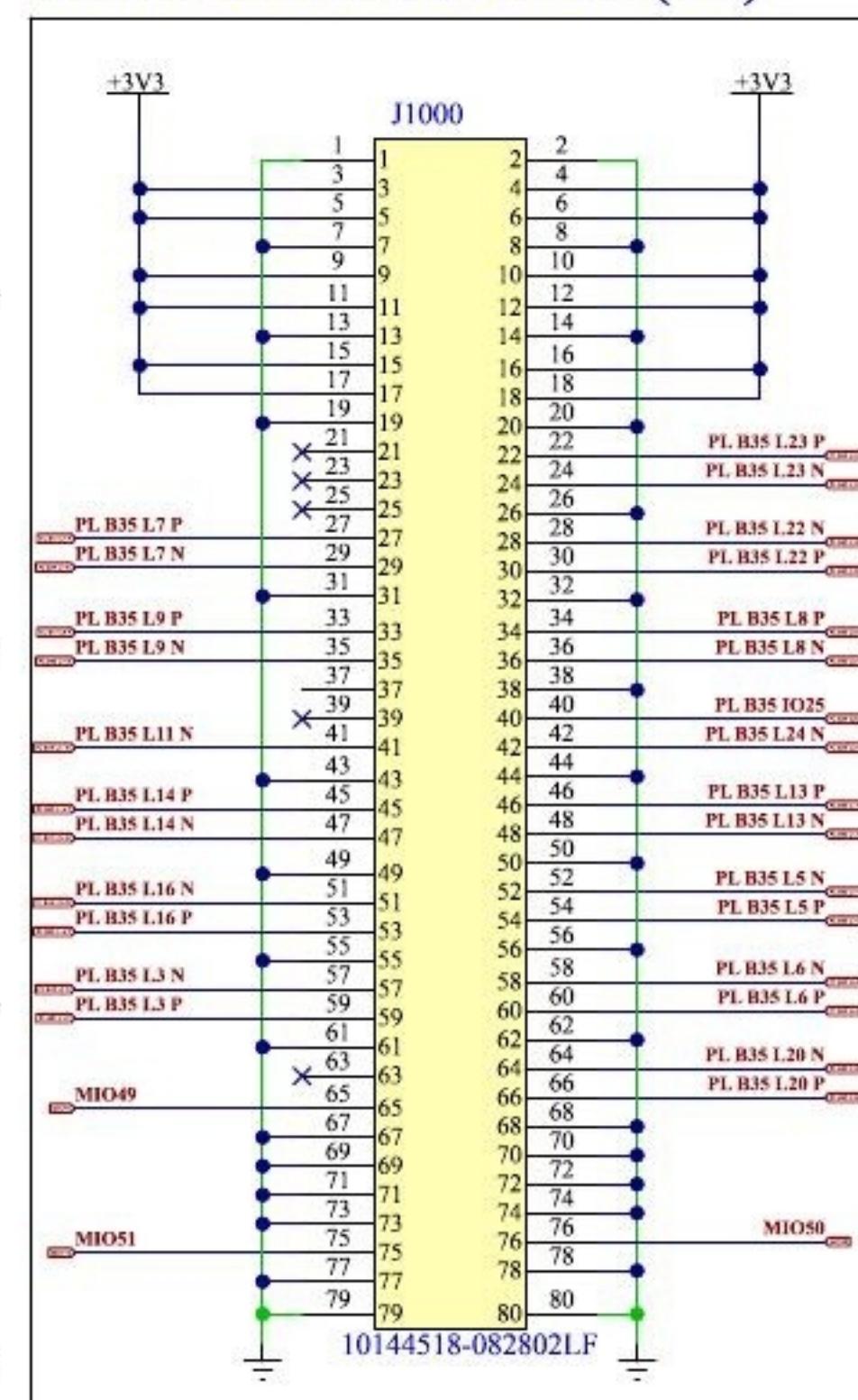
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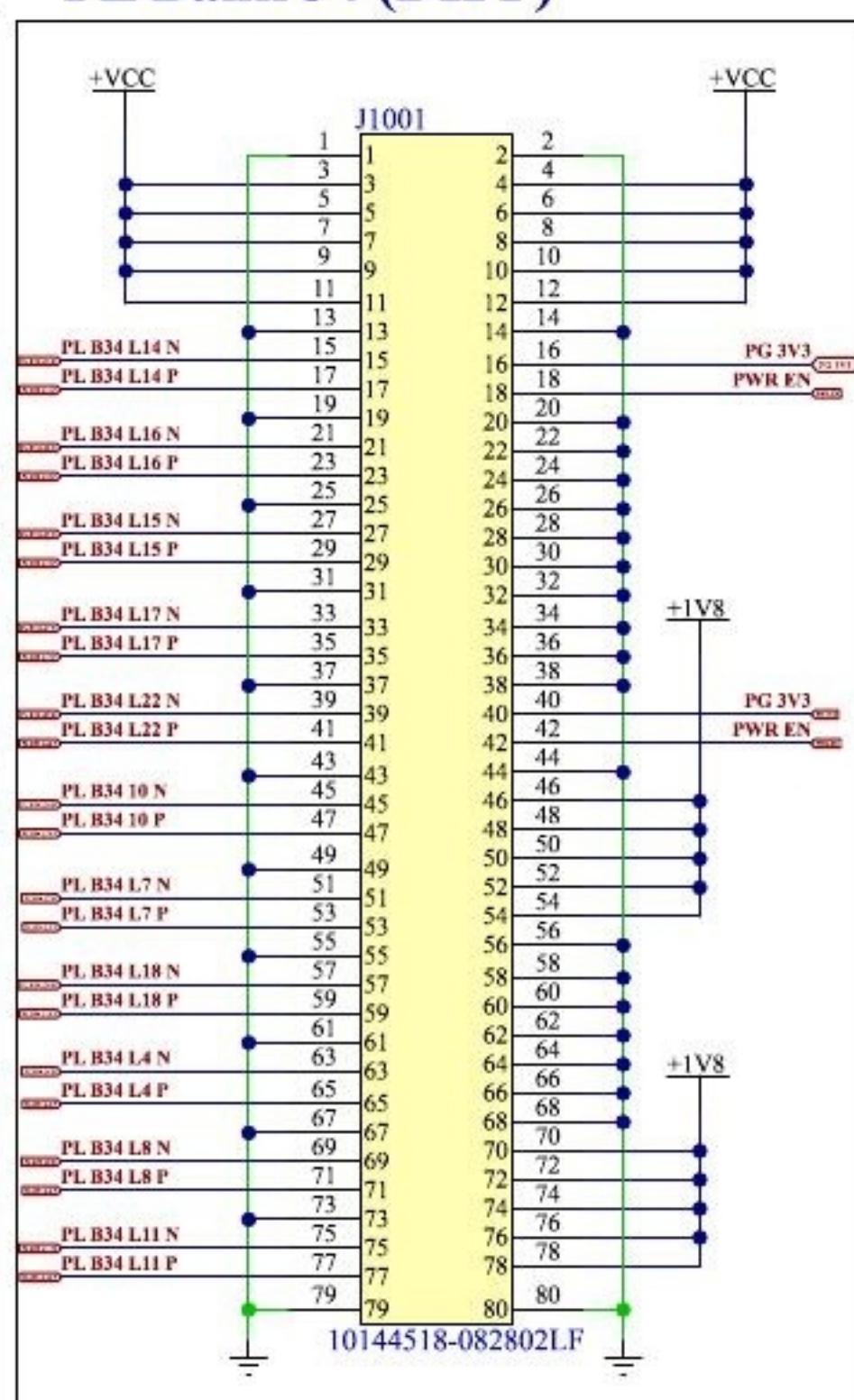


10. Mezzanine Connectors

A PS MIO & PL Bank 35 (SE)



A PL Bank 34 (DIFF)



- H901
Mounting Hole
- H902
Mounting Hole
- H903
Mounting Hole
- H904
Mounting Hole

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