Alexandria University
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Computer Architecture
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Reorder Buffer Report

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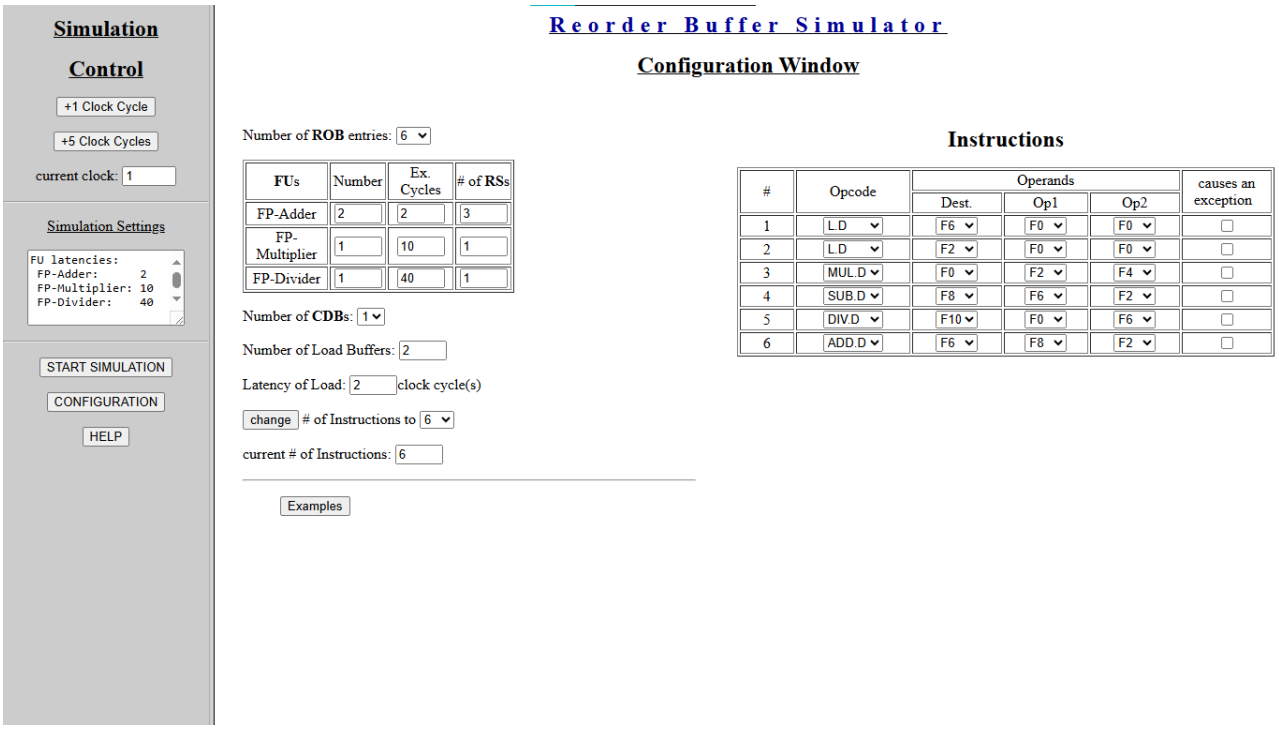
1. Introduction:

In this lab, we explored how Reorder Buffers (ROB) enhance instruction-level parallelism and precise exception handling in modern CPUs. Using a web-based ROB simulator, we constructed and evaluated two instruction sets: one where the ROB provides clear performance benefits through out-of-order execution, and another where the ROB offers little to no advantage due to structural hazards. This lab deepened our understanding of dynamic scheduling and the internal behavior of superscalar processors when executing dependent and independent instructions.

Example 1.

1. Code:



2. Simulation:

Cycle 0

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 59

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
HEAD,TAIL	1					
	2					
	3					
	4					
	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Add2-1	no						
Add2-2	no						
Add2-3	no						
Mul1-1	no						
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #																
Busy	no	no	no	no	no	no	no	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 1

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 1

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

SUB.D F8 F6 F2
MUL.D F0 F2 F4
L.D F2 x Ry

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
HEAD	1	L.D F6 x Ry	F6		0	0
TAIL	2					
	3					
	4					
	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Add2-1	no						
Add2-2	no						
Add2-3	no						
Mul1-1	no						
Div1-1	no						

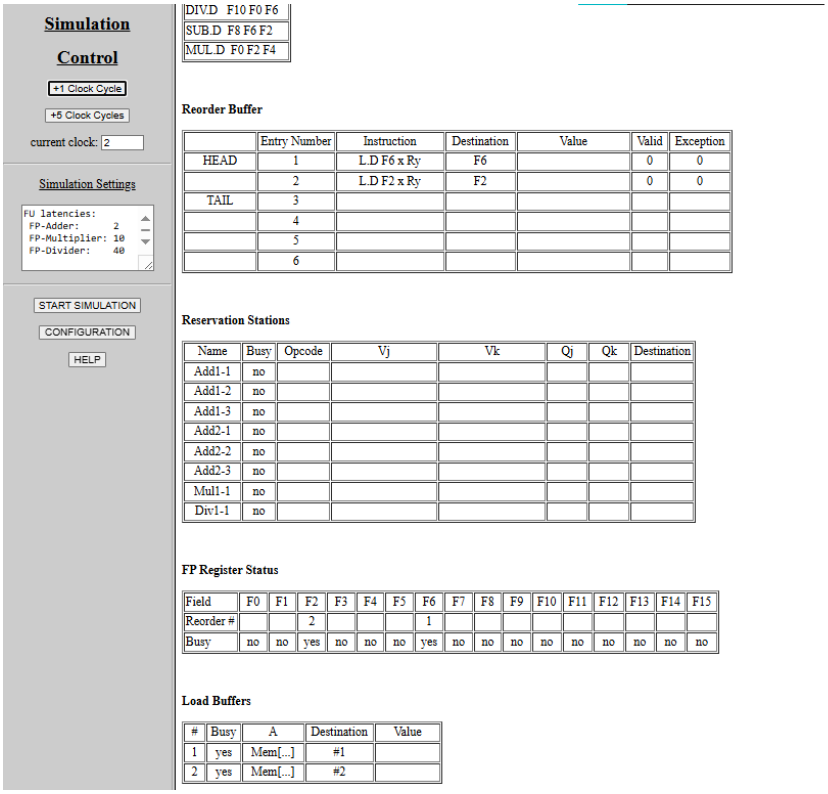
FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #							1									
Busy	no	no	no	no	no	no	yes	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	yes	Mem[...]	#1	
2	no			

Cycle 2



Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 2

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

DIV.D F10 F0 F6
SUB.D F8 F6 F2
MUL.D F0 F2 F4

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
HEAD	1	L.D F6 x Ry	F6		0	0
	2	L.D F2 x Ry	F2		0	0
TAIL	3					
	4					
	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Add2-1	no						
Add2-2	no						
Add2-3	no						
Mul1-1	no						
Div1-1	no						

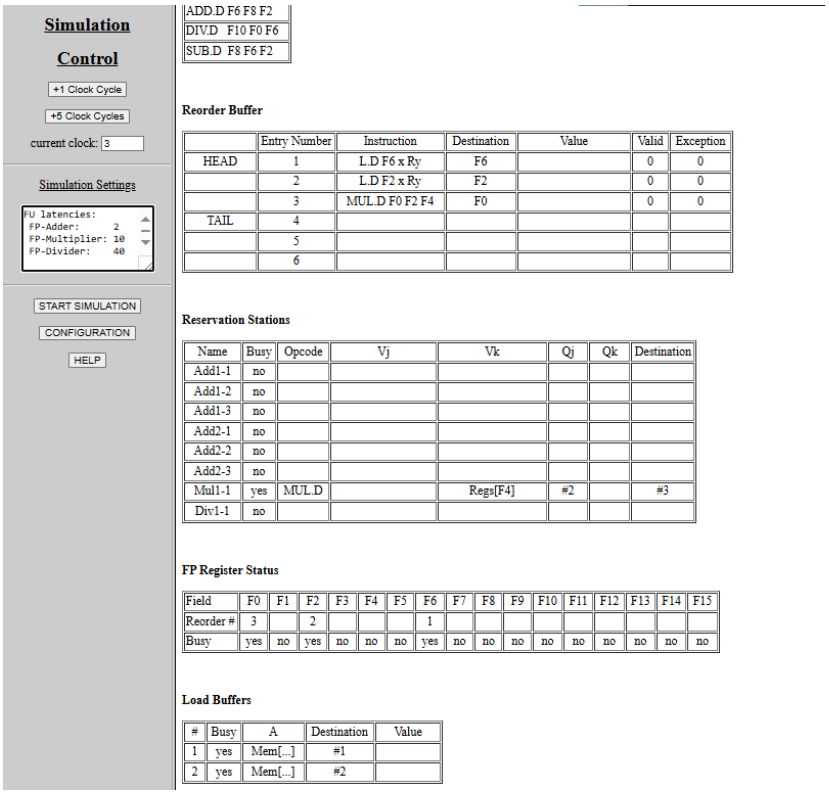
FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #			2				1									
Busy	no	no	yes	no	no	no	yes	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	yes	Mem[...]	#1	
2	yes	Mem[...]	#2	

Cycle 3



Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 3

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

ADD.D F6 F8 F2
DIV.D F10 F0 F6
SUB.D F8 F6 F2

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
HEAD	1	L.D F6 x Ry	F6		0	0
	2	L.D F2 x Ry	F2		0	0
	3	MUL.D F0 F2 F4	F0		0	0
TAIL	4					
	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Add2-1	no						
Add2-2	no						
Add2-3	no						
Mul1-1	yes	MUL.D		Regs[F4]	#2		#3
Div1-1	no						

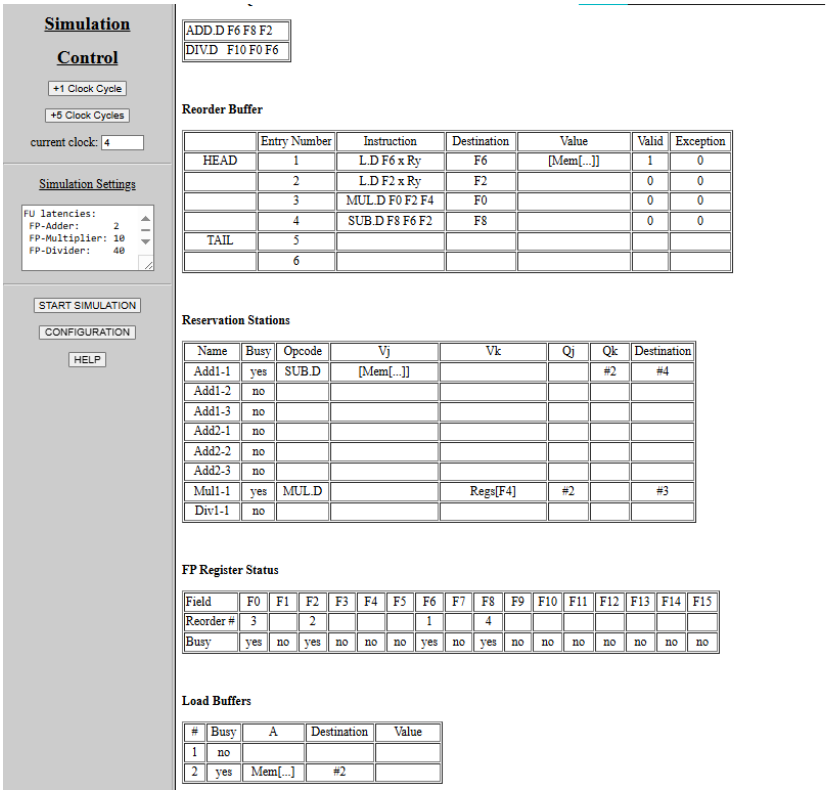
FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #	3		2				1									
Busy	yes	no	yes	no	no	no	yes	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	yes	Mem[...]	#1	
2	yes	Mem[...]	#2	

Cycle 4



Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 4

Simulation Settings

```
FU latencies:
FP-Adder:      2
FP-Multiplier: 10
FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

ADD.D F6 F8 F2
DIV.D F10 F0 F6

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
HEAD	1	L.D F6 x Ry	F6	[Mem[...]]	1	0
	2	L.D F2 x Ry	F2		0	0
	3	MUL.D F0 F2 F4	F0		0	0
	4	SUB.D F8 F6 F2	F8		0	0
TAIL	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	yes	SUB.D	[Mem[...]]			#2	#4
Add1-2	no						
Add1-3	no						
Add2-1	no						
Add2-2	no						
Add2-3	no						
Mul1-1	yes	MUL.D		Regs[F4]	#2		#3
Div1-1	no						

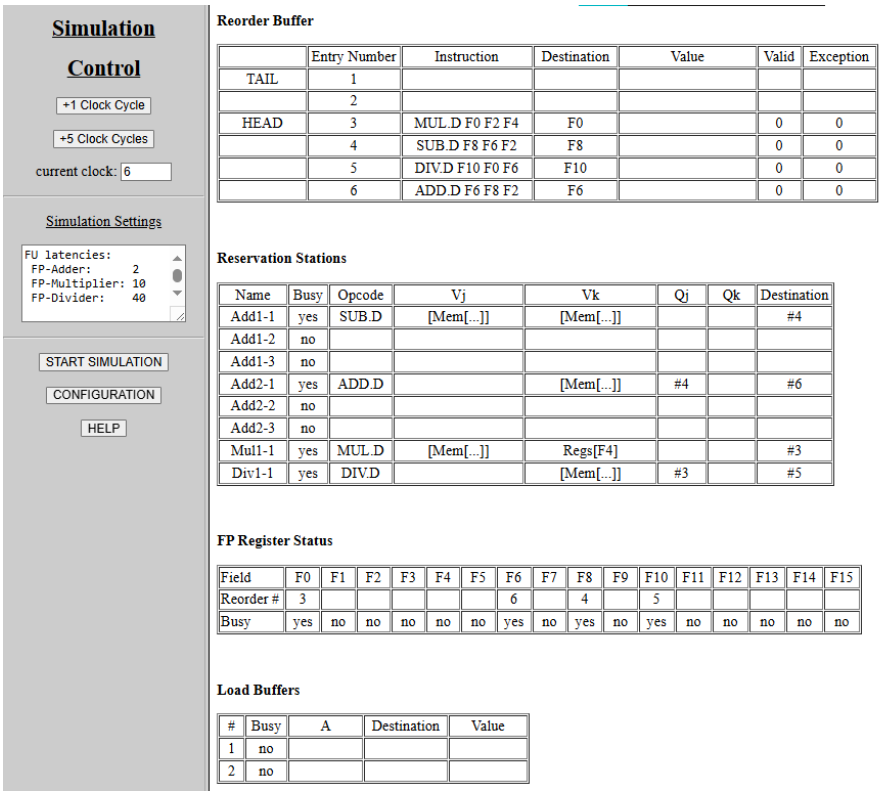
FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #	3		2				1		4							
Busy	yes	no	yes	no	no	no	yes	no	yes	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	yes	Mem[...]	#2	

Cycle 6



Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 6

Simulation Settings

```
FU latencies:
FP-Adder:      2
FP-Multiplier: 10
FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
TAIL	1					
	2					
HEAD	3	MUL.D F0 F2 F4	F0		0	0
	4	SUB.D F8 F6 F2	F8		0	0
	5	DIV.D F10 F0 F6	F10		0	0
	6	ADD.D F6 F8 F2	F6		0	0

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	yes	SUB.D	[Mem[...]]	[Mem[...]]			#4
Add1-2	no						
Add1-3	no						
Add2-1	yes	ADD.D		[Mem[...]]	#4		#6
Add2-2	no						
Add2-3	no						
Mul1-1	yes	MUL.D	[Mem[...]]	Regs[F4]			#3
Div1-1	yes	DIV.D		[Mem[...]]	#3		#5

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #	3						6		4		5					
Busy	yes	no	no	no	no	no	yes	no	yes	no	yes	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 7

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
TAIL	1					
	2					
HEAD	3	MUL.D F0 F2 F4	F0		0	0
	4	SUB.D F8 F6 F2	F8		0	0
	5	DIV.D F10 F0 F6	F10		0	0
	6	ADD.D F6 F8 F2	F6		0	0

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	yes	SUB.D	[Mem[...]]	[Mem[...]]			#4
Add1-2	no						
Add1-3	no						
Add2-1	yes	ADD.D		[Mem[...]]	#4		#6
Add2-2	no						
Add2-3	no						
Mul1-1	yes	MUL.D	[Mem[...]]	Regs[F4]			#3
Div1-1	yes	DIV.D		[Mem[...]]	#3		#5

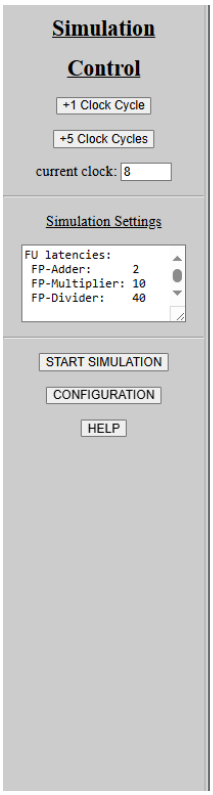
FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #	3						6		4		5					
Busy	yes	no	no	no	no	no	yes	no	yes	no	yes	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 8



Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
TAIL	1					
	2					
HEAD	3	MUL.D F0 F2 F4	F0		0	0
	4	SUB.D F8 F6 F2	F8	#1-#2	1	0
	5	DIV.D F10 F0 F6	F10		0	0
	6	ADD.D F6 F8 F2	F6		0	0

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Add2-1	yes	ADD.D	#1-#2	[Mem[...]]			#6
Add2-2	no						
Add2-3	no						
Mul1-1	yes	MUL.D	[Mem[...]]	Regs[F4]			#3
Div1-1	yes	DIV.D		[Mem[...]]	#3		#5

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #	3						6		4		5					
Busy	yes	no	no	no	no	no	yes	no	yes	no	yes	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 11

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 11

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
TAIL	1					
	2					
HEAD	3	MUL.D F0 F2 F4	F0		0	0
	4	SUB.D F8 F6 F2	F8	#1-#2	1	0
	5	DIV.D F10 F0 F6	F10		0	0
	6	ADD.D F6 F8 F2	F6	#4+#2	1	0

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Add2-1	no						
Add2-2	no						
Add2-3	no						
Mul1-1	yes	MUL.D	[Mem[...]]	Regs[F4]			#3
Div1-1	yes	DIV.D		[Mem[...]]	#3		#5

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #	3						6		4		5					
Busy	yes	no	no	no	no	no	yes	no	yes	no	yes	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 16

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 16

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
TAIL	1					
	2					
HEAD	3	MUL.D F0 F2 F4	F0	#2*Regs[F4]	1	0
	4	SUB.D F8 F6 F2	F8	#1-#2	1	0
	5	DIV.D F10 F0 F6	F10		0	0
	6	ADD.D F6 F8 F2	F6	#4+#2	1	0

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Add2-1	no						
Add2-2	no						
Add2-3	no						
Mul1-1	no						
Div1-1	yes	DIV.D	#2*Regs[F4]	[Mem[...]]			#5

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #	3						6		4		5					
Busy	yes	no	no	no	no	no	yes	no	yes	no	yes	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 17

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 17

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
TAIL	1					
	2					
	3					
HEAD	4	SUB.D F8 F6 F2	F8	#1-#2	1	0
	5	DIV.D F10 F0 F6	F10		0	0
	6	ADD.D F6 F8 F2	F6	#4+#2	1	0

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Add2-1	no						
Add2-2	no						
Add2-3	no						
Mul1-1	no						
Div1-1	yes	DIV.D	#2*Regs[F4]	[Mem[...]]			#5

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #							6		4		5					
Busy	no	no	no	no	no	no	yes	no	yes	no	yes	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 18

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 18

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
TAIL	1					
	2					
	3					
	4					
HEAD	5	DIV.D F10 F0 F6	F10		0	0
	6	ADD.D F6 F8 F2	F6	#4+#2	1	0

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Add2-1	no						
Add2-2	no						
Add2-3	no						
Mul1-1	no						
Div1-1	yes	DIV.D	#2*Regs[F4]	[Mem[...]]			#5

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #							6				5					
Busy	no	no	no	no	no	no	yes	no	no	no	yes	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 57

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 57

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
TAIL	1					
	2					
	3					
	4					
HEAD	5	DIV.D F10 F0 F6	F10	#3 #1	1	0
	6	ADD.D F6 F8 F2	F6	#4+#2	1	0

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Add2-1	no						
Add2-2	no						
Add2-3	no						
Mul1-1	no						
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #							6				5					
Busy	no	no	no	no	no	no	yes	no	no	no	yes	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 58

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 58

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
TAIL	1					
	2					
	3					
	4					
	5					
HEAD	6	ADD.D F6 F8 F2	F6	#4+#2	1	0

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Add2-1	no						
Add2-2	no						
Add2-3	no						
Mul1-1	no						
Div1-1	no						

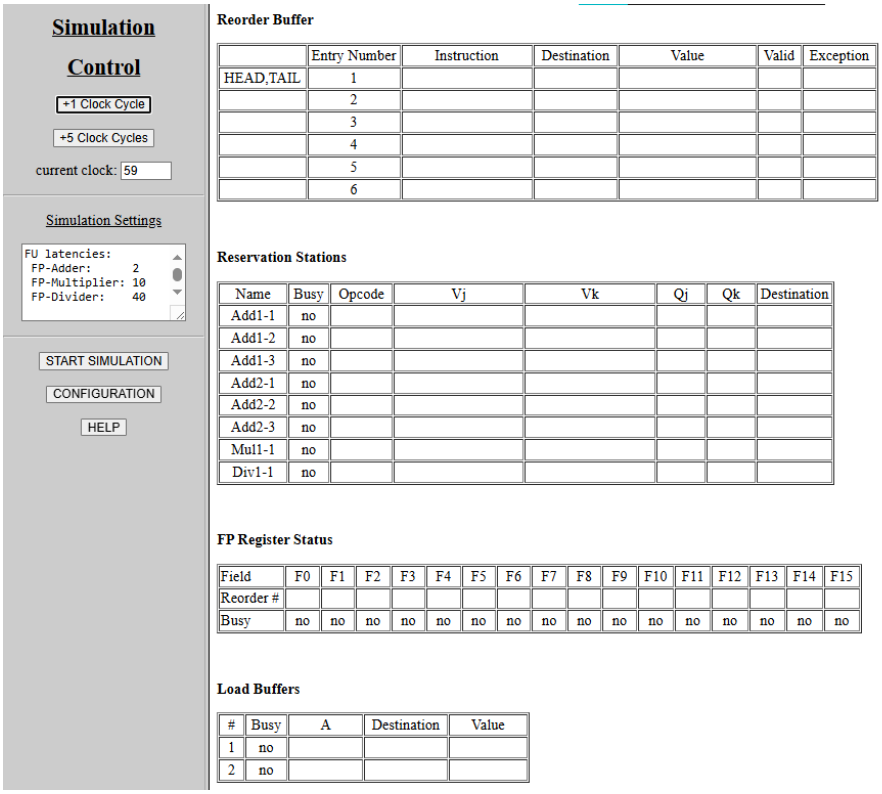
FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #							6									
Busy	no	no	no	no	no	no	yes	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 59



Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 59

Simulation Settings

```
FU latencies:
 FP-Adder:       2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
HEAD,TAIL	1					
	2					
	3					
	4					
	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Add2-1	no						
Add2-2	no						
Add2-3	no						
Mul1-1	no						
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #																
Busy	no	no	no	no	no	no	no	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

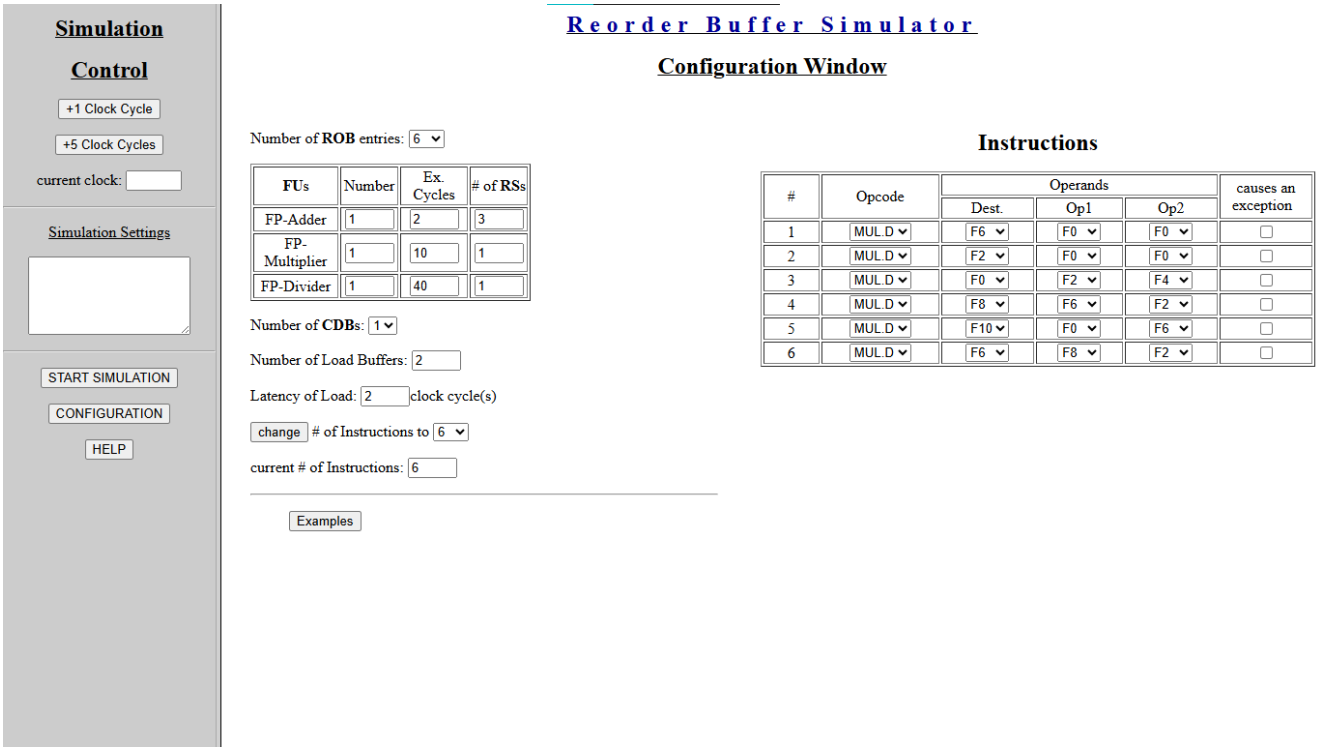
3. Simulation Results

A diverse instruction set using different functional units (load, add, multiply, divide) allowed out-of-order execution. The Reorder Buffer enabled parallelism by issuing independent instructions early, resulting in efficient resource usage and shorter overall execution time.

Completed in = 59 cycles

Example 2.

1. Code:



Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock:

Simulation Settings

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer Simulator

Configuration Window

Number of **ROB** entries: 6

FUs	Number	Ex. Cycles	# of **RSs**
FP-Adder	1	2	3
FP-Multiplier	1	10	1
FP-Divider	1	40	1

Number of **CDBs**: 1

Number of Load Buffers: 2

Latency of Load: 2 clock cycle(s)

change # of Instructions to 6

current # of Instructions: 6

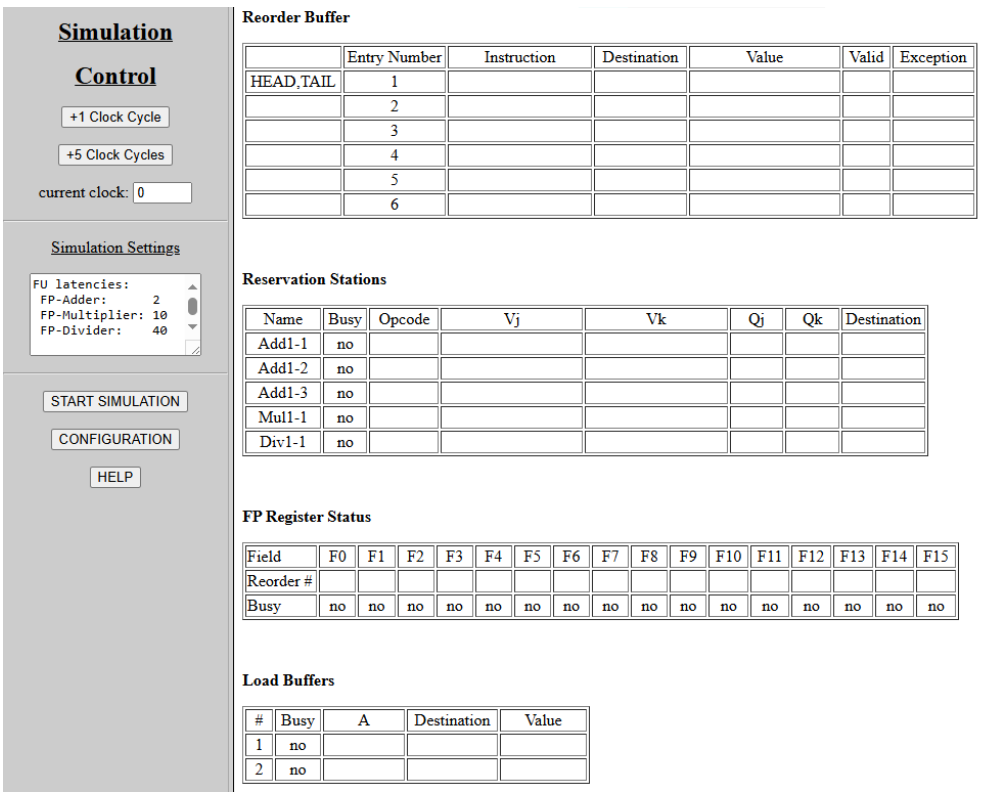
Examples

Instructions

#	Opcode	Operands			causes an exception
		Dest.	Op1	Op2	
1	MUL.D	F6	F0	F0	
2	MUL.D	F2	F0	F0	
3	MUL.D	F0	F2	F4	
4	MUL.D	F8	F6	F2	
5	MUL.D	F10	F0	F6	
6	MUL.D	F6	F8	F2	

2. Simulation:

Cycle 0



Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 0

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
HEAD,TAIL	1					
	2					
	3					
	4					
	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Mul1-1	no						
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #																
Busy	no	no	no	no	no	no	no	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 1

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 1

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
HEAD	1	MUL.D F6 F0 F0	F6		0	0
TAIL	2					
	3					
	4					
	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Mul1-1	yes	MUL.D	Regs[F0]	Regs[F0]			#1
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #							1									
Busy	no	no	no	no	no	no	yes	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 12

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 12

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
HEAD	1	MUL.D F6 F0 F0	F6	Regs[F0]*Regs[F0]	1	0
	2	MUL.D F2 F0 F0	F2		0	0
TAIL	3					
	4					
	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Mul1-1	yes	MUL.D	Regs[F0]	Regs[F0]			#2
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #			2				1									
Busy	no	no	yes	no	no	no	yes	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 13

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 13

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
	1					
HEAD	2	MUL.D F2 F0 F0	F2		0	0
TAIL	3					
	4					
	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Mul1-1	yes	MUL.D	Regs[F0]	Regs[F0]			#2
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #			2													
Busy	no	no	yes	no	no	no	no	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 23

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 23

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
	1					
HEAD	2	MUL.D F2 F0 F0	F2	Regs[F0]*Regs[F0]	1	0
	3	MUL.D F0 F2 F4	F0		0	0
TAIL	4					
	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Mul1-1	yes	MUL.D	Regs[F0]*Regs[F0]	Regs[F4]			#3
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #	3		2													
Busy	yes	no	yes	no	no	no	no	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 24

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 24

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
	1					
	2					
HEAD	3	MUL.D F0 F2 F4	F0		0	0
TAIL	4					
	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Mul1-1	yes	MUL.D	Regs[F0]*Regs[F0]	Regs[F4]			#3
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #	3															
Busy	yes	no	no	no	no	no	no	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 34

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 24

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
	1					
	2					
HEAD	3	MUL.D F0 F2 F4	F0		0	0
TAIL	4					
	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Mul1-1	yes	MUL.D	Regs[F0]*Regs[F0]	Regs[F4]			#3
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #	3															
Busy	yes	no	no	no	no	no	no	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 35

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 35

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
	1					
	2					
	3					
HEAD	4	MUL.D F8 F6 F2	F8		0	0
TAIL	5					
	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Mul1-1	yes	MUL.D	Regs[F6]	Regs[F2]			#4
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #									4							
Busy	no	no	no	no	no	no	no	no	yes	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 45

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 45

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
	1					
	2					
	3					
HEAD	4	MUL.D F8 F6 F2	F8	Regs[F6]*Regs[F2]	1	0
	5	MUL.D F10 F0 F6	F10		0	0
TAIL	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Mul1-1	yes	MUL.D	Regs[F0]	Regs[F6]			#5
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #									4		5					
Busy	no	no	no	no	no	no	no	no	yes	no	yes	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 46

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 46

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
	1					
	2					
	3					
	4					
HEAD	5	MUL.D F10 F0 F6	F10		0	0
TAIL	6					

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Mul1-1	yes	MUL.D	Regs[F0]	Regs[F6]			#5
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #											5					
Busy	no	no	no	no	no	no	no	no	no	no	yes	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 56

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 56

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
TAIL	1					
	2					
	3					
	4					
HEAD	5	MUL.D F10 F0 F6	F10	Regs[F0]*Regs[F6]	1	0
	6	MUL.D F6 F8 F2	F6		0	0

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Mul1-1	yes	MUL.D	Regs[F8]	Regs[F2]			#6
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #							6				5					
Busy	no	no	no	no	no	no	yes	no	no	no	yes	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 57

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 57

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
TAIL	1					
	2					
	3					
	4					
	5					
HEAD	6	MUL.D F6 F8 F2	F6		0	0

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Mul1-1	yes	MUL.D	Regs[F8]	Regs[F2]			#6
Div1-1	no						

FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #							6									
Busy	no	no	no	no	no	no	yes	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 67

Simulation Control

+1 Clock Cycle

+5 Clock Cycles

current clock: 67

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

Reorder Buffer

	Entry Number	Instruction	Destination	Value	Valid	Exception
TAIL	1					
	2					
	3					
	4					
	5					
HEAD	6	MUL.D F6 F8 F2	F6	Regs[F8]*Regs[F2]	1	0

Reservation Stations

Name	Busy	Opcode	Vj	Vk	Qj	Qk	Destination
Add1-1	no						
Add1-2	no						
Add1-3	no						
Mul1-1	no						
Div1-1	no						

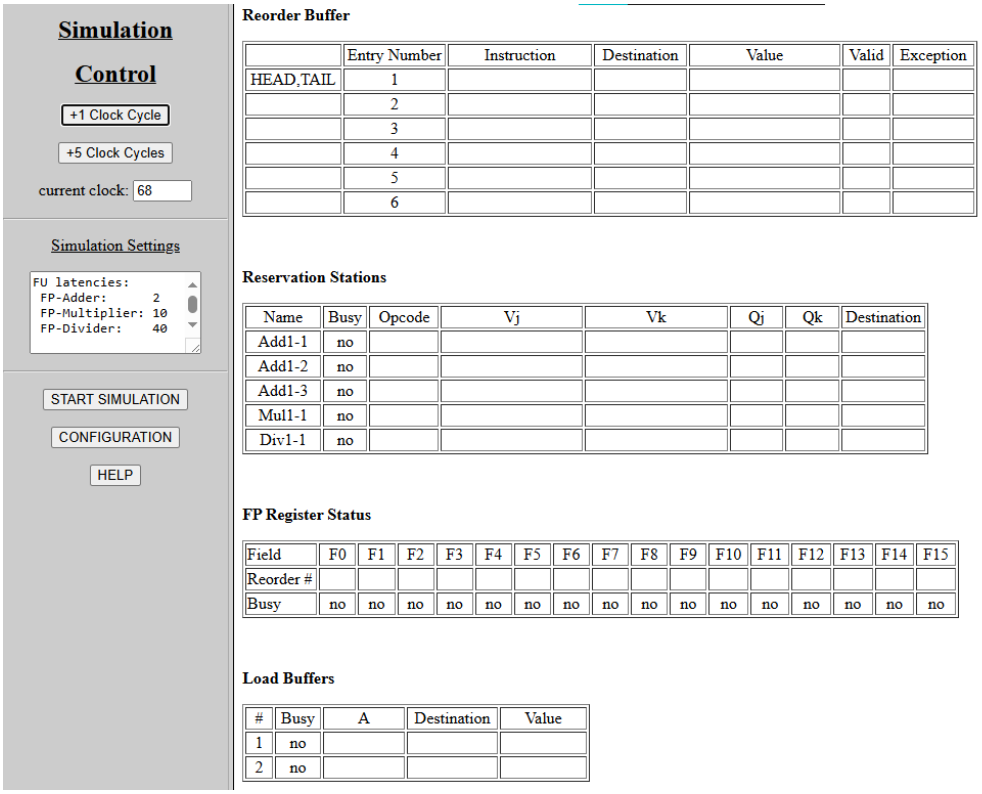
FP Register Status

Field	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Reorder #							6									
Busy	no	no	no	no	no	no	yes	no	no	no	no	no	no	no	no	no

Load Buffers

#	Busy	A	Destination	Value
1	no			
2	no			

Cycle 68



3. Simulation Results:

A sequence of dependent MUL.D instructions caused a bottleneck at the single floating-point multiplier. Due to both data hazards and limited functional units, the instructions were executed serially. The Reorder Buffer couldn't resolve the stall, offering no speedup.

Completed in = 68 cycles

2. Tools and Environment:

ROB simulator was used for simulation.

3. Submission Details:

The report includes:

- Screenshots demonstrating simulation results.
- A link to the complete lab repository:
  https://github.com/moateff/Computer-Architecture-labs.git

4. Conclusion:

The Reorder Buffer improves performance when instructions can run in parallel on different units. However, when instructions are dependent or use the same unit, the ROB offers little advantage. Its benefit depends on the instruction mix and hardware availability. Its effectiveness is limited by hardware constraints and instruction-level parallelism.