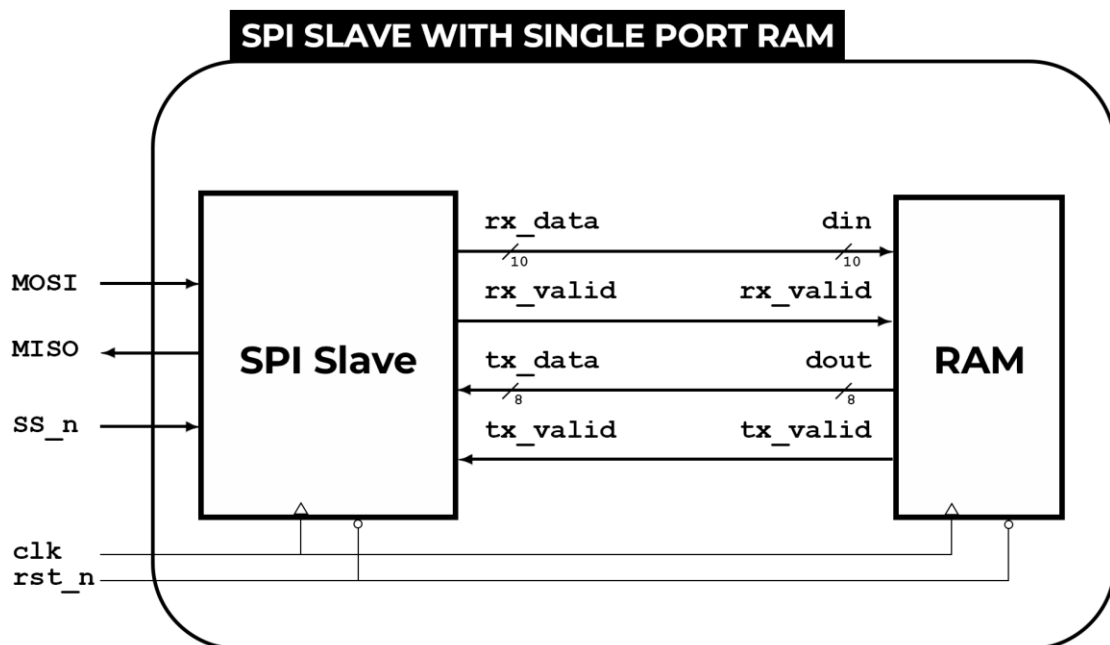
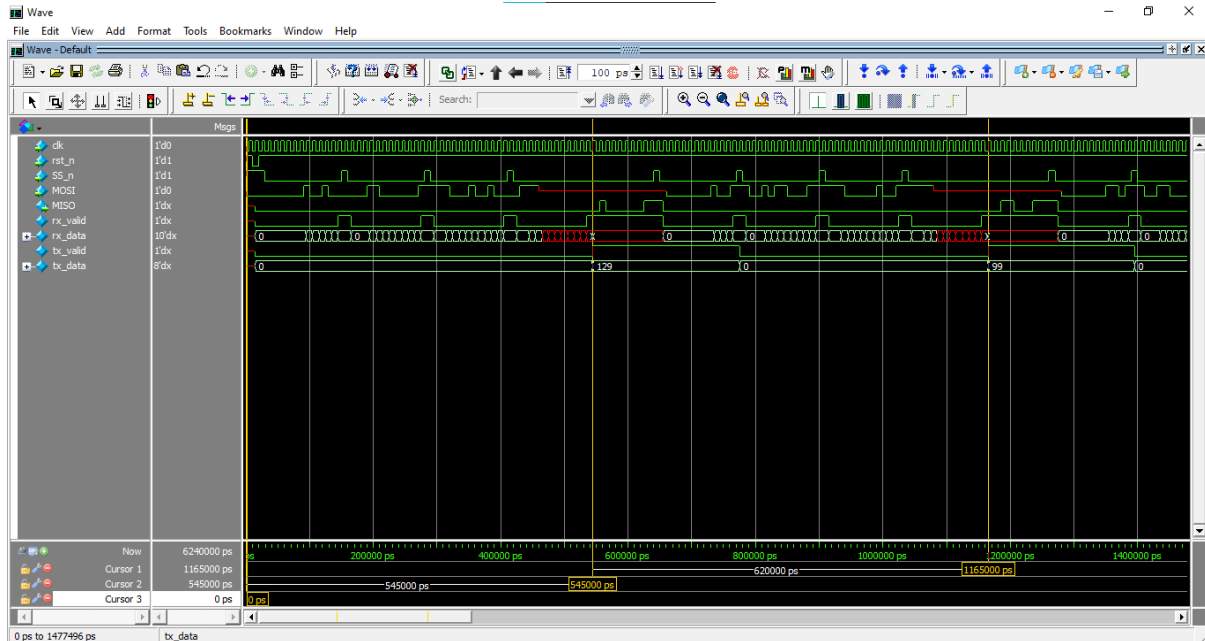


SPI Slave with Single Port RAM



Mohamed Atef Yousef Moawad
Ahmed Tarek Abdallah Mohamed
Mohamed Mahmoud Mohamed

QuestaSim snippet



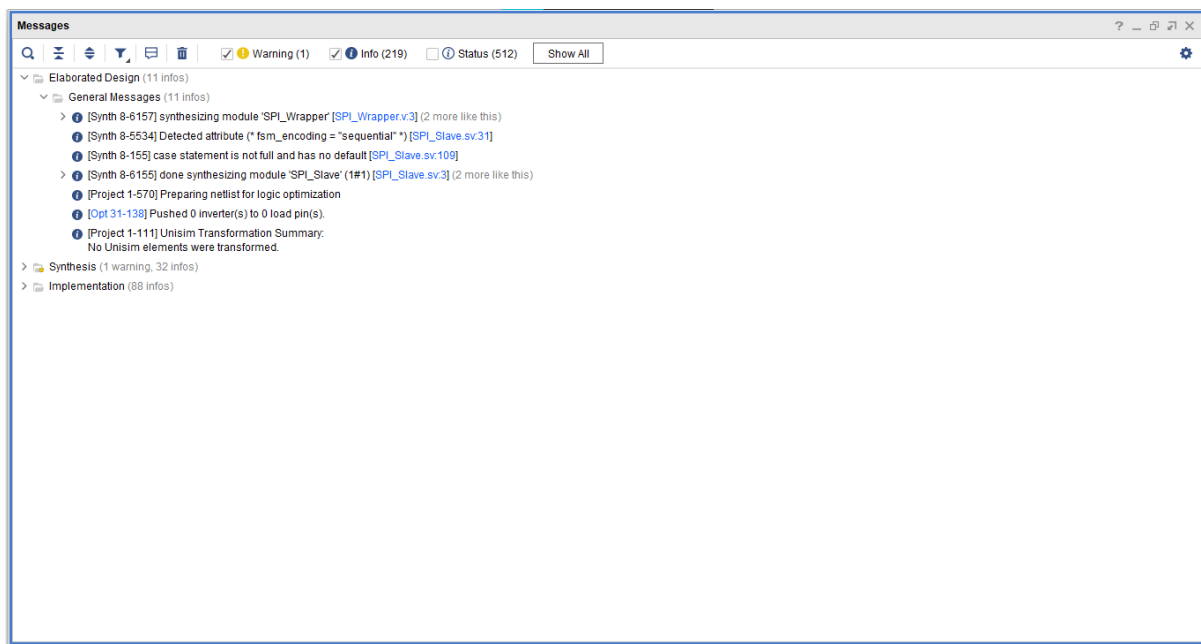
```
# ----- Test Case 1 -----  
#  
# Master Operation: Transmitting Write Address: 36  
# Master TX Started. Control Bits: 000, Transmitted Data: 00100100  
# Master TX Completed.  
#  
# Master Operation: Transmitting Write Data: 129  
# Master TX Started. Control Bits: 001, Transmitted Data: 10000001  
# Master TX Completed.  
#  
# Master Operation: Transmitting Read Address: 36  
# Master TX Started. Control Bits: 110, Transmitted Data: 00100100  
# Master TX Completed.  
#  
# Master Operation: Receiving Read data  
# Master RX Started. Control Bits: 111  
# Master RX Completed. Received Data: 129  
#  
# [MATCH] Addr = 36, Expected = 129, Received = 129  
#  
# ----- Test Case 2 -----  
#  
# Master Operation: Transmitting Write Address: 9  
# Master TX Started. Control Bits: 000, Transmitted Data: 00001001  
# Master TX Completed.  
#
```

```
# Master Operation: Transmitting Write Data: 99
# Master TX Started. Control Bits: 001, Transmitted Data: 01100011
# Master TX Completed.
#
# Master Operation: Transmitting Read Address: 9
# Master TX Started. Control Bits: 110, Transmitted Data: 00001001
# Master TX Completed.
#
# Master Operation: Receiving Read data
# Master RX Started. Control Bits: 111
# Master RX Completed. Received Data: 99
#
# [MATCH] Addr = 9, Expected = 99, Received = 99
```

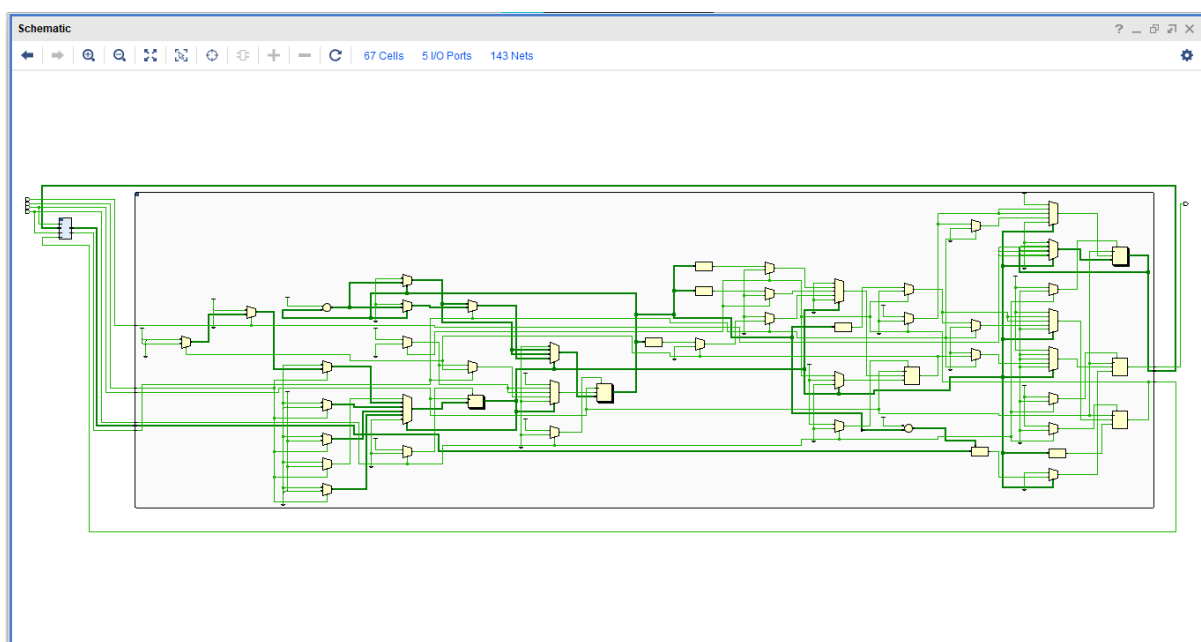
```
(* fsm_encoding = "sequential" *)
```

Elaboration

“Messages” tab

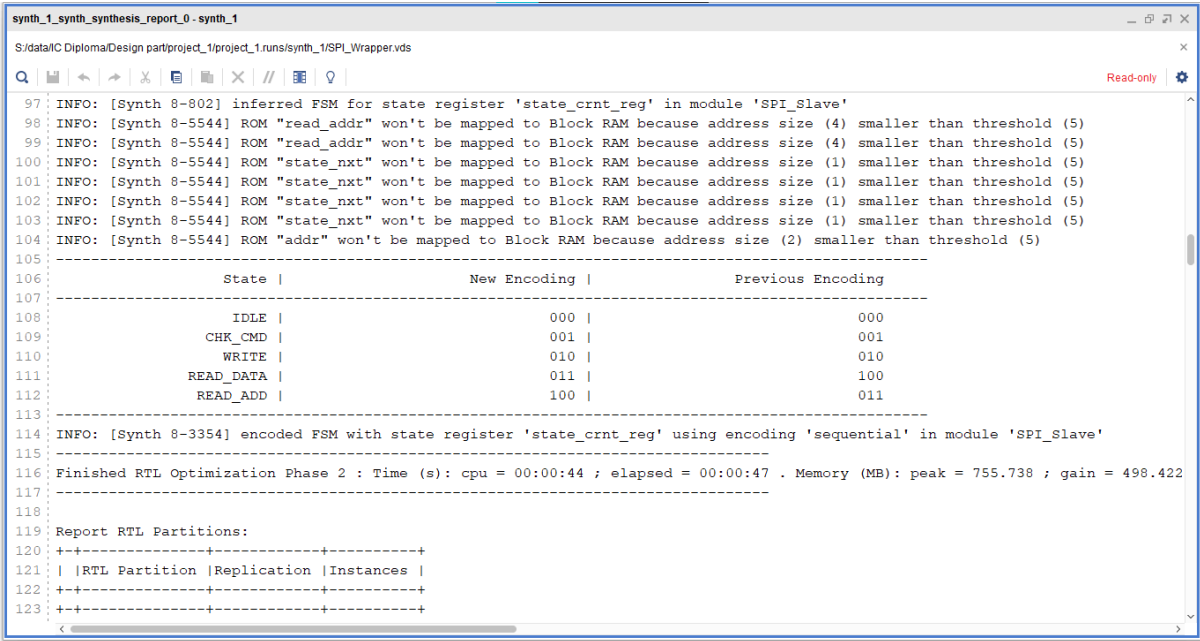


Schematic snippet

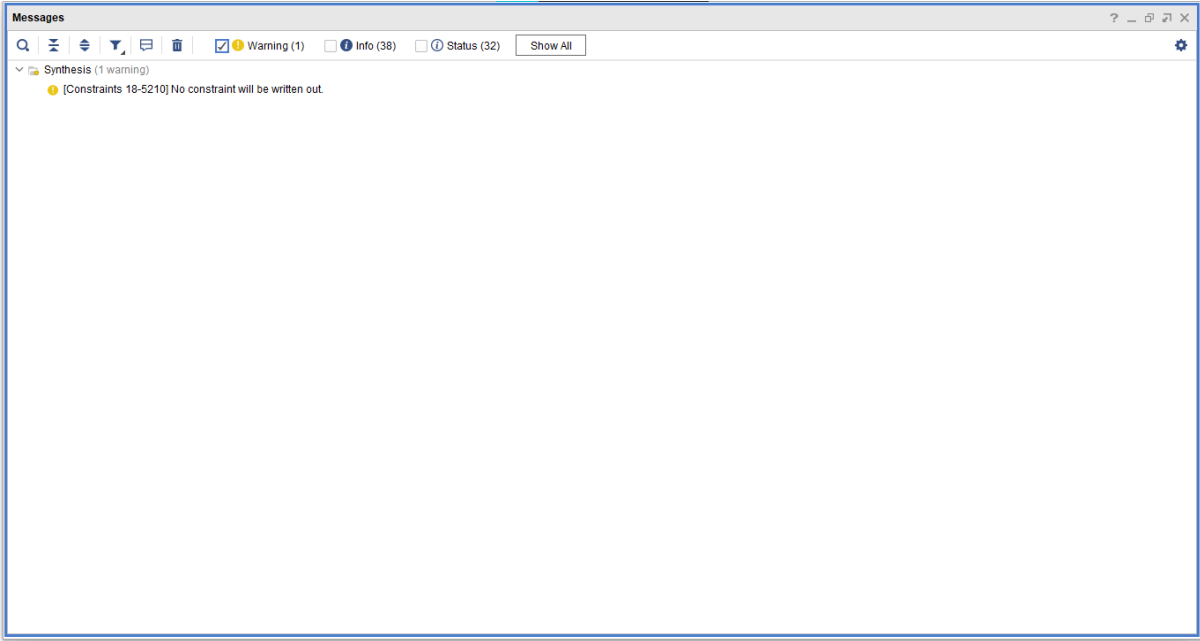


Synthesis

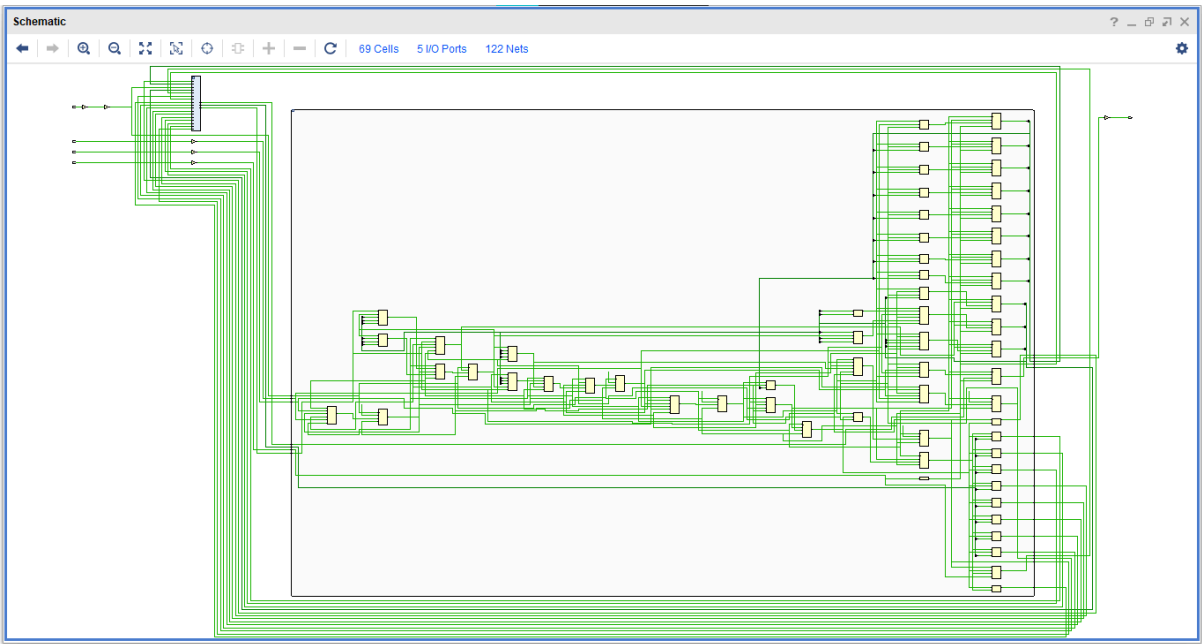
Synthesis report



“Messages” tab



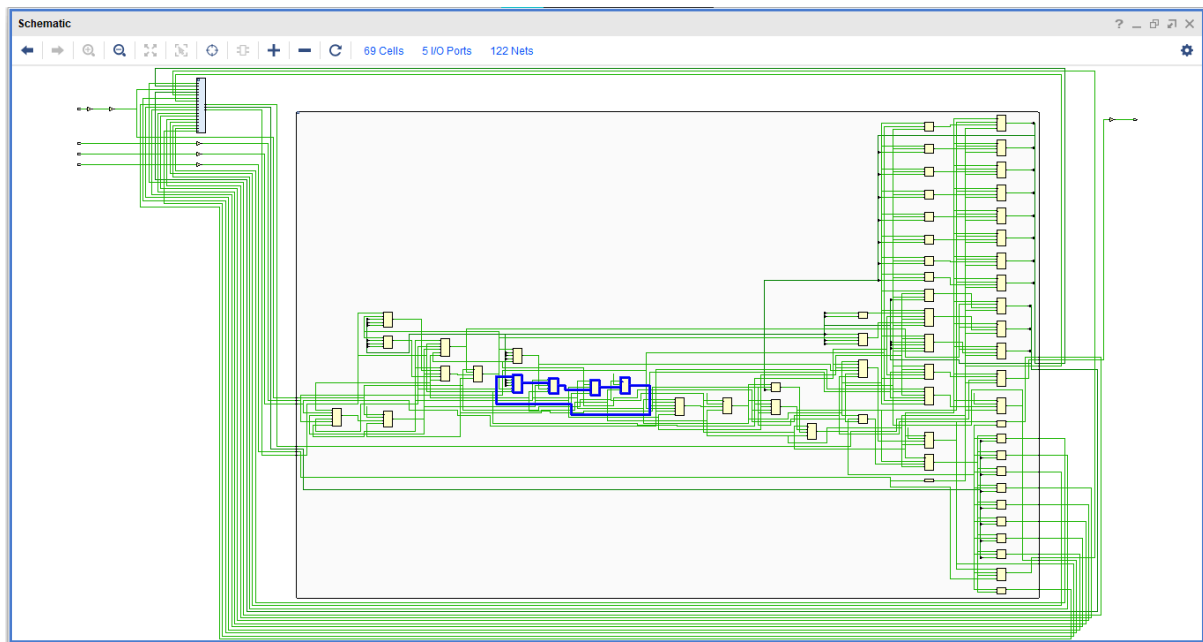
Schematic snippet



Timing report

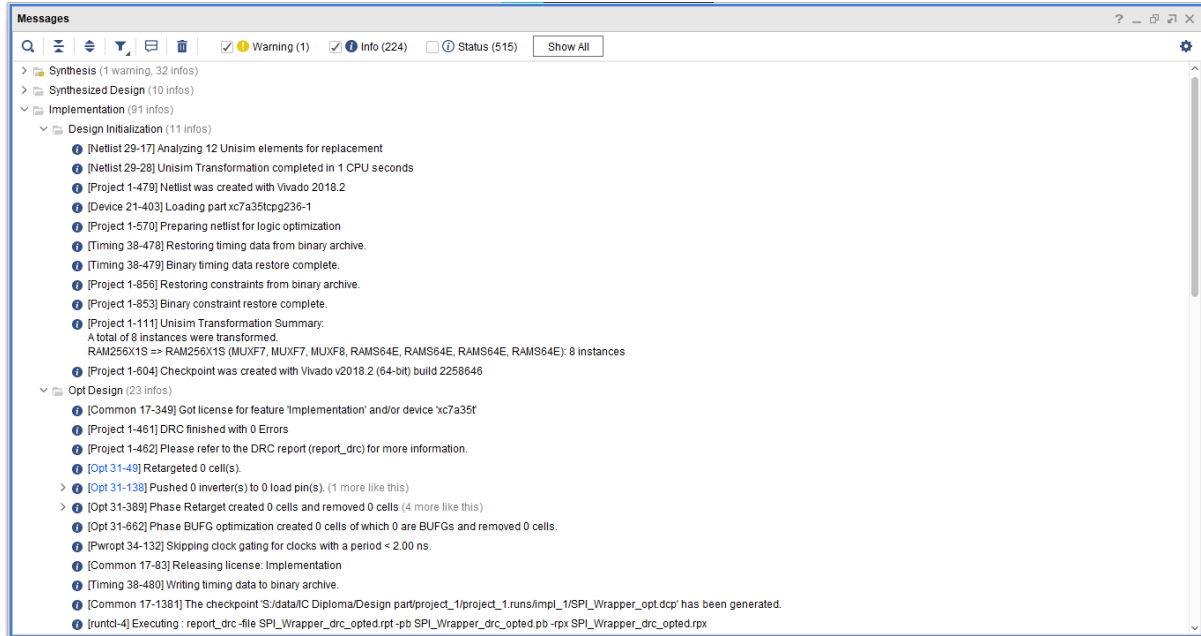
Timing			
Design Timing Summary			
<div>General Information</div> <div>Timer Settings</div> <div>Design Timing Summary</div> <div>Clock Summary (1)</div> <div>Check Timing (4)</div> <div>Intra-Clock Paths</div> <div>Inter-Clock Paths</div> <div>Other Path Groups</div> <div>User Ignored Paths</div> <div>Unconstrained Paths</div>	Setup		Hold
	Worst Negative Slack (WNS): 1.982 ns		Worst Hold Slack (WHS): 0.077 ns
	Total Negative Slack (TNS): 0.000 ns		Total Hold Slack (THS): 0.000 ns
	Number of Failing Endpoints: 0		Number of Failing Endpoints: 0
	Total Number of Endpoints: 389		Total Number of Endpoints: 389
	All user specified timing constraints are met.		
		Pulse Width	
		Worst Pulse Width Slack (WPWS): 1.250 ns	
		Total Pulse Width Negative Slack (TPWS): 0.000 ns	
		Number of Failing Endpoints: 0	
		Total Number of Endpoints: 70	

Critical path



Implementation

“Messages” tab

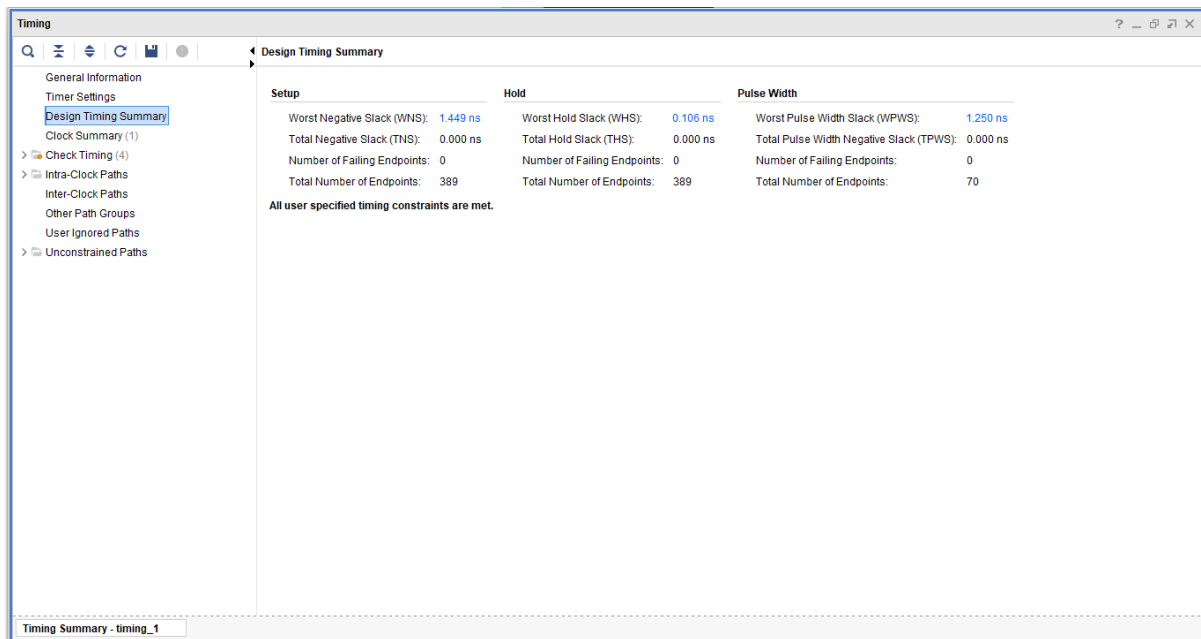


Utilization report

The Utilization window displays a hierarchy of utilization metrics. The metrics are categorized by type: Hierarchy, Summary, and Logic. The metrics are sorted by time, with the most recent at the top. The metrics include:

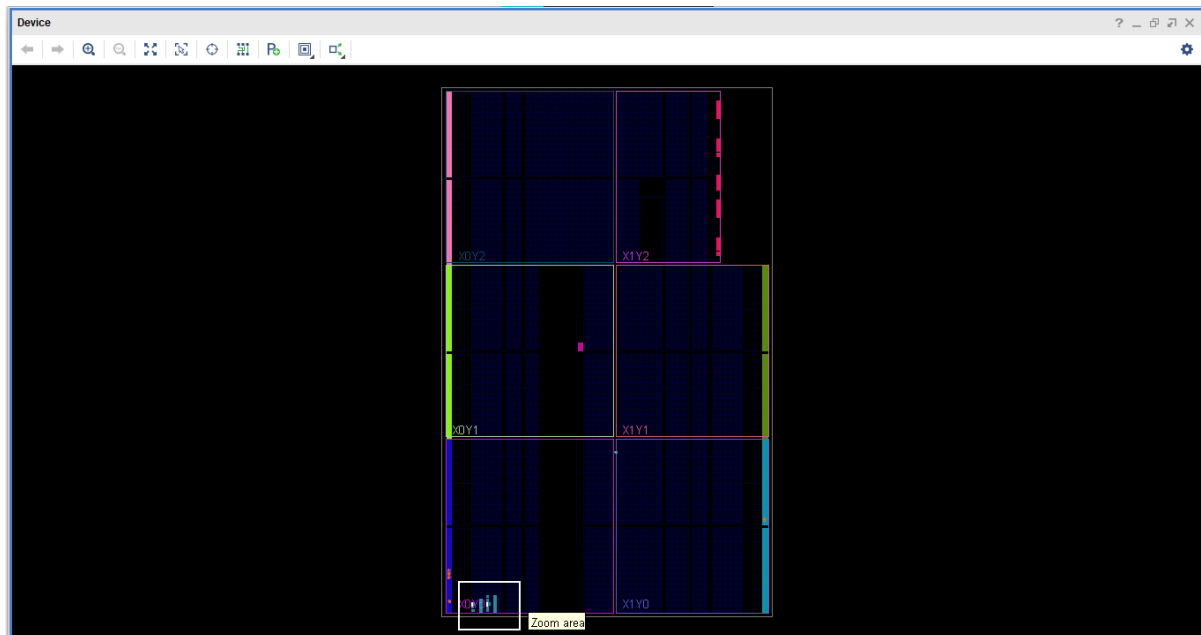
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
SPL_Wrapper	75	37	16	8	32	43	32	29	5	1
ram_inst (RAM)	35	17	16	8	21	3	32	0	0	0
spl_slave_inst (SPL_SLAVE)	40	20	0	0	22	40	0	19	0	0

Timing report

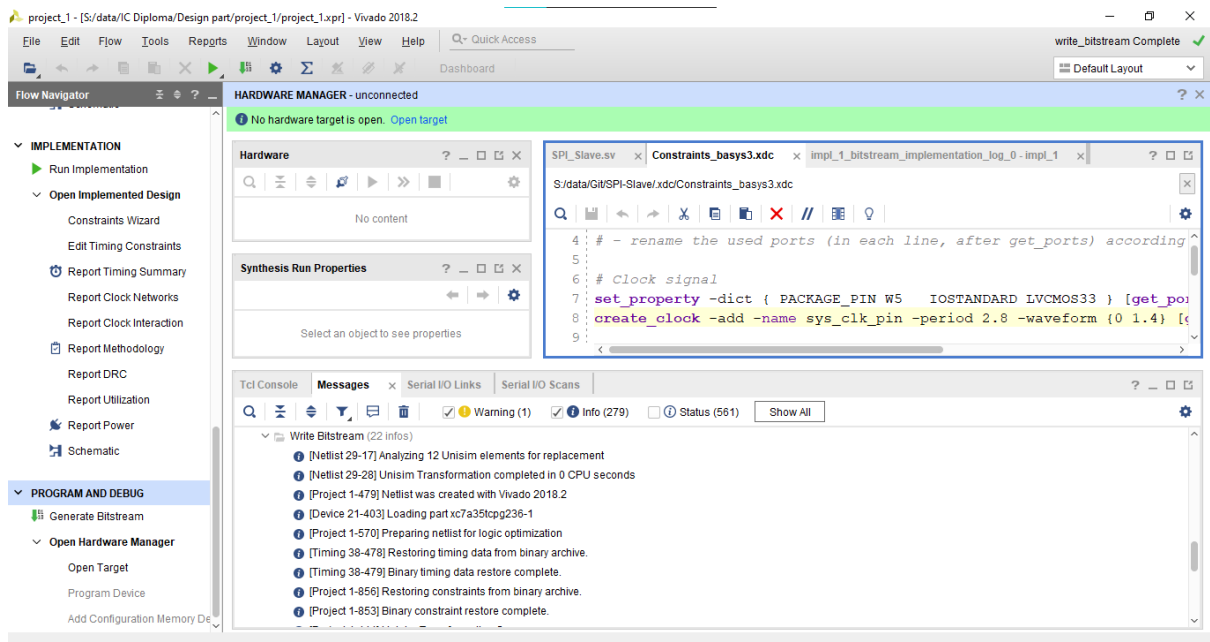


$$WNS = 1.449 \text{ ns}$$

Device snippet



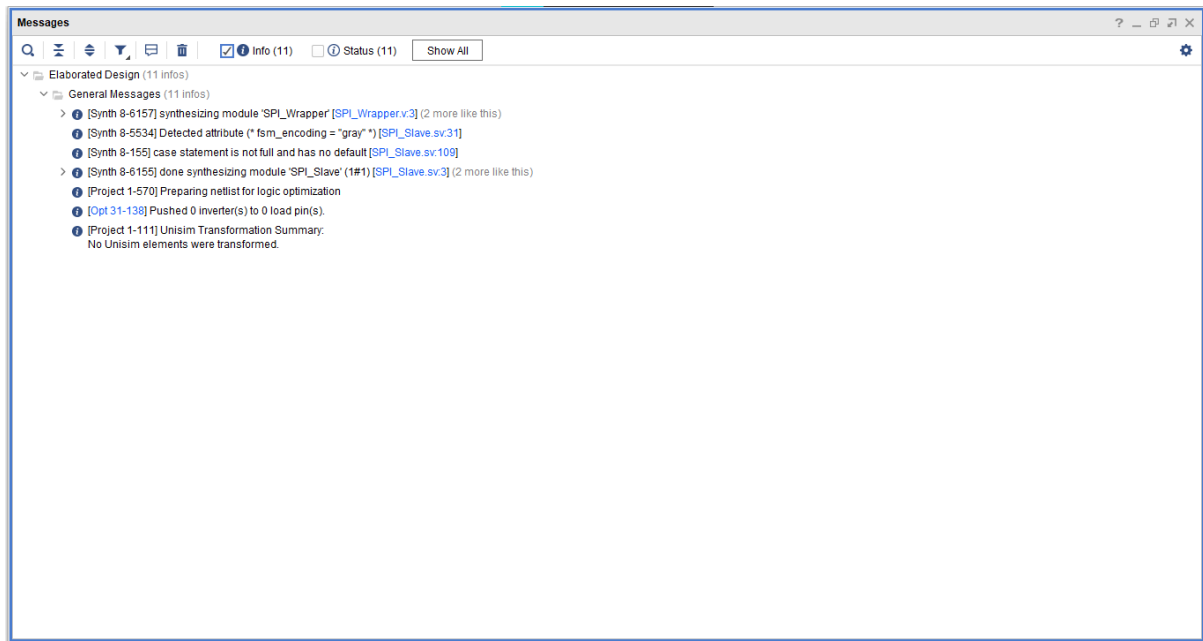
Bitstream Generation



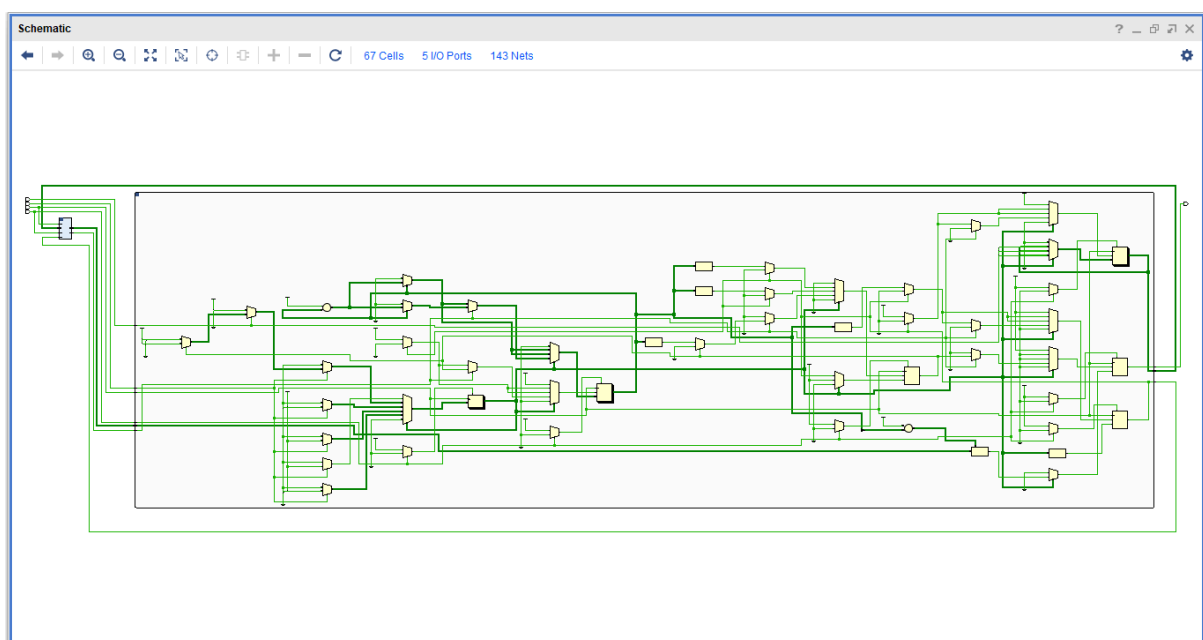
```
(* fsm_encoding = "gray" *)
```

Elaboration

“Messages” tab



Schematic snippet



Synthesis report

```
synth_1_synth_synth_report_0 - 1
```

S:/data/IC Diploma/Design part/project_1/runs/synth_1/SPI_Wrapper.vds

97 INFO: [Synth 8-802] inferred FSM for state register 'state_crnt_reg' in module 'SPI_Slave'

98 INFO: [Synth 8-5544] ROM "read_addr" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

99 INFO: [Synth 8-5544] ROM "read_addr" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

100 INFO: [Synth 8-5544] ROM "state_nxt" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

101 INFO: [Synth 8-5544] ROM "state_nxt" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

102 INFO: [Synth 8-5544] ROM "state_nxt" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

103 INFO: [Synth 8-5544] ROM "state_nxt" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

104 INFO: [Synth 8-5544] ROM "addr" won't be mapped to Block RAM because address size (2) smaller than threshold (5)

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	011	010
READ_DATA	010	100
READ_ADD	111	011

114 INFO: [Synth 8-3354] encoded FSM with state register 'state_crnt_reg' using encoding 'gray' in module 'SPI_Slave'

116 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:47 ; elapsed = 00:00:52 . Memory (MB): peak = 757.070 ; gain = 499.547

119 Report RTL Partitions:

RTL Partition	Replication	Instances
+	+	+
+	+	+
+	+	+
+	+	+

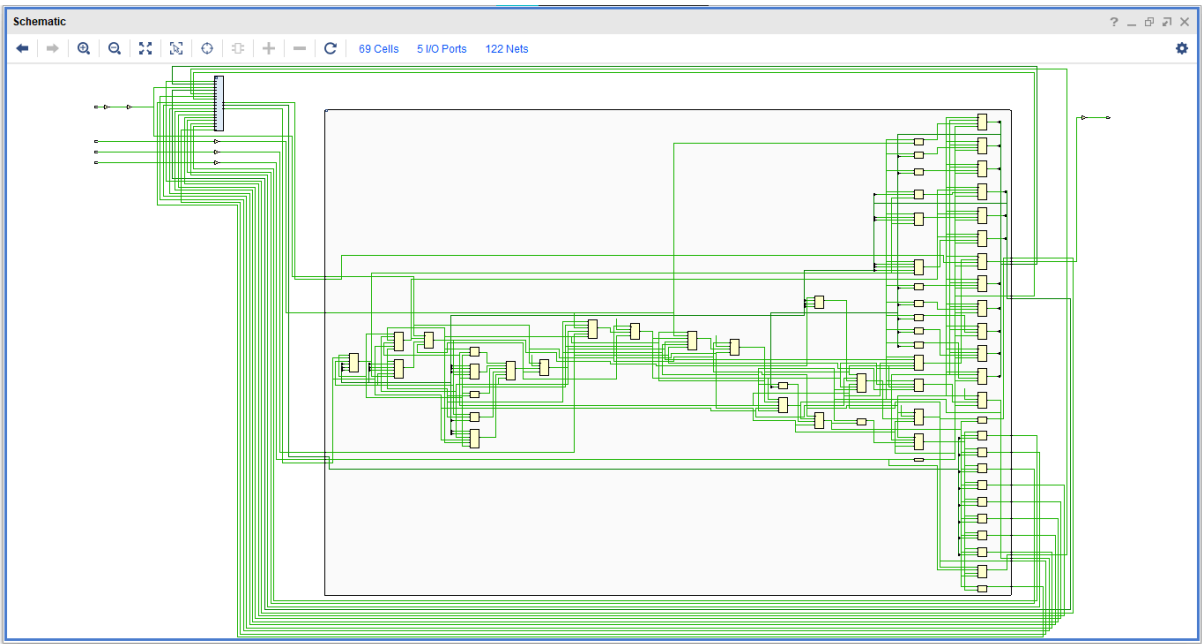
“Messages” tab

Messages

Warning (1) Info (43) Status (24) Show All

- Elaborated Design (11 Infos)
- Synthesis (1 warning, 32 Infos)
 - [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35f'
 - [Synth 8-6157] synthesizing module 'SPL_Wrapper' [SPL_Wrapper.v3] (2 more like this)
 - [Synth 8-5534] Deleted attribute (" fsm_encoding = "gray") [SPL_Slave.sv:31]
 - [Synth 8-155] case statement is not full and has no default [SPL_Slave.sv:109]
 - [Synth 8-6155] done synthesizing module 'SPL_Slave' (1#1) [SPL_Slave.sv:3] (2 more like this)
 - [Device 21-403] Loading part xc7a35tcpg236-1
 - [Project 1-236] Implementation specific constraints were found while reading constraint file [S:/data/Git/SPI-Slave/xdc/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation.
Impacted constraints are listed in the file [X:/SPL_Wrapper_proprietary.xdc].
Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
 - [Synth 8-802] inferred FSM for state register 'state_cmt_reg' in module 'SPL_Slave'
 - [Synth 8-5544] ROM "read_addr" won't be mapped to Block RAM because address size (4) smaller than threshold (5) (6 more like this)
 - [Synth 8-3354] encoded FSM with state register 'state_cmt_reg' using encoding 'gray' in module 'SPL_Slave'
 - [Project 1-571] Translating synthesized netlist
 - [Netlist 29-17] Analyzing 12 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-570] Preparing netlist for logic optimization (1 more like this)
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
 - [Common 17-83] Releasing license: Synthesis
 - [Constraints 18-5210] No constraint will be written out.
 - [Common 17-1381] The checkpoint 'S:/data/C/Diploma/Design part/project_1/runs/synth_1/SPL_Wrapper.dcp' has been generated.
 - [runtci-4] Executing : report_utilization -file SPL_Wrapper_utilization_synth.rpt -pb SPL_Wrapper_utilization_synth.pb
 - [Common 17-206] Exiting Vivado at Tue Sep 9 02:48:32 2025...

Schematic snippet



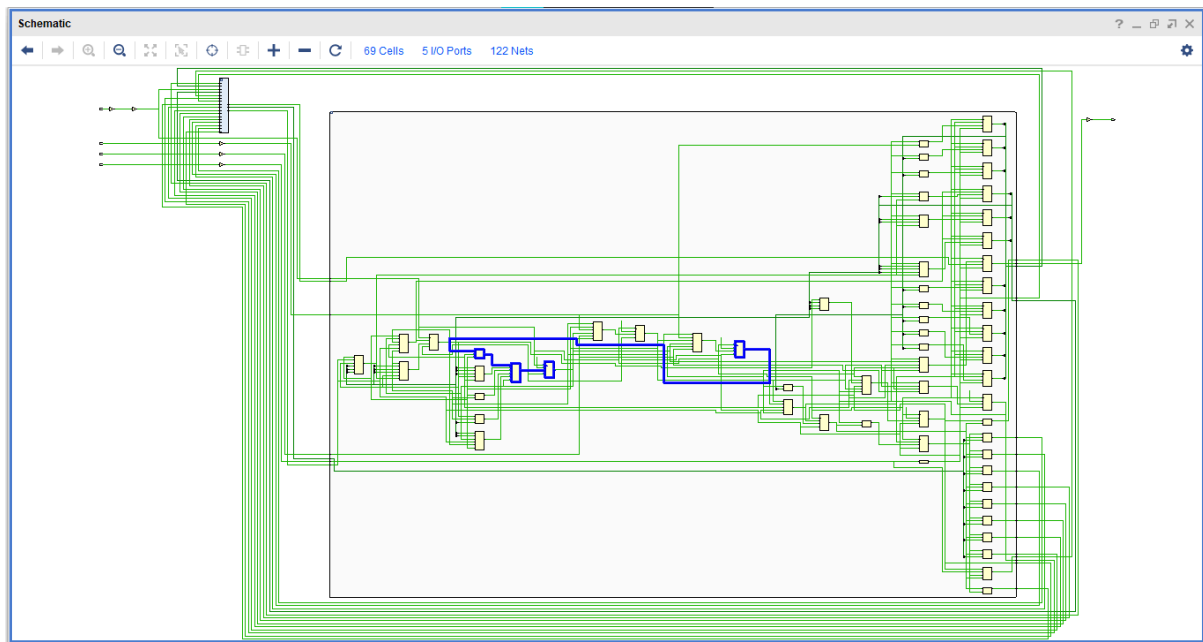
Timing report

A screenshot of a timing report window titled "Timing". The window displays a "Design Timing Summary" table. The table is organized into three columns: Setup, Hold, and Pulse Width. Each column contains several rows of timing data. The "Setup" column shows Worst Negative Slack (WNS), Total Negative Slack (TNS), Number of Failing Endpoints, and Total Number of Endpoints. The "Hold" column shows Worst Hold Slack (WHS), Total Hold Slack (THS), Number of Failing Endpoints, and Total Number of Endpoints. The "Pulse Width" column shows Worst Pulse Width Slack (WPWS), Total Pulse Width Negative Slack (TPWS), Number of Failing Endpoints, and Total Number of Endpoints. The table indicates that all user specified timing constraints are met.

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 2.081 ns	Worst Hold Slack (WHS): 0.077 ns	Worst Pulse Width Slack (WPWS): 1.250 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 389	Total Number of Endpoints: 389	Total Number of Endpoints: 70

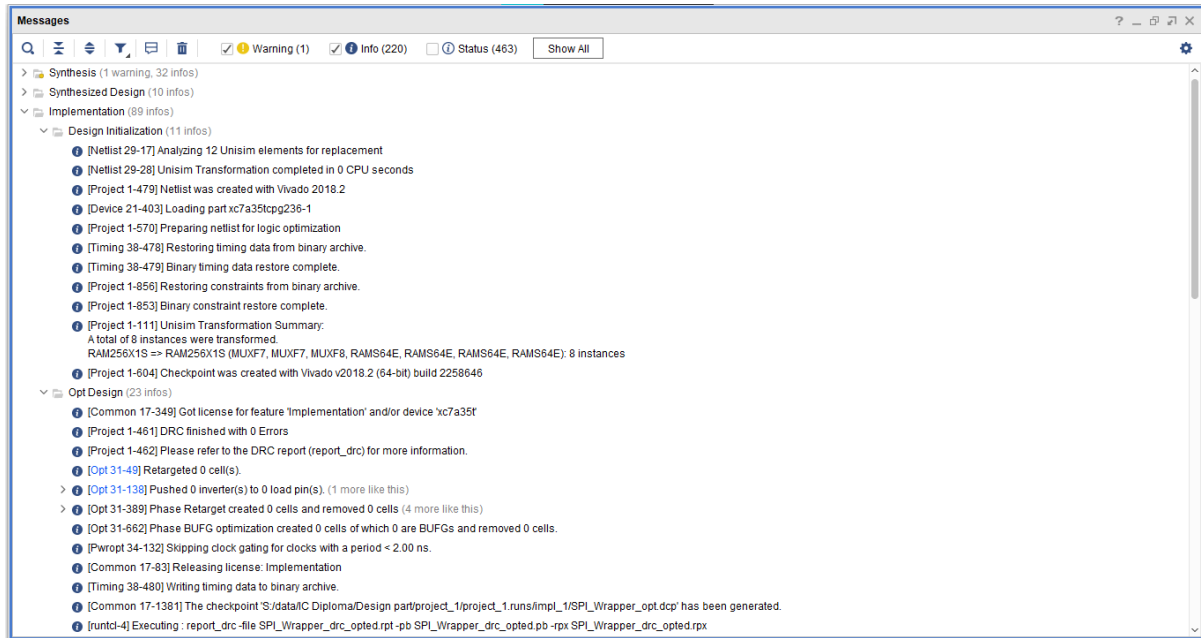
All user specified timing constraints are met.

Critical path



Implementation

“Messages” tab



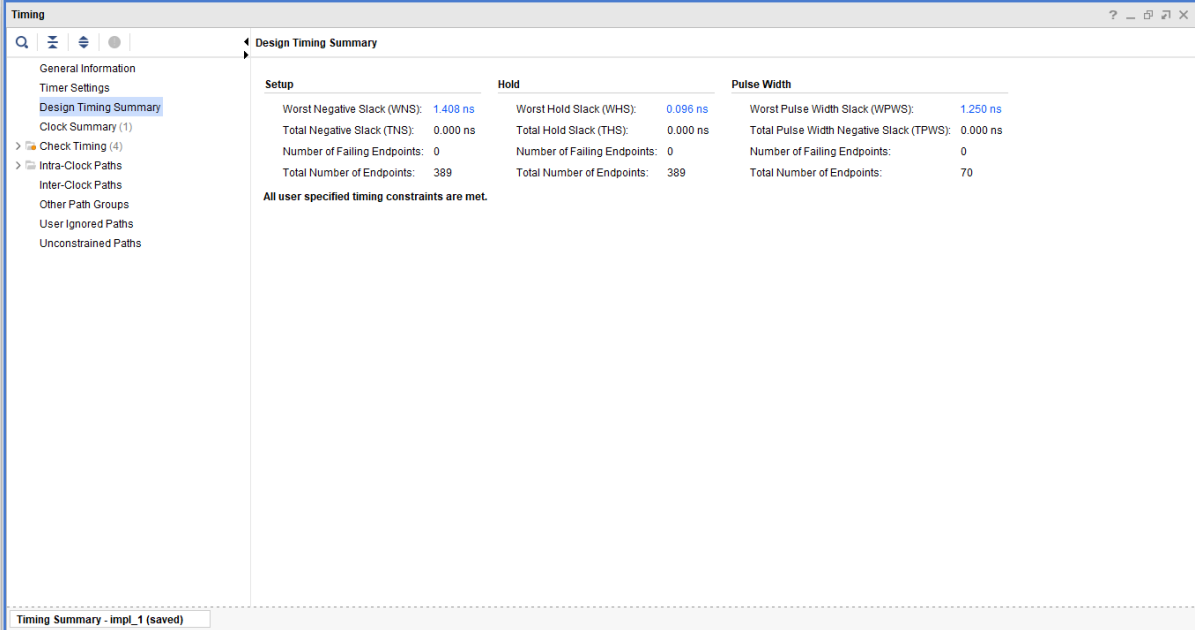
Utilization report

The Utilization window displays a table of resource utilization for the SPL_Wrapper design. The table is organized into a hierarchy, with the following categories visible:

- Hierarchy
 - Summary
 - Slice Logic
 - Slice LUTs (1%)
 - LUT as Memory (1%)
 - LUT as Distributed F
 - LUT as Logic (<1%)
 - F8 Muxes (<1%)
 - F7 Muxes (<1%)
 - Slice Registers (<1%)
 - Register as Flip Flop (<1%)
 - Slice Logic Distribution
 - Slice (<1%)
 - SLICEM
 - SLICEL
 - LUT as Memory (1%)
 - LUT as Distributed RAM
 - using O6 output only
 - LUT Flip Flop Pairs (<1%)
 - LUT-FF pairs with one ur
 - fully used LUT-FF pairs
 - LUT-FF pairs with one ur
 - LUT as Logic (<1%)
 - using O5 and O6
 - using O6 output only
 - Memory
 - DSP
 - In and Out Specific

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
SPL_Wrapper	70	37	16	8	23	38	32	24	5	1
ram_inst (RAM)	35	17	16	8	14	3	32	0	0	0
spl_slave_inst (SPL_SLAVE)	35	20	0	0	14	35	0	19	0	0

Timing report



The image shows a screenshot of the 'Timing' window in a design tool, specifically the 'Design Timing Summary' tab. The window has a sidebar on the left with a tree view containing 'General Information', 'Timer Settings', 'Design Timing Summary' (selected), 'Clock Summary (1)', 'Check Timing (4)', 'Intra-Clock Paths', 'Inter-Clock Paths', 'Other Path Groups', 'User Ignored Paths', and 'Unconstrained Paths'. The main area displays a table with three columns: 'Setup', 'Hold', and 'Pulse Width'. Each column contains three rows of data: 'Worst Negative Slack (WNS)', 'Total Negative Slack (TNS)', and 'Number of Failing Endpoints'. The 'WNS' value is 1.408 ns, 'TNS' is 0.000 ns, and the number of failing endpoints is 0. Below the table, a message states 'All user specified timing constraints are met.' The bottom status bar shows 'Timing Summary - impl_1 (saved)'.

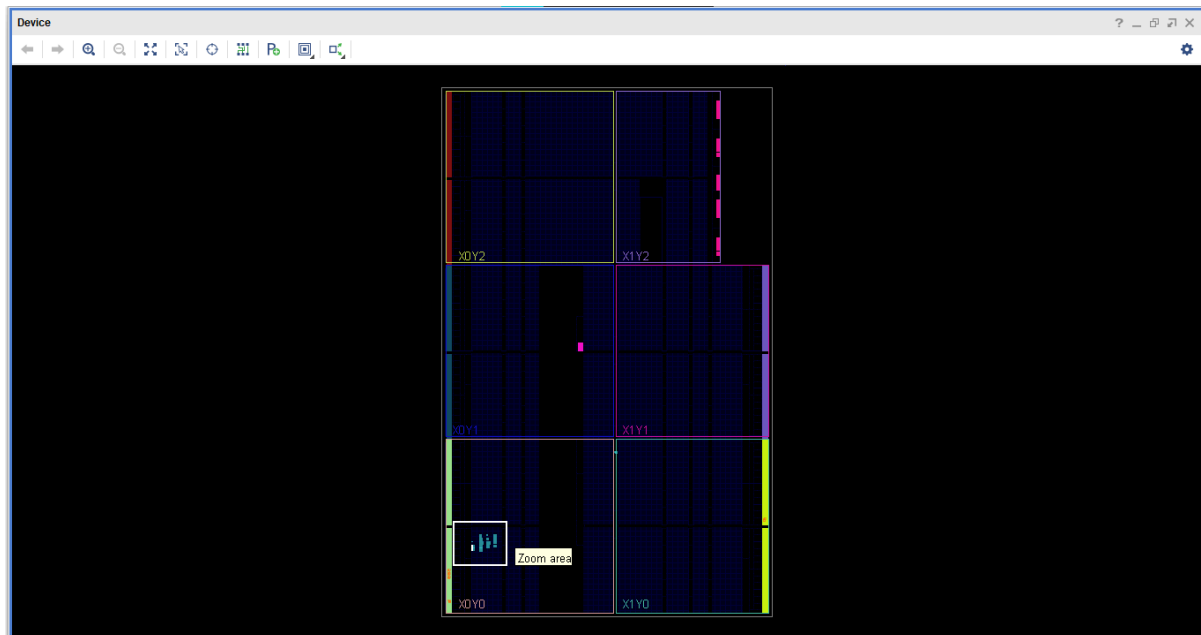
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 1.408 ns	Worst Hold Slack (WHS): 0.096 ns	Worst Pulse Width Slack (WPWS): 1.250 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 389	Total Number of Endpoints: 389	Total Number of Endpoints: 70

All user specified timing constraints are met.

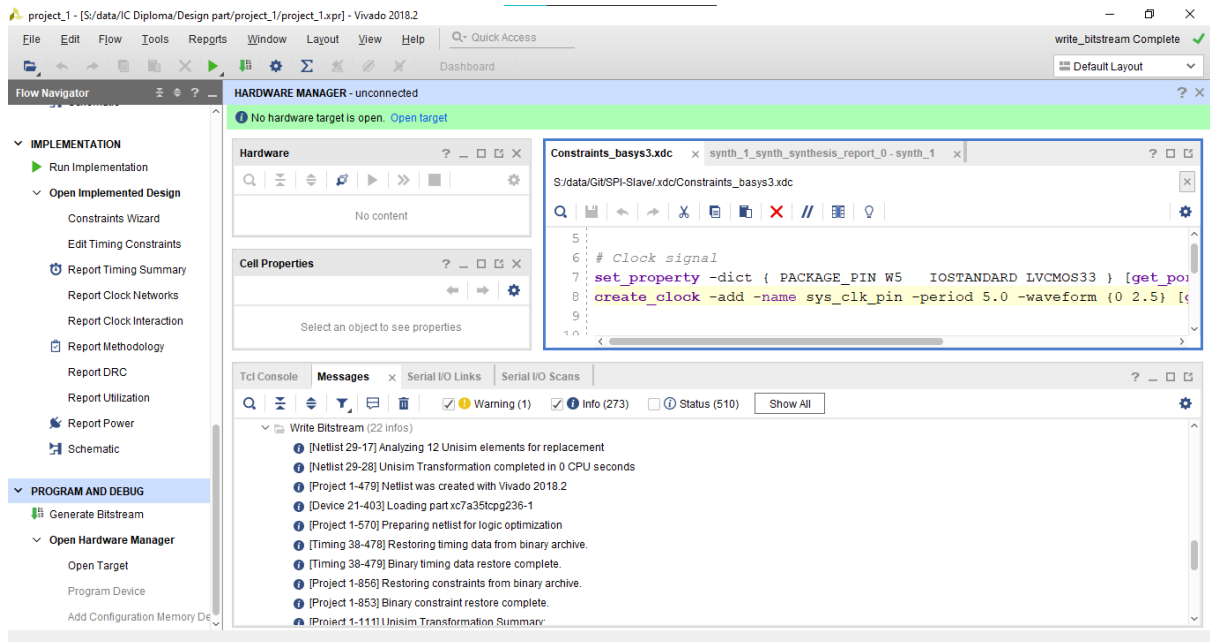
Timing Summary - impl_1 (saved)

$$WNS = 1.408 \text{ ns}$$

Device snippet



Bitstream Generation



HARDWARE MANAGER - unconnected

No hardware target is open. [Open target](#)

Hardware

No content

Cell Properties

Select an object to see properties

Constraints_basys3.xdc

```
5
6 # Clock signal
7 set_property -dict { PACKAGE_PIN W5  IOSTANDARD LVCMOS33 } [get_ports sys_clk_pin]
8 create_clock -add -name sys_clk_pin -period 5.0 -waveform {0 2.5} [get_ports sys_clk_pin]
9
```

Tcl Console

Messages

Warning (1) Info (273) Status (510) Show All

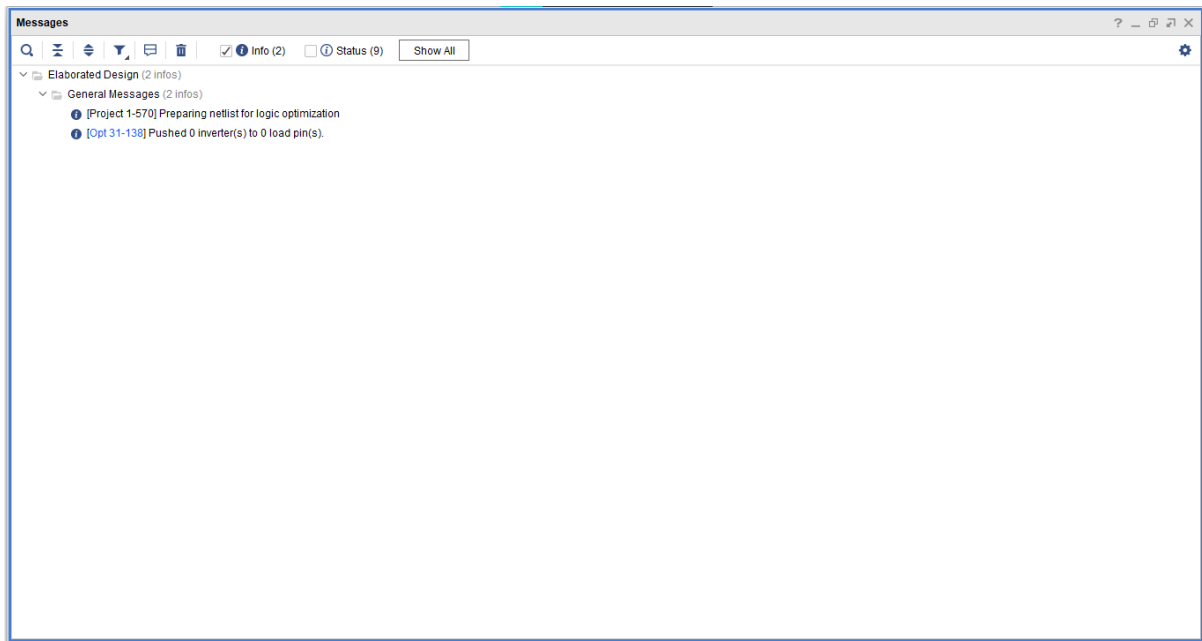
Write Bitstream (22 Infos)

- [Netlist 29-17] Analyzing 12 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-478] Netlist was created with Vivado 2018.2
- [Device 21-403] Loading part xc7a35tcbg236-1
- [Project 1-570] Preparing netlist for logic optimization
- [Timing 38-478] Restoring timing data from binary archive.
- [Timing 38-479] Binary timing data restore complete.
- [Project 1-856] Restoring constraints from binary archive.
- [Project 1-853] Binary constraint restore complete.
- [Project 1-1111] Unisim Transformation Summary

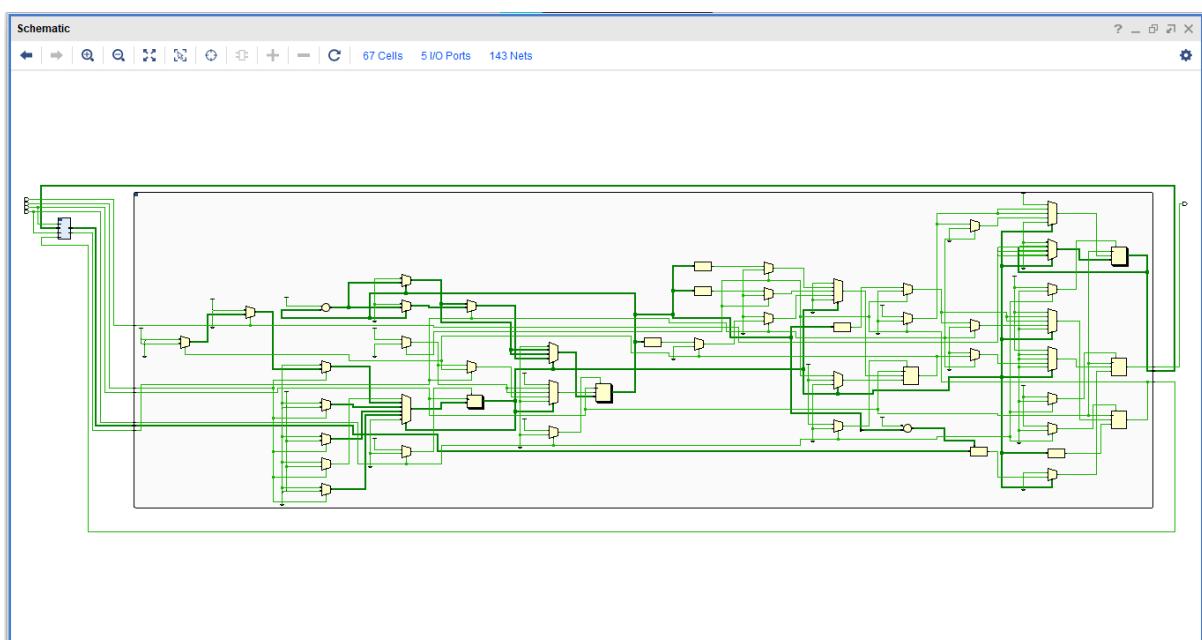
```
(* fsm_encoding = "one_hot" *)
```

Elaboration

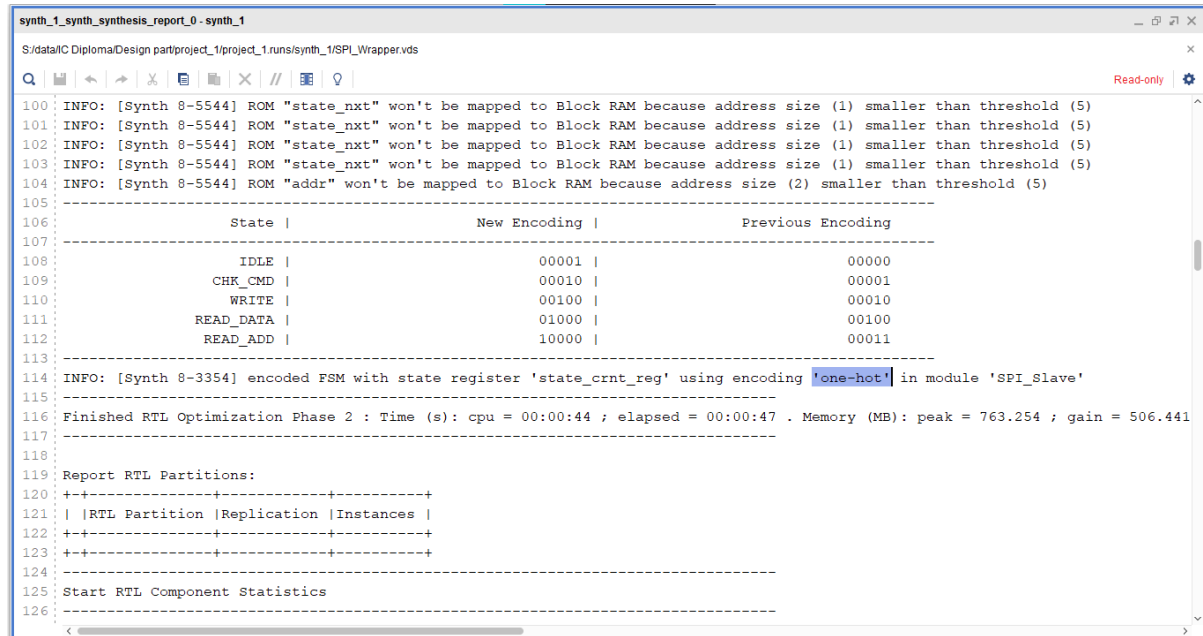
“Messages” tab



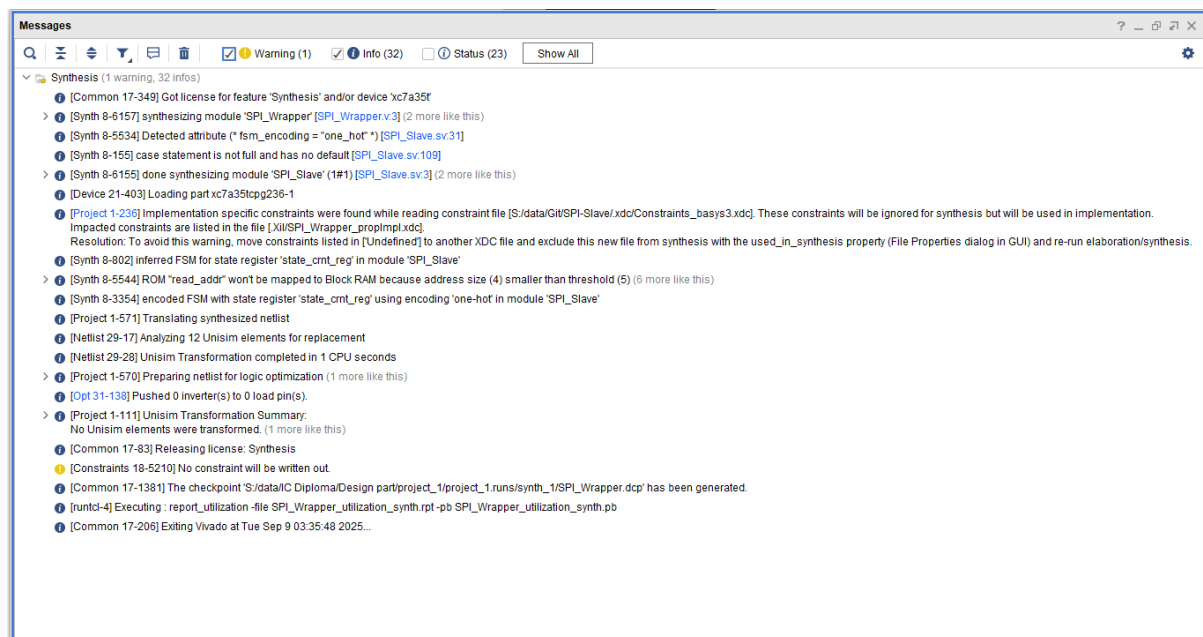
Schematic snippet



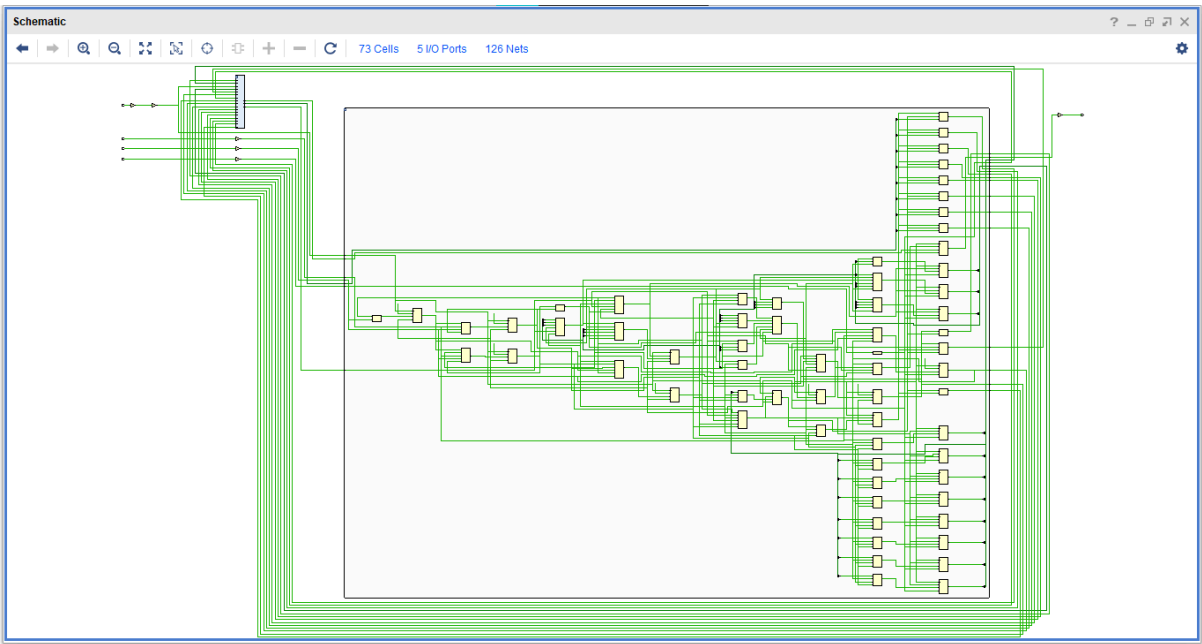
Synthesis report



“Messages” tab



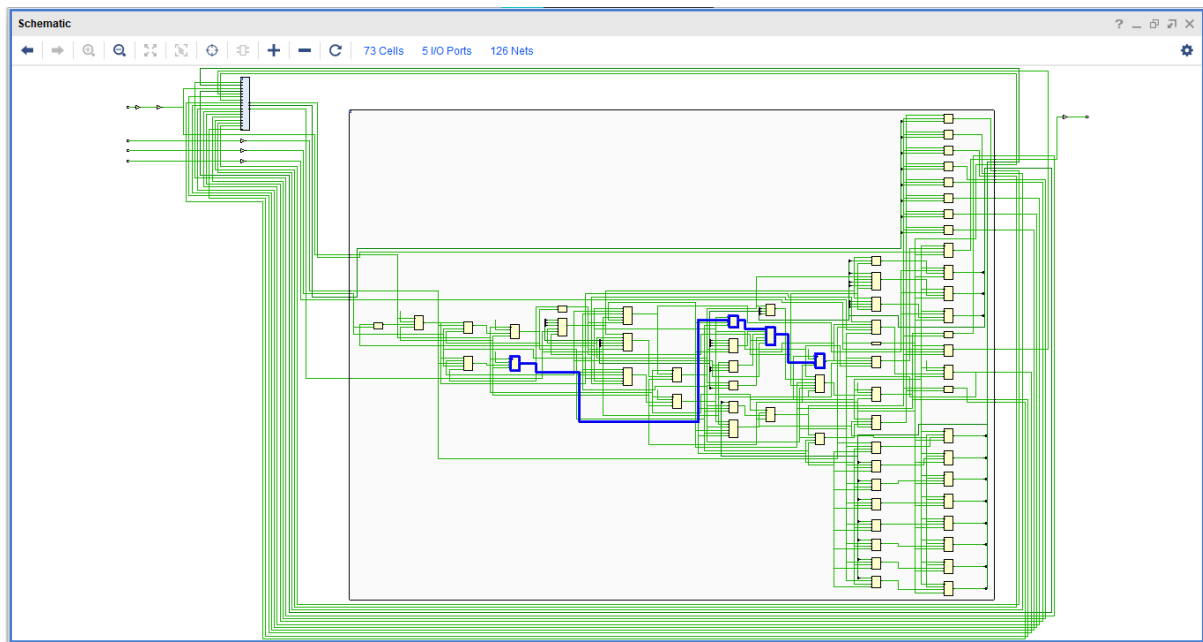
Schematic snippet



Timing report

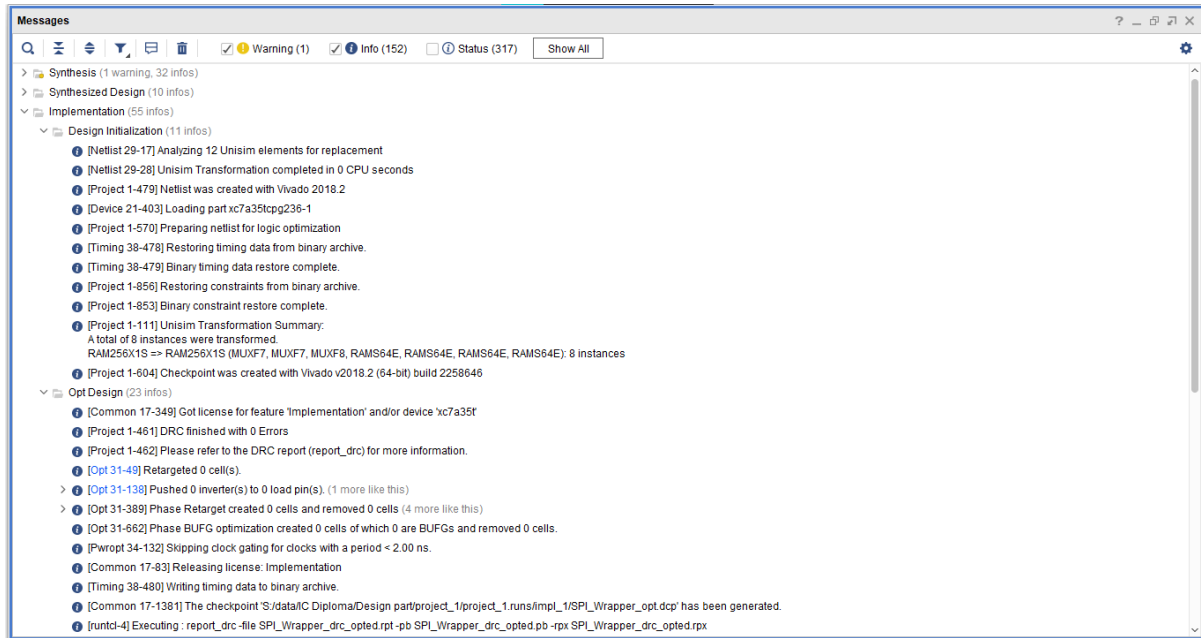
Timing			
Design Timing Summary			
General Information			
Timer Settings			
Design Timing Summary			
Clock Summary (1)			
Check Timing (4)			
Intra-Clock Paths			
Inter-Clock Paths			
Other Path Groups			
User Ignored Paths			
Unconstrained Paths			
Setup			
Hold			
Pulse Width			
Worst Negative Slack (WNS): 2.069 ns			
Worst Hold Slack (WHS): 0.077 ns			
Worst Pulse Width Slack (WPWS): 1.250 ns			
Total Negative Slack (TNS): 0.000 ns			
Total Hold Slack (THS): 0.000 ns			
Total Pulse Width Negative Slack (TPWS): 0.000 ns			
Number of Failing Endpoints: 0			
Number of Failing Endpoints: 0			
Number of Failing Endpoints: 0			
Total Number of Endpoints: 391			
Total Number of Endpoints: 391			
Total Number of Endpoints: 72			
All user specified timing constraints are met.			
Timing Summary - timing_1			

Critical path



Implementation

“Messages” tab

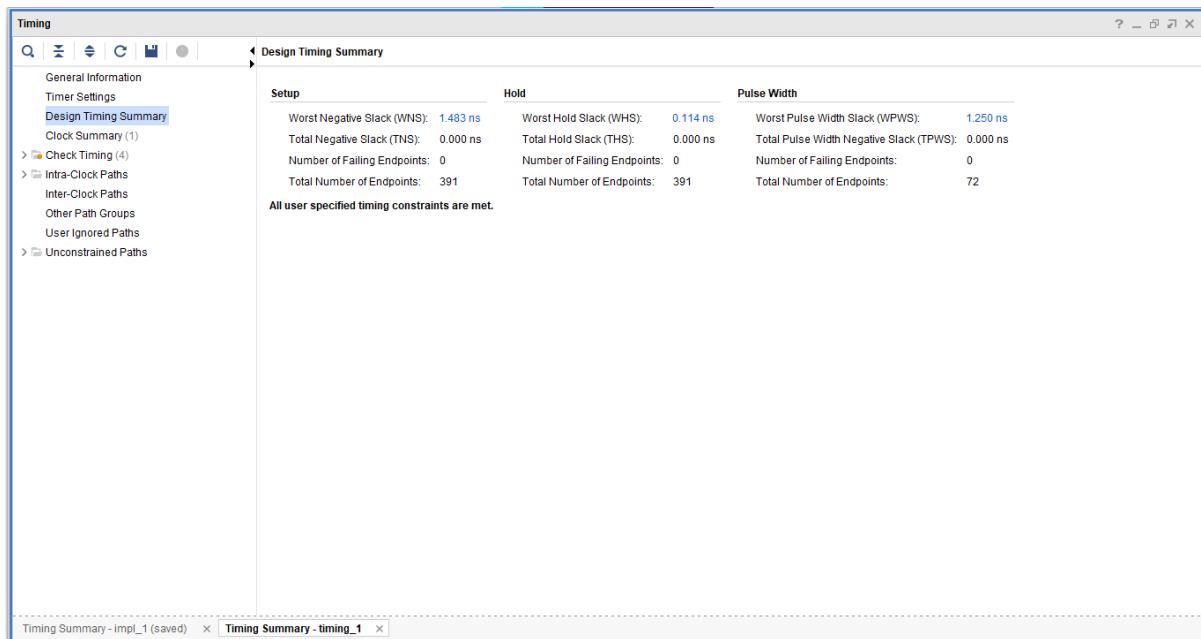


Utilization report

The Utilization window displays the utilization report for the design. The report is organized into a hierarchy of categories, including Slice Logic, Slice Registers, Slice Logic Distribution, Memory, and DSP. The report shows the utilization of various resources, including Slice LUTs, Slice Registers, F7 Muxes, F8 Muxes, Slice (815 0), LUT as Logic (20800), LUT as Memory (9600), LUT Flip Flop Pairs (20800), Bonded IOB (106), and BUFGCTRL (32).

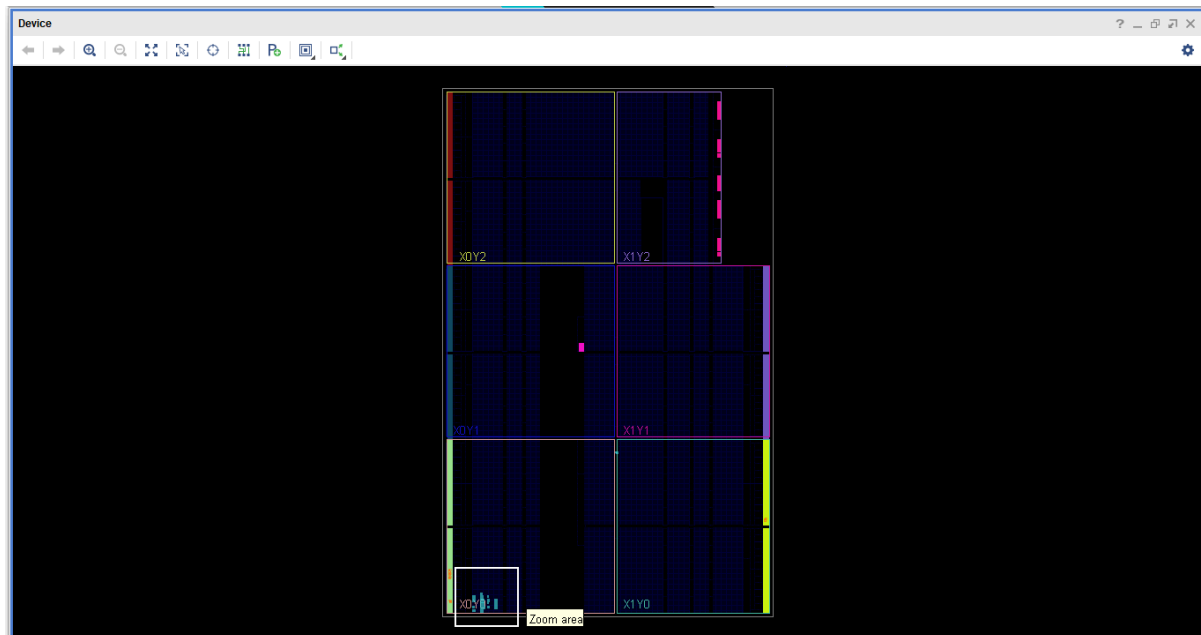
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (815 0)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
SPL_Wrapper	71	39	16	8	23	39	32	25	5	1
ram_inst (RAM)	35	17	16	8	16	3	32	0	0	0
spl_slave_inst (SPL_SLAVE)	36	22	0	0	13	36	0	20	0	0

Timing report

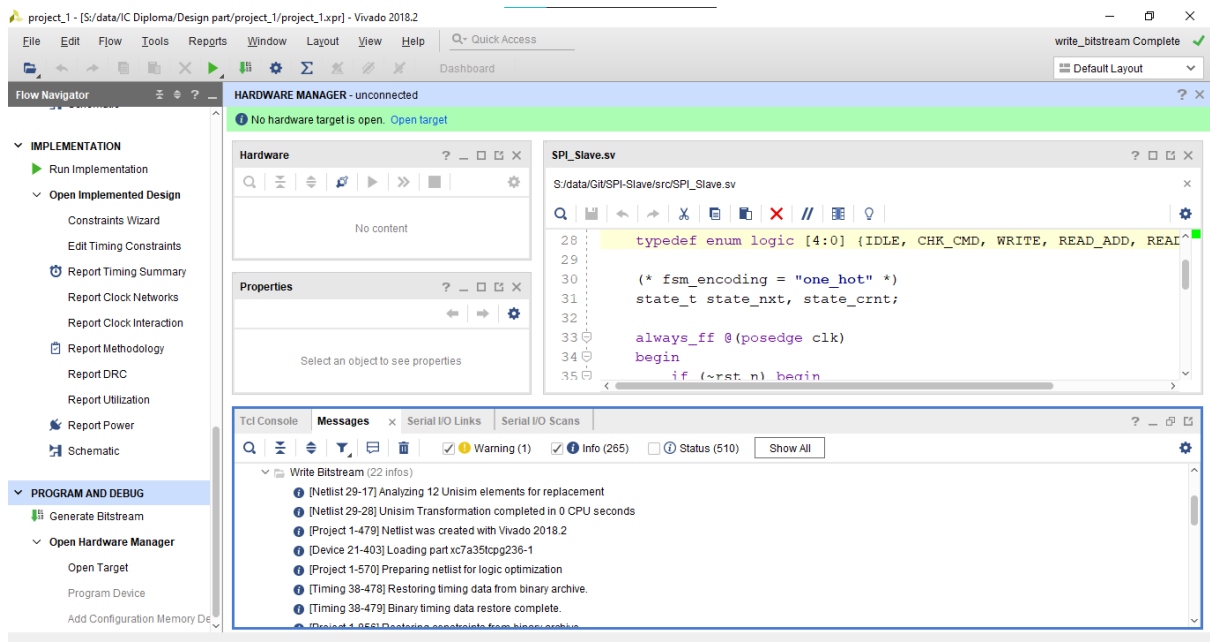


$$WNS = 1.483 \text{ ns}$$

Device snippet



Bitstream Generation



The fsm encoding that achieved the highest positive setup slack is the one will achieve the highest frequency (* fsm_encoding = "one_hot" *)