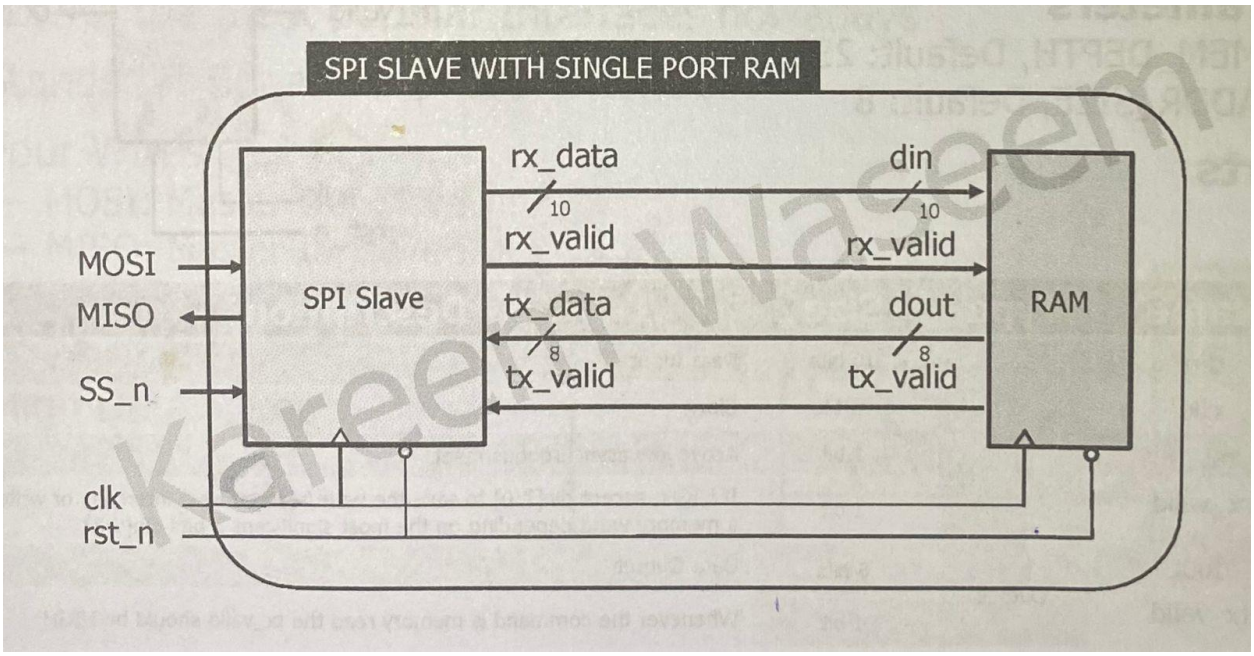
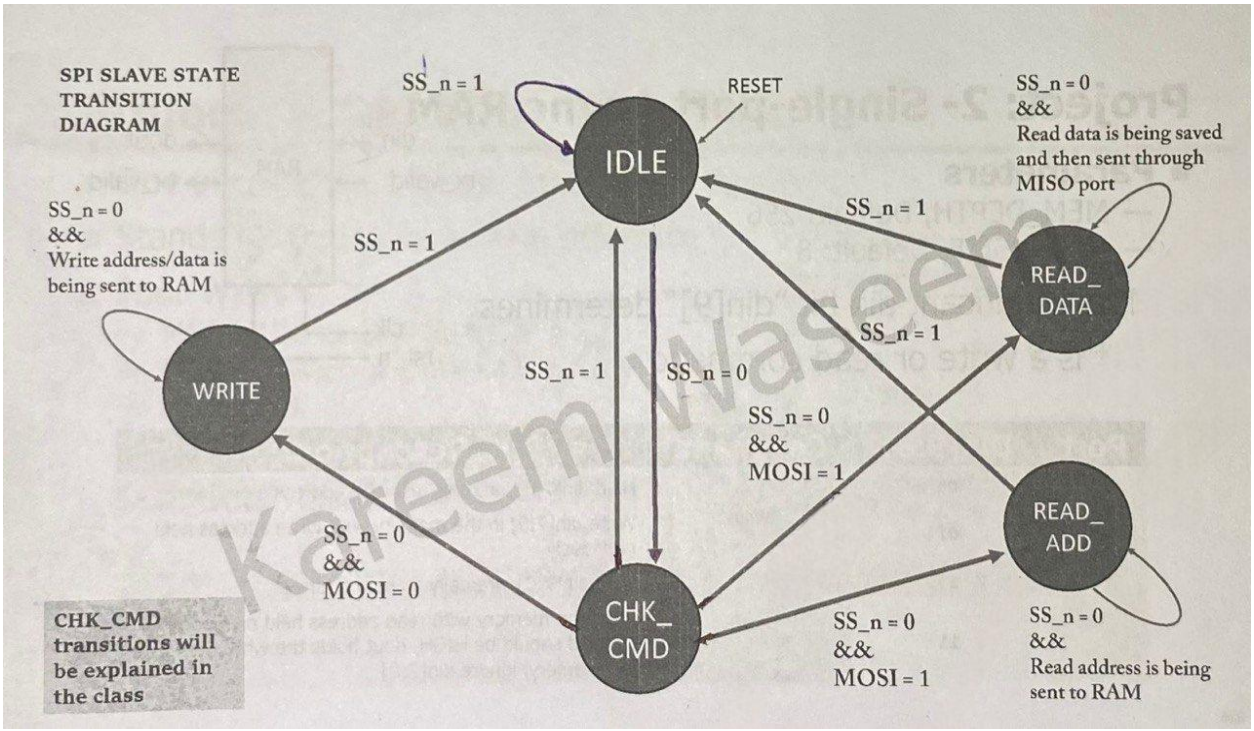
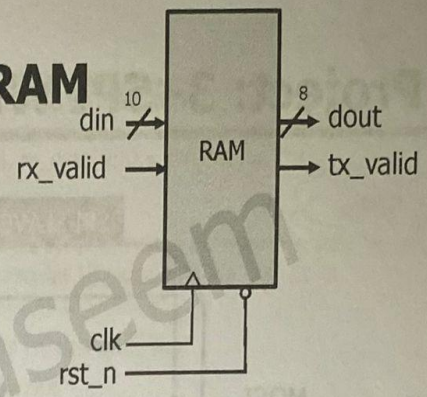
SPI SLAVE WITH SINGLE PORT RAM





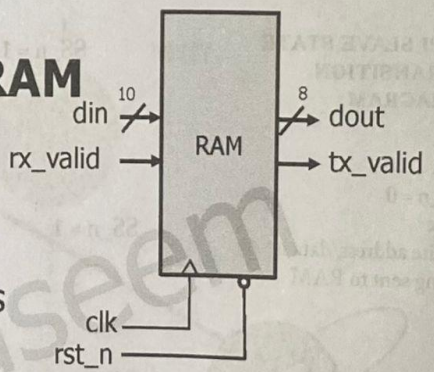
Project: 2- Single-port Async RAM



- **Parameters**
  - MEM_DEPTH, Default: 256
  - ADDR_SIZE, Default: 8
- **Ports**

Name	Type	Size	Description
din	Input	10 bits	Data Input
clk		1 bit	Clock
rst_n		1 bit	Active low asynchronous reset
rx_valid		1 bit	If HIGH: accept din[7:0] to save the write/read address internally or write a memory word depending on the most significant 2 bits din[9:8]
dout	Output	8 bits	Data Output
tx_valid		1 bit	Whenever the command is memory read the tx_valid should be HIGH

Project: 2- Single-port Async RAM



- **Parameters**
  - MEM_DEPTH, Default: 256
  - ADDR_SIZE, Default: 8
- Most significant din bit "din[9]" determines if it is a write or read command

Port	Din[9:8]	Command	Description
din	00	Write	Hold din[7:0] internally as write address
	01		Write din[7:0] in the memory with write address held previously
	10	Read	Hold din[7:0] internally as read address
	11		Read the memory with read address held previously, tx_valid should be HIGH, dout holds the word read from the memory, ignore din[7:0]

*sync RAM .