EECS 247

Analog-Digital Interface Integrated Circuits

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Instructor's Technical Background

- Ph.D., EECS department -UC Berkeley 1985, advisor Prof. P.R. Gray
 - Thesis topic: Continuous-time CMOS high-frequency filters
- · Industrial background
 - 11 years at ATT & Bell Laboratories, N.J., in the R&D area as a circuit designer
 - Circuits for wireline communications: CODECs, ISDN, and DSL including ADCs (nyquist rate & over-sampled), DACs, filters, VCOs
 - Circuits intended for wireless applications
 - Fiber-optics circuits
 - 3 years at Philips Semiconductors, Sunnyvale, CA
 - Managed a group in the RF IC department- developed ICs for CDMA & analog cell phones
 - 3 years @ Broadcom Corp. Director of Analog/RF ICs in San Jose, CA.
 - Projects: Gigabit-Ethernet, TV tuners, and DSL circuitry
 - Currently consultant for IC design
- Teaching experience
 - Has taught/co-taught EE247 @ UCB since 2003
 - Instructor for short courses offered by MEAD Electronics
 - Adjunct Prof. @ Rutgers Univ., N.J.: Taught a graduate level IC course

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Administrative Issues

Course web page:

http://inst.eecs.berkeley.edu/~EE247/fa08

- Course notes will be uploaded on the course website prior to each class
- Homeworks & due dates are posted on the course website
- Announcements regarding the course will be posted on the home page, please visit course website often

Lectures are web cast

http://webcast.berkelev.edu/courses

- Please try to attend the classes live to benefit from direct interactions
- Make sure you use the provided microphones when asking questions or commenting in the class

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Office Hours & Grading

- · Office hours:
 - Tues./Thurs. 2:30-3:30pm @ 477 Cory Hall (unless otherwise announced in the class)
 - Extra office hours by appointment
 - Feel free to discuss issues via email: haidehk@eecs.berkeley.edu
- Course grading:
 - Homework/project 50%
 - Midterm 20% (tentative date: Oct. 16)

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- Final 30%

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Prerequisites & CAD Tools

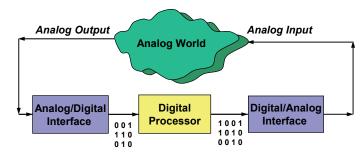
- Prerequisites
 - Basic course in signal processing (Laplace and ztransform, discrete Fourier transform) i.e. EE120
 - Fundamental circuit concepts i.e. EE105 and EE140
- CAD Tools:
 - Hspice or Spectre
 - Matlab

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Analog-Digital Interface Circuitry



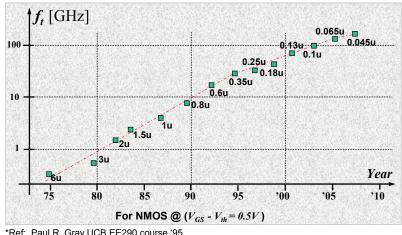
- Naturally occurring signals are analog
- To process signals in the digital domain
 - :. Need Analog/Digital & Digital/Analog interface circuitry

Question: Why not perform the signal processing in the analog domain only & thus eliminate need for A/D & D/A?

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*Ref: Paul R. Gray UCB EE290 course '95
International Technology Roadmap for Semiconductors,

http://public.itrs.net

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CMOS Device Evolution Progression from 1975 to 2005

Minimum feature sizes ~X1/100

• Cut-off frequency f_t ~X300

• Minimum size device area ~1/L²

Number of interconnect layers ~X8

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Impact of CMOS Scaling on Digital Signal Processing

Direct beneficiary of VLSI technology down scaling

- Digital circuits deal with "0" & "1" signal levels only
 - → Not sensitive to "analog" noise
- Si Area/function reduced drastically due to
 - · Shrinking of feature sizes
 - Multi metal levels for interconnections (currently >8 metal level v.s. only 1 in the 1970s)
- Enhanced functionality & flexibility
- Amenable to automated design & test
- "Arbitrary" precision
- Provides inexpensive storage capability

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Analog Signal Processing Characteristics

- · Sensitive to "analog" noise
- Has not fully benefited from technology down scaling:
 - Supply voltages scale down accordingly
 - → Reduced voltage swings → more challenging analog design
 - Reduced voltage swings requires lowering of the circuit noise to keep a constant dynamic range
 - → Higher power dissipation and chip area
- Not amenable to automated design
- Extra precision comes at a high price
- Rapid progress in DSP has imposed higher demands on analog/digital interface circuitry
 - →Plenty of room for innovations!

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Cost/Function Comparison DSP & Analog

- Digital circuitry: Fully benefited from CMOS device scaling
 - Cost/function decreases by ~29% each year
 Cost/function X1/30 in 10 years*
- Analog circuitry: Not fully benefited from CMOS scaling
 - Device scaling mandates drop in supply voltages > threaten analog feasibility
 - Cost/function for analog ckt almost constant or increase
- Rapid shift of function implementation from processing in analog domain to digital & hence increased need for A/D & D/A interface circuitry

*Ref: International Technology Roadmap for Semiconductors,

http://public.itrs.ne

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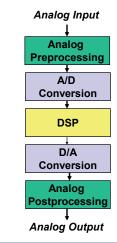
Digitally Assisted Analog Circuitry

- Analog design has indeed benefited from the availability of inexpensive onchip digital capabilities
- Examples:
 - Compensating/calibrating ADC & DAC inaccuracies
 - Automatic frequency tuning of filters & VCOs
 - DC offset compensation

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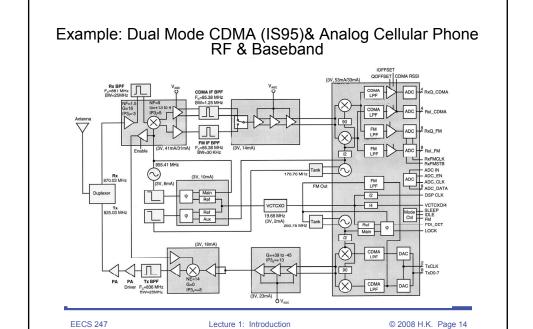
Analog Digital Interface Circuitry Example: Digital Audio

- Goal-Lossless archival and transmission of audio signals
- Circuit functions:
 - Preprocessing
 - Amplification
 - Anti-alias filtering
 - A/D Conversion
 - Resolution→16Bits
 - DSP
 - Storage
 - Processing (e.g. recognition)
 - D/A Conversion
 - Postprocessing
 - Smoothing filter
 - Variable gain amplification



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Example: Typical Dual Mode Cell Phone

Contains in integrated form the following interface circuitry:

- · 4 RX filters
- · 3 or 4 TX filters
- 4 RX ADCs
- 2 TX DACs
- 3 Auxiliary ADCs
- 8 Auxiliary DACs

Dual Standard, I/Q

Audio, Tx/Rx power control, Battery charge control, display, ...



Total: Filters → 8

ADCs → 7

DACs → 12

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Areas Utilizing Analog/Digital Interface Circuitry

Communications

- Wireline communications
 - Telephone related (DSL, ISDN, CODEC)
 - Television circuitry (Cable modems, TV tuners...)
 - Ethernet (Gigabit, 10/100BaseT...)

Wireless

- Cellular telephone (CDMA, Analog, GSM....)
- Wireless LAN (Blue tooth, 802.11a/b/g....)
- Radio (analog & digital), Television
- · Personal Data Assistants

Computing & Control

- Storage media (disk drives, digital tape)
- Imagers & displays



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Areas Utilizing Analog/Digital Interface Circuitry

Instrumentation

- Electronic test equipment & manufacturing environment ATEs
- environment ATEsSemiconductor test equipment
- Physical sensors & actuators
- Medical equipment

Consumer Electronics

- Audio (CD, DAT, MP3)
- Automotive control, appliances, toys







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UCB Graduate Level Analog Courses EECS 247 - 240 - 242

• EECS 240

- Transistor level, building blocks such as opamps, buffers, comparator....
- Device and circuit fundamentals
- CAD Tools → SPICE

• EECS 247

- Filters, ADCs, DACs, some system level
- Signal processing fundamentals
- Macro-models, large systems, some transistor level, constraints such as finite gain, supply voltage, noise, dynamic range considered
- CAD Tools → Matlab, SPICE

• EECS 242

- RF amplification, mixing
- Oscillators
- Exotic technology devices
- Nonlinear circuits

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Material Covered in EE247

- Filters
 - Continuous-time filters
 - · Biquads & ladder type filters
 - Opamp-RC, Opamp-MOSFET-C, gm-C filters
 - · Automatic frequency tuning techniques
 - Switched capacitor (SC) filters
- Data Converters
 - D/A converter architectures
 - A/D converter
 - · Nyquist rate ADC- Flash, Pipeline ADCs,....
 - · Oversampled converters
 - · Self-calibration techniques
- · Systems utilizing analog/digital interfaces
 - Wireline communication systems- ISDN, XDSL...
 - Wireless communication systems- Wireless LAN, Cellular telephone,...
 - Disk drive electronics
 - Fiber-optics systems

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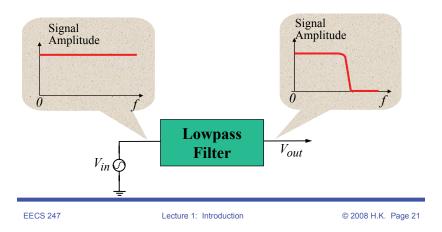
Books (on reserve @ Eng. Library) (NOT required to be purchased),

- Filters
 - A. Williams and F. Taylor, Electronic Filter Design Handbook, 3rd edition, McGraw-Hill, 1995.
 - W. Heinlein & W. Holmes, "Active Filters for Integrated Circuits", Prentice Hall Int., Inc. Chap. 8, 1974. Good reference for signal flowgraph techniques
 - A. Zverev, Handbook of Filter Synthesis, Wiley, 1967.
 A classic; focus is on passive ladder filters. Tables for implementing ladder filters (replaces a CAD tool).
- · Data Converters
 - R. van de Plassche, Integrated Analog-to-Digital and Digital-to-Analog Converters, 2nd edition, Kluwer, 2003.
 - B. Razavi, Data Conversion System Design, IEEE Press, 1995.
 - S. Norsworthy et al (eds), *Delta-Sigma Data Converters*, IEEE Press, 1997.
- General
 - Gray, Hurst, Lewis, Meyer, Analysis & Design of Analog Integrated Circuits, Wiley 2001.
 - Johns, Martin, Analog Integrated Circuit Design, Wiley 1997.
- Note: a list of relevant IEEE publications is posted on the course website. Some will be noted as mandatory reading and the rest optional

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Filtering → Provide frequency selectivity and/or phase shaping
 Oldest & most common type of signal processing



Introduction to Filters

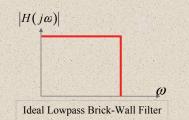
- Typical filter applications:
 - Extraction of desired signal from many (radio, TV, cell phone, ADSL.....)
 - Separating signal and noise
 - Anti-aliasing
 - Phase equalization
 - Amplifier bandwidth limitations

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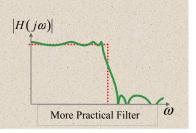
Ideal versus Practical Filters Example: Lowpass Filter

- · Ideal filter
 - Brick-wall characteristics
 - Flat magnitude response in the passband
 - Infinite level of rejection of out-of-band signals



· Practical filter

- Ripple in passband magnitude response
- Limited rejection of out-ofband signals



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Simplest Filter First-Order Lowpass RC Filter (LPF1)



Steady-state frequency response:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1 + \frac{s}{\omega_o}}$$

$$with \qquad \omega_o = \frac{1}{RC} = 2\pi \times 100kHz$$
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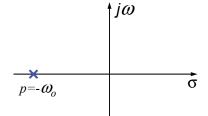
S-Plane Poles and Zeros

$$H(s) = \frac{1}{1 + \frac{s}{\omega_o}}$$

Zero: $z \rightarrow \infty$

$$|H(s)| = \left| \frac{1}{1 + j \frac{\omega}{\omega_o}} \right| = \frac{1}{\sqrt{1 + \frac{\omega^2}{\omega_o^2}}}$$

s-plane (pzmap):



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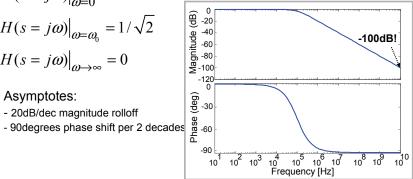
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Filter Frequency Response Bode Plot

$$|H(s=j\omega)|_{\omega=0}=1$$

$$\begin{aligned} & \left| H(s = j\omega) \right|_{\omega = 0} = 1 \\ & \left| H(s = j\omega) \right|_{\omega = \omega_0} = 1/\sqrt{2} \\ & \left| H(s = j\omega) \right|_{\omega \to \infty} = 0 \end{aligned}$$

$$|H(s=j\omega)|_{\omega\to\infty}=0$$



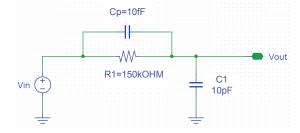
Question:

can we really get 100dB attenuation at 10GHz?

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First-Order Low-Pass RC Filter Including Parasitics (LPF2)



$$H(s) = \frac{1 + sRC_P}{1 + sR(C + C_P)}$$

Pole:
$$p = -\frac{1}{R(C + C_p)} \approx -\frac{1}{RC}$$

Zero:
$$z = -\frac{1}{RC_P}$$

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Filter Frequency Response

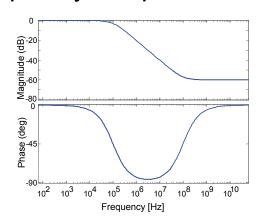
$$|H(j\omega)|_{\omega=0} = 1$$

$$|H(j\omega)|_{\omega\to\infty} = \frac{C_P}{C + C_P}$$

$$\approx \frac{C_P}{C}$$

$$= 10^{-3}$$

$$= -60dB$$



• Beware of important parasitics & include them in the model ...

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Dynamic Range & Electronic Noise

- Dynamic range is defined as the ratio of maximum possible signal handled by a circuit and the minimum useful signal
 - Maximum signal handling capability usually determined by maximum possible voltage swings which in turn is a function of supply voltage & circuit non-linearity
 - Minimum signal handling capability is normally determined by electronic noise
 - · Amplifier noise due to device thermal and flicker noise
 - · Resistor thermal noise
- Dynamic range in analog ckts has direct implications for power dissipation

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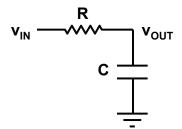
Analog Dynamic Range Example: First Order Lowpass Filter

- Once the poles and zeroes of the analog filter transfer function are defined then special attention must be paid to the actual implementation
- Of the infinitely many ways to build a filter with a given transfer function, each of those combinations result in a different level of output noise!
- As an example noise and dynamic range for the 1st order lowpass filter will be derived

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First Order Filter Noise

- Capacitors are noiseless
- Resistors have thermal noise
 - This noise is uniformly distributed in the frequency domain from dc to infinity
 - Frequency-independent noise is called "white noise"



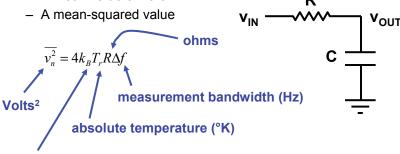
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Resistor Noise

- Resistor noise characteristics
 - A mean value of zero



Boltzmann's constant = 1.38e-23 J/°K

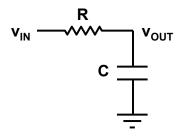
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Resistor Noise

- Theoretically, resistor rms noise voltage in a 10Hz band centered at 1kHz is the same as resistor rms noise in a 10Hz band centered at 1GHz
- Resistor noise spectral density, N₀, is the rms noise per √Hz of bandwidth:

$$N_0 = \sqrt{\frac{\overline{v_n^2}}{\Delta f}} = \sqrt{4k_B T_r R}$$



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Resistor Noise

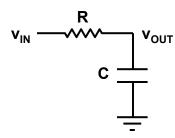
Good numbers to memorize:

- N₀ for a 1kΩ resistor at room temperature is 4nV/√Hz
- Scaling R,
 - A 10MΩ resistor gives 400nV/√Hz
 - A 50Ω resistor gives 0.9nV/√Hz
- · Or, remember

$$k_B T_r = 4x10^{-21} J$$
 $(T_r = 17 \, {}^{\circ}C)$

Or, remember

$$k_B T_r / q = 26 \text{mV}$$
 (q = 1.6x10⁻¹⁹ C)

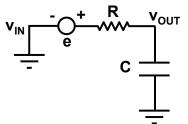


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First Order Filter Noise

- To derive noise @ the output node:
 - Short circuit the input to ground.
 - Resistor noise gives the filter a non-zero output when v_{IN}=0
 - In this simple example, both the input signal and the resistor noise obviously have the same transfer functions to the output
 - Since noise has random phase, we can use any polarity convention for a noise source (but we have to use it consistently)



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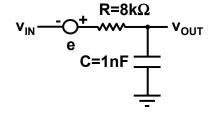
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First Order Filter Noise

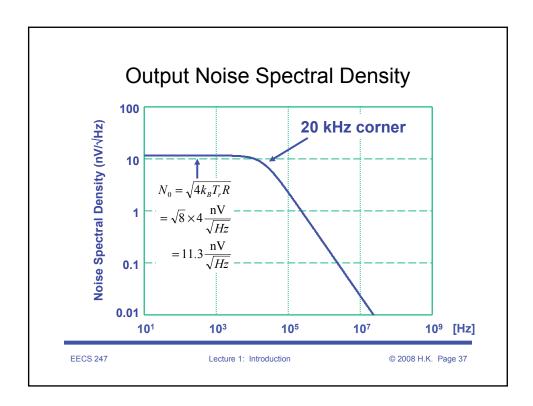
- What is the thermal noise of this RC filter?
- Let's ask SPICE! Netlist:

*Noise from RC LPF vin vin 0 ac 1V r1 vin vout 8kOhm c1 vout 0 1nF .ac dec 100 10Hz 1GHz .noise V(vout) vin .end



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Total Noise

- Total noise is what the display on a volt-meter connected to v_o would show!
- Total noise is found by integrating the noise power spectral density within the frequency band of interest
- Note that noise is integrated in the mean-squared domain, because noise in a bandwidth df around frequency f_l is uncorrelated with noise in a bandwidth df around frequency f_2
 - Powers of uncorrelated random variables add
 - Squared transfer functions appear in the mean-squared integral

$$\overline{v_o^2} = \int_{f_I}^{f_2} \overline{v_n^2} |H(j\omega)|^2 df$$

$$\overline{v_o^2} = \int_{0}^{\infty} 4k_B T R |H(2\pi jf)|^2 df$$

*Ref: "Analysis & Design of Analog Integrated Circuits", Gray, Hurst, Lewis, Meyer- Chapter 11

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Total Noise

$$\overline{v_o^2} = \int_0^\infty 4k_B TR |H(2\pi jf)|^2 df$$

$$= \int_0^\infty 4k_B TR \left| \frac{1}{1 + 2\pi jfRC} \right|^2 df$$

$$\rightarrow \overline{v_o^2} = \frac{k_B T}{C}$$

- This interesting and somewhat counter intuitive result means that even though resistors are the components generating the noise, total noise is determined by noiseless capacitors!
- For a given capacitance, as resistance goes up, the increase in noise density is balanced by a decrease in noise bandwidth

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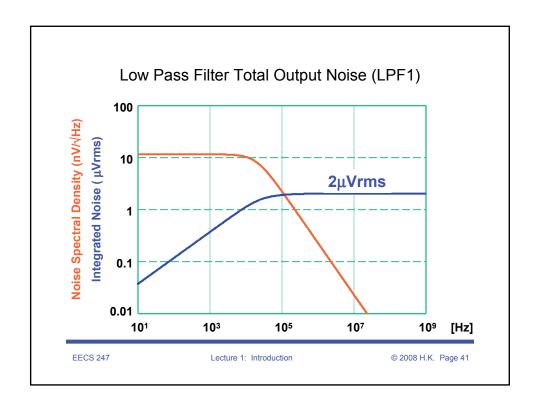
kT/C Noise

- kT/C noise is a fundamental analog circuit limitation
- The rms noise voltage of the simplest possible (first order) filter is $(k_BT/C)^{1/2}$
- For 1pF capacitor, $(k_BT/C)^{1/2} = 64 \mu V$ -rms (at 298°K)
- 1000pF gives 2 μV-rms
- The noise of a more complex & higher order filter is given by: $(\alpha \times k_{_{\rm R}}T/C)^{1/2}$

where α depends on implementation and features such as filter order

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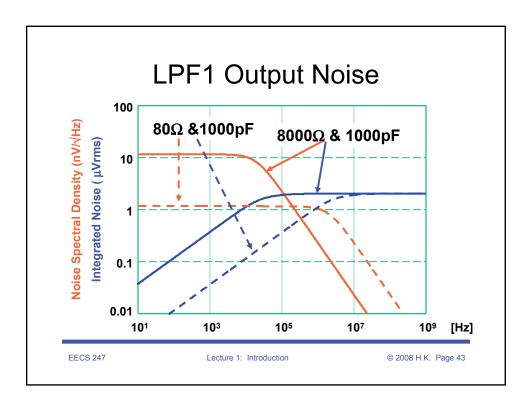


LPF1 Output Noise

- Note that the integrated noise essentially stops growing above 100kHz for this 20kHz lowpass filter
- Beware of faulty intuition which might tempt you to believe that an 80Ω , 1000pF filter has lower integrated noise compared to our 8000Ω , 1000pF filter...

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Analog Circuit Dynamic Range

- Maximum voltage swing for analog circuits (assuming no inductors are used!) can at most be equal to power supply voltage V_{DD} (normally is smaller) Assuming a sinusoid signal $\rightarrow V_{max}(rms) = \frac{1}{\sqrt{2}} \frac{V_{DD}}{2}$
- Noise for a filter $\rightarrow V_n(rms) = \sqrt{\alpha \frac{k_B T}{C}}$

$$D.R. = \frac{V_{\text{max}}(rms)}{V_n(rms)} = \frac{V_{DD}\sqrt{C}}{\sqrt{8\alpha k_B T}}$$
 [V/V]

→ Dynamic range in dB is:

=
$$20\log_{10}\left(V_{DD}\sqrt{\frac{C}{\alpha}}\right) + 75$$
 [dB] with C in [pF]

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Analog Circuit Dynamic Range

- For integrated circuits built in modern CMOS processes, VDD < 1.5V and C < 100pF
 - **D.R.** < **98 dB** (assuming $\alpha = 1$)
- For PC board circuits built with "old-fashioned" 30V opamps and discrete capacitors of < 100nF
 - -D.R. < 140dB
 - A 42dB advantage!

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Dynamic Range versus Number of Bits

Number of bits and dB are related:

$$D.R. = (1.76 + 6.02N)$$
 [dB]

 $N \rightarrow$ number of bits

- see "quantization noise", later in the course
- Hence

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Dynamic Range versus Power Dissipation

- Each extra bit corresponds to 6dB extra dynamic range
- Increasing dynamic range by one bit → 6dB less noise → decrease in noise power by 4x!
- This translates into 4x larger capacitors
- To keep speed constant (speed prop G_m/C): G_m must increase 4x
- Power dissipation is proportional to G_m (for fixed supply and V_{dsat})

In analog circuits with performance limited by thermal noise,

1 extra bit costs 4x power dissipation

E.g. 16Bit ADC at 200mW → 17Bit ADC at 800mW

Do not overdesign the dynamic range of analog circuits!

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Noise & Dynamic Range Summary

- Thermal noise is a fundamental property of (electronic) circuits
- In filters, noise is closely related to
 - Capacitor size
- In higher order filters, noise is a function of C, filter order, Q, and depends on implementation
- Operational amplifiers used in active filters can contribute significant levels of extra noise to overall filter noise
- Reducing noise in most analog circuits is costly in terms of power dissipation and chip area

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