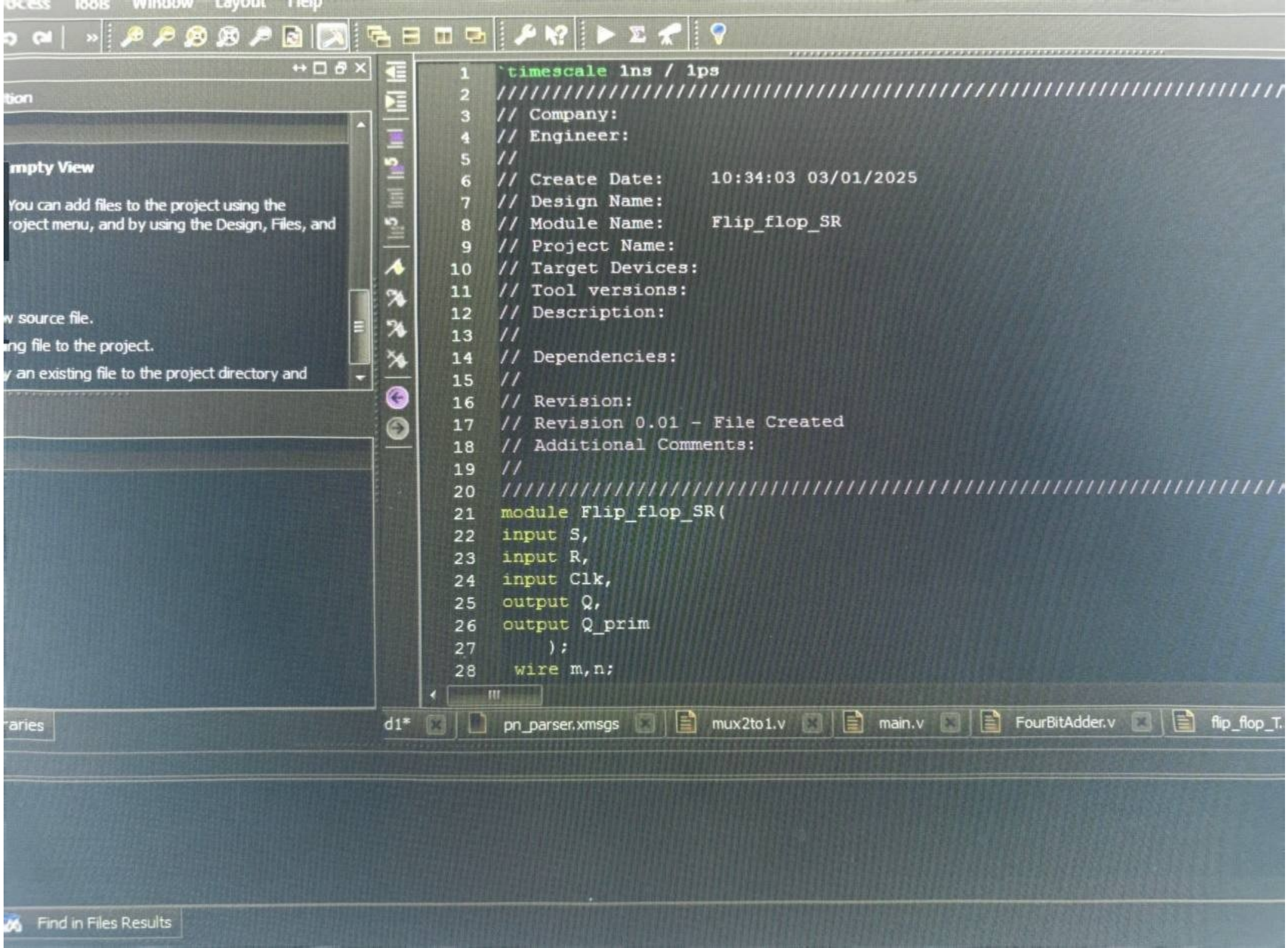
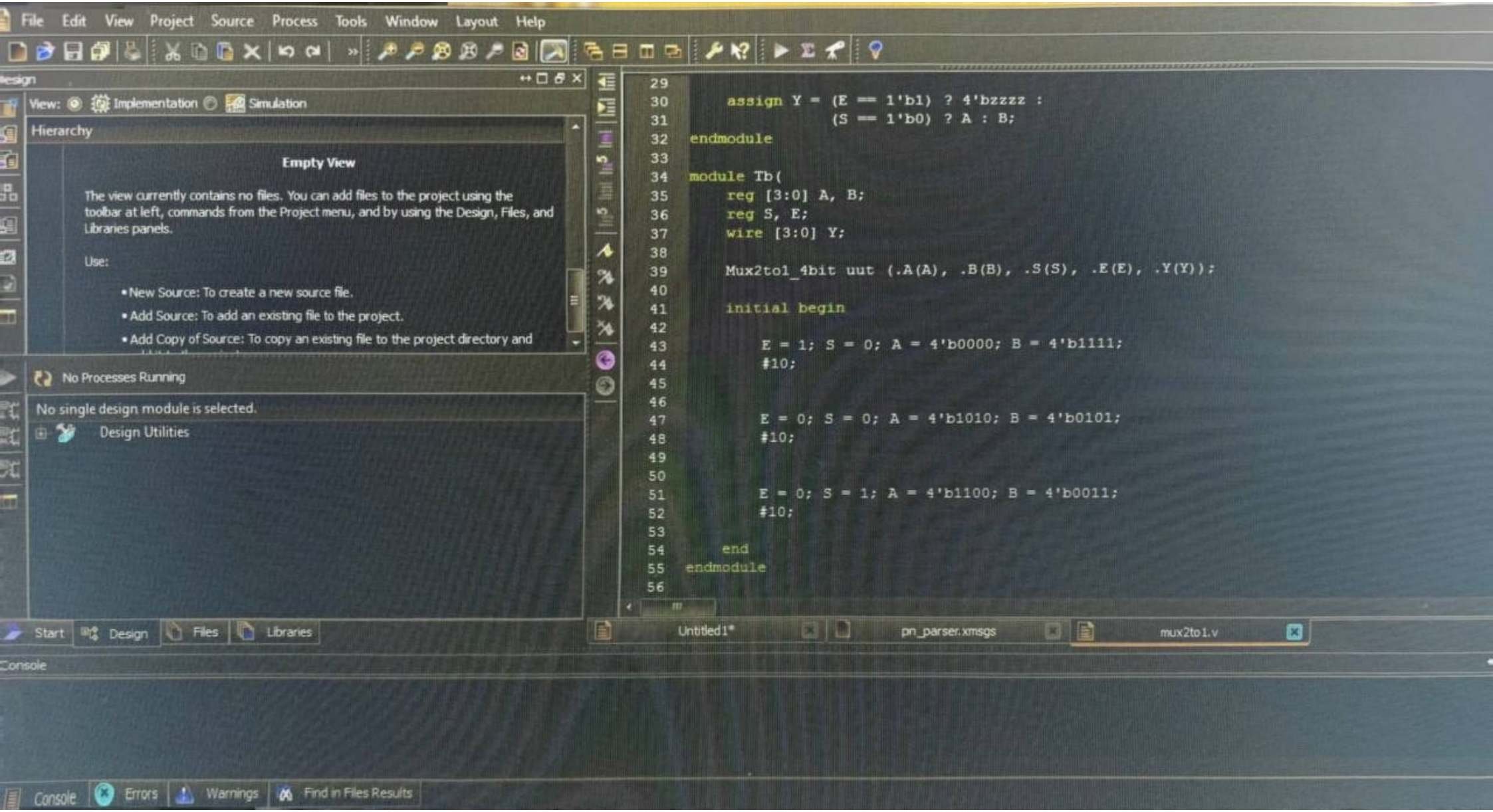
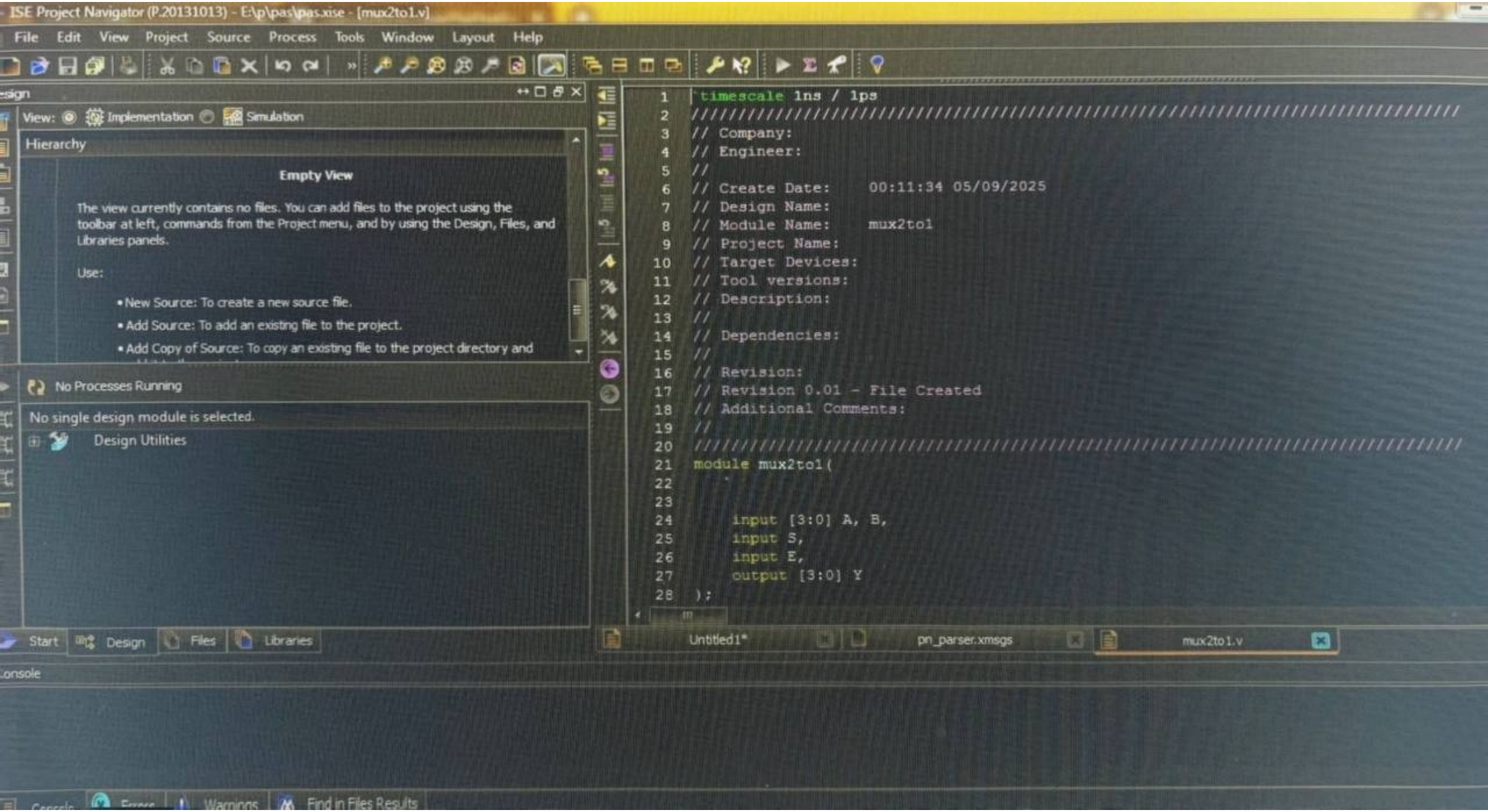
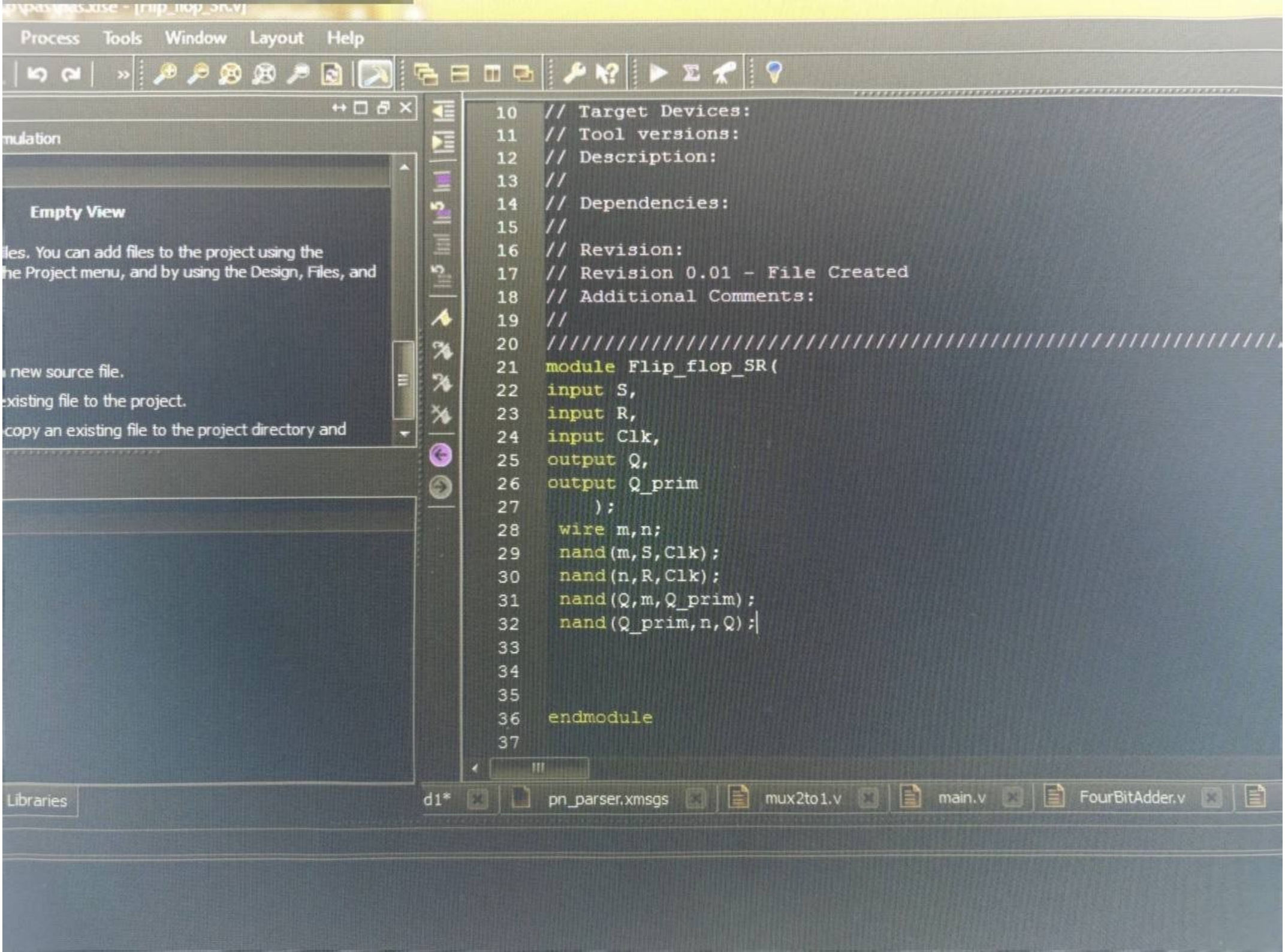
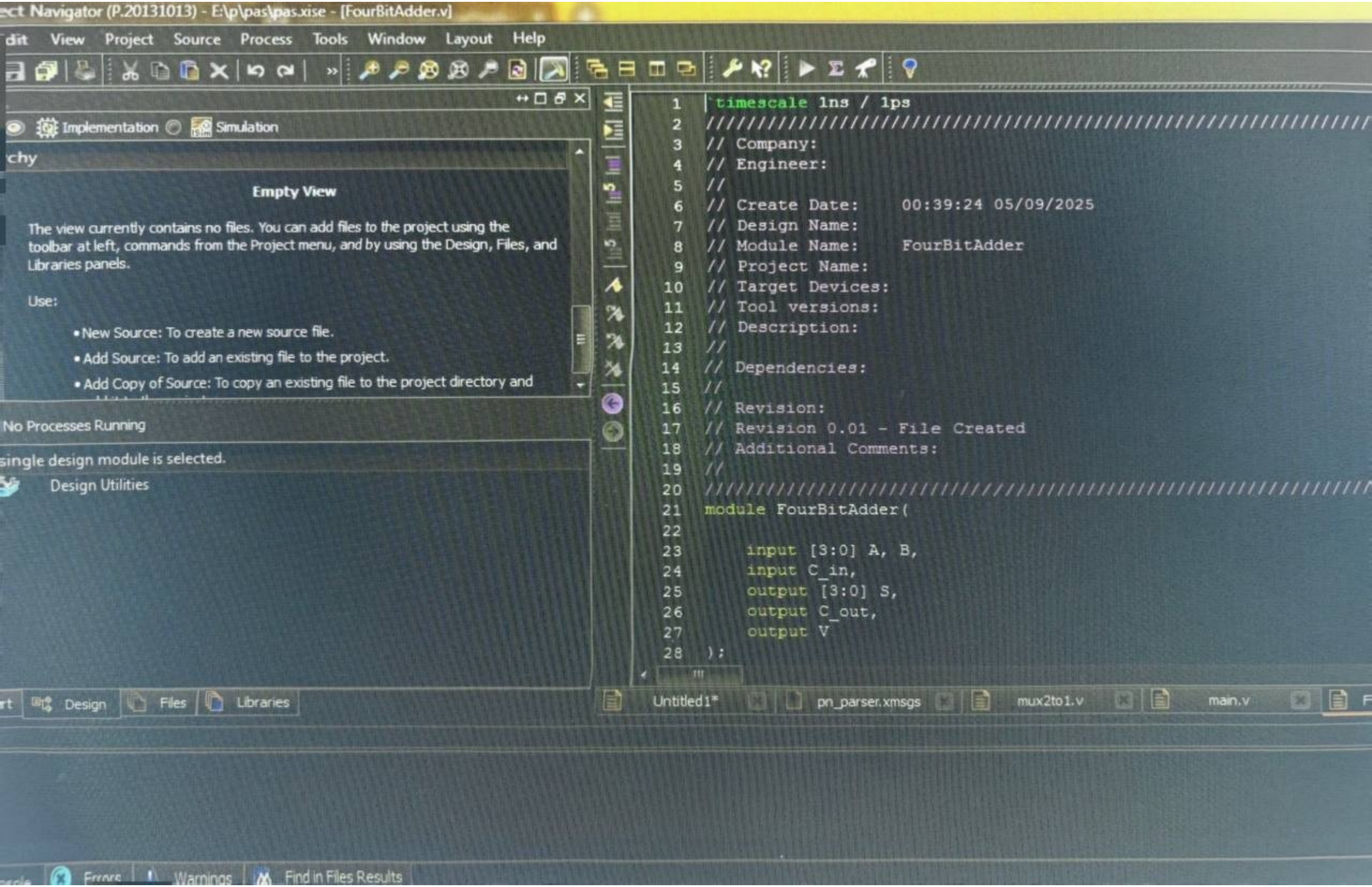
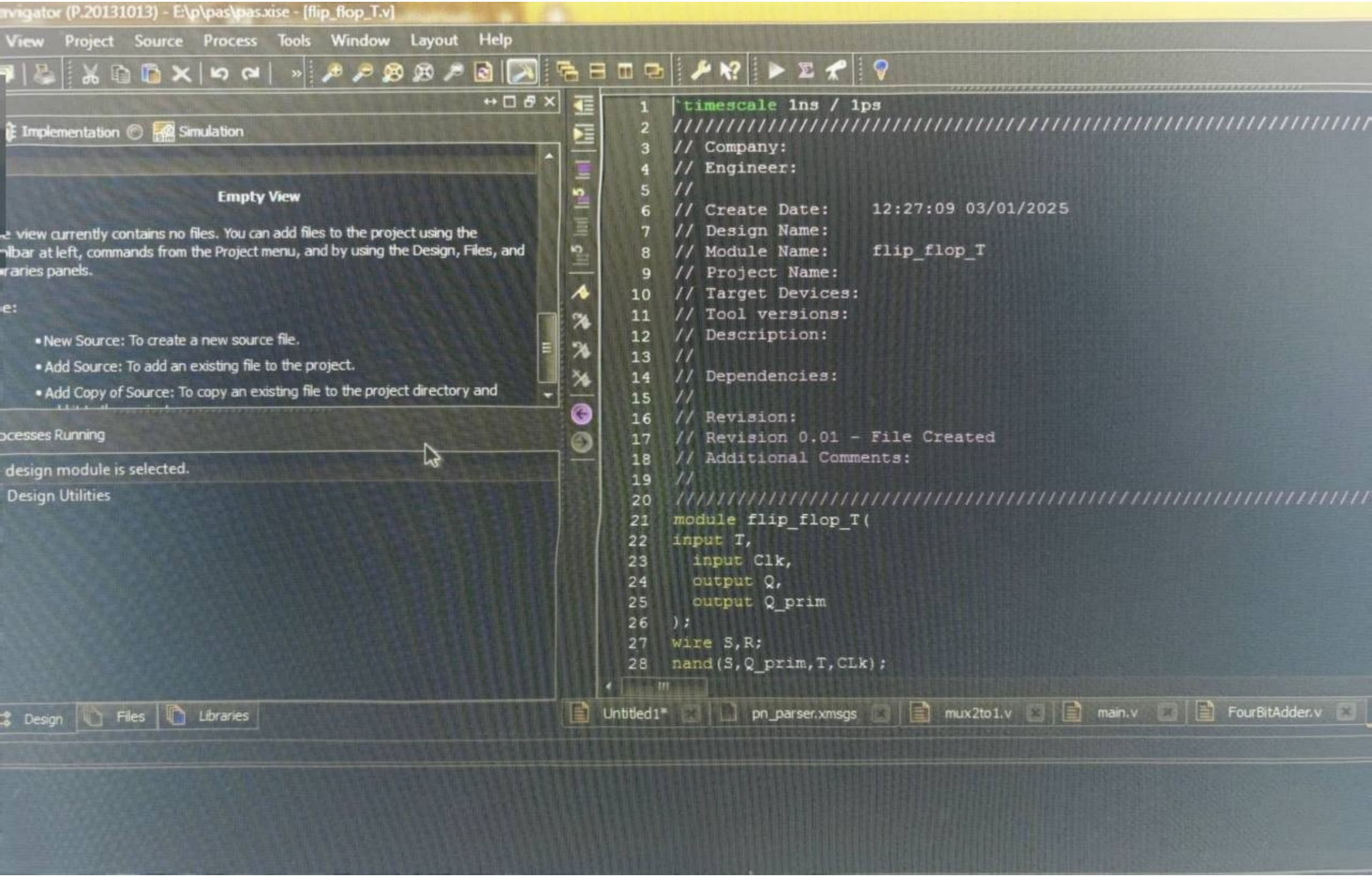

mpty View
You can add files to the project using the
oject menu, and by using the Design, Files, and
w source file.
ng file to the project.
an existing file to the project directory and
`timescale 1ns / 1ps
//
// Company:
// Engineer:
//
// Create Date: 10:34:03 03/01/2025
// Design Name:
// Module Name: Flip_flop_SR
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module Flip_flop_SR(
input S,
input R,
input Clk,
output Q,
output Q_prim
);
wire m,n;
d1*
pn_parser.xmsgs
mux2to1.v
main.v
FourBitAdder.v
flip_flop_T.
Find in Files Results

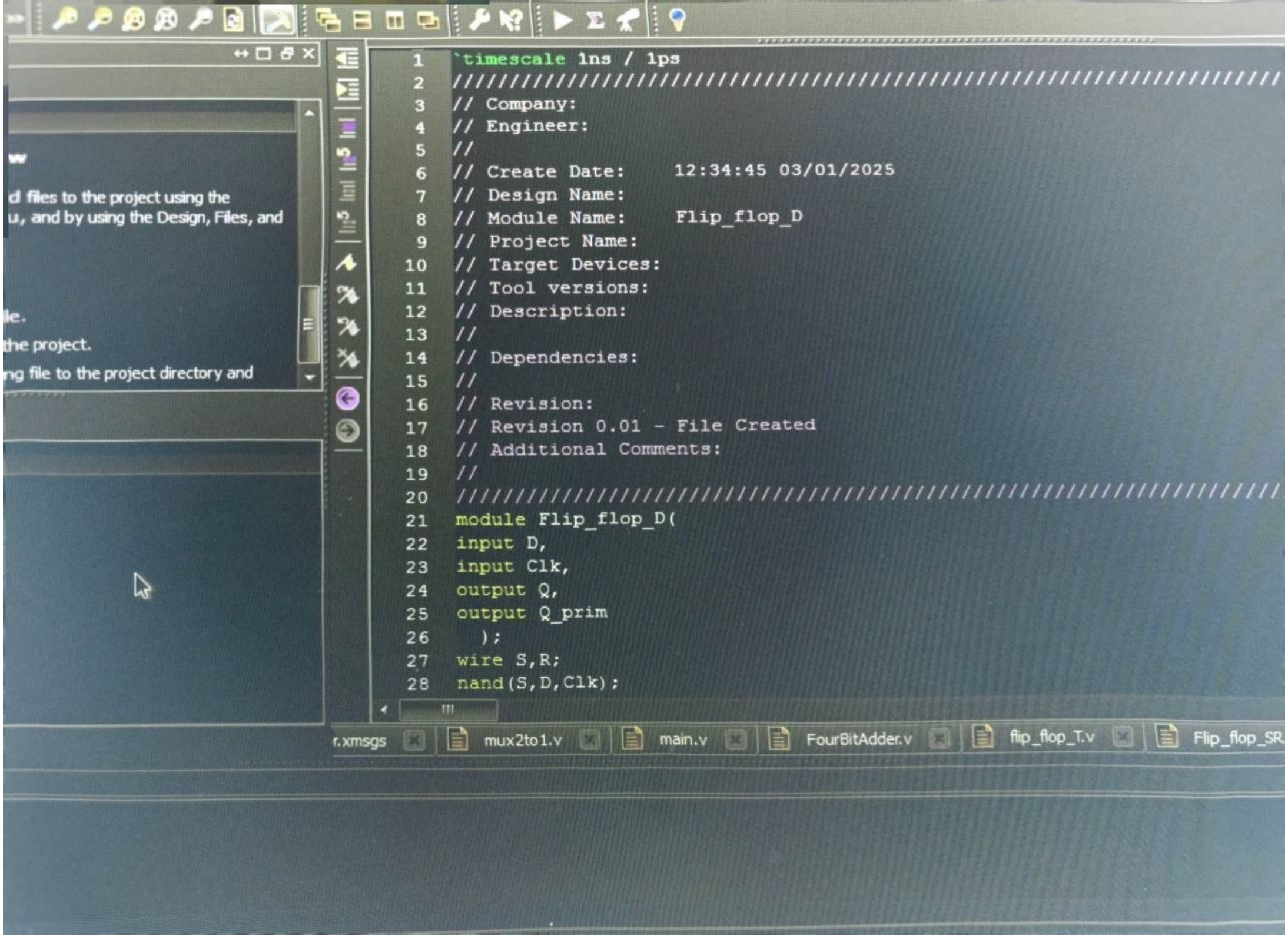

File Edit View Project Source Process Tools Window Layout Help
View: Implementation Simulation
Hierarchy
Empty View
The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.
Use:
• New Source: To create a new source file.
• Add Source: To add an existing file to the project.
• Add Copy of Source: To copy an existing file to the project directory and
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
29
30 assign Y = (E == 1'b1) ? 4'bzzzz :
31 (S == 1'b0) ? A : B;
32 endmodule
33
34 module Tb(
35 reg [3:0] A, B;
36 reg S, E;
37 wire [3:0] Y;
38
39 Mux2to1_4bit uut (.A(A), .B(B), .S(S), .E(E), .Y(Y));
40
41 initial begin
42
43 E = 1; S = 0; A = 4'b0000; B = 4'b1111;
44 #10;
45
46
47 E = 0; S = 0; A = 4'b1010; B = 4'b0101;
48 #10;
49
50
51 E = 0; S = 1; A = 4'b1100; B = 4'b0011;
52 #10;
53
54 end
55 endmodule
56
Untitled1*
pn_parser.xmsgs
mux2to1.v
Console
Console Errors Warnings Find in Files Results

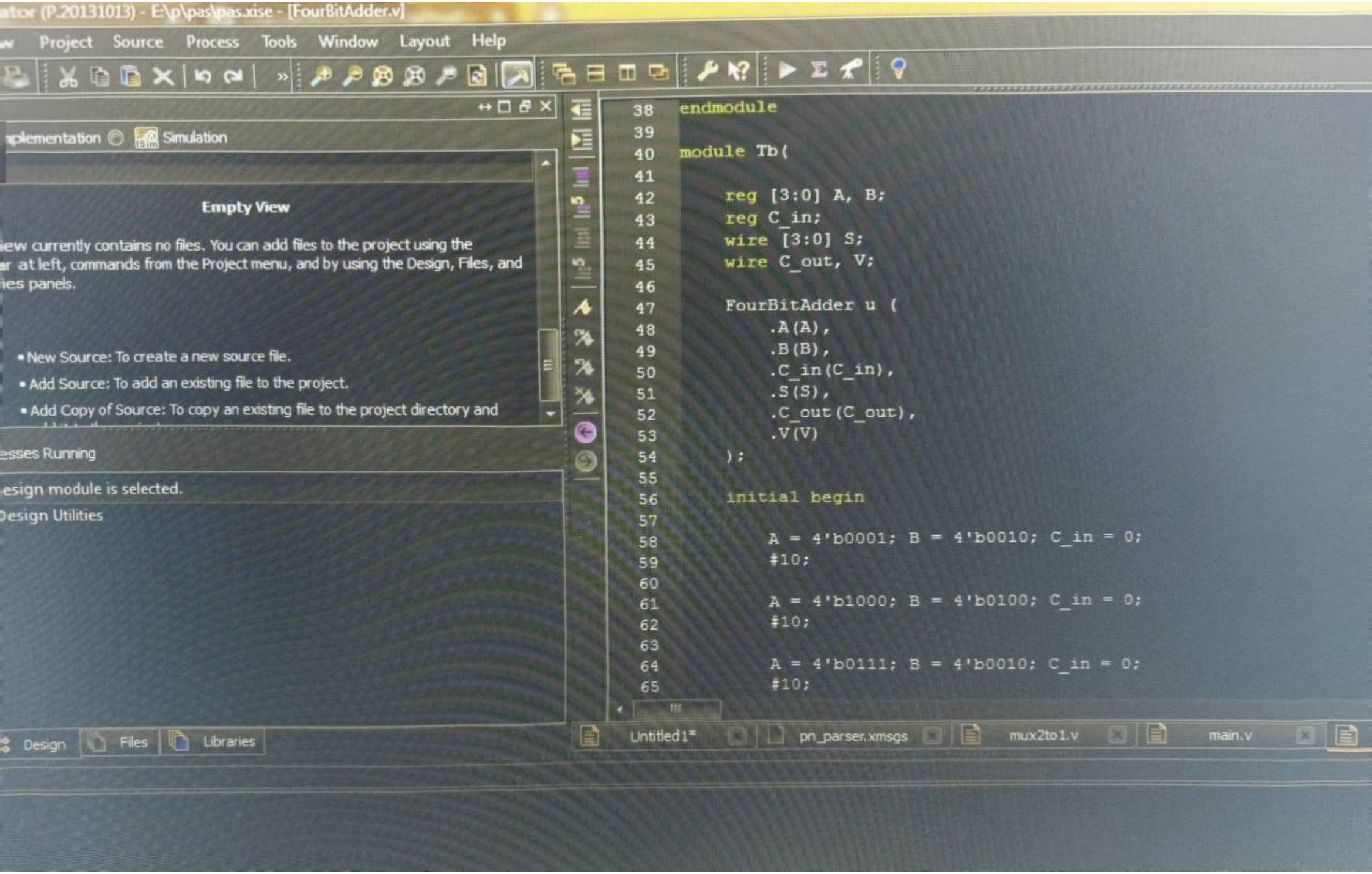

ISE Project Navigator (P.20131013) - E:\p\pas\pas.xise - [mux2to1.v]
File Edit View Project Source Process Tools Window Layout Help
View: Implementation Simulation
Hierarchy
Empty View
The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.
Use:
• New Source: To create a new source file.
• Add Source: To add an existing file to the project.
• Add Copy of Source: To copy an existing file to the project directory and
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
1 `timescale 1ns / 1ps
2 //
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 00:11:34 05/09/2025
7 // Design Name:
8 // Module Name: mux2to1
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module mux2to1(
22
23
24 input [3:0] A, B,
25 input S,
26 input E,
27 output [3:0] Y
28);
Untitled1*
pn_parser.xmsgs
mux2to1.v
Console
Errors
Warnings
Find in Files Results

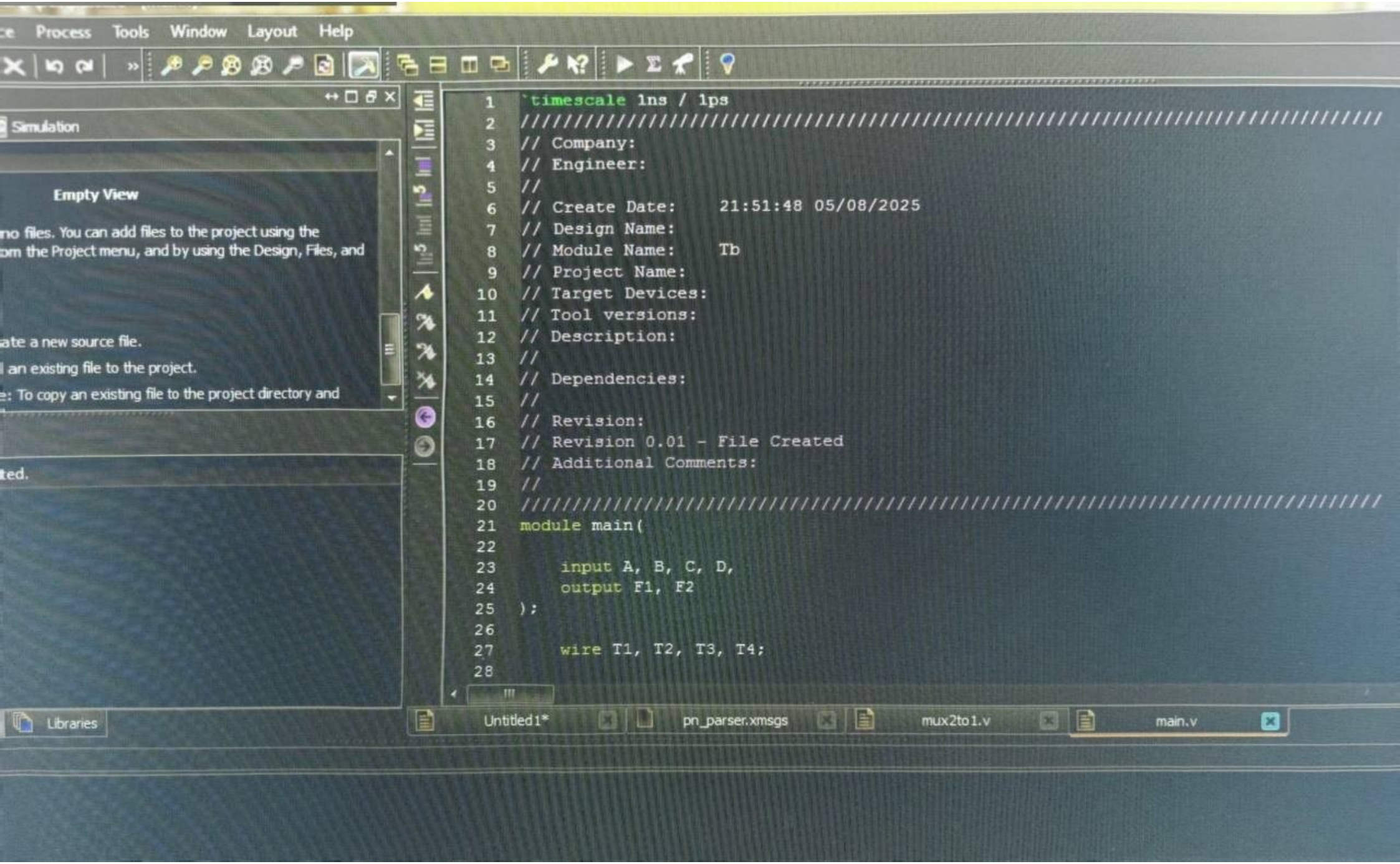

Process Tools Window Layout Help
mulation
Empty View
les. You can add files to the project using the
he Project menu, and by using the Design, Files, and
new source file.
existing file to the project.
copy an existing file to the project directory and
Libraries
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module Flip_flop_SR(
22 input S,
23 input R,
24 input Clk,
25 output Q,
26 output Q_prim
27);
28 wire m,n;
29 nand(m,S,Clk);
30 nand(n,R,Clk);
31 nand(Q,m,Q_prim);
32 nand(Q_prim,n,Q);
33
34
35
36 endmodule
37
d1*
pn_parser.xmsgs
mux2to1.v
main.v
FourBitAdder.v


ect Navigator (P.20131013) - E:\p\pas\pas.xise - [FourBitAdder.v]
dit View Project Source Process Tools Window Layout Help
Implementation
Simulation
chy
Empty View
The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.
Use:
• New Source: To create a new source file.
• Add Source: To add an existing file to the project.
• Add Copy of Source: To copy an existing file to the project directory and
No Processes Running
single design module is selected.
Design Utilities
rt Design Files Libraries
1 `timescale 1ns / 1ps
2 //
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 00:39:24 05/09/2025
7 // Design Name:
8 // Module Name: FourBitAdder
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module FourBitAdder(
22
23 input [3:0] A, B,
24 input C_in,
25 output [3:0] S,
26 output C_out,
27 output V
28);
Untitled1*
pn_parser.xmsgs
mux2to1.v
main.v
Errors
Warnings
Find in Files Results


rvigator (P.20131013) - E:\p\pas\pas.xise - [flip_flop_T.v]
View Project Source Process Tools Window Layout Help
Implementation Simulation
Empty View
e view currently contains no files. You can add files to the project using the
lbar at left, commands from the Project menu, and by using the Design, Files, and
raries panels.
e:
• New Source: To create a new source file.
• Add Source: To add an existing file to the project.
• Add Copy of Source: To copy an existing file to the project directory and
ocesses Running
design module is selected.
Design Utilities
Design Files Libraries
`timescale 1ns / 1ps
//
// Company:
// Engineer:
//
// Create Date: 12:27:09 03/01/2025
// Design Name:
// Module Name: flip_flop_T
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module flip_flop_T(
input T,
input Clk,
output Q,
output Q_prim
);
wire S,R;
nand(S,Q_prim,T,CLk);
Untitled1*
pn_parser.xmsgs
mux2to1.v
main.v
FourBitAdder.v

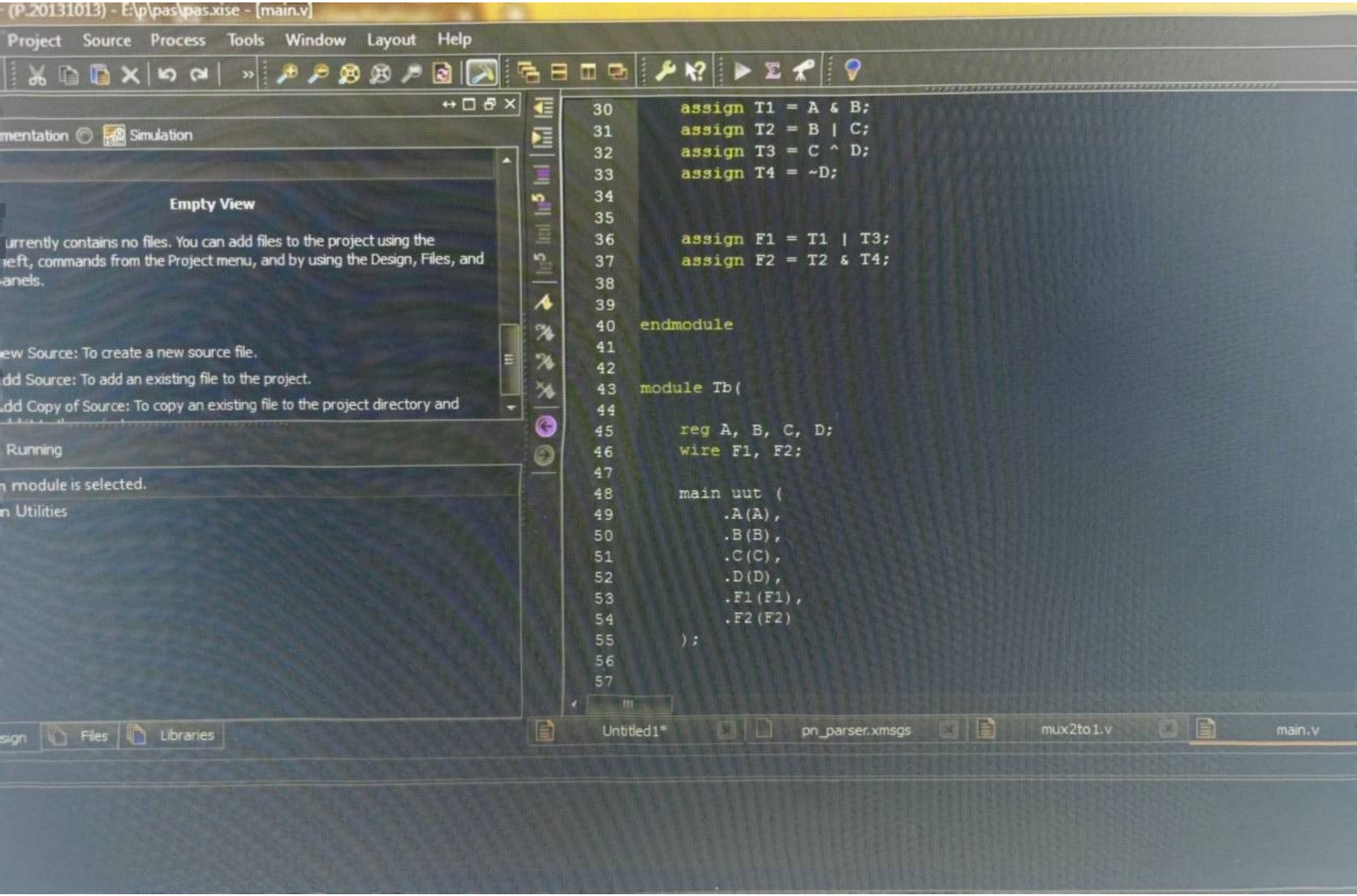

d files to the project using the
u, and by using the Design, Files, and
ie.
the project.
ng file to the project directory and
1 `timescale 1ns / 1ps
2 //
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 12:34:45 03/01/2025
7 // Design Name:
8 // Module Name: Flip_flop_D
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module Flip_flop_D(
22 input D,
23 input Clk,
24 output Q,
25 output Q_prim
26);
27 wire S,R;
28 nand(S,D,Clk);
r.xmsgs
mux2to1.v
main.v
FourBitAdder.v
flip_flop_T.v
Flip_flop_SR


ator (P.20131013) - E:\p\pas\pas.xise - [FourBitAdder.v]
Project Source Process Tools Window Layout Help
plementation Simulation
Empty View
iew currently contains no files. You can add files to the project using the
ar at left, commands from the Project menu, and by using the Design, Files, and
ies panels.
• New Source: To create a new source file.
• Add Source: To add an existing file to the project.
• Add Copy of Source: To copy an existing file to the project directory and
esses Running
esign module is selected.
Design Utilities
Design Files Libraries
38 endmodule
39
40 module Tb(
41
42 reg [3:0] A, B;
43 reg C_in;
44 wire [3:0] S;
45 wire C_out, V;
46
47 FourBitAdder u (
48 .A(A),
49 .B(B),
50 .C_in(C_in),
51 .S(S),
52 .C_out(C_out),
53 .V(V)
54);
55
56 initial begin
57
58 A = 4'b0001; B = 4'b0010; C_in = 0;
59 #10;
60
61 A = 4'b1000; B = 4'b0100; C_in = 0;
62 #10;
63
64 A = 4'b0111; B = 4'b0010; C_in = 0;
65 #10;
Untitled1*
pn_parser.xmsgs
mux2to1.v
main.v


Process Tools Window Layout Help
Simulation
Empty View
no files. You can add files to the project using the
om the Project menu, and by using the Design, Files, and
ate a new source file.
an existing file to the project.
e: To copy an existing file to the project directory and
ted.
Libraries
`timescale 1ns / 1ps
//
// Company:
// Engineer:
//
// Create Date: 21:51:48 05/08/2025
// Design Name:
// Module Name: Tb
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module main(
input A, B, C, D,
output F1, F2
);
wire T1, T2, T3, T4;
Untitled1*
pn_parser.xmsgs
mux2to1.v
main.v

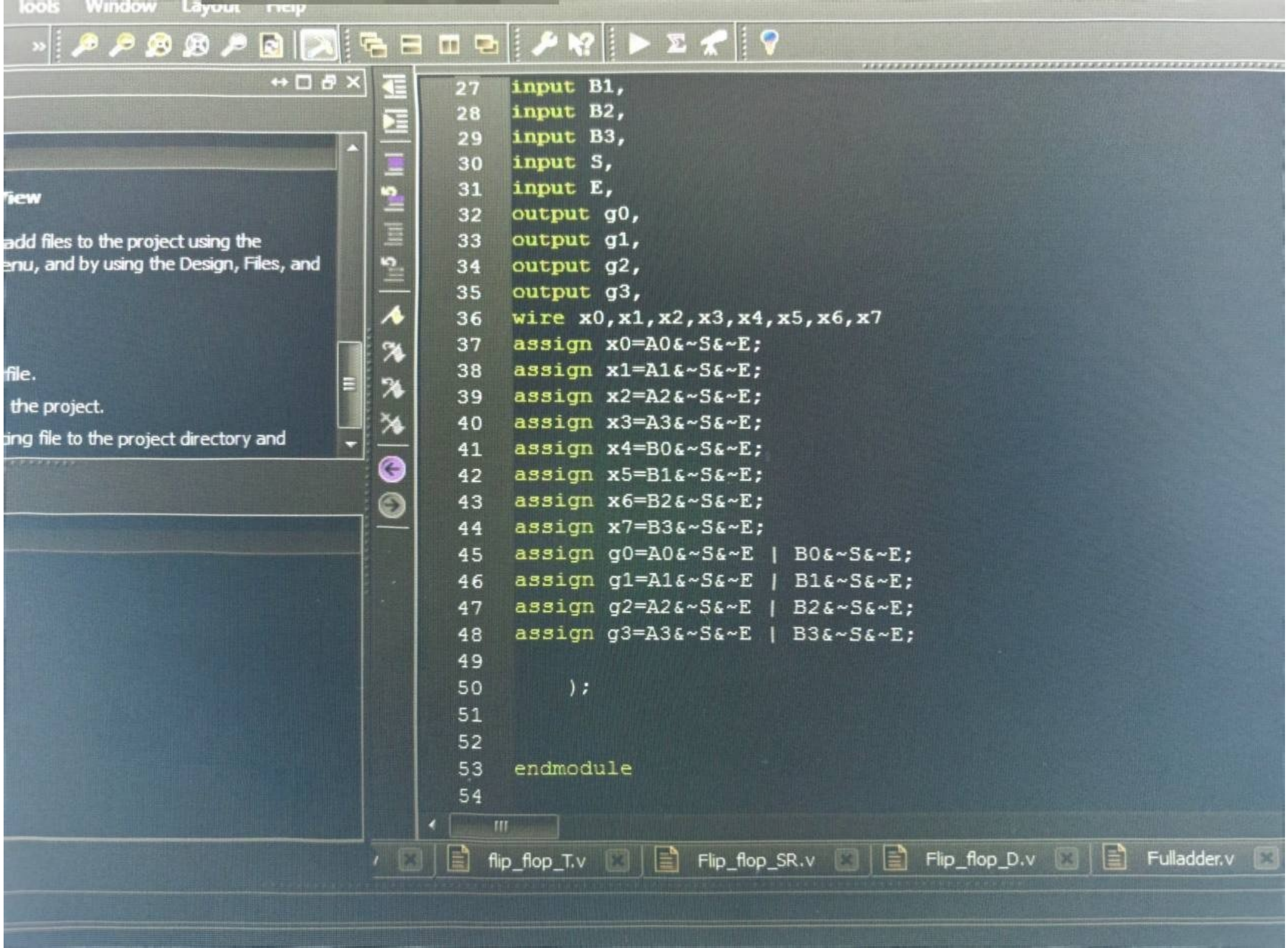
```
36
37  assign g0= A0&~B0;
38  assign g1= B0&~A0;
39  assign g2= A1&~b1;
40  assign g3= B1&~A0;
41  assign g4= A2&~B2;
42  assign g5= B2&~A2;
43  assign g6= A3&~B3;
44  assign g7= B3&~A3;
45  assign x0= A0&~B0|B0&~A0;
46  assign x1= A1&~B1|B1&~A1;
47  assign x2= A2&~B2|B2&~A2;
48  assign x3= A3&~B3|B3&~A3;
49  assign w0= A0&~B0|B0&~A0&A1&~B1|B1&~A1&A2&~B2|B2&~A2&A3&~B3|B3&~A3;
50  assign w1= A0&~B0&A1&~B1|B1&~A1&A2&~B2|B2&~A2&A3&~B3|B3&~A3;
51  assign w2= B0&~A0&A1&~B1|B1&~A1&A2&~B2|B2&~A2&A3&~B3|B3&~A3;
52  assign w3= A1&~b1&A2&~B2|B2&~A2&A3&~B3|B3&~A3;
53  assign w4= B1&~A0&A2&~B2|B2&~A2&A3&~B3|B3&~A3;
54  assign w5= A2&~B2&A3&~B3|B3&~A3;
55  assign w6= B2&~A2&A3&~B3|B3&~A3;
56  assign A_smaller_B= B3&~A3 | B2&~A2&A3&~B3|B3&~A3 | B1&~A0&A2&~B2|B2&~A2&A3&~B3|B3&~A3 |
57  assign A_bigger_B= A3&~B3 | A2&~B2&A3&~B3|B3&~A3 | A1&~b1&A2&~B2|B2&~A2&A3&~B3|B3&~A3 |
58  assign A_equal_B= A0&~B0&A1&~B1|B1&~A1&A2&~B2|B2&~A2&A3&~B3|B3&~A3;
59
60
61  endmodule
62
63
```

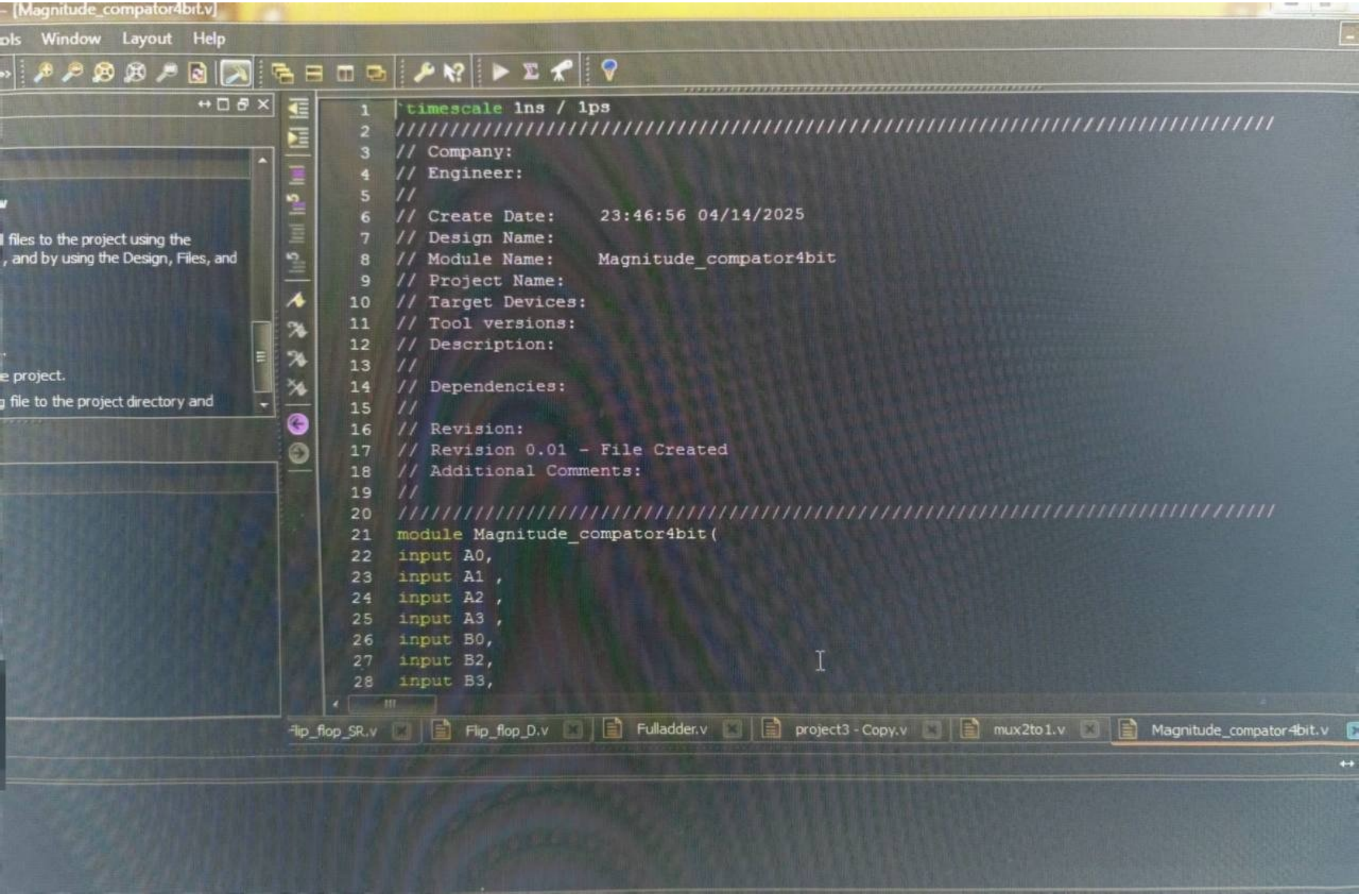
lip_flop_SR.v | Flip_flop_D.v | Fulladder.v | project3 - Copy.v | mux2to1.v | Magnitude_compator4bit.v

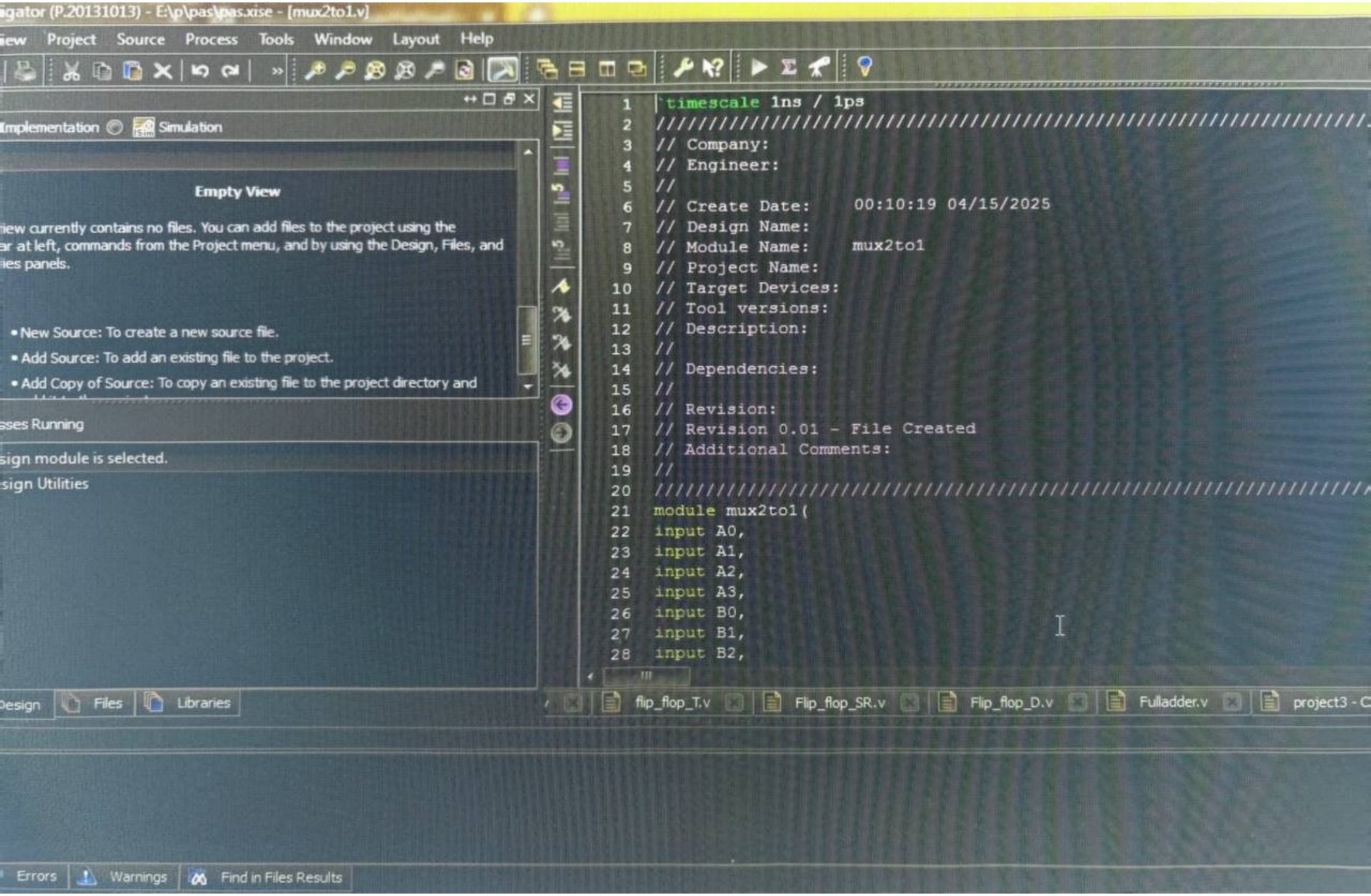

(P.20131013) - E:\p\pas\pas.xise - [main.v]
Project Source Process Tools Window Layout Help
mentation Simulation
Empty View
urrently contains no files. You can add files to the project using the
ieft, commands from the Project menu, and by using the Design, Files, and
anels.
ew Source: To create a new source file.
dd Source: To add an existing file to the project.
dd Copy of Source: To copy an existing file to the project directory and
Running
module is selected.
n Utilities
sign
Files
Libraries
30 assign T1 = A & B;
31 assign T2 = B | C;
32 assign T3 = C ^ D;
33 assign T4 = ~D;
34
35
36 assign F1 = T1 | T3;
37 assign F2 = T2 & T4;
38
39
40 endmodule
41
42
43 module Tb(
44
45 reg A, B, C, D;
46 wire F1, F2;
47
48 main uut (
49 .A(A),
50 .B(B),
51 .C(C),
52 .D(D),
53 .F1(F1),
54 .F2(F2)
55);
56
57
Untitled1*
pn_parser.xmsgs
mux2to1.v
main.v

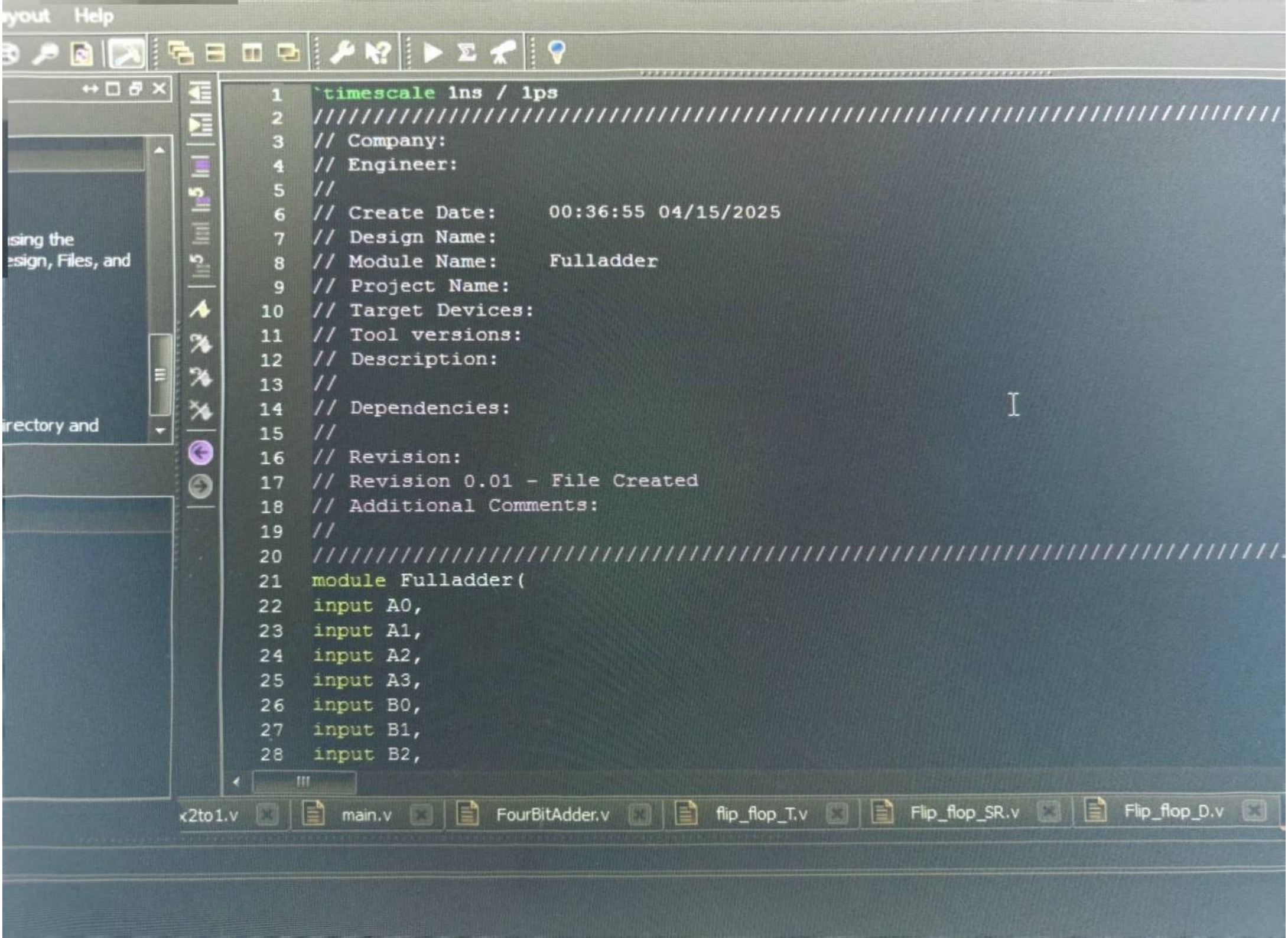
```
23      input B,
24      input C,
25      input D,
26      output F1,
27      output F2
28      );
29    wire T1,T2,T3,T4;
30
31
32      assign T1 = ~B&C;
33      assign T2 = ~A&B;
34      assign T3 =  A|(~B&C);
35      assign T4 = (~A&B)^D;
36      assign f1 = (A|~B&C)|(~A&B^D);
37      assign f2 = (~A^B)|D;
38
39
40  endmodule
41
```

FourBitAdder.v | flip_flop_T.v | Flip_flop_SR.v


Tools Window Layout Help
add files to the project using the
enu, and by using the Design, Files, and
file.
the project.
ing file to the project directory and
27 input B1,
28 input B2,
29 input B3,
30 input S,
31 input E,
32 output g0,
33 output g1,
34 output g2,
35 output g3,
36 wire x0,x1,x2,x3,x4,x5,x6,x7
37 assign x0=A0&~S&~E;
38 assign x1=A1&~S&~E;
39 assign x2=A2&~S&~E;
40 assign x3=A3&~S&~E;
41 assign x4=B0&~S&~E;
42 assign x5=B1&~S&~E;
43 assign x6=B2&~S&~E;
44 assign x7=B3&~S&~E;
45 assign g0=A0&~S&~E | B0&~S&~E;
46 assign g1=A1&~S&~E | B1&~S&~E;
47 assign g2=A2&~S&~E | B2&~S&~E;
48 assign g3=A3&~S&~E | B3&~S&~E;
49
50);
51
52
53 endmodule
54
flip_flop_T.v
Flip_flop_SR.v
Flip_flop_D.v
Fulladder.v


[Magnitude_compator4bit.v]
ols Window Layout Help
l files to the project using the
, and by using the Design, Files, and
e project.
g file to the project directory and
`timescale 1ns / 1ps
//
// Company:
// Engineer:
//
// Create Date: 23:46:56 04/14/2025
// Design Name:
// Module Name: Magnitude_compator4bit
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module Magnitude_compator4bit(
input A0,
input A1 ,
input A2 ,
input A3 ,
input B0,
input B2,
input B3,
lip_flop_SR.v
Flip_flop_D.v
Fulladder.v
project3 - Copy.v
mux2to1.v
Magnitude_compator4bit.v

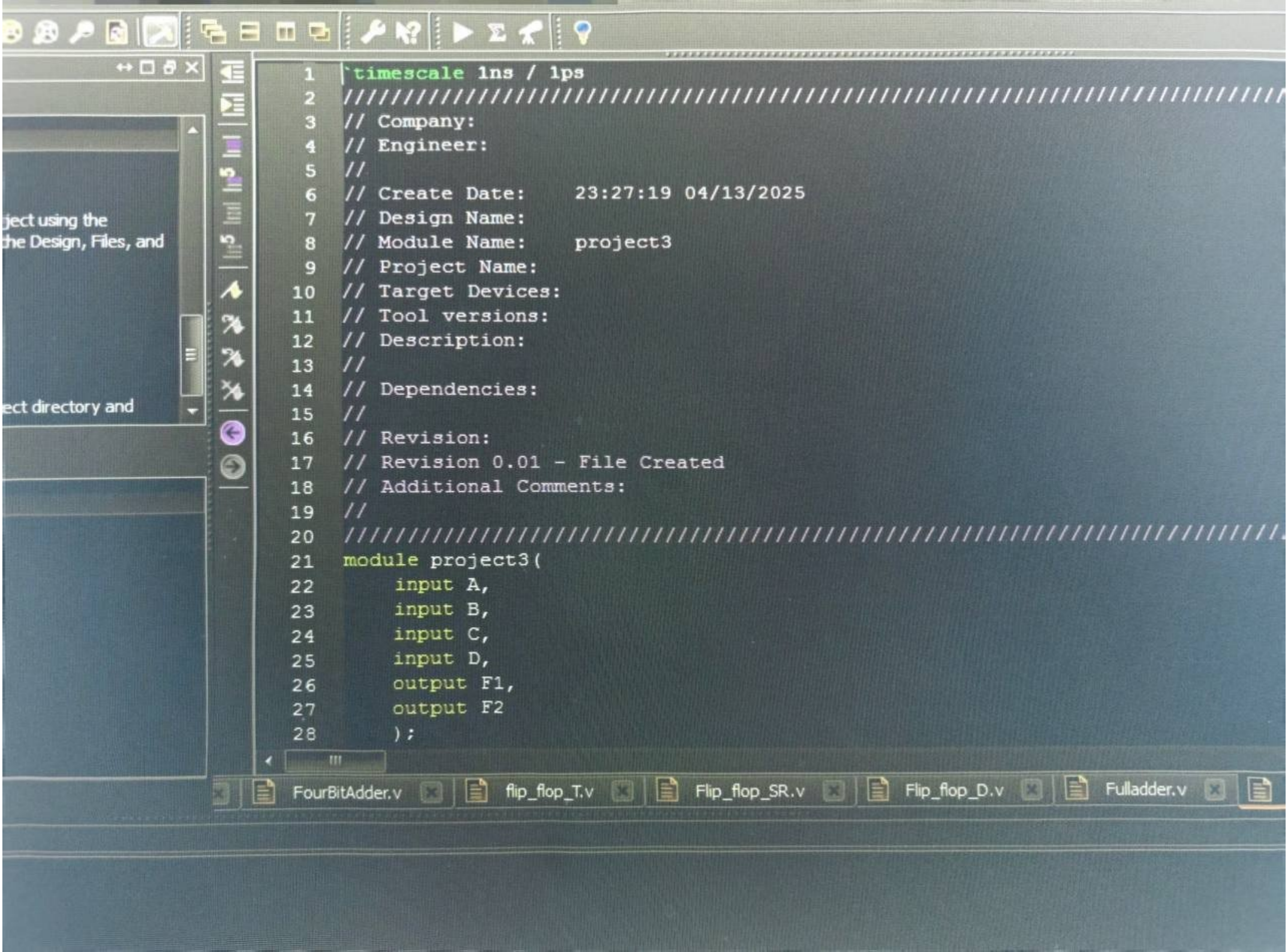

igator (P.20131013) - E:\p\pas\pas.xise - [mux2to1.v]
iew Project Source Process Tools Window Layout Help
Implementation Simulation
Empty View
iew currently contains no files. You can add files to the project using the
er at left, commands from the Project menu, and by using the Design, Files, and
ies panels.
• New Source: To create a new source file.
• Add Source: To add an existing file to the project.
• Add Copy of Source: To copy an existing file to the project directory and
sses Running
sign module is selected.
sign Utilities
Design Files Libraries
1 `timescale 1ns / 1ps
2 //
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 00:10:19 04/15/2025
7 // Design Name:
8 // Module Name: mux2to1
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module mux2to1(
22 input A0,
23 input A1,
24 input A2,
25 input A3,
26 input B0,
27 input B1,
28 input B2,
flip_flop_T.v
Flip_flop_SR.v
Flip_flop_D.v
Fulladder.v
project3 - C
Errors
Warnings
Find in Files Results

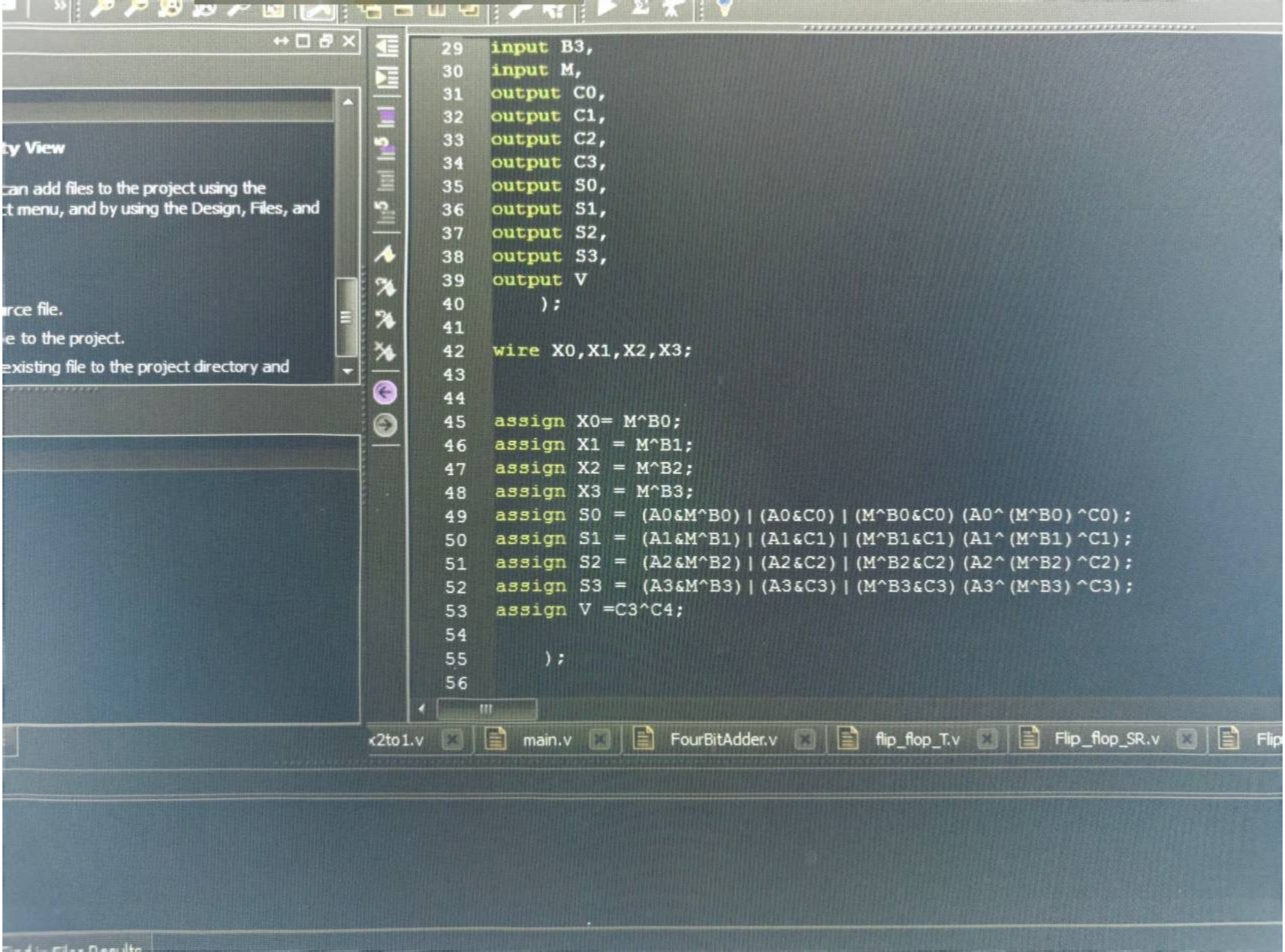

yout Help
sing the
esign, Files, and
irectory and
1 `timescale 1ns / 1ps
2 //
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 00:36:55 04/15/2025
7 // Design Name:
8 // Module Name: Fulladder
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module Fulladder(
22 input A0,
23 input A1,
24 input A2,
25 input A3,
26 input B0,
27 input B1,
28 input B2,
x2to1.v
main.v
FourBitAdder.v
flip_flop_T.v
Flip_flop_SR.v
Flip_flop_D.v

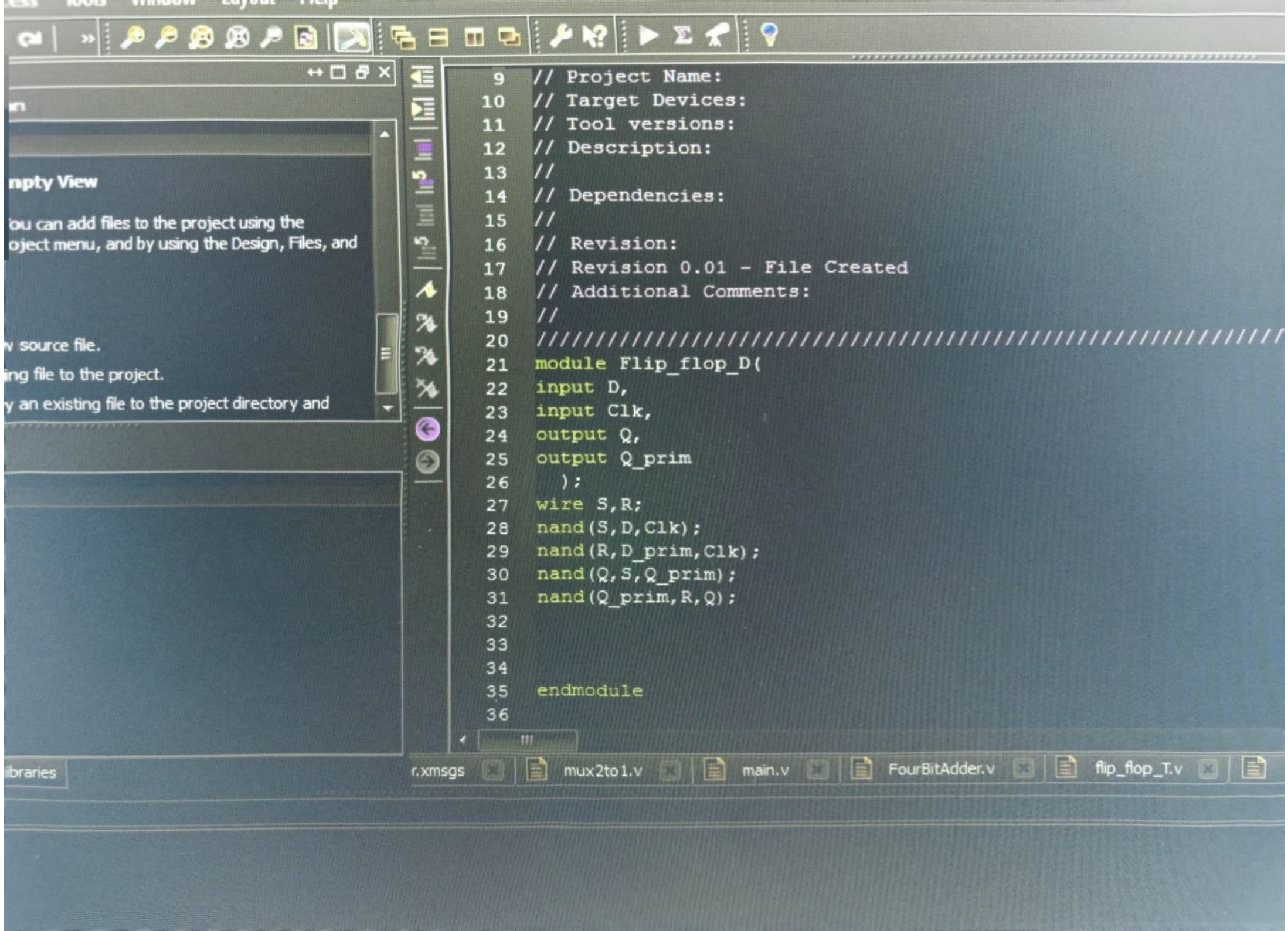
```
;2&~A2&A3&~B3|B3&~A3;
.3&~B3|B3&~A3;
.3&~B3|B3&~A3;


·A3 | B1&~A0&A2&~B2|B2&~A2&A3&~B3|B3&~A3 | B0&~A0&A1&~B1|B1&~A1&A2&~B2|B2&~A2&A3&~B3|B3&~A3
.3 | A1&~b1&A2&~B2|B2&~A2&A3&~B3|B3&~A3 | A0&~B0&A1&~B1|B1&~A1&A2&~B2|B2&~A2&A3&~B3|B3&~A3;
;2&~A2&A3&~B3|B3&~A3;
```

R.v | Flip_flop_D.v | Fulladder.v | project3 - Copy.v | mux2to1.v | Magnitude_compator4bit.v


`timescale 1ns / 1ps
//
// Company:
// Engineer:
//
// Create Date: 23:27:19 04/13/2025
// Design Name:
// Module Name: project3
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module project3(
input A,
input B,
input C,
input D,
output F1,
output F2
);
ject using the
he Design, Files, and
ect directory and
FourBitAdder.v
flip_flop_T.v
Flip_flop_SR.v
Flip_flop_D.v
Fulladder.v


ty View
can add files to the project using the
t menu, and by using the Design, Files, and
rce file.
e to the project.
existing file to the project directory and
input B3,
input M,
output C0,
output C1,
output C2,
output C3,
output S0,
output S1,
output S2,
output S3,
output V
);
wire X0,X1,X2,X3;
assign X0= M^B0;
assign X1 = M^B1;
assign X2 = M^B2;
assign X3 = M^B3;
assign S0 = (A0&M^B0)|(A0&C0)|(M^B0&C0)(A0^(M^B0)^C0);
assign S1 = (A1&M^B1)|(A1&C1)|(M^B1&C1)(A1^(M^B1)^C1);
assign S2 = (A2&M^B2)|(A2&C2)|(M^B2&C2)(A2^(M^B2)^C2);
assign S3 = (A3&M^B3)|(A3&C3)|(M^B3&C3)(A3^(M^B3)^C3);
assign V =C3^C4;
);
x2to1.v
main.v
FourBitAdder.v
flip_flop_T.v
Flip_flop_SR.v


npty View
ou can add files to the project using the
oject menu, and by using the Design, Files, and
v source file.
ing file to the project.
y an existing file to the project directory and
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module Flip_flop_D(
input D,
input Clk,
output Q,
output Q_prim
);
wire S,R;
nand(S,D,Clk);
nand(R,D_prim,Clk);
nand(Q,S,Q_prim);
nand(Q_prim,R,Q);
endmodule
r.xmsgs
mux2to1.v
main.v
FourBitAdder.v
flip_flop_T.v