Frankenserver

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Project Overview

When the world moves between DDR generations (3 to 4, 4 to 5), it presents the question: what happens to the ramsticks of the prior generation? Invariably, they find themselves in recycling plants and landfills. However, recent research has shown that there is a sustainability argument to be made for repurposing older technology for general computation in a server setting[1]. This prior work on reusing older smartphones has shown that you can offset the carbon costs of manufacturing a new device by increasing the time you utilize older hardware. Frankenserver is a project that aims to take a more granular approach to sustainability research and examine the usefulness of repurposing older-generation DDR RAM.

Project Approach

The most straightforward way of repurposing last-generation RAM is to implement conversion logic to connect last-generation memory to a device that expects current-generation memory. Because DDR5 technology is still maturing, this project will focus on the conversion of DDR3 to DDR4 for the sake of prototyping ease. After verifying the conversion logic, this design could then be implemented on an FPGA for real hardware testing.

Additionally, we will also examine the carbon tradeoffs of using DDR3 vs DDR4 in a server setting. In order to do so, we must create or build off of prior work on carbon-intensity metrics. Our examination will help us to determine whether RAM conversion is promising or not. The latter result is still valuable for future research.

Minimum Viable Product (MVP)

- Simulation of RAM translation logic
    - RAM translation logic will be written in Verilog and target Xilinx FPGAs. The design will be simulated using Vivado. Primarily, the goal of the translation logic is to convert DDR4 commands to DDR3 commands. Questions we hope to answer are:
        - Can we sufficiently translate enough commands for seamless integration? (ie, plug-and-play)
        - Is additional DDR3 RAM required in order to compensate for its slower frequency? (Inter-weaved accessing)
        - What will the resulting FPGA requirements be for the logic?

[1] https://dl.acm.org/doi/10.1145/3575693.3575710

- New CCI metrics
    - In order for our granular approach to computational sustainability to work, we must be able to quantify our carbon savings. To achieve this, we will work off of the CCI metrics presented in “Junkyard Computing: Repurposing Discarded Smartphones to Minimize Carbon” and modify it so that we can understand CCI as a function of a computer’s RAM.
    - To enable future work beyond the scope of this class, our carbon analysis work and hardware work will be well documented and presented in a writeup.

Constraints, Risks, and Feasibility

By parallelizing hardware and carbon analysis work, we believe that our MVP should be attainable in less than a month. The greatest risk to the project is discovering that the conversion between DDR3 to DDR4 is impossible or highly impractical. In this event, we will be able to prove, or provide an argument for why the conversion is infeasible. Regardless of the outcome, we will provide information that will be useful for future computational sustainability work.

Group Management

The Frankenserver team consists of two groups: the hardware group and the carbon analysis group. Communication is conducted in a dedicated Slack channel and our team meets weekly. Our team also collaborates with external members, including two graduate students and a faculty member.

Project Development

Alexander Redding is responsible for the hardware group, and both Alexander Yang and Gavin Yuan manage the carbon analysis team.

The hardware team will do its simulation work using Vivado on an AWS EC2 instance. Credits for this have already been provided through Cloudbank. The translation logic will be developed in a publicly accessible GitHub repository.

Project Milestones and Schedule

- Week 3
  - Hardware
    - Create a table comparing DDR3 and DDR4 (commands, electrical characteristics, timing, etc).
    - Setup AWS EC2 instance for development.
  - Carbon Analysis
    - Read “Junkyard Computing: Repurposing Discarded Smartphones to Minimize Carbon” and derive CCI formula as a function of RAM.
- Week 4
  - Both (hardware and carbon analysis)
    - Simulate basic DDR3 read/writes.
  - Hardware
    - Begin writing translation logic.
  - Carbon Analysis
    - Parse and compare different data sources to estimate DDR3 and DDR4 carbon footprint.
- Week 5
  - Hardware
    - Continue writing translation logic.
  - Carbon Analysis
    - Answer power consumption questions:
      - How much more power does DDR3 use over DDR4?
      - Is using larger sticks of RAM more power efficient?
      - Can we directly measure this? (ie, find and order computer that uses both types of RAM)
- Week 6
  - Hardware
    - Have basic translation logic completed.
    - Identify potential target FPGA(s).
  - Carbon Analysis
    - Estimate power consumption of translation logic.
    - If we find a computer that uses both DDR3 and DDR4, have it ordered and determine power consumption difference.