Lab1

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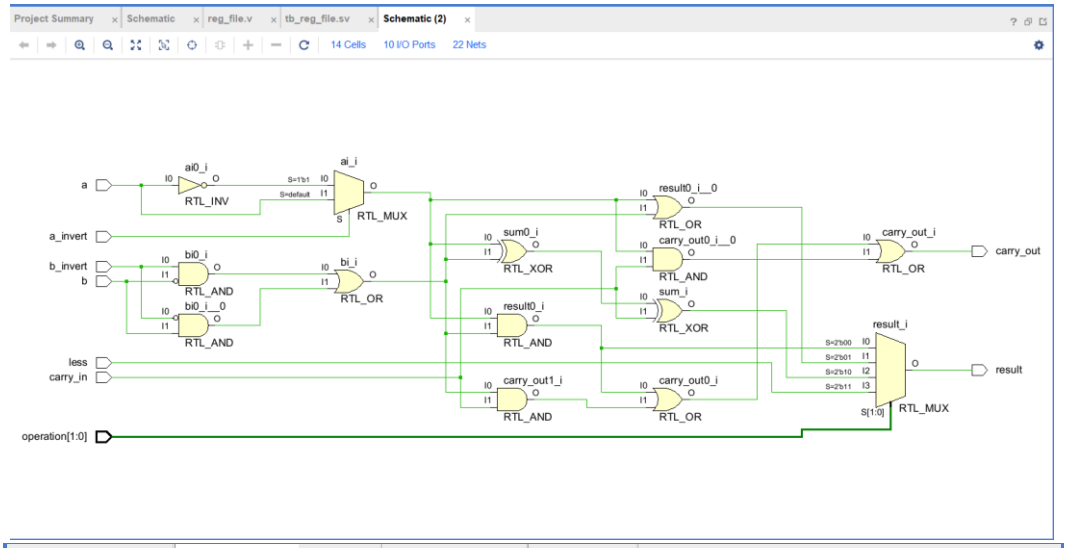
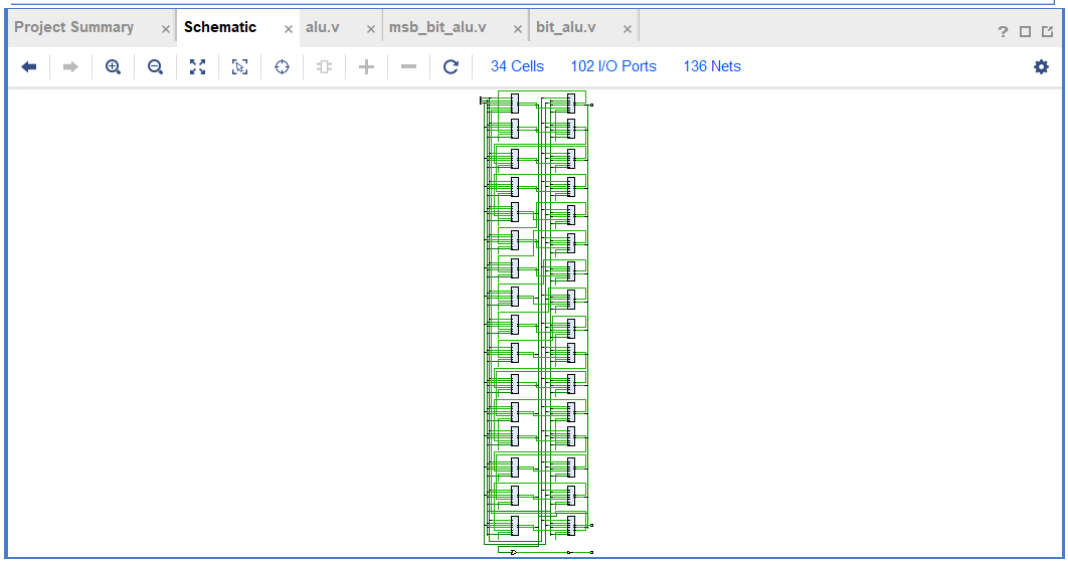
1. Architecture Diagrams

   Show your 1-bit & 32-bit ALU design by “Schematic” tool in Vivado.





2. Answer the following Questions

   1. How overflow is calculated?

      I calculate the overflow by “(operation == 2'b10) & over;”

      Over is “~(ai ^ bi) & (bi ^ carry_in);”

      Because overflow has value when doing ADD or SUB, orrurs when signals of ai and bi are same and different from the signal of ai + bi. Therefore, the possible signals are (ai, bi, carry_in) = (0, 0, 1) and (1, 1, 0).

   2. Explain why ALU control signal of SUB is 0110 and NOR is 1100 ?

      Because from left to right, first bit controls whether a should do the invert, and second bit controls whether b should do the invert, and last two bits

are the operation. Therefore, in SUB, we have to invert b and do the ADD, so it's 0110. In NOR, we have to invert a and b, and to the bitwise AND, so it's 1100 ((a|b)' = a' & b')

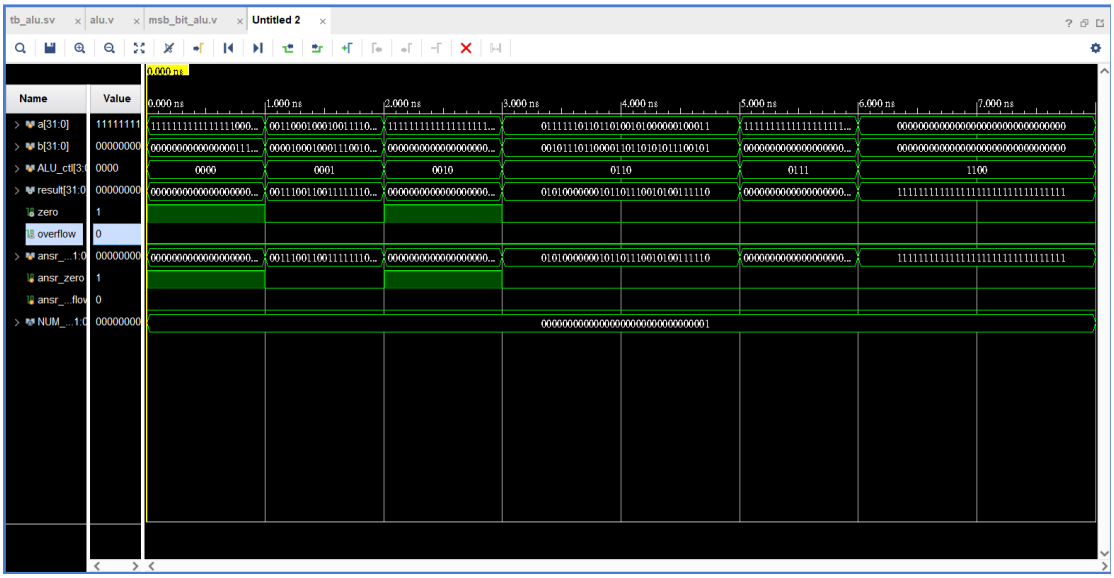
3. (2 cont'd) If you assign different signal to these operation, what problems you may encountered?

   If using different signal to design, there will be some different. First, a_invert and b_invert actually can be ignored because they are the same as the ALU_ctl[3] and ALU_ctl[2]. However, if we change to another signal, there won't appear the connection between inverting signal and ALU_ctl. Second, due to the way of signal, we can design the case in the bit_alu.v with only two signals. Otherwise, we may consider more complicated way to implement.

4. True or false: Because the register file is both read and written on the same clock cycle, any MIPS datapath using edge-triggered writes must have more than one copy of the register file. Explain your answer.

   False. We don't need another register file to store because if we use edge-triggered, we synchronize the action. It makes that read and write do in the same time. Therefore, they won't influence each other.

3. Experimental Result(ALU Only)
   1. Show the waveform screen shot of the testbench tb_alu.0.txt result



   2. What other cases you've tested? Why you choose them?

      I choose the case that a equals to 0x7fffffff, b equals to 0xffffffff for slt. The reason is because this case will cause overflow which makes slt generate the wrong answer.

      I choose the case that a equals to 0x0fffffff, b equals to 0x0f352548 for add. The reason is because I want to make sure that my bit counting is

correct.

I choose the case that a equals to 0x7fffffff, b equals to 0xffffffff for sub. The reason is because I want to make sure whether overflow and invert are correct.

4. Problems Encountered & Solution

Only one problem I met was that when I tested the reg_file.v, I thought that my answers were correct because of the message in console, however, the signal in the waveform became 'X' and red. After tested by the updated file, the problem was solved.