

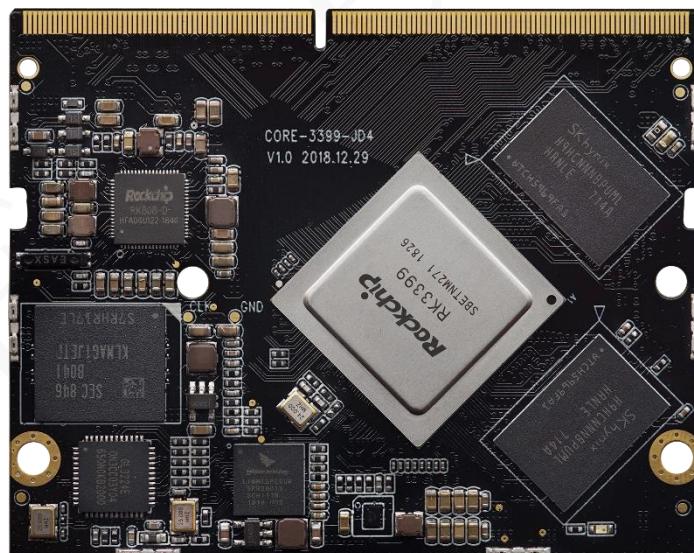


T-CHIP TECHNOLOGY

Core-3399-JD4

Product Specification

V1.0



| Version | Date | Updated content |
|---------|------------|------------------|
| V1.0 | 2019-05-06 | Original version |
| | | |
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1. Product Overview

1. Six-core 64-bit High-performance Processor

Adopts RK3399 six-core 64-bit (A72x2+A53x4) high-performance processor, frequency up to 1.8GHz, integrated quad-core ARM high-end GPU Mali-T860. Provide a variety of storage configuration options, users only need to expand the function backplane to quickly achieve project development.

2. AI Neural Network Processor NPU

Onboard AI neural network acceleration chip SPR2801S, adopts AI special architecture APiM, its computing capability up to 2.8 Tops, 9.3 Tops/W ultra-high efficiency. It can be used in the application domain of low energy consumption and high computing performance products.

3. Rich Extension Interfaces

With rich interfaces such as I2C, SPI, UART, ADC, PWM, GPIO, PCIe, USB3.0, I2S (supports 8-way digital microphone array input), and so on.

4. Powerful Hardware Decoding Capability

Supports MIPI-DSI, EDP, HDMI, DP1.2 multiple display output interfaces, dual-screen identical display/dual-screen differential display, supports 4K VP9, 4K 10bits H265/H264, 1080P (VC-1, MPEG-1/2/4, VP8) multi-format video decoding, and 1080P (H.264, VP8) video coding.

5. Stable And Reliable

With SODIMM 260P interface, the data transmission and expansion performance can be best achieved, immersion gold process pin, corrosion resistant, 2 studs fixed, stable and reliable. Designed measurement is only 69.6mm x 55mm for saving more precious space.

6. Support For Multiple OS

Supports Android, Linux+QT, Ubuntu multiple operating system, the performance is stable and reliable

7. Open Source

Complete with SDK, tutorial, technical information and development tools can be downloaded on the website, and provide development base plate for purchase, making development and learning easier.

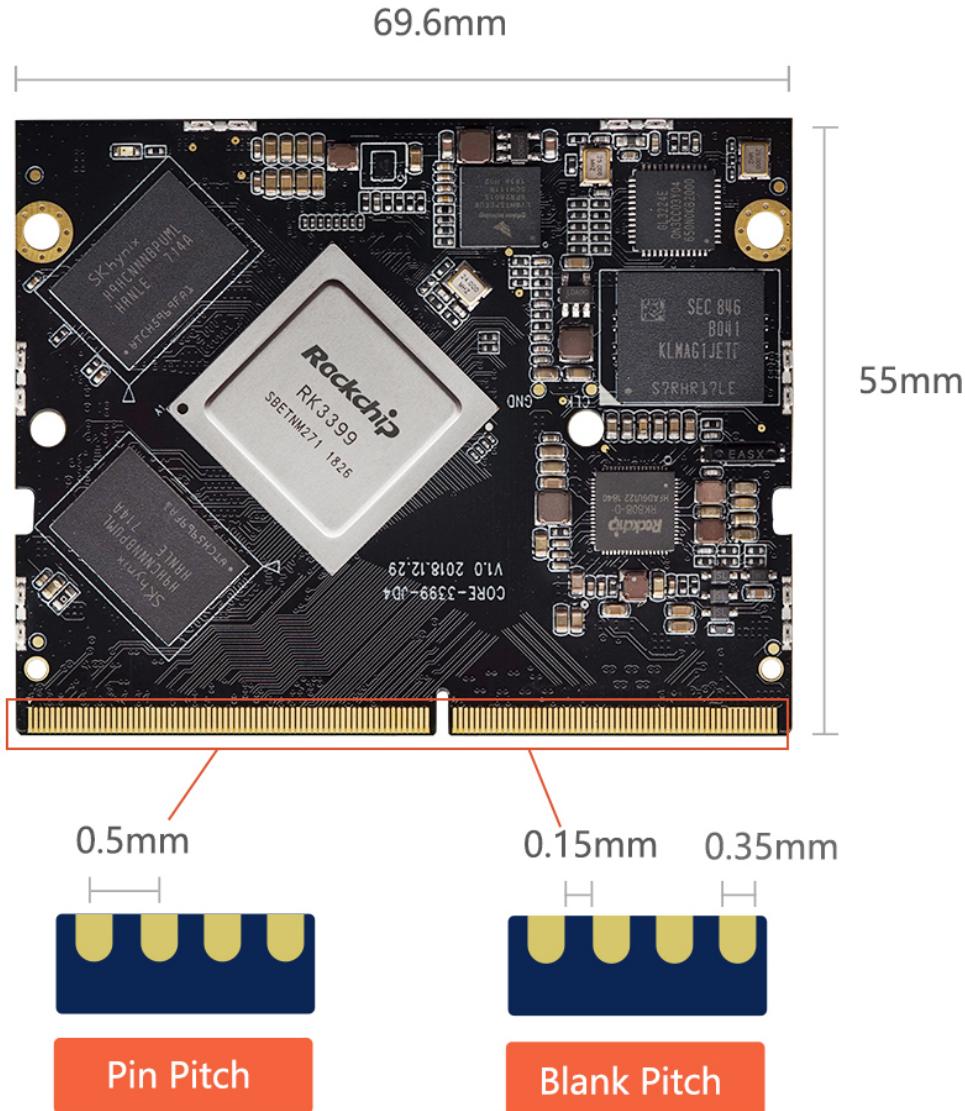
8. Application

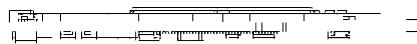
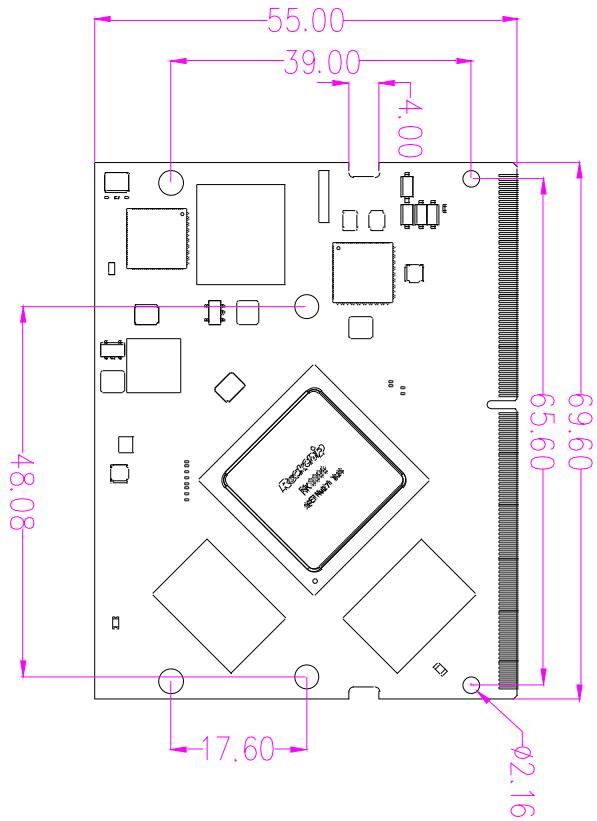
It is suitable for cluster servers, high-performance computing/storage, computer vision, gaming equipment, commercial display equipment, medical equipment, vending machines, industrial computers, etc.

2. Product Specification

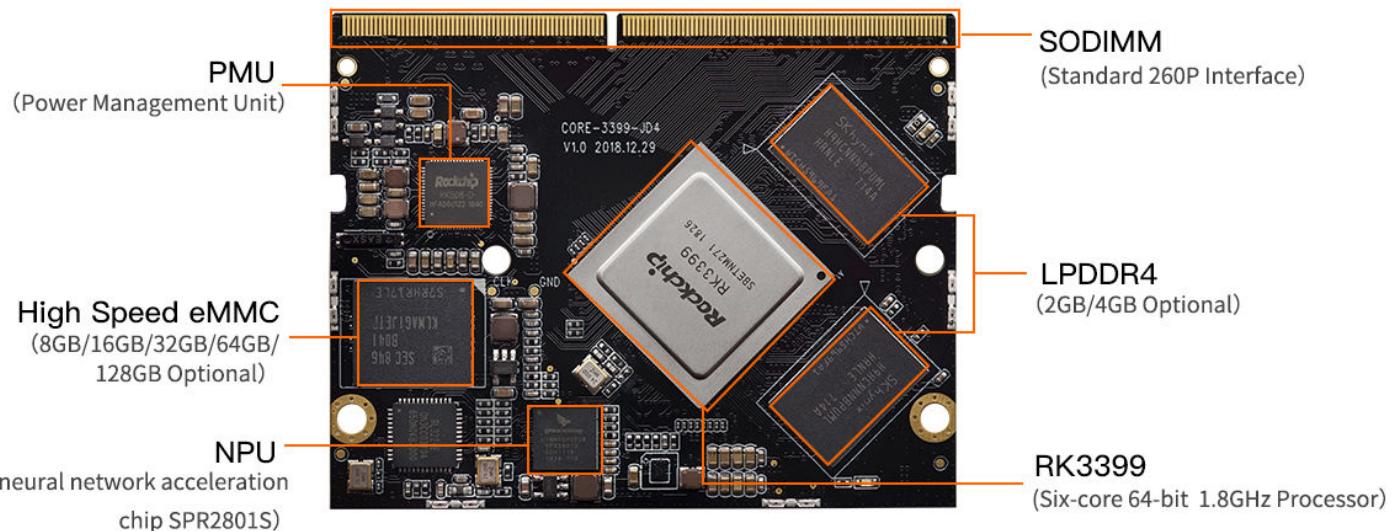
| Specification | |
|-------------------|--|
| SOC | Rockchip RK3399 (28nm HKMG Process) |
| CPU | Six-Core ARM 64-bit processor, up to 1.8GHz Based on Big.Little architecture, Dual-Core Cortex-A72 and Quad-Core Cortex-A53 with separate NEON coprocessor |
| GPU | ARM® Mali-T860 MP4 Quad-core GPU Support OpenGL ES1.1/2.0/3.0/3.1, OpenVG1.1, OpenCL, DX11 Support AFBC(frame buffer compression) |
| VPU | Support 4K VP9 and 4K 10bits H265/H264 video decoding, up to 60fps 1080P multi-format video decoding (WMV, MPEG-1/2/4, VP8) 1080P video coding, support H.264 , VP8 format Video post processor, de-interlacing, de-noising, edge/detail/color optimization |
| RAM | 2GB LPDDR4 (2GB/4GB) |
| Storage | 16GB high-speed eMMC 5.1 (16GB/32GB/128GB) Support TF Card Extended Storage Support M.2 PCIe M-KEY extend NVMe SSD |
| NPU | Onboard AI neural network processor SPR2801S: Computing power up to 2.8 TOPS , peak up to 5.6Tops , 9.3Tops/W ultra-high efficiency Support PLAI (PyTorch) and MDK (Caffe) model training tools Follow-up support TensorFlow Support Image Classification Model VGG-16(GNet1)、GNet18 and Gnetfc Support Target Detection Model: SSD (Based on VGG) |
| Hardware Features | |
| Ethernet | 10 / 100 / 1000 MbpsEthernet interface (RJ45) |
| WiFi | Extend WiFi & Bluetooth via SDIO3.0 |
| Display | 1 x HDMI 2.0, support 4K@60HZ output and HDCP 1.4/2.2 1 x MIPI-DSI , support single channel 1080P@60fps output 1 x eDP 1.3 (4 lanes with 10.8Gbps) 1 x DP 1.2 (DisplayPort), support 4K@60Hz output Support dual-screen identical display/dual-screen differential display |
| Audio | 1 x HDMI 2.0 audio output 1 x SPDIF, for audio output 2 x I2S for audio output and input |
| Camera | 2x MIPI-CSI camera interface (built-in dual-ISP, Maximum support single 13Mpixel or dual 8Mpixel) |
| USB | 3 x USB2.0 Host, 1 x USB3.0 Type-C |
| Interface | I2C×8, SPI×5, UART×5, ADC×4, PWM×3, GPIO×107, PCIe×1, I2S×2 (Support 8-way digital microphone array input) |
| Power | DC input voltage 5V |
| OS / Software | |
| OS | Android, Linux+QT, Ubuntu |
| Software | Support PLAI (PyTorch) and MDK (Caffe) model training tools Follow-up support TensorFlow Support Image Classification Model VGG-16(GNet1)、GNet18 and Gnetfc Support Target Detection Model: SSD (Based on VGG) |
| Appearance | |
| Core Board | Gold finger (SODIMM 260P, 0.5mm pitch) 69.6mm × 55 mm, 10-layer board design |

3. PCB Size





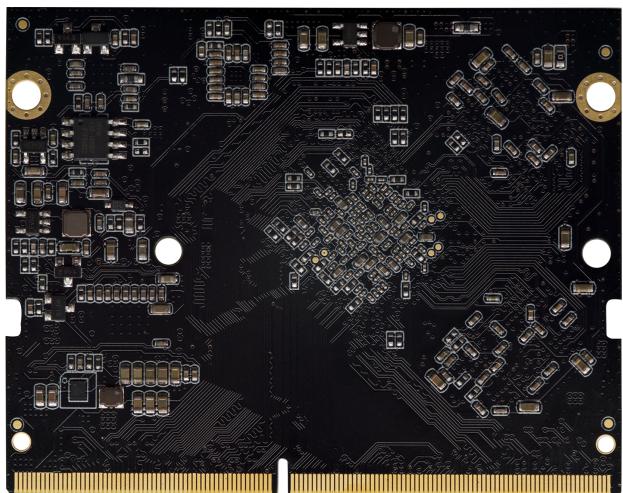
4. Interface definition



Pin Arrangement

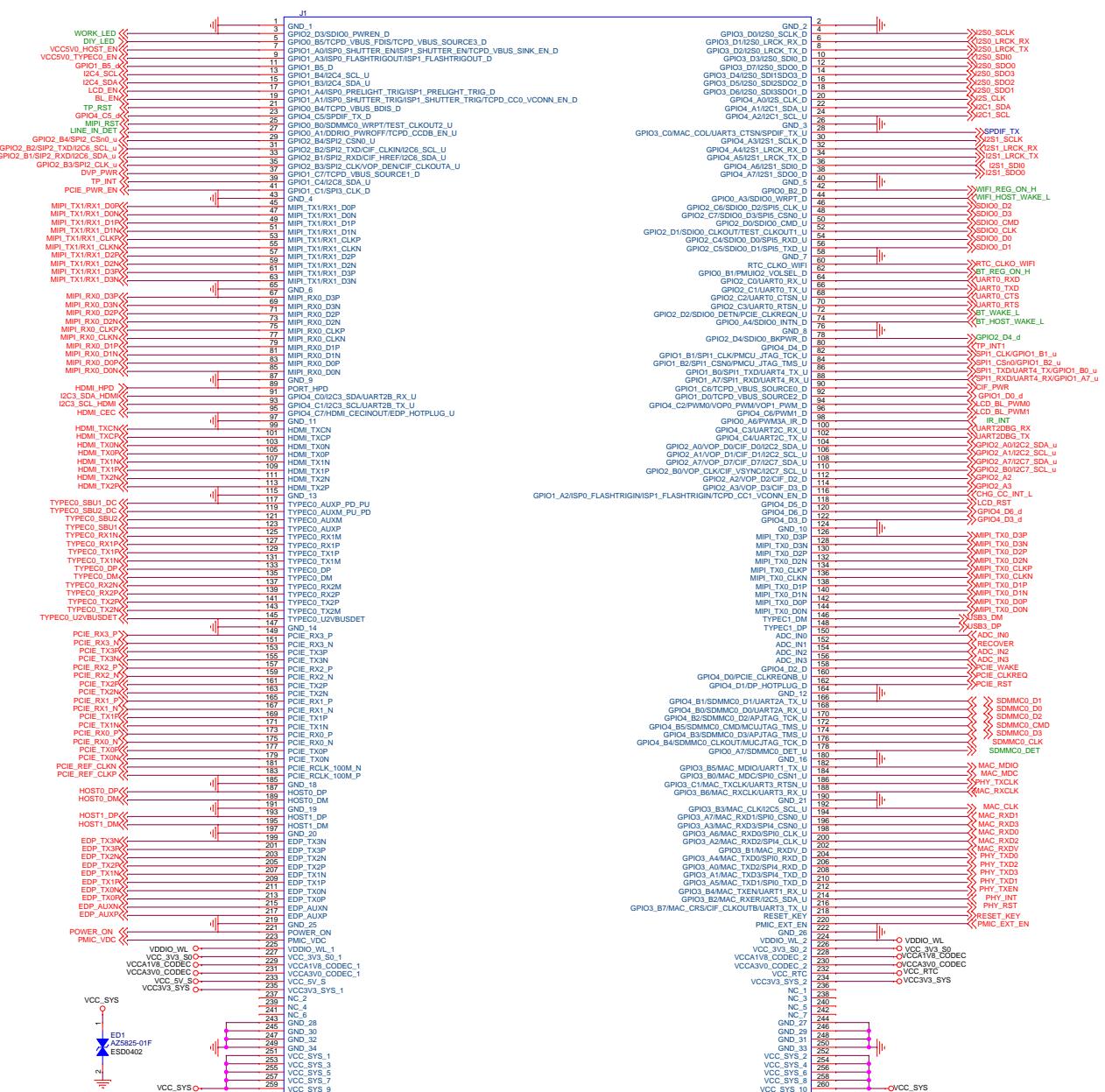


1, 3, 5, 7, 9, 11 253, 255, 257, 259



260, 258, 256, 254 12, 10, 8, 6, 4, 2

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Notes1:

Pin type: I = input, O = output, I/O = input/output (bidirectional) , G= Ground , P = power supply , DOWN = Internal pull down , UP = Internal pull UP

| Part A | pin | Core board pin definition | Pin type | I/O Pull | Function for Floor(MB-RK3399-JD4) | Default function description | IO Power domain | RK3399 Pin Number | RK3399 Pin Name |
|--------|-----|---|----------|----------|-----------------------------------|---|-----------------|-------------------|---|
| | 1 | GND_1 | G | | GND | GND | | | |
| | 3 | GPIO2_D3/SDIO0_PWREN_D_1.8V | I/O | DOWN | WORK_LED | System LED control 1:Enable 0:Disable | 1. 8V | AD9 | GPIO2_D3/SDIO0_PWREN |
| | 5 | GPIO0_B5/TCPD_VBUS_FDIS/TCPD_VBUS_SOURCE3_D_1.8V | I/O | DOWN | DIY_LED | Diy led control 1:Enable 0:Disable | 1. 8V | P24 | GPIO0_B5/TCPD_VBUS_FDIS/TCPD_VBUS_SOURCE3 |
| | 7 | GPIO1_A0/ISPO_SHUTTER_EN/ISP1_SHUTTER_EN/TCPD_VBUS_SINK_EN_D_3.0V | I/O | DOWN | VCC5V0_HOST_EN | Host usb 5v power enable 1:Enable 0:Disable Core board internal series resistance 33R | 3. 0V | R25 | GPIO1_A0/ISPO_SHUTTER_EN/ISP1_SHUTTER_EN/TCPD_VBUS_SINK_EN |
| | 9 | GPIO1_A3/ISPO_FLASHTRIGOUT/ISP1_FLASHTRIGOUT_D_3.0V | I/O | DOWN | VCC5V0_TYPECO_EN | OTG 5v power enable 1:Enable 0:Disable Core board internal series resistance 33R | 3. 0V | R27 | GPIO1_A3/ISPO_FLASHTRIGOUT /ISP1_FLASHTRIGOUT |
| | 11 | GPIO1_B5_D_3.0V | I/O | DOWN | LVDS_RESX | LVDS Reset | 3. 0V | M24 | GPIO1_B5 |
| | 13 | GPIO1_B4/I2C4_SCL_U_3.0V | I/O | UP | I2C4_SCL | I2C clock , Core board interiorl pull up Resistor 2.2K | 3. 0V | P30 | GPIO1_B4/I2C4_SCL |
| | 15 | GPIO1_B3/I2C4_SDA_U_3.0V | I/O | UP | I2C4_SDA | I2C data , Core board interiorl pull up Resistor 2.2K | 3. 0V | P31 | GPIO1_B3/I2C4_SDA |
| | 17 | GPIO1_A4/ISPO_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG_D_3.0V | I/O | DOWN | LCD_EN | LCD enable , Core board internal series resistance 33R | 3. 0V | R28 | GPIO1_A4/ISPO_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG |
| | 19 | GPIO1_A1/ISPO_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_CCO_VCONN_EN D 3.0V | I/O | DOWN | CAM_PWR | Camera power enable , Core board internal series resistance 33R | 3. 0V | T31 | GPIO1_A1/ISPO_SHUTTER_TRIG /ISP1_SHUTTER_TRIG/TCPD_CCO_VCONN_EN |
| | 21 | GPIO0_B4/TCPD_VBUS_BDIS_D_1.8V | I/O | DOWN | MIPI_PWR_EN | MIPI power enable | 1. 8V | V26 | GPIO0_B4/TCPD_VBUS_BDIS |

| | | | | | | | | |
|----|--|-----|------|----------------------------|--|------|-----|---------------------------------------|
| 23 | GPIO4_C5/SPDIF_TX_D_3.0V | I/O | DOWN | GPIO4_C5 | GPIO | 3.0V | AK1 | GPIO4_C5/SPDIF_TX |
| 25 | GPIO0_B0/SDMMC0_WRPT/TEST_CLK0_UT2_U_1.8V | I/O | UP | MIPI_RST | Mipi reset | 1.8V | U28 | GPIO0_B0/SDMMC0_WRPT/TEST_CLKOUT2 |
| 27 | GPIO0_A1/DDRIO_PWRON/TCPD_CCD_B_EN_U_1.8V | I/O | UP | LCD_BL_EN | LCD panel power enable | 1.8V | R29 | GPIO0_A1/DDRIO_PWRON/TCPD_CCDB_EN |
| 29 | GPIO2_B4/SPI2_CSNO_U_3.0V | I/O | UP | GPIO2_B4/SPI2_CS_n0 | SPI bus port 2 | 3.0V | F31 | GPIO2_B4/SPI2_CSNO |
| 31 | GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL_U_3.0V | I/O | UP | GPIO2_B2/SIP2_TXD/I2C6_SCL | SPI bus port 2, I2C serial port 6, need external pull-up | 3.0V | H24 | GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL |
| 33 | GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA_U_3.0V | I/O | UP | GPIO2_B1/SIP2_RXD/I2C6_SDA | SPI bus port 2, I2C serial port 6, need external pull-up | 3.0V | F30 | GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA |
| 35 | GPIO2_B3/SPI2_CLK/VOP_DEN/CIF_CLKOUTA_U_3.0V | I/O | UP | GPIO2_B3/SPI2_CLK | GPIO / SP2 CLK / MIPI CLK | 3.0V | H31 | GPIO2_B3/SPI2_CLK/VOP_DEN/CIF_CLKOUTA |
| 37 | GPIO1_C7/TCPD_VBUS_SOURCE1_D_3.0V | I/O | DOWN | TP_RST | TP Reset(Active Low) | 3.0V | M31 | GPIO1_C7/TCPD_VBUS_SOURCE1 |
| 39 | GPIO1_C4/I2C8_SDA_U_3.0V | I/O | UP | GPIO1_C4 | GPIO | 3.0V | M29 | GPIO1_C4/I2C8_SDA |
| 41 | GPIO1_C1/SPI3_CLK_D_3.0V | I/O | DOWN | GPIO1_C1 | GPIO | 3.0V | M27 | GPIO1_C1/SPI3_CLK |
| 43 | GND_4 | G | | GND | GND | | | |
| 45 | MIPI_TX1/RX1_DOP | I/O | | MIPI_TX1/RX1_DOP | MIPI-DSI1/CSI1 differential lane 0 positive | 1.8V | AK6 | MIPI_TX1/RX1_DOP |
| 47 | MIPI_TX1/RX1_DON | I/O | | MIPI_TX1/RX1_DON | MIPI-DSI1/CSI1 differential lane 0 negative | 1.8V | AL6 | MIPI_TX1/RX1_DON |
| 49 | MIPI_TX1/RX1_D1P | I/O | | MIPI_TX1/RX1_D1P | MIPI-DSI1/CSI1 differential lane 1 positive | 1.8V | AK7 | MIPI_TX1/RX1_D1P |
| 51 | MIPI_TX1/RX1_D1N | I/O | | MIPI_TX1/RX1_D1N | MIPI-DSI1/CSI1 differential lane 1 negative | 1.8V | AL7 | MIPI_TX1/RX1_D1N |
| 53 | MIPI_TX1/RX1_CLKP | I/O | | MIPI_TX1/RX1_CLK_P | MIPI-DSI1/CSI1 differential clock lane positive | 1.8V | AK8 | MIPI_TX1/RX1_CLKP |
| 55 | MIPI_TX1/RX1_CLKN | I/O | | MIPI_TX1/RX1_CLK_N | MIPI-DSI1/CSI1 differential clock lane negative | 1.8V | AL8 | MIPI_TX1/RX1_CLKN |

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|----|------------------------------------|-----|----|------------------|---|--------------|------|-----------------------------|
| 57 | MIPI_TX1/RX1_D2P | I/O | | MIPI_TX1/RX1_D2P | MIPI-DSI1/CSI1 differential lane 2 positive | 1.8V | AK9 | MIPI_TX1/RX1_D2P |
| 59 | MIPI_TX1/RX1_D2N | I/O | | MIPI_TX1/RX1_D2N | MIPI-DSI1/CSI1 differential lane 2 negative | 1.8V | AL9 | MIPI_TX1/RX1_D2N |
| 61 | MIPI_TX1/RX1_D3P | I/O | | MIPI_TX1/RX1_D3P | MIPI-DSI1/CSI1 differential lane 3 positive | 1.8V | AK10 | MIPI_TX1/RX1_D3P |
| 63 | MIPI_TX1/RX1_D3N | I/O | | MIPI_TX1/RX1_D3N | MIPI-DSI1/CSI1 differential lane 3 negative | 1.8V | AL10 | MIPI_TX1/RX1_D3N |
| 65 | GND_6 | G | | GND | GND | | | |
| 67 | MIPI_RX0_D3P | I | | MIPI_RX0_D3P | MIPI-CSI0 differential lane 3 positive | 1.8V | AK11 | MIPI_RX0_D3P |
| 69 | MIPI_RX0_D3N | I | | MIPI_RX0_D3N | MIPI-CSI0 differential lane 3 positive | 1.8V | AL11 | MIPI_RX0_D3N |
| 71 | MIPI_RX0_D2P | I | | MIPI_RX0_D2P | MIPI-CSI0 differential lane 2 positive | 1.8V | AK12 | MIPI_RX0_D2P |
| 73 | MIPI_RX0_D2N | I | | MIPI_RX0_D2N | MIPI-CSI0 differential lane 2 negative | 1.8V | AL12 | MIPI_RX0_D2N |
| 75 | MIPI_RX0_CLKP | I | | MIPI_RX0_CLKP | MIPI-CSI0 differential clock lane positive | 1.8V | AK13 | MIPI_RX0_CLKP |
| 77 | MIPI_RX0_CLKN | I | | MIPI_RX0_CLKN | MIPI-CSI0 differential clock lane negative | 1.8V | AL13 | MIPI_RX0_CLKN |
| 79 | MIPI_RX0_D1P | I | | MIPI_RX0_D1P | MIPI-CSI0 differential lane 1 positive | 1.8V | AK14 | MIPI_RX0_D1P |
| 81 | MIPI_RX0_D1N | I | | MIPI_RX0_D1N | MIPI-CSI0 differential lane 1 negative | 1.8V | AL14 | MIPI_RX0_D1N |
| 83 | MIPI_RX0_D0P | I | | MIPI_RX0_D0P | MIPI-CSI0 differential lane 0 positive | 1.8V | AK15 | MIPI_RX0_D0P |
| 85 | MIPI_RX0_D0N | I | | MIPI_RX0_D0N | MIPI-CSI0 differential lane 0 negative | 1.8V | AL15 | MIPI_RX0_D0N |
| 87 | GND_9 | G | | GND | GND | | | |
| 89 | HDMI_HPD | I | | HDMI_HPD | HDMI Hot Plug Detection interrupt with 5V tolerance | HDMI_DE_T_IN | AE15 | HDMI_HPD |
| 91 | GPIO4_CO/I2C3_SDA/UART2B_RX_U_3.0V | I/O | UP | I2C3_SDA_HDMI | I2C serial port 3, for HDMI, need external pull-up | 3.0V | AG6 | GPIO4_CO/I2C3_SDA/UART2B_RX |

| | | | | | | | | |
|-----|---|-----|----|----------------|--|------|------|------------------------------------|
| 93 | GPIO4_C1/I2C3_SCL/UART2B_TX_U_3.0V | I/O | UP | I2C3_SCL_HDMI | I2C serial port 3, for HDMI, need external pull-up | 3.0V | AL2 | GPIO4_C1/I2C3_SCL/UART2B_TX |
| 95 | GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG_U_3.0V | I/O | UP | HDMI_CEC | HDMI CEC communication | 3.0V | AD7 | GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG |
| 97 | GND_11 | G | | GND | GND | | | |
| 99 | HDMI_TCN | 0 | | HDMI_TXCN | HDMI differential pixel clock negative | 1.8V | AL16 | HDMI_TCN |
| 101 | HDMI_TCP | 0 | | HDMI_TXCP | HDMI differential pixel clock positive | 1.8V | AK16 | HDMI_TCP |
| 103 | HDMI_TXON | 0 | | HDMI_TXON | HDMI channel 0 differential serial data negative | 1.8V | AL17 | HDMI_TXON |
| 105 | HDMI_TXOP | 0 | | HDMI_TXOP | HDMI channel 0 differential serial data positive | 1.8V | AK17 | HDMI_TXOP |
| 107 | HDMI_TX1N | 0 | | HDMI_TX1N | HDMI channel 1 differential serial data negative | 1.8V | AL18 | HDMI_TX1N |
| 109 | HDMI_TX1P | 0 | | HDMI_TX1P | HDMI channel 1 differential serial data positive | 1.8V | AK18 | HDMI_TX1P |
| 111 | HDMI_TX2N | 0 | | HDMI_TX2N | HDMI channel 2 differential serial data negative | 1.8V | AL19 | HDMI_TX2N |
| 113 | HDMI_TX2P | 0 | | HDMI_TX2P | HDMI channel 2 differential serial data positive | 1.8V | AK19 | HDMI_TX2P |
| 115 | GND_13 | G | | GND | GND | | | |
| 117 | TYPECO_AUXP_PD_PU | | | TYPECO_SBU1_DC | TYPECO AUX pull-up/pull-down polarity reversal pins. | | AH17 | TYPECO_AUXP_PD_PU |
| 119 | TYPECO_AUXM_PU_PD | | | TYPECO_SBU2_DC | TYPECO AUX pull-up/pull-down polarity reversal pins. | | AG17 | TYPECO_AUXM_PU_PD |
| 121 | TYPECO_AUXM | I/O | | TYPECO_SBU2 | TYPECO AUX differential TX/RX serial data | | AL20 | TYPECO_AUXM |
| 123 | TYPECO_AUXP | I/O | | TYPECO_SBU1 | TYPECO AUX differential TX/RX serial data | | AK20 | TYPECO_AUXP |
| 125 | TYPECO_RX1M | I | | TYPECO_RX1N | TYPECO negative half of first Super Speed RX differential pair | | AL21 | TYPECO_RX1M |
| 127 | TYPECO_RX1P | I | | TYPECO_RX1P | TYPECO positive half of first Super Speed RX differential pair | | AK21 | TYPECO_RX1P |

| | | | | | | | | |
|-----|------------------|---|--|------------------|---|------|------|------------------|
| 129 | TYPECO_TX1P | 0 | | TYPECO_TX1P | TYPECO positive half of first Super Speed TX differential pair. | | AL22 | TYPECO_TX1P |
| 131 | TYPECO_TX1M | 0 | | TYPECO_TX1N | TYPECO negative half of first Super Speed TX differential pair | | AK22 | TYPECO_TX1M |
| 133 | TYPECO_DP | A | | TYPECO_DP | TYPECO Data Plus port(for system update) | | AG23 | TYPECO_DP |
| 135 | TYPECO_DM | A | | TYPECO_DM | TYPECO Data Minus port(for system update) | | AH23 | TYPECO_DN |
| 137 | TYPECO_RX2M | I | | TYPECO_RX2N | TYPECO negative half of second SuperSpeedRX differential pair. | | AL23 | TYPECO_RX2M |
| 139 | TYPECO_RX2P | I | | TYPECO_RX2P | TYPECO positive half of second SuperSpeedRX differential pair. | | AK23 | TYPECO_RX2P |
| 141 | TYPECO_TX2P | 0 | | TYPECO_TX2P | TYPECO positive half of second SuperSpeedTX differential pair. | | AL24 | TYPECO_TX2P |
| 143 | TYPECO_TX2M | 0 | | TYPECO_TX2N | TYPECO negative half of second SuperSpeedTX differential pair. | | AK24 | TYPECO_TX2M |
| 145 | TYPECO_U2VBUSDET | I | | TYPECO_U2VBUSDET | TYPECO connected / vbus power detect for USB2.0 | | AK30 | TYPECO_U2VBUSDET |
| 147 | GND_14 | G | | GND | GND | | | |
| 149 | PCIE_RX3_P | I | | PCIE_RX3_P | PCIE differential lane 3 positive input | 1.8V | AF27 | PCIE_RX3_P |
| 151 | PCIE_RX3_N | I | | PCIE_RX3_N | PCIE differential lane 3 negative input | 1.8V | AF28 | PCIE_RX3_N |
| 153 | PCIE_TX3_P | 0 | | PCIE_TX3P | PCIE differential lane 3 positive output | 1.8V | AD27 | PCIE_TX3_P |
| 155 | PCIE_TX3_N | 0 | | PCIE_TX3N | PCIE differential lane 3 negative output | 1.8V | AD28 | PCIE_TX3_N |
| 157 | PCIE_RX2_P | I | | PCIE_RX2_P | PCIE differential lane 2 positive input | 1.8V | AC27 | PCIE_RX2_P |
| 159 | PCIE_RX2_N | I | | PCIE_RX2_N | PCIE differential lane 2 negative input | 1.8V | AC28 | PCIE_RX2_N |
| 161 | PCIE_TX2_P | 0 | | PCIE_TX2P | PCIE differential lane 2 positive output | 1.8V | AA27 | PCIE_TX2_P |
| 163 | PCIE_TX2_N | 0 | | PCIE_TX2N | PCIE differential lane 2 negative output | 1.8V | AA28 | PCIE_TX2_N |

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|-----|------------------|---|--|---------------|---|------|------|------------------|
| 165 | PCIE_RX1_P | I | | PCIE_RX1_P | PCIE differential lane 1 positive input | 1.8V | AH30 | PCIE_RX1_P |
| 167 | PCIE_RX1_N | I | | PCIE_RX1_N | PCIE differential lane 1 negative input | 1.8V | AH31 | PCIE_RX1_N |
| 169 | PCIE_TX1_P | 0 | | PCIE_TX1P | PCIE differential lane 1 positive output | 1.8V | AG30 | PCIE_TX1_P |
| 171 | PCIE_TX1_N | 0 | | PCIE_TX1N | PCIE differential lane 1 negative output | 1.8V | AG31 | PCIE_TX1_N |
| 173 | PCIE_RX0_P | I | | PCIE_RX0_P | PCIE differential lane 0 positive input | 1.8V | AF30 | PCIE_RX0_P |
| 175 | PCIE_RX0_N | I | | PCIE_RX0_N | PCIE differential lane 0 negative input | 1.8V | AF31 | PCIE_RX0_N |
| 177 | PCIE_TX0_P | 0 | | PCIE_TX0P | PCIE differential lane 0 positive output | 1.8V | AE30 | PCIE_TX0_P |
| 179 | PCIE_TX0_N | 0 | | PCIE_TX0N | PCIE differential lane 0 negative output | 1.8V | AE31 | PCIE_TX0_N |
| 181 | PCIE_RCLK_100M_N | 0 | | PCIE_REF_CLKN | PCIE 100MHz reference clock as input to PLL | 1.8V | AD30 | PCIE_RCLK_100M_N |
| 183 | PCIE_RCLK_100M_P | 0 | | PCIE_REF_CLKP | PCIE 100MHz reference clock as input to PLL | 1.8V | AD31 | PCIE_RCLK_100M_P |
| 185 | GND_18 | G | | GND | GND | | | |
| 187 | HOST0_DP | | | HOST0_DP | USB HOST0 Data Plus port | | AB30 | USBO_DP |
| 189 | HOST0_DM | | | HOST0_DM | USB HOST0 Data Minus port | | AB31 | USBO_DN |
| 191 | GND_19 | G | | GND | GND | | | |
| 193 | HOST1_DP | | | HOST1_DP | USB HOST1 Data Plus port | | AA30 | USB1_DP |
| 195 | HOST1_DM | | | HOST1_DM | USB HOST1 Data Minus port | | AA31 | USB1_DN |
| 197 | GND_20 | G | | GND | GND | | | |
| 199 | EDP_TX3N | 0 | | EDP_TX3N | eDP differential lane 3 negative output | 1.8V | D31 | EDP_TX3N |

| | | | | | | | | |
|-----|-----------------|-----|--|---------------|---|---------------|-----|----------|
| 201 | EDP_TX3P | 0 | | EDP_TX3P | eDP differential lane 3 positive output | 1.8V | D30 | EDP_TX3P |
| 203 | EDP_TX2N | 0 | | EDP_TX2N | eDP differential lane 2 negative output | 1.8V | C31 | EDP_TX2N |
| 205 | EDP_TX2P | 0 | | EDP_TX2P | eDP differential lane 2 positive output | 1.8V | C30 | EDP_TX2P |
| 207 | EDP_TX1N | 0 | | EDP_TX1N | eDP differential lane 1 negative output | 1.8V | A30 | EDP_TX1N |
| 209 | EDP_TX1P | 0 | | EDP_TX1P | eDP differential lane 1 positive output | 1.8V | B30 | EDP_TX1P |
| 211 | EDP_TXON | 0 | | EDP_TXON | eDP differential lane 0 negative output | 1.8V | A29 | EDP_TXON |
| 213 | EDP_TXOP | 0 | | EDP_TXOP | eDP differential lane 0 positive output | 1.8V | B29 | EDP_TXOP |
| 215 | EDP_AUXN | I/O | | EDP_AUXN | eDP differential AUX channel positive output | 1.8V | A28 | EDP_AUXN |
| 217 | EDP_AUXP | I/O | | EDP_AUXP | eDP differential AUX channel negative output | 1.8V | B28 | EDP_AUXP |
| 219 | GND_25 | G | | GND | GND | | | |
| 221 | POWER_ON | | | POWER_ON | Power on Signal Input, External connection Power key , active low | To POWER_K EV | | |
| 223 | PMIC_VDC | P | | VCC_5V_S | Input Voltage 3.3V~5.5V, Rated input current 50mA | 5V | | |
| 225 | VDDIO_WL_1 | P | | VDDIO_WL | 1.8V output, Max current 1A to WIFI_IO | 1.8V | | |
| 227 | VCC_3V3_S0 | P | | VCC_LAN | 3.3V output, Max current 300mA TO LAN | 3.3V | | |
| 229 | VCCA1V8_CODEC_1 | P | | VCCA1V8_CODEC | 1.8V output, Max current 150mA to Codec | 1.8V | | |
| 231 | VCCA3V0_CODEC_1 | P | | VCCA3V0_CODEC | 3.0V output, Max current 300mA to Codec | 3.0V | | |
| 233 | VCC_5V_S | P | | VCC_5V_S | 5.0V input, Max current 50mA | 5.0V | | |
| 235 | VCC3V3_SYS_1 | P | | VCC3V3_SYS | 3.3V output, Max current 1A | 3.3V | | |

| 237 | NC_2 | | | | | | | |
|--------|-----------|------------------------------|----------|------------|---|--------------------------------------|-----------------|-------------------|
| 239 | NC_4 | | | | | | | |
| 241 | NC_6 | | | | | | | |
| 243 | GND_28 | G | | GND | Power ground | | | |
| 245 | GND_30 | G | | GND | Power ground | | | |
| 247 | GND_32 | G | | GND | Power ground | | | |
| 249 | GND_34 | G | | GND | Power ground | | | |
| 251 | VCC_SYS_1 | P | | VCC5V0_SYS | Input Voltage 4.8V~5.5V | 5.0V | | |
| 253 | VCC_SYS_3 | P | | VCC5V0_SYS | Input Voltage 4.8V~5.5V | 5.0V | | |
| 255 | VCC_SYS_5 | P | | VCC5V0_SYS | Input Voltage 4.8V~5.5V | 5.0V | | |
| 257 | VCC_SYS_7 | P | | VCC5V0_SYS | Input Voltage 4.8V~5.5V | 5.0V | | |
| 259 | VCC_SYS_9 | P | | VCC5V0_SYS | Input Voltage 4.8V~5.5V | 5.0V | | |
| Part B | pin | Core board pin definition | Pad type | IO Pull | Function for Floor(MB-JD4-RK3300&2300PRO) | Default function description | IO Power domain | RK3399 Pin Number |
| | 2 | GND_2 | G | | GND | GND | | |
| | 4 | GPIO3_D0/I2S0_SCLK_D_1.8V | I/O | DOWN | I2S0_SCLK | I2S 0 serial clock , for audio codec | 1.8V | AG3 |
| | 6 | GPIO3_D1/I2S0_LRCK_RX_D_1.8V | I/O | DOWN | I2S0_LRCK_RX | I2S 0 port , for audio codec | 1.8V | AF4 |
| | 8 | GPIO3_D2/I2S0_LRCK_TX_D_1.8V | I/O | DOWN | I2S0_LRCK_TX | I2S 0 port , for audio codec | 1.8V | AJ2 |
| | 10 | GPIO3_D3/I2S0_SDIO_D_1.8V | I/O | DOWN | I2S0_SDIO | I2S serial data input 0 | 1.8V | Y7 |

| | | | | | | | | |
|----|---|-----|------|------------------|---|------|-----|--------------------------------------|
| 12 | GPIO3_D7/I2S0_SD00_D_1.8V | I/O | DOWN | I2S0_SD00 | I2S serial data output 0 | 1.8V | AH1 | GPIO3_D7/I2S0_SD00 |
| 14 | GPIO3_D4/I2S0_SDI1SD03_D_1.8V | I/O | DOWN | I2S0_SD03 | I2S serial data output 3 | 1.8V | AE5 | GPIO3_D4/I2S0_SDI1SD03 |
| 16 | GPIO3_D5/I2S0_SDI2SD02_D_1.8V | I/O | DOWN | I2S0_SD02 | I2S serial data output 2 | 1.8V | AA6 | GPIO3_D5/I2S0_SDI2SD02 |
| 18 | GPIO3_D6/I2S0_SDI3SD01_D_1.8V | I/O | DOWN | I2S0_SD01 | I2S serial data output 1 | 1.8V | AH2 | GPIO3_D6/I2S0_SDI3SD01 |
| 20 | GPIO4_A0/I2S_CLK_D_1.8V | I/O | DOWN | I2S_CLK | I2S MCLK, for both I2S0 and I2S1 | 1.8V | AC7 | GPIO4_A0/I2S_CLK |
| 22 | GPIO4_A1/I2C1_SDA_U_1.8V | I/O | UP | I2C1_SDA | I2C serial port 1, for Audio, Core board interiorl pull up Resistor 2.2K | 1.8V | AG1 | GPIO4_A1/I2C1_SDA |
| 24 | GPIO4_A2/I2C1_SCL_U_1.8V | I/O | UP | I2C1_SCL | I2C serial port 1, for Audio, Core board interiorl pull up Resistor 2.2K | 1.8V | Y6 | GPIO4_A2/I2C1_SCL |
| 26 | GND_3 | G | | GND | GND | | | |
| 28 | GPIO3_CO/MAC_COL/UART3_CTSN/SPDIF_TX_U_3.3V | I/O | UP | EAR_CTL | EARPHONE out EN (Active high) | 3.3V | D27 | GPIO3_CO/MAC_COL/UART3_CTSN/SPDIF_TX |
| 30 | GPIO4_A3/I2S1_SCLK_D_1.8V | I/O | DOWN | I2S1_SCLK | I2S 1 port, | 1.8V | AF3 | GPIO4_A3/I2S1_SCLK |
| 32 | GPIO4_A4/I2S1_LRCK_RX_D_1.8V | I/O | DOWN | I2S1_LRCK_RX | I2S 1 port, | 1.8V | AA7 | GPIO4_A4/I2S1_LRCK_RX |
| 34 | GPIO4_A5/I2S1_LRCK_TX_D_1.8V | I/O | DOWN | I2S1_LRCK_TX | I2S 1 port, | 1.8V | AJ1 | GPIO4_A5/I2S1_LRCK_TX |
| 36 | GPIO4_A6/I2S1_SDIO_D_1.8V | I/O | DOWN | I2S1_SDIO | I2S 1 port, | 1.8V | AD6 | GPIO4_A6/I2S1_SDIO |
| 38 | GPIO4_A7/I2S1_SD00_D_1.8V | I/O | DOWN | I2S1_SD00 | I2S 1 port, | 1.8V | AC6 | GPIO4_A7/I2S1_SD00 |
| 40 | GND_5 | G | | GND | GND | | | |
| 42 | GPIO0_B2_D_1.8V | I/O | DOWN | WIFI_REG_ON_H | WIFI module power enable(active high) | 1.8V | W31 | GPIO0_B2 |
| 44 | GPIO0_A3/SDIO0_WRPT_D_1.8V | I/O | DOWN | WIFI_HOST_WAKE_L | WIFI module wake up AP(Wifi-->RK3399) | 1.8V | V31 | GPIO0_A3/SDIO0_WRPT |
| 46 | GPIO2_C6/SDIO0_D2/SPI5_CLK_U_1.8V | I/O | UP | SDIO0_D2 | SDIO0 data2 , for WIFI module | 1.8V | AG7 | GPIO2_C6/SDIO0_D2/SPI5_CLK |

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|----|---|-----|------|--------------------|---|------|------|------------------------------------|
| 48 | GPIO2_C7/SDIO0_D3/SPI5_CSNO_U_1.8V | I/O | UP | SDIO0_D3 | SDIO0 data3 , for WIFI module | 1.8V | AE8 | GPIO2_C7/SDIO0_D3/SPI5_CSNO |
| 50 | GPIO2_D0/SDIO0_CMD_U_1.8V | I/O | UP | SDIO0_CMD | SDIO0 command output , for WIFI module | 1.8V | AH6 | GPIO2_D0/SDIO0_CMD |
| 52 | GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1_U_1.8V | I/O | UP | SDIO0_CLK | SDIO0 clock output, for WIFI module | 1.8V | AF7 | GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1 |
| 54 | GPIO2_C4/SDIO0_D0/SPI5_RXD_U_1.8V | I/O | UP | SDIO0_D0 | SDIO0 data0 , for WIFI module | 1.8V | AD8 | GPIO2_C4/SDIO0_D0/SPI5_RXD |
| 56 | GPIO2_C5/SDIO0_D1/SPI5_TXD_U_1.8V | I/O | UP | SDIO0_D1 | SDIO0 data1, for WIFI module | 1.8V | AK5 | |
| 58 | GND_7 | G | | GND | GND | | | |
| 60 | RTC_CLKO_WIFI | | | RTC_CLKO_WIFI | 32.768K clock output to WIFI Core board interiorl pull up Resistor 10K | 1.8V | | |
| 62 | GPIO0_B1/PMUI02_VOLSEL_D_1.8V | I/O | DOWN | BT_REG_ON_H | B1 module power enable 1:Enable 0:Disable Core board interiorl pull up Resistor 10K | 1.8V | V30 | GPIO0_B1/PMUI02_VOLSEL |
| 64 | GPIO2_CO/UART0_RX_U_1.8V | I/O | UP | UART0_RXD | UART0 RX, for BT module | 1.8V | AE9 | GPIO2_CO/UART0_RX |
| 66 | GPIO2_C1/UART0_TX_U_1.8V | I/O | UP | UART0_TXD | UART0 RX, for BT module | 1.8V | AH8 | GPIO2_C1/UART0_TX |
| 68 | GPIO2_C2/UART0_CTSN_U_1.8V | I/O | UP | UART0_CTS | UART0 CTS, for BT module(hardware flow control) | 1.8V | AG8 | GPIO2_C2/UART0_CTSN |
| 70 | GPIO2_C3/UART0_RTSN_U_1.8V | I/O | UP | UART0_RTS | UART0 RTS, for BT module(hardware flow control) | 1.8V | AL5 | GPIO2_C3/UART0_RTSN |
| 72 | GPIO2_D2/SDIO0_DETN/PCIE_CLKREQN_U_1.8V | I/O | UP | BT_WAKE_L | AP wake up BT module | 1.8V | AL4 | GPIO2_D2/SDIO0_DETN/PCIE_CLKREQN |
| 74 | GPIO0_A4/SDIO0_INTN_D_1.8V | I/O | DOWN | BT_HOST_WAKE_L | BT module wake up AP | 1.8V | AA25 | GPIO0_A4/SDIO0_INTN |
| 76 | GND_8 | G | | GND | GND | | | |
| 78 | GPIO2_D4/SDIO0_BKPWR_D_1.8V | I/O | DOWN | GPIO2_D4/3G_PWR_EN | 3G Power_EN (active high) | 1.8V | AF8 | GPIO2_D4/SDIO0_BKPWR |
| 80 | GPIO4_D4_D_3.0V | I/O | DOWN | TP_INT1 | Touch pannel interrupt input 1 | 3.0V | AH5 | GPIO4_D4 |

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|-----|--|-----|------|----------------------------------|---|------|-----|--|
| 82 | GPIO1_B1/SPI1_CLK/PMCU_JTAG_TC K_U_3.0V | I/O | UP | SPI1_CLK/GPIO1_B 1_u | SPI bus port 1 | 3.0V | P28 | GPIO1_B1/SPI1_CLK/PMCU_JTA G_TCK |
| 84 | GPIO1_B2/SPI1_CSNO/PMCU_JTAG_T MS_U_3.0V | I/O | UP | SPI1_CSNO/GPIO1_B 2_u | SPI bus port 1 | 3.0V | P29 | GPIO1_B2/SPI1_CSNO/PMCU_JT AG_TMS |
| 86 | GPIO1_B0/SPI1_TXD/UART4_RX_U_3 .0V | I/O | UP | SPI1_TXD/UART4_T X/GPIO1_B0_u | SPI bus port 1 | 3.0V | R31 | GPIO1_B0/SPI1_TXD/UART4_RX |
| 88 | GPIO1_A7/SPI1_RXD/UART4_RX_U_3 .0V | I/O | UP | SPI1_RXD/UART4_R X/GPIO1_A7_u | SPI bus port 1 | 3.0V | P27 | GPIO1_A7/SPI1_RXD/UART4_RX |
| 90 | GPIO1_C6/TCPD_VBUS_SOURCE0_D_3 .0V | I/O | DOWN | SDMMCO_PWR | TF_Card Power_EN (active high) | 3.0V | L25 | GPIO1_C6/TCPD_VBUS_SOURCE0 |
| 92 | GPIO1_D0/TCPD_VBUS_SOURCE2_D_3 .0V | I/O | DOWN | GPIO1_D0_d | GPIO | 3.0V | L26 | GPIO1_D0/TCPD_VBUS_SOURCE2 |
| 94 | GPIO4_C2/PWM0/VOPO_PWM/VOP1_PW M_D_3.0V | I/O | DOWN | LCD_BL_PWM0 | PWM0 output:EDP backlight control(external) | 3.0V | AF5 | GPIO4_C2/PWM0/VOPO_PWM/VOP 1_PWM |
| 96 | GPIO4_C6/PWM1_D_3.0V | I/O | DOWN | LCD_BL_PWM1 | PWM1 output:MIPI backlight control | 3.0V | AL3 | GPIO4_C6/PWM1 |
| 98 | GPIO0_A6/PWM3A_IR_D_1.8V | I/O | DOWN | IR_INT | IR receiver input | 1.8V | P25 | GPIO0_A6/PWM3A_IR |
| 100 | GPIO4_C3/UART2C_RX_U_3.0V | I/O | UP | UART2DBG_RX | Uart2 serial port data input, for AP debug | 3.0V | AK2 | GPIO4_C3/UART2C_RX |
| 102 | GPIO4_C4/UART2C_TX_U_3.0V | I/O | UP | UART2DBG_TX | Uart2 serial port data output , for AP debug | 3.0V | AJ4 | GPIO4_C4/UART2C_TX |
| 104 | GPIO2_A0/VOP_D0/CIF_D0/I2C2_SD A_U_3.0V | I/O | UP | GPIO2_B0/MIPI_PD N0_H | MIPI Camera0 enable | 3.0V | G31 | GPIO2_A0/VOP_D0/CIF_D0/I2C 2_SDA |
| 106 | GPIO2_A1/VOP_D1/CIF_D1/I2C2_SC L_U_3.0V | I/O | UP | GPIO2_A1/MIPI_PD N1_H | MIPI Camera1 enable | 3.0V | H25 | GPIO2_A1/VOP_D1/CIF_D1/I2C 2_SCL |
| 108 | GPIO2_A7/VOP_D7/CIF_D7/I2C7_SD A_U_3.0V | I/O | UP | EDP_HPD | EDP_DET Input | 3.0V | G30 | GPIO2_A7/VOP_D7/CIF_D7/I2C 7_SDA |
| 110 | GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C 7_SCL_U_3.0V | I/O | UP | WK2124_INT | WK2124_INT Input | 3.0V | H28 | GPIO2_B0/VOP_CLK/CIF_VSYNC /I2C7_SCL |
| 112 | GPIO2_A2/VOP_D2/CIF_D2_D_3.0V | I/O | DOWN | TP_INT | TP_INT Input | 3.0V | H30 | GPIO2_A2/VOP_D2/CIF_D2 |
| 114 | GPIO2_A3/VOP_D3/CIF_D3_D_3.0V | I/O | DOWN | AT18_RST | AT18_Reset Output (active low) | 3.0V | F28 | GPIO2_A3/VOP_D3/CIF_D3 |
| 116 | GPIO1_A2/ISPO_FLASHTRIGIN/ISPI _FLASHTRIGIN/TCPD_CC1_VCONN_EN D_3.0V | I/O | DOWN | WK2124_RST | WK2124_Reset Output (active low) | 3.0V | R26 | GPIO1_A2/ISPO_FLASHTRIGIN/ ISPI_FLASHTRIGIN/TCPD_CC1 _VCONN_EN |

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|-----|-----------------|-----|------|---------------|--|------|------|---------------|
| 118 | GPIO4_D5_D_3.0V | I/O | DOWN | LCD_RST | LCD panel reset output (active low) | 3.0V | AJ3 | GPIO4_D5 |
| 120 | GPIO4_D6_D_3.0V | I/O | DOWN | PCIE_RST | PCIE_Reset Output (active low) | 3.0V | AG4 | GPIO4_D6 |
| 122 | GPIO4_D3_D_3.0 | I/O | DOWN | GPIO4_D3_d | GPIO | 3.0V | AK3 | GPIO4_D3 |
| 124 | GND_10 | G | | GND | GND | | | |
| 126 | MIPI_TX0_D3P | 0 | | MIPI_TX0_D3P | MIPI-DSI0 differential lane 3 positive | 1.8V | AG9 | MIPI_TX0_D3P |
| 128 | MIPI_TX0_D3N | 0 | | MIPI_TX0_D3N | MIPI-DSI0 differential lane 3 negative | 1.8V | AH9 | MIPI_TX0_D3N |
| 130 | MIPI_TX0_D2P | 0 | | MIPI_TX0_D2P | MIPI-DSI0 differential lane 2 positive | 1.8V | AG11 | MIPI_TX0_D2P |
| 132 | MIPI_TX0_D2N | 0 | | MIPI_TX0_D2N | MIPI-DSI0 differential lane 2 negative | 1.8V | AH11 | MIPI_TX0_D2N |
| 134 | MIPI_TX0_CLKP | 0 | | MIPI_TX0_CLKP | MIPI-DSI0 differential clock lane positive | 1.8V | AG12 | MIPI_TX0_CLKP |
| 136 | MIPI_TX0_CLKN | 0 | | MIPI_TX0_CLKN | MIPI-DSI0 differential clock lane negative | 1.8V | AH12 | MIPI_TX0_CLKN |
| 138 | MIPI_TX0_D1P | 0 | | MIPI_TX0_D1P | MIPI-DSI0 differential lane 1 positive | 1.8V | AG14 | MIPI_TX0_D1P |
| 140 | MIPI_TX0_D1N | 0 | | MIPI_TX0_D1N | MIPI-DSI0 differential lane 1 negativ | 1.8V | AH14 | MIPI_TX0_D1N |
| 142 | MIPI_TX0_D0P | 0 | | MIPI_TX0_D0P | MIPI-DSI0 differential lane 0 positive | 1.8V | AG15 | MIPI_TX0_D0P |
| 144 | MIPI_TX0_D0N | 0 | | MIPI_TX0_D0N | MIPI-DSI0 differential lane 0 negativ | 1.8V | AH15 | MIPI_TX0_D0N |
| 146 | TYPEC1_DM | | | USB3_DM | TYPEC1 Data Minus port | | AH24 | TYPEC1_DN |
| 148 | TYPEC1_DP | | | USB3_DP | TYPEC1 Data Plus port | | AG24 | TYPEC1_DP |
| 150 | ADC_IN0 | I | | ADC_IN0 | ADC0 input, Core board interiorl pull up Resistor 10K | 1.8V | AG26 | ADC_IN0 |
| 152 | ADC_IN1 | I | | RECOVER | ADC0(recover_key) input, Core board interiorl pull up Resistor 10K | 1.8V | AH26 | ADC_IN1 |

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|-----|---|-----|------|-------------|--|--------|------|------------------------------------|
| 154 | ADC_IN2 | I | | LINE_IN_DET | ADC2 input, Core board interiorl pull up Resistor 10K | 1.8V | AG25 | ADC_IN2 |
| 156 | ADC_IN3 | I | | HP_DET | AD3C input, Core board interiorl pull up Resistor 10K | 1.8V | AG28 | ADC_IN3 |
| 158 | GPIO4_D2_D_3.0V | I/O | DOWN | PCIE_WAKE | AP wake up PCIE Output | 3.0V | AH3 | GPIO4_D2 |
| 160 | GPIO4_D0/PCIE_CLKREQNB_U_3.0V | I/O | UP | PCIE_CLKREQ | PCIE CLKREQN Output | 3.0V | AE6 | GPIO4_D0/PCIE_CLKREQNB |
| 162 | GPIO4_D1/DP_HOTPLUG_D_3.0V | I/O | DOWN | GPIO4_D1 | GPIO | 3.0V | AK4 | GPIO4_D1/DP_HOTPLUG |
| 164 | GND_12 | G | | GND | GND | | | |
| 166 | GPIO4_B1/SDMMC0_D1/UART2A_TX_U_3.0V | I/O | UP | SDMMC0_D1 | SDMMC0 data1 (TF-Card) | Note 2 | Y26 | GPIO4_B1/SDMMC0_D1/UART2A_TX |
| 168 | GPIO4_B0/SDMMC0_D0/UART2A_RX_U_3.0V | I/O | UP | SDMMC0_D0 | SDMMC0 data0 (TF-Card) | | Y27 | GPIO4_B0/SDMMC0_D0/UART2A_RX |
| 170 | GPIO4_B2/SDMMC0_D2/APJTAG_TCK_U_3.0V | I/O | UP | SDMMC0_D2 | SDMMC0 data2 (TF-Card) | | Y28 | GPIO4_B2/SDMMC0_D2/APJTAG_TCK |
| 172 | GPIO4_B5/SDMMC0_CMD/MCUJTAG_TMS_U_3.0V | I/O | UP | SDMMC0_CMD | SDMMC0 command output (TF-Card) | | V25 | GPIO4_B5/SDMMC0_CMD/MCUJTAG_TMS |
| 174 | GPIO4_B3/SDMMC0_D3/APJTAG_TMS_U_3.0V | I/O | UP | SDMMC0_D3 | SDMMC0 data3 (TF-Card) | | U27 | GPIO4_B3/SDMMC0_D3/APJTAG_TMS |
| 176 | GPIO4_B4/SDMMC0_CLKOUT/MUCJTAG_TCK_D_3.0V | I/O | DOWN | SDMMC0_CLK | SDMMC0 clock output (TF-Card) Core board internal series resistance 22p | | V29 | GPIO4_B4/SDMMC0_CLKOUT/MUCJTAG_TCK |

Note 2: Default is 3.0V; SDMMC0 1.8V (SDIO3.0 model)/3.0V (SDIO2.0 model) Auto

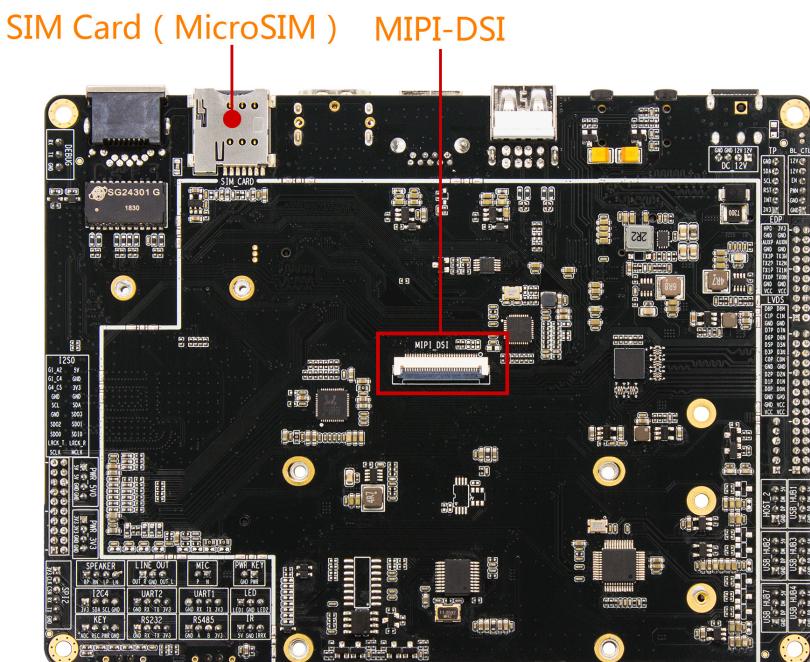
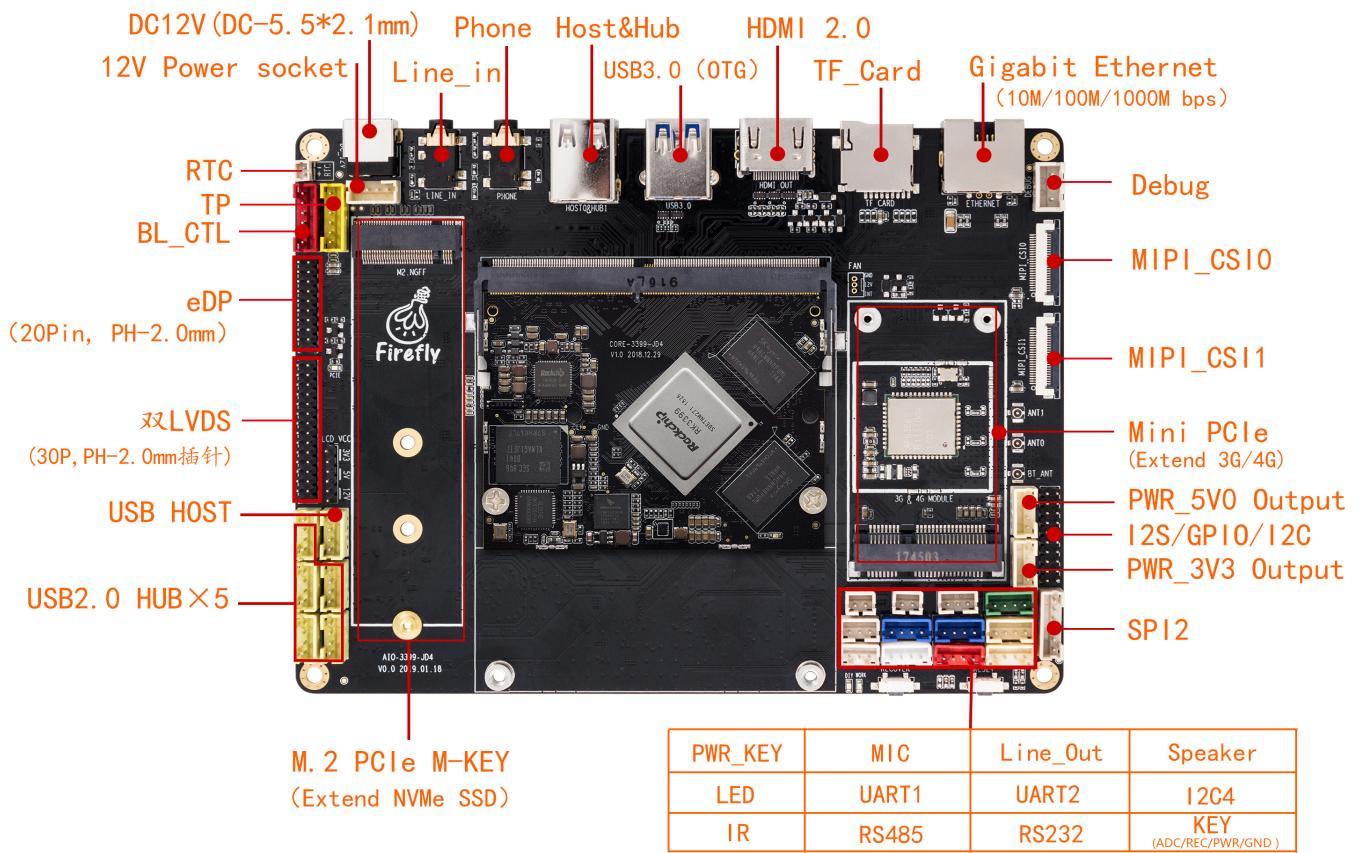
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|-----|--------------------------------------|-----|----|------------|---|------|-----|-------------------------------|
| 178 | GPIO0_A7/SDMMC0_DET_U_1.8V | I/O | UP | SDMMC0_DET | SDMMC0 detect input (active low) | 1.8V | V28 | GPIO0_A7/SDMMC0_DET |
| 180 | GND_16 | G | | GND | GND | | | |
| 182 | GPIO3_B5/MAC_MDIO/UART1_TX_U_3.3V | I/O | UP | MAC_MDIO | MAC management command and data | 3.3V | G26 | GPIO3_B5/MAC_MDIO/UART1_TX |
| 184 | GPIO3_B0/MAC_MDC/SPI0_CSN1_U_3.3V | I/O | UP | MAC_MDC | MAC management clock | 3.3V | E29 | GPIO3_B0/MAC_MDC/SPI0_CSN1 |
| 186 | GPIO3_C1/MAC_TXCLK/UART3_RTSN_U_3.3V | I/O | UP | PHY_TXCLK | MAC transmit clock Core board internal series resistance 22p | 3.3V | E28 | GPIO3_C1/MAC_TXCLK/UART3_RTSN |

| | | | | | | | | |
|-----|--|-----|------|-------------|--|------|-----|---------------------------------------|
| 188 | GPIO3_B6/MAC_RXCLK/UART3_RX_U_3.3V | I/O | UP | MAC_RXCLK | MAC receive clock | 3.3V | F25 | GPIO3_B6/MAC_RXCLK/UART3_RX |
| 190 | GND_21 | G | | GND | GND | | | |
| 192 | GPIO3_B3/MAC_CLK/I2C5_SCL_U_3.3V | I/O | UP | MAC_CLK | MAC reference clock output , I2C serial port 5, need external pull-up Core board internal series resistance 22R | 3.3V | G24 | GPIO3_B3/MAC_CLK/I2C5_SCL |
| 194 | GPIO3_A7/MAC_RXD1/SPI0_CSNO_U_3.3V | I/O | UP | MAC_RXD1 | MAC receive data | 3.3V | F27 | GPIO3_A7/MAC_RXD1/SPI0_CSNO |
| 196 | GPIO3_A3/MAC_RXD3/SPI4_CSNO_U_3.3V | I/O | UP | MAC_RXD3 | MAC receive data | 3.3V | E25 | GPIO3_A3/MAC_RXD3/SPI4_CSNO |
| 198 | GPIO3_A6/MAC_RXD0/SPI0_CLK_U_3.3V | I/O | UP | MAC_RXD0 | MAC receive data | 3.3V | E26 | GPIO3_A6/MAC_RXD0/SPI0_CLK |
| 200 | GPIO3_A2/MAC_RXD2/SPI4_CLK_U_3.3V | I/O | UP | MAC_RXD2 | MAC receive data | 3.3V | E30 | GPIO3_A2/MAC_RXD2/SPI4_CLK |
| 202 | GPIO3_B1/MAC_RXDV_D_3.3V | I/O | DOWN | MAC_RXDV | MAC receive data valid | 3.3V | C27 | GPIO3_B1/MAC_RXDV |
| 204 | GPIO3_A4/MAC_TXD0/SPI0_RXD_D_3.3V | I/O | DOWN | PHY_TXD0 | MAC transmit data Core board internal series resistance 22p | 3.3V | D26 | GPIO3_A4/MAC_TXD0/SPI0_RXD |
| 206 | GPIO3_A0/MAC_TXD2/SPI4_RXD_D_3.3V | I/O | DOWN | PHY_TXD2 | MAC transmit data Core board internal series resistance 22R | 3.3V | F24 | GPIO3_A0/MAC_TXD2/SPI4_RXD |
| 208 | GPIO3_A1/MAC_TXD3/SPI4_TXD_D_3.3V | I/O | DOWN | PHY_TXD3 | MAC transmit data Core board internal series resistance 22R | 3.3V | H23 | GPIO3_A1/MAC_TXD3/SPI4_TXD |
| 210 | GPIO3_A5/MAC_TXD1/SPI0_TXD_D_3.3V | I/O | DOWN | PHY_TXD1 | MAC transmit data Core board internal series resistance 22p | 3.3V | G23 | GPIO3_A5/MAC_TXD1/SPI0_TXD |
| 212 | GPIO3_B4/MAC_TXEN/UART1_RX_U_3.3V | I/O | UP | PHY_TXEN | MAC transmit enable Core board internal series resistance 22R | 3.3V | H22 | GPIO3_B4/MAC_TXEN/UART1_RX |
| 214 | GPIO3_B2/MAC_RXER/I2C5_SDA_U_3.3V | I/O | UP | FAN_CTL | PHY interrupt input, I2C serial port 5, need external pull-up Core board internal series resistance 22R | 3.3V | F23 | GPIO3_B2/MAC_RXER/I2C5_SDA |
| 216 | GPIO3_B7/MAC_CRS/CIF_CLKOUTB/UART3_TX_U_3.3V | I/O | UP | PHY_RST | phy reset output(active low) | 3.3V | B27 | GPIO3_B7/MAC_CRS/UART3_TX/CIF_CLKOUTB |
| 218 | RESET_KEY | | | RESET_KEY | system reset signal Input, External connection Reset key, active low | | | |
| 220 | PMIC_EXT_EN | | | PMIC_EXT_EN | External Power enable output, Voltage 5V | | | |

| | | | | | | | | |
|-----|-----------------|---|--|---------------|---|----------|--|--|
| 222 | GND_26 | G | | GND | GND | | | |
| 224 | VDDIO_WL_2 | P | | VDDIO_WL | 1.8V output, Max current 1A to WIFI_IO | 1.8V_OUT | | |
| 226 | VCC_3V3_SO_2 | P | | VCC_LAN | 3.3V output, Max current 300mA TO LAN | 3.3V_OUT | | |
| 228 | VCCA1V8_CODEC_2 | P | | VCCA1V8_CODEC | 1.8V output, Max current 150mA to Codec | 1.8V_OUT | | |
| 230 | VCCA3V0_CODEC_2 | P | | VCCA3V0_CODEC | 3.0V output, Max current 300mA to Codec | 3.0V_OUT | | |
| 232 | VCC_RTC | P | | VCC_RTC | 5.0V input, Max current 50mA | 5.0V_IN | | |
| 234 | VCC3V3_SYS_2 | P | | VCC3V3_SYS | 3.3V output, Max current 1A | 3.3V_OUT | | |
| 236 | NC_1 | | | | | | | |
| 238 | NC_3 | | | | | | | |
| 240 | NC_5 | | | | | | | |
| 242 | NC_7 | | | | | | | |
| 244 | GND_27 | G | | GND | Power ground | | | |
| 246 | GND_29 | G | | GND | Power ground | | | |
| 248 | GND_31 | G | | GND | Power ground | | | |
| 250 | GND_33 | G | | GND | Power ground | | | |
| 252 | VCC_SYS_2 | P | | VCC5V0_SYS | Input Voltage 4.8V-5.5V | 5.0V_IN | | |
| 254 | VCC_SYS_4 | P | | VCC5V0_SYS | Input Voltage 4.8V-5.5V | 5.0V_IN | | |
| 256 | VCC_SYS_6 | P | | VCC5V0_SYS | Input Voltage 4.8V-5.5V | 5.0V_IN | | |

| | | | | | | | | |
|-----|------------|---|--|------------|-------------------------|---------|--|--|
| 258 | VCC_SYS_8 | P | | VCC5V0_SYS | Input Voltage 4.8V-5.5V | 5.0V_IN | | |
| 260 | VCC_SYS_10 | P | | VCC5V0_SYS | Input Voltage 4.8V-5.5V | 5.0V_IN | | |

5. Industry Backplane





Appendix

1. Company Profile

T-Chip Intelligent Technology Co., Ltd. was founded in 2005. It has more than 10 years of research and development experience in scientific and technological products, has 6 invention patents and more than 30 computer software copyrights, and is a national high-tech enterprise. We focus on the research and development, design, production and sales of open source intelligent hardware, internet of things and digital audio products, and provide the overall solution for intelligent hardware products meanwhile.



Firefly is a brand owned by T-chip Technology. It operates open source products, open source communities and online stores. It has a large number of enterprise users and developer users, and its products are well received by users. Firefly open source products include open source boards, core boards, industry mainboards, etc. The open-source board series is the recommended board card by chip original factory Rockchip and obtain the support of native SDK. The core boards and industrial mainboards are widely used in commercial displays, advertisement integrated machines, intelligent POS, face recognition terminals, internet of things, intelligent cities, etc. At present, there are more than 100,000 users, including over 2,000 enterprise users. And well-known users include ARM, Google, Baidu, Tencent, Alibaba, etc.

Firefly team has more than 60 research and development members and has the research and development capabilities in schematic design, PCB layout, mainboard production, embedded development, system development, application program development, etc., which accelerates the research and development process for many technology entrepreneurs and start-ups, and provides professional technical services..

" Make technology more simple, Make life more intelligent " is the idea of Firefly team. We hope to make the research and development of various technology products efficient and simple, and let intelligent technology integrate in our lives through the open source products and technical services of Firefly.



2. Source code acquisition

Please visit the official website : ([please click here](#))

The screenshot shows a web browser window with the Firefly logo and slogan at the top. The URL in the address bar is en.t-firefly.com/doc/download/page/id/31.html. The page content features a large dark background with the word 'Download' in white. Below it, a sub-headline reads 'Complete SDK is free of charge, complete software and hardware data'. A red box highlights the 'Download' button in the navigation menu.

3. Contact Us

| | | |
|--|--------------------------|---|
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