Neha Tiwari
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SUMMARY

Strategic and execution-driven engineering professional with 6+ years of experience managing complex silicon validation programs at Intel and Qualcomm. Proven ability to lead cross-functional teams through SoC bring-up, subsystem debug, and power management across simulation, FPGA, and silicon platforms. Recognized through multiple awards (DRAs, Superstar, QPB+) for delivering high-impact outcomes and accelerating time-to-market in fast-paced development cycles. Demonstrated focus on innovation and process automation, having developed reusable frameworks for concurrency and fuse validation that reduced debug time and manual effort significantly. Published multiple peer-reviewed technical papers on concurrency, debug, and fuse validation, contributing to internal IP development and knowledge sharing. Adept at breaking down complex technical efforts into actionable execution plans, managing stakeholder expectations, driving continuous improvement, and ensuring quality delivery. Proficient in JIRA, Confluence, Tableau, and Power BI for agile project tracking and executive reporting. Currently pursuing an MS in Business Analytics at ASU (Dec 2025) to deepen expertise in AI/ML, data-driven decision-making, and product-led innovation.

PROFESSIONAL EXPERIENCE

Intel Technology Pvt. Ltd. — Bangalore, India
System Software Validation Engineer, Client Computing Group | Mar 2022 – Nov 2024

- Owned power management validation for Intel SoCs, driving on-time milestone delivery and identifying critical issues that shaped design improvements and earned recognition through the Superstar Award and QPB+.
- Coordinated planning, execution, debug, and issue triage across cross-functional teams, driving alignment among power, thermal, BIOS, and OS domains to achieve zero customer escapes.
- Served as concurrency stress tool SPOC; enhanced tool capability and validation coverage, reducing debug cycles and accelerating readiness for production release.
- Debugged low-power entry/exit sequences involving CPU, GPU, and NPU interactions with system thermal and power domains.
- Co-authored *"Improved Quality and Stability of Next-Gen AI-PC Using Concurrency Validation Framework,"* presented at DTTC'24, showcasing how the framework identified critical NPU bugs.

Qualcomm — Bangalore, India
Senior Validation Engineer, ConVex Group | May 2021 – Feb 2022

- Developed and executed comprehensive validation plans for value- and premium-tier mobile SoCs, ensuring reliability and peak performance.
- Engineered comprehensive test plans and executed focus and concurrency testing, optimizing performance and reliability.
- Designed a groundbreaking system-level debug flow for Premier Tier products, enhancing test efficiency and coverage across multiple platforms (emulation, simulation, silicon).
- Presented research paper *"A Novel Method to Maintain ConVex in Lockstep Between a Parent and Derivative Program"* at the 2021 Qualcomm Annual Summit.

Intel Technology Pvt. Ltd. — Bangalore, India
System Validation Engineer, Data Centric Group | May 2018 – May 2021

- Led concurrency validation program for Intel QAT 2.0 and 3.0 generations; coordinated test planning, execution, and triage across concurrency, compression, cryptography, fuses, and debug module owners, ensuring product integrity and performance.
- Delivered end-to-end validation ownership: created, reviewed, and executed test plans/cases for FPGA, Simics, and silicon platforms; drove debug, triage, and final issue disposition from pre-silicon through post-silicon phases, aligning with product requirements.
- Demonstrated proficiency in debugging, unit testing, and version control using Git, enabling efficient issue resolution.

- Published technical research papers: *"Enhanced Data Security for Intel Server SoC"* (DTTC 2019) and *"End-to-End Functional Fuse Validation Automation for QAT IP"* (DCG Innovation Summit 2019).

PROJECTS

- **AI Tutor** – 1st Place, ASU × NVIDIA Hackathon'2025 : Built "M⁶ AI Tutor"- a GPU-accelerated, semi-Socratic learning platform using RAG and LLMs to teach data science interactively. Led model selection, optimization, and tutor pipeline integration (https://www.youtube.com/watch?v=7OfkW2ry0wI).
- **GPT Workload Optimization**: Designed MILP model (Gurobi + Excel Solver) to optimize GPT backend routing; achieved cost-latency balance in AI workloads for simulated data.
- **Employee Attrition Prediction:** Built and evaluated 10+ ML models (Logistic Regression, Decision Tree, Naïve Bayes, SVM, MLP, RF, Gradient Boosting, XGBoost, KNN, Ensemble, Clustering) to predict attrition using IBM HR dataset. Identified key churn drivers and achieved >90% accuracy, AUC, and recall.
- **Proposal Process Redesign**: Applied Lean Six Sigma, FMEA, and RPA to reduce proposal creation DPMO by 60% and improve sigma from 2.08 to ~3.5 in a service process case study.

SKILLS & TOOLS

- **Pre/Post-Silicon Validation**:
  Power Management, Concurrency, DMA Engines, Cryptography, Compression Pipelines, Fuse Automation, SoC Boot & Reset Flows, PCIe, DMA & DDR validation, Clock/Power Gating, Coverage Analysis
- **Platforms & Environments**:
  Silicon, FPGA, Simics, ZeBu Emulation, Veloce
- **Debug & Tools**:
  Trace32, JTAG, Oscilloscopes, Logic Analyzers, UART Logging, UEFI Shell, BIOS Logs, Git
- **Programming & Simulation**:
  Python (NumPy, Pandas, Scikit-Learn), C/C++, SQL, MATLAB, HTML
- **Analytics & Optimization**:
  Gurobi, Excel Solver, Tableau, Power BI, Linear Programming, Descriptive, Predictive and Prescriptive Analytics
- **Database & Querying**:
  Relational DBMS, SQL-based query design, data integrity and normalization
- **AI/ML Exposure**:
  Retrieval-Augmented Generation (RAG), LLM Integration, cuDF, PyTorch
- **Project & Risk Management**:
  JIRA, Agile, Risk Tracking, Lean Six Sigma (DMAIC), FMEA, Root Cause Analysis (RCA)

EDUCATION

W. P. Carey School of Business, Arizona State University — Tempe, AZ
MS, Business Analytics, Big Data (Expected Dec 2025)

National Institute of Technology — Goa, India
M. Tech, Computer Science (May 2019)

Shaheed Rajguru College of Applied Sciences, University of Delhi — Delhi, India
B. Tech, Computer Science (May 2017)

RESEARCH PUBLICATIONS

- Compression with Authenticated Encryption for Enhanced Security on Data Centric Products | IEEE Conference Publication
- Review article Brain computer interface: A comprehensive survey
- Innovation Study on Gadget Addiction (https://www.rajgurucollege.com/Innovation-Projects)