L-WEA2012

Product Preview

400x400 TDDI for IOT/Wearable

This document contains information on a product under development. Solomon Systech reserves the right to change or discontinue this product without notice.



APPENDIX: IC REVISION HISTORY OF L-WEA2012 SPECIFICATION

Version	Change Items	Effective Date
0.10	1st Release	20-Jan-2021
0.20	Section 2, for MIPI section, removed Video mode	05-Feb-2021
0.30	Section 5, added die floor plan Section 6, added SPI/DSPI/QSPI timing, RAM block description Section 8, updated un-used pin setting Section 15, updated Power on/off sequence	29-Mar-2021



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1 GENERAL DESCRIPTION

L-WEA2012 is a display driver supporting a-Si panel up to 400RGB x 400 resolution with 24bit color depth. The IC has integrated with RAM and self-cap incell touch controller.

2 FEATURES

Display

- IOT solution for TFT display
- Support various resolution, from 240RGB x 240 to 400RGB x 400
- Display color modes: 16.7M color (24bit 8R:8G:8B)
- Support Column/1dot/2dot inversion
- Dual Gate GIP driving

Touch

- Low Power Touch Standby mode
- Support max 49 touch nodes sensing signal
- Support Vblank touch sensing mode, up to 60Hz report rate
- I2C/SPI for communication with Host (AP)
- 8 channels virtual touch key

Interface

- MIPI
 - MIPI lane speed up to 500Mbps per lane
 - MIPI DSI (version 1.1) with D-PHY (version 1.1)
 - Support command mode
 - Command set compliant with MIPI DCS (version 1.4)
 - 1 data lane and 1 clock lane
- SPI
- Support SPI/DSPI/QSPI
- 1/2/4 data lane and 1 clock lane
- Data rate up to 40Mbps

RAM

• Embedded 80000 bytes RAM (400x400/2)

Power

- Power Supply
 - VDDIO: 1.65V 3.3V
 - VCI: 2.5V ~ 3.3V
- Max VGH VGL: 28Vp-p
- Low Current Sleep Mode and 8-color display mode for power saving

Function

- Programmable Gamma Correction Curve
- Programmable VCOM (-0.2V ~ -2.7V)
- CABC dynamics backlight control with PWM output

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3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	Package Form	Remark
L-WEA2012Z	COG	



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4 BLOCK DIAGRAM

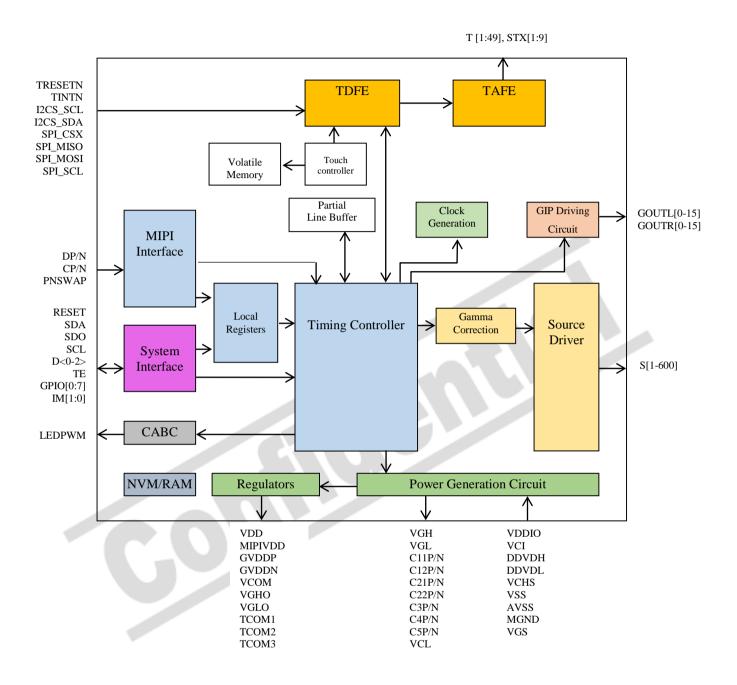
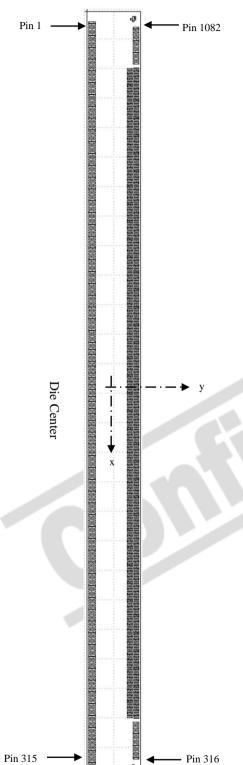


Figure 4-1: L-WEA2012 Block Diagram

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5 DIE PAD FLOOR PLAN



Alignment Mark (center)	X (um)	Y (um)
Left	-6333.8	330.8
Right	6333.8	330.8

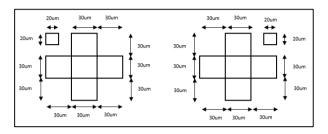


Figure 5-1: Alignment Marks

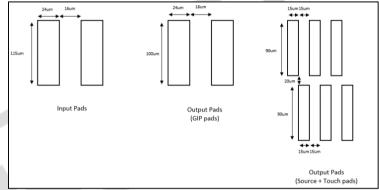


Figure 5-2: Pad Arrangement (die face-up, all in um)

Table 5-1: Die Information

Die Size	13004um x 998um (w/ scribe line)
Die Thickness	200um
Typical Bump Height	9 um
Bump Co-planarity (within die)	≤ 2 um
Bump Size 1	24 x 115 μm ² (pin 1-315)
Pad Pitch 1	40 μm
Bump Size 2	24 x 100 μm ² (pin 316-331,1067-1082)
Pad Pitch 2	40 um
Bump Size 3	15 x 90 μm ² (pin 332-1066)
Pad Pitch 3	30 um, 2 layers stagger
Bump Hardness	90 +/-20 Hv

Figure 5-3: L-WEA2012 Die Pad Floor Plan (die face up)

Note

- (1) Coordinates are referenced to center of the chip.
- (2) Coordinate units and size of all alignment marks are in um.
- (3) All alignment keys do not contain gold bump.

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6 BLOCK FUNCTION DESCRIPTION

6.1 MIPI Interface

L-WEA2012 supports MIPI DSI interface which can be used to transmit display data. It can also be used to program the L-WEA2012 registers.

The MIPI DPHY in L-WEA2012 supports flexible data and clock lane polarity swap. It is controlled by hardware pin. Please see the diagram below for possible arrangement.

Table 6-1: MIPI Bus Configuration

Physical Pin	DP	DN	CP	CN
PNSWAP	Functional Outpu		l Output	
1	DP	DN	CP	CN
0	DN	DP	CN	CP

6.2 System Interface

 $L ext{-WEA2012}$ supports SPI interface which can be used to transmit display data. It can also be used to program the $L ext{-WEA2012}$ registers.

SPI/DSPI/QSPI are supported.

SPI interface or MIPI interface is selected by hardwire pins IM[0:1].

Table 6-2: Interface Selection

IM[1]	IM[0]	Interface	Used pins
0	0 Reserved		
0	1	4-wire SPI (0xE4=0)	PNSWAP(CSX), TEST_I[2](DCX), SCL, SDA
0	1	4-wire DSPI (0xE4=1)	PNSWAP(CSX), TEST_I[2](DCX), SCL, SDA, D[0]
1	0	MIPI	PNSWAP, CP, CN, DP, DN
1	1 _	3-wire SPI	PNSWAP(CSX), TEST_I[2](DCX)=GND, SCL, SDA
1	1	QSPI	PNSWAP(CSX), TEST_I[2](DCX)=VDDIO, SCL, SDA, D[0:2]

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6.2.1 4-wire SPI Timing

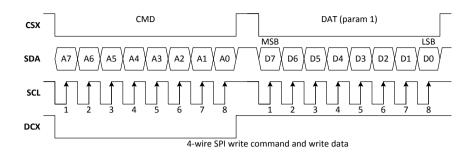


Figure 6-1: 4-wire SPI write command and write data

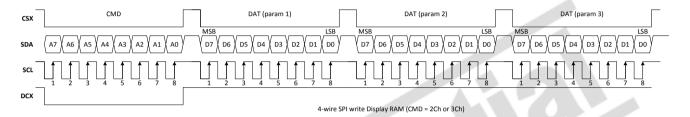


Figure 6-2: 4-wire SPI write RAM data (Note: for each time using 0x2C or 0x3C cmd to write RAM data, please write 4 pixels data or more.)

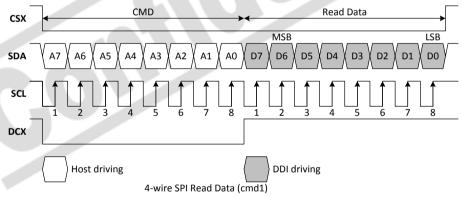


Figure 6-3: 4-wire SPI Read

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6.2.2 4-wire DSPI Timing

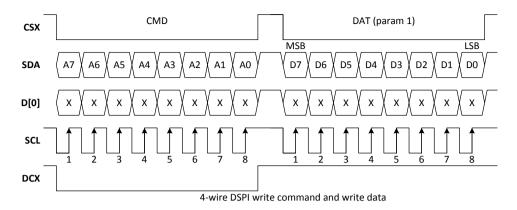


Figure 6-4: 4-wire DSPI write command and write data

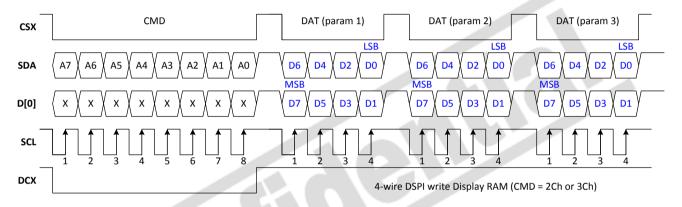
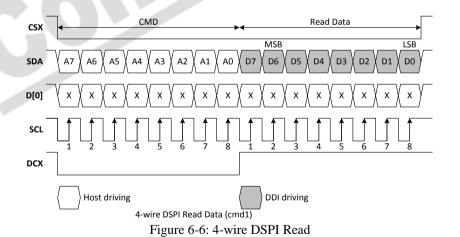


Figure 6-5: 4-wire DSPI write RAM data

(Note: for each time using 0x2C or 0x3C cmd to write RAM data, please write 4 pixels data or more.)



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6.2.3 3-wire SPI Timing

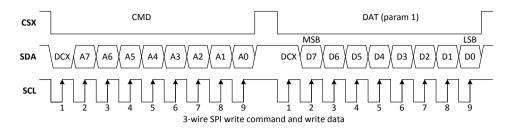


Figure 6-7: 3-wire SPI write command and write data

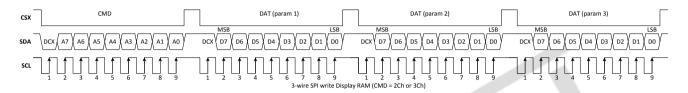
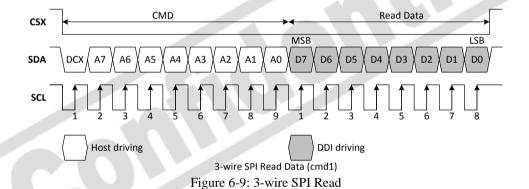


Figure 6-8: 3-wire SPI write RAM data (Note: for each time using 0x2C or 0x3C cmd to write RAM data, please write 4 pixels data or more.)



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6.2.4 QSPI Timing

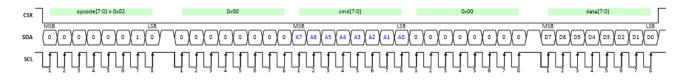


Figure 6-10: QSPI write command and write data (1 data lane)

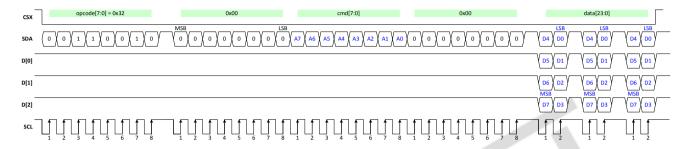


Figure 6-11: QSPI write command and write data (4 data lanes) (Note: for each time using 0x2C or 0x3C cmd to write RAM data, please write 4 pixels data or more.)



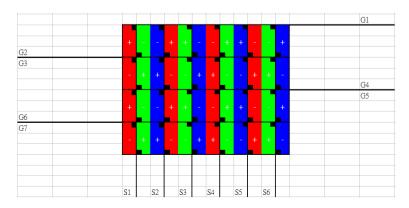
Figure 6-12: QSPI Read

6.3 Regulator / Power Generation Circuit

This block generates the voltage of VGH, VGL, VCOM etc which are necessary for operating L-WEA2012.

6.4 GIP Driving Circuits

This block generates the controls signals that are used in the Gate-Driver In Panel (GIP). Dual gate driving is supported.



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6.5 RAM

There are 80000 bytes RAM (400x400/2). RAM must be written as 1 pixel (3 bytes for 16.7M/262k color format, 2 bytes for 65k color format). Number of pixel must be in multiple of 4.

Use 0x2C and 0x3C to write whole frame data. (Please do not only use 0x2C to write whole frame data.) For each time using 0x2C or 0x3C command to write RAM data, please write 4 pixels data or more.

Read RAM is not supported.

6.6 Non-Volatile Memory (NVM)

NVM is available. It has a reserved area for below purpose. Each one can be programmed.

- Vendor ID
- VCOM tuning
- Full Gamma setting

6.7 Clock Generation Circuit

L-WEA2012 supports generating operational clock by itself through local oscillator and PLL.

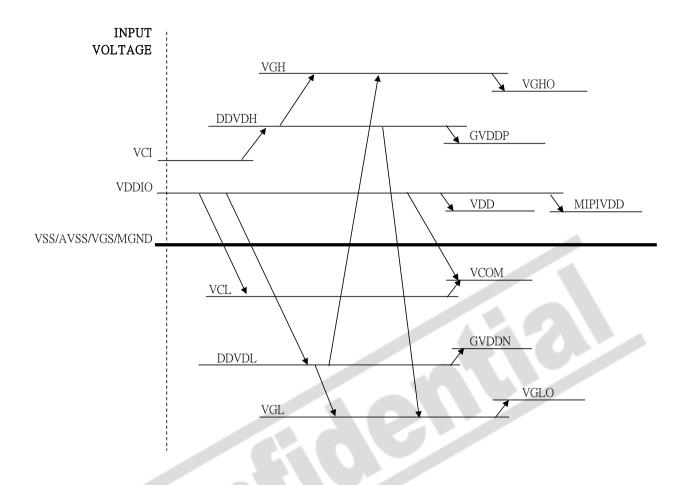
6.8 Touch

L-WEA2012 has integrated the Touch Module Controller (TMC), Touch Digital Front End (TDFE), and Touch Analog Front End (TAFE).

TMC is able to process all the raw touch data and generate the final touch location and communicate with the AP.

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7 POWER SCHEME



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8 PIN DESCRIPTIONS

Key:

I = Input

O =Output

IO = Bi-directional (input/output)

P = Power pin

GIP = Gate In Panel

BLU = Back Light Unit

8.1 Power Pins

Table 8-1: Power Supply Pins

Name	Type	Connect to	Function	Description	When not in use
VDDIO	P	Power Supply	Power supply for logic I/O	Power Supply for logic I/O - Connect to voltage source between 1.65V to 3.3V	-
VCI	P	Power Supply	Power supply for Analog	Power supply for Power Supply for analog circuit	
AVSS	P	GND	Ground of the Power Supply Analog circuit ground		-
VSS	P	GND	Ground of the Power Supply System ground pin		
MGND	P	GND	Ground of MIPI logic	MIPI analog circuit ground pin	-
VGS	P	GND	Reference Voltage	VGS is the ground reference voltage for gamma circuit.	-

Table 8-2: Power Generation / Regulation Pins

Name	Туре	Connect to	Function	Description	When not in use
VCOM	O	LCD	LCD Driving Voltage	Supply voltage to the common electrode of TFT panel	-
VGH	I/O	Stabilizing Capacitor	LCD Driving Voltage	A positive power output pin for gate driver	-
VGL	I/O	Stabilizing Capacitor	LCD Driving Voltage	A negative power output pin for gate driver	-
VGHO	О	Stabilizing Capacitor	LCD Driving Voltage	A regulated positive power output pin for gate driver	-
VGLO	О	Stabilizing Capacitor	LCD Driving Voltage	A regulated negative power output pin for gate driver	-
DDVDH	0	Stabilizing Capacitor	LCD Driving Voltage	Positive power supply for LCD driving	-
DDVDL	0	Stabilizing Capacitor	LCD Driving Voltage	Positive power supply for LCD driving	-
VCL	О	Stabilizing Capacitor	LCD Driving Voltage	A negative power output pin for driver IC internal circuit.	-
GVDDP	О	Stabilizing Capacitor	Reference Voltage	VREG1OUT is a positive source driver grayscale reference voltage	-
GVDDN	О	Stabilizing Capacitor	Reference Voltage	VREG2OUT is a negative source driver grayscale reference voltage	-
MIPIVDD	0	Stabilizing Capacitor	Power supply for MIPI circuits	Regulator output that needed to be connected with stabilizing capacitor for MIPI block	-
VDD	О	Stabilizing Capacitor	Power supply for logic circuits	Power Supply for logic circuits	-
C21N, C21P	I/O	Step-up capacitor	Booster Circuit	Connect booster capacitors to generate DDVDL.	Open
C22N, C22P	I/O	Step-up capacitor	Booster Circuit	Connect booster capacitors to generate DDVDL	Open
C11N, C11P	I/O	Step-up capacitor	Booster Circuit	Connect booster capacitors to generate DDVDH	Open
C12N, C12P	I/O	Step-up capacitor	Booster Circuit	Connect booster capacitors to generate DDVDH	Open
C3N, C3P	I/O	Step-up capacitor	Booster Circuit	Connect booster capacitors to generate VCL	Open

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Name	Туре	Connect to	Function	Description	When not in use
C4N, C4P	I/O	Step-up capacitor	Booster Circuit	Connect booster capacitors to generate VGH	Open
C5N, C5P	I/O	Step-up capacitor	Booster Circuit	Connect booster capacitors to generate VGL	Open
TCOM1	О	Stabilizing Capacitor	Touch Driving Voltage	Used for touch application	Open
TCOM2	О	Stabilizing Capacitor	Touch Driving Voltage	Used for touch application	Open
TCOM3	О	Stabilizing Capacitor	Touch Driving Voltage	Used for touch application	Open

8.2 Interfaces Logic Pins

Table 8-3: Interfaces Logic Pins

Name	Туре	Connect to	Function	Description	When not in use
RESET	I	MPU	System Reset	System reset pin. (active low)	VDDIO
TE	0	MPU	Logic Control	Frame head pulse signal. Utilize this signal when synchronizing RAM data write operations.	Open
LED_PWM	О	BLU	-	BLU PWM signal	Open
IM[0:1]	I	MPU		IM[1] IM[0] Interface 0 0 Reserved 0 1 4-wire SPI (0xE4=0) 0 1 4-wire DSPI (0xE4=1) 1 0 MIPI 1 1 3-wire SPI (DCX=GND) 1 1 QSPI (DCX=VDDIO)	

8.3 Output Driver Pins

Table 8-4: Output Driver Pins

Name	Туре	Connect to	Function	Description	When not in use
GOUTL[0-15] GOUTR[0-15]	0	LCD	GIP Control Signals	These pins are used for GIP control signal. Unused pins should leave open	Open
S[1-600]	О	LCD	LCD Driving Signals	Source driver output pins	Open

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8.4 MIPI Interface

Table 8-5: MIPI Interfaces Pins

Name	Туре	Connect to	Function	Description	When not in use
DP	I/O		MIPI differential	Positive polarity of low voltage differential data signal	Open/VSS
DN	1/0	MIPI Interface	Data Pair	Negative polarity of low voltage differential data signal	Open/VSS
CP	I	Signal	MIPI	Positive polarity of low voltage differential clock signal	Open/VSS
CN	I		differential Clock Pair	Negative polarity of low voltage differential clock signal	Open/VSS
PNSWAP	I	MPU	Logic Control	PNSWAP polarity swap of MIPI signal	VDDIO

8.5 SPI Interface

Table 8-6: SPI Interfaces Pins

Name	Туре	Connect to	Function	Description	When not in use
SCL	I		SPI	SPI clock signal	VSS
SDA	I	MPU	SPI	SPI data signal	VSS
D[0:2]	I		SPI	SPI data signal	VSS

8.6 Touch Interface

Table 8-7: Touch Interfaces Pins

Name	Type	Connect to	Function	Description	When not in use
TRESETN	I	MPU	Touch reset	Reset signal for touch circuit	VSS
SPI_CSX	I	Flash/MPU	SPI	SPI chip selection pin	VSS
SPI_MISO	I	Flash/MPU	SPI	SPI Data Output pin	VSS
SPI_MOSI	О	Flash/MPU	SPI	SPI Data Input pin	Open
SPI_SCL	I	Flash/MPU	SPI	SPI Clock pin	VSS
I2CS_SDA	I	MPU	I2C	Serial data pin of I2C interface for touch circuit	VSS
I2CS_SCL	I	MPU	I2C	Serial clock pin of I2C interface for touch circuit	VSS
TINTN	I	MPU	Touch interrupt	Interrupt signal for touch circuit	VSS
STX[1:9]	0	LCD	Touch control signal	Touch key channels	Open
T[1-49]	I/O	LCD	Touch control signal/VCOM	Touch channels/VCOM	Open

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8.7 Other Pins

Table 8-8: Other Pins

Name	Туре	Connect to	Function	Description	When not in use
DBIST	I	-	-	Test pin	VSS
GPO[0:7]	I/O	-	-	Test pin	Open
CL	О	-	-	Test pin	Open
VCOM_OPT[0:1]	О			Test pin	Open
DUMMY	-	-	-	Dummy pin	Open
TEST_I[0:2]	I			Test pin	VSS



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9 MAXIMUM RATINGS

Table 9-1: Maximum Rating (Voltage reference to VSS)

Symbol	Parameter	Pin	Value	Unit
VDDIO	Supply Voltage	VDDIO	-0.3 to +3.3	V
VCI	Supply Voltage	VCI	-0.3 to +3.3	V
VGH-VGL	Gate Driver Supply Voltage	-	-0.3 to +28.0	V
DP, DN CP,CN	Differential Input Voltage	-	1.65	V
T_{A}	Operating Temperature	-	-40 to +85	°C
${ m T_{STG}}$	Storage Temperature	-	-55 to +125	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

Display driver IC is a UV sensitive device; so do not let the front or backside of an IC under UV exposure. An appropriate coating, module design and assembly methods to adequately protect the IC from UV are required for application.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

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10 AC CHARACTERISTICS

10.1 MIPI CHARACTERISTICS

Table 10-1: MIPI DPHY Characteristics

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
		MIPI HS Receiver				
F_{SPEED}	MIPI Data Lane Speed	Please see Note 1	400		500	Mbps
UI	Unit Interval	Please see Note 2	2			ns
T_{SETUP}	Data to Clock Setup Time	Please see Note 3	0.2			UI
T_{HOLD}	Data to Clock Hold Time	Please see Note 3	0.2			UI
T_{SKEW}	Data to Clock Skew	Please see Note 4	-0.2			UI
		MIPI LP Receiver				
$T_{ m LPX}$	LP transmission pulse width		50			ns

Note 1: The MIPI data lane speed depends on the number of data lanes, the bit per pixel (bpp) value of the display data and the operation mode (command mode).

Note 2: $UI = 1 / F_{SPEED}$

Note 3: Total setup and hold window for receiver of 0.3*UI when max rate less than 1Gbps.

Note 4: Total silicon and package skew delay budget of 0.3*UI when max rate less than 1Gbps.

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Table 10-2: Global Operation Timing Parameters

Symbol	Parameter	Min	Тур	Max	Unit
T _{CLK-POST}	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode. Interval is defined as the period from the end of Ths-trail to the beginning of	60ns + 52UI			ns
T _{CLK-PRE}	TCLK-TRAIL. Minimum time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8			UI
T _{CLK-PREPARE}	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
T _{CLK-SETTLE}	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL.MAX.			38	ns
Tclk-trail	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	1		ns
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	IV		ns
Td-term-en	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VILMAX.			35ns + 4UI	ns
Теот	Transmitted time interval from the start of Ths-trail or Tclktrail, to the start of the LP-11 state following a HS burst.	1		105ns + n*12UI	ns
Ths-exit	Time that the transmitter drives LP-11 following a HS burst.	100			ns
T _{HS-PREPARE}	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4UI		85ns + 6UI	ns
$T_{\text{HS-PREPARE}} + \\ T_{\text{HS-ZERO}}$	Ths-prepare + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10UI			ns
Ths-zero	Time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence	100			ns
Ths-settle	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of Theorem.	85ns + 6UI		145ns + 10UI	ns
Ths-skip	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
Ths-trail	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	100			ns
Tlpx	Transmitted length of any Low-Power state period		100		ns
Ratio T _{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3		3/2	
T _{TA-GET}	Time to drive LP-00 by new TX		5TLPX		
T_{TA-GO}	Time to drive LP-00 after Turnaround Request		4TLPX		
T _{TA-SURE}	Time-out before new TX side starts driving	1*TLPX		2*TLPX	
$T_{WAKEUP} \\$	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms

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Note: Please refer to the diagram below for the definition of the MIPI parameter.

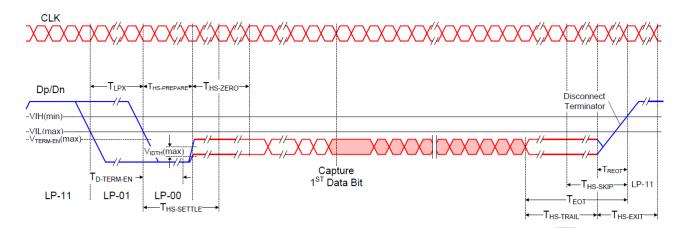


Figure 10-1: High-Speed Data Transmission in Bursts

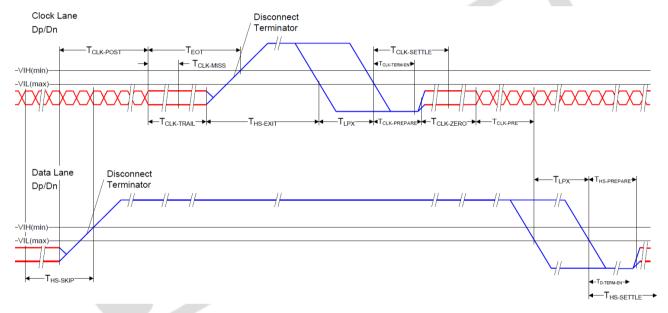


Figure 10-2: Switching the Clock Lane between Clock Transmission and Low Power Mode

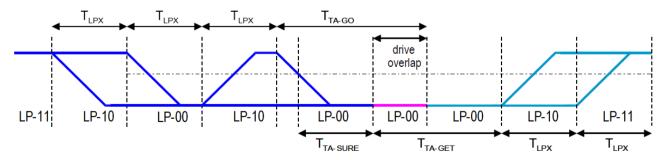


Figure 10-3: MIPI BUS Turnaround Procedure

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11 DC CHARACTERISTICS

Table 11-1: DC Characteristics

(Unless otherwise specified, Voltage Referenced to VSS, TA = -40 to 85 °C)

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
Power Supply	•		•		•	•
VDDIO	Power Supply for Logic circuit	-	1.65	-	3.30	V
VCI	Power Supply for Analog circuit		2.5		3.30	V
Digital IO Inp	ut/Output		•		•	•
V_{IH}	Logic High Level Input voltage	-	0.8 * VDDIO	-	VDDIO	V
V_{IL}	Logic Low Level Input voltage	-	VSS	-	0.2 * VDDIO	V
Vон	Logic High Level Output Voltage	Iout= 1mA	0.9 * VDDIO	-	VDDIO	V
V_{OL}	Logic Low Level Output Voltage	Iout= -1mA	VSS	•	0.1 * VDDIO	V
\mathbf{I}_{IH}	Logic High Input Current Source (Non MIPI Pin)	-	-	-	1	μΑ
${ m I}_{ m IL}$	Logic Low Input Current Drain (Non MIPI Pin)	-	-1		1	μΑ
I_{IH_M}	Logic High Input Current Source (MIPI Pin Only)	-	4	7	10	μΑ
I _{IL_M}	Logic Low Input Current Drain (MIPI Pin Only)		-10	4-7	-	μΑ
Power Genera	tion / Regulation Output					•
VDD	Power supply for Logic circuit		N. P.	1.2	-	V
MIPIVDD	Regulated Output for MIPI logic circuits		-	1.2	-	V
VCOM	VCOM Voltage		-2.7	-	0	V
DDVDH	Source Circuit Positive Power Supply		4.50	-	6.00	V
DDVDL	Source Circuit Negative Power Supply		-6.00	-	-4.50	V
VGH	GIP Pin Positive Power Supply	VCI=3.3V with No Loading	DDVDH+ VDDIO	-	2x DDVDH - DDVDL	V
VGL	GIP Pin Negative Power Supply	-	2x DDVDL - DDVDH	-	DDVDL- VDDIO	v
	VGH-VGL	-	-	-	30	V
VGHO	Regulated positive power output pin for gate driver	-	6	-	15	V
VGLO	Regulated negative power output pin for gate driver	-	-14	-	-5	V
Source Driver						
Deviation	GVDDP/GVDDN deviation	Note 1,2 GVDDP/GVDDN set @ +/- 5.00V	-	-	45	mV
$S_{ m off}$	Source Output offset voltage	Note 1,2 VREG1OUT/VREG2OUT set @ +/-5.00V	-	-	45	mV

Note 1: VDDIO = 1.8V and at Room Temperature (25°C)

Note 2: VCI = 3V

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Table 11-2: Current Consumptions (to be updated)

(Unless otherwise specified, Voltage Referenced to VSS, TA = 25 °C, Display Resolution is 400x400 @ 60Hz)

Symbol	Parameter	Test Condition		Min	Тур	Max	Unit
Current Consu	nptions						
т	Sleep mode current	VDDIO = 1.8V VCI = 3V	VDDIO	-	TBD	-	μΑ
I_{sleep}			VCI	-	TBD	-	μΑ
Ţ	Display on current	VDDIO = 1.8V VCI = 3V White pattern	VDDIO	-	TBD	-	mA
IDISPLAY			VCI	-	TBD	-	mA

Note 1: VDDIO= 1.8V, VCI = 3V at Room Temperature (25°C)

Table 11-3: MIPI DC Characteristics

(Unless otherwise specified, Voltage Referenced to VSS, TA = -40 to 85 °C)

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
v				-JP		
MIPI LP Tr	ansmitter					•
V_{OH}	Thevenin output high level	-	1.15	1.2	1.35	V
V_{OL}	Thevenin output low level	-	-50	-	50	mV
MIPI LP Re	ceiver					
V _{IH}	Logic 1 input voltage	-	880	A- 9	\-\	mV
V_{IL}	Logic 0 input voltage	-		-	550	mV
MIPI HS Re	ceiver		-			
V _{CMRX(} DC)	Common mode voltage, HS Receiver mode		70		330	mV
V_{IDTH}	Differential input high threshold			-	70	mV
V_{IDTL}	Differential input low threshold		-70	-	-	mV
V_{IHHS}	Single-ended input high voltage		-	-	460	mV
V _{ILHS}	Single-ended input low voltage		-40	-	-	mV
V _{TERM-EN}	Single-ended threshold for HS termination enable		-	-	450	mV
Z_{ID}	Differential input impedance		80	100	125	ohm

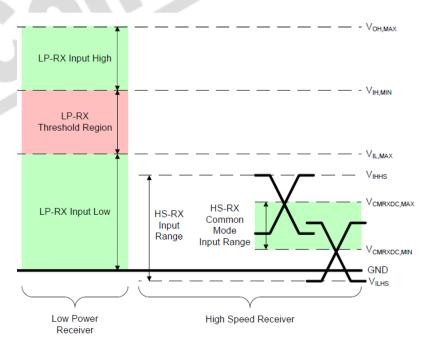


Figure 11-1: MIPI Signal Voltage Level

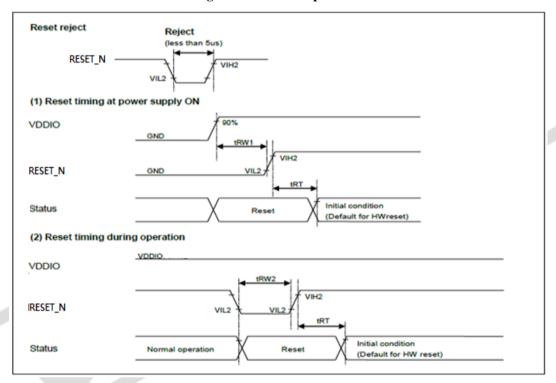
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12 RESET CHARACTERISTICS

Table 12-1: Reset Characteristics

Item	Symbol	Unit	Test Condition	Min.	Тур.	Max.
Reset "Low" level width 1	tRW1	ms	Power On	1	-	-
Reset "Low" level width 2	tRW2	ms	Operation	1	-	-
Reset time	tRT	ms	-	20	-	-

Figure 12-1: Reset Operation



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13 COMMAND TABLE

Table 13-1: User Command Set Table

Han Cada	C	D/C	W/D	D7	D(D.F	D4	D2	D2	D1	Do
R00h	Command NOP	D/C C	W/R W	D7	D6	D5	D4 0	D3	D2	D1	D0
R01h	SWRESET	D	W	0	0	0	0	0	0	0	1
R04h	ID	C	W	0	0	0	0	0	1	0	0
10411	1st Parameter	D	R	0	· ·	U	ID1[7			Ü	U
	2nd Parameter	D	R				ID2[7				
	3rd Parameter	D	R				ID3[7	_			
R09h	RDISPMODE	С	W	0	0	0	0	1	0	0	1
	1st Parameter	D	R	0	0	0	0	RGB	0	SS	GS
	2nd Parameter	D	R	0	0	0	0	IDMON	0	SLPOUT	NORM
	3rd Parameter	D	R	0	0	INV	0	0	DISPON	TEON	0
	4th Parameter	D	R	0	0	TELOM	0	0	0	0	0
R0Ah	RDDPM	C	W	0	0	0	0	1	0	1	0
	1st Parameter	D	R	0	IDMON	0	SLPOUT	NORON	DISON	0	0
R0Bh	RDDMADCTL	C	W	0	0	0	0	1	0	1	1
Doc!	1st Parameter	D	R	0	0	0	0	BGR	0	SS	GS
R0Ch	RDPIX	C D	W R	0	0	0	0	0	1	0 DBI[2:0]	0
R0Dh	1st Parameter RDDIM	C	W	0	0	0	0	1	1	0	1
KUDII	1st Parameter	D	R	0	0	INV	0	0	0	0	0
R0Eh	RDDSM	C	W	0	0	0	0	1	1	1	0
TOLII	1st Parameter	D	R	TEON	TELOM	0	0	0	0	0	EDSI
R0Fh	RDDSDR	C	W	0	0	0	0	1	1	1	1
	1st Parameter	D	R	NVLD	FUND	0	0	0	0	0	0
R10h	SLPIN	C	W	0	0	0	1	0	0	0	0
R11h	SLPOUT	С	W	0	0	0	1	0	0	0	1
R13h	NORON	C	W	0	0	0	1	0	0	1	1
R20h	INVOFF	C	W	0	0	1	0	0	0	0	0
R21h	INVON	C	W	0	0	1	0	0	0	0	1
R28h	DISPOFF	C	W	0	0	1	0	1	0	0	0
R29h	DISPON	C	W	0	0	1	0	1	0	0	1
R2Ah	SETCOL	С	W	0	0	1	0	1	0	1	0
	1st Parameter	D D	W				SC[15				
	2nd Parameter 3rd Parameter	D	W		\leftarrow		SC[7 EC[15				
	4th Parameter	D	W				EC[7				
R2Bh	SETPAGE	C	W	0	0	1	0	1	0	1	1
REBII	1st Parameter	D	W	0		•	SP[15				
	2nd Parameter	D	W				SP[7:				
	3rd Parameter	D	W				EP[15	:8]			
	4th Parameter	D	W				EP[7:	:0]			
R2Ch	WRMEMST	C	W	0	0	1	0	1	1	0	0
R34h	TEOFF	С	W	0	0	1	1	0	1	0	0
R35h	TEON	C	W	0	0	1	1	0	1	0	1
	1st Parameter	D	W	0	0	0	0	0	0	0	TELOM
R36h	MADCTR	C	W	0	0	1	1	0	1	1	0
D 201-	1st Parameter IDMOFF	D	W	0	0	0	ML	BGR	0	SS	GS
R38h R39h	IDMOFF	C C	W	0	0	1	1	1	0	0	0
R3Ah	SETPIXEL	C	W	0	0	1	1	1	0	1	0
IXJ/MI	1st Parameter	D	W	0	0	0	0	0	0	DBI[2:0]	U
R3Ch	WRMEMCONT	C	W	0	0	1	1	1	1	0	0
R44h	TESS	C	W	0	1	0	0	0	1	0	0
	1st Parameter	D	W			-	STS [1				
	2nd Parameter	D	W				STS[7				
R45h	RSS	С	W	0	1	0	0	0	1	0	1
	1st Parameter	D	R				GTS [1				
	2nd Parameter	D	R				GTS[7				
R51h	SETBR	C	W	0	1	0	1	0	0	0	1
	1st Parameter	D	W				DBV[1		01		
D 521	2nd Parameter	D	W	0	0	0	1	DBV[5	_	1 1	1
R53h	SETMODE 1st Parameter	C D	W	0	1	0	1	DD DD	0	0	0
R54h	1st Parameter RDMODE	C	W	0	0	BCTRL 0	0	0	BL 1	0	0
NJ4II	1st Parameter	D	R	0	0	BCTRL	0	DD	BL	0	0
R55h	SETPWR	C	W	0	1	0	1	0	1	0	1
10011	1st Parameter	D	W	0	0	0	0	0		PS[2:0]	
u		_ ~				Ÿ	Ÿ	,		· ~ [~·~]	

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Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D0
R56h	RDPWR	C	W	0	1	0	1	0	1	1	0
	1st Parameter	D	R	0	0	0	0	0		PS[2:0]	
R5Eh	SETMINBR	C	W	0	1	0	1	1	1	1	0
	1st Parameter	D	W				CMB	[13:6]			
	2nd Parameter	D	W	0	0			CMB	[5:0]		
R5Fh	RDMINBR	C	W	0	1	0	1	1	1	1	1
	1st Parameter	D	R				CMB	[15:8]			
	2nd Parameter	D	R	0	0			CMB	[5:0]		
A1h	RDDDBST	C	W	1	0	1	0	0	0	0	1
A8h	RDDDBCON	C	W	1	0	1	0	1	0	0	0



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14 COMMAND DESCRIPTION

14.1 User Command Set

14.1.1 NOP (00h)

Hex Code	Command	D/C	WR	D7	D6	D5	D4	D3	D2	D1	D0	POR
R00h	NOP	C	W	0	0	0	0	0	0	0	0	-

Description	- This command is an empty command; it does not ha	ave any effect on the display module.
Restriction	-	
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Sleep In	Availability Yes Yes Yes Yes

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14.1.2 Software Reset (01h)

Hex Code	Command	D/C	WR	D7	D6	D5	D4	D3	D2	D1	D 0	POR
R01h	SWRESET	С	W	0	0	0	0	0	0	0	1	-

I—————————————————————————————————————		
Description	- When the Software Reset command is written, it commands and parameters to their S/W Reset defa (See default tables in each command description.) - The display is blank immediately. The display to on the panel type.	ault values
Restriction	 It will be necessary to wait 5msec before sending The display module loads all display module factors 5msec. If Software Reset is applied during Sleep Out mobefore sending Sleep Out command. Software Reset Command cannot be sent during NVM will reload when hardware reset is applied. 	tory default values to the registers during ode, it will be necessary to wait 120msec Sleep Out sequence.
		A 3130
	Status	Availability
Register	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Availability	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

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14.1.3 Read ID (04h)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D0	POR
R04h	ID	С	W	0	0	0	0	0	1	0	0	-
	1st Parameter	D	R				ID1[7	:0]				00h
	2 nd Parameter	D	R				ID2[7	:0]				00h
	3 rd Parameter	D	R				ID3[7	:0]				00h

Description	- This command read back ID code.	
Restriction	-	
	Status	Availability
Register	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Availability	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

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14.1.4 Read Display Mode (09h)

Hex Code	Command	D/C	W/R	D 7	D6	D5	D4	D3	D2	D1	D0	POR
R09h	RDISPMODE	C	W	0	0	0	0	1	0	0	1	-
	1st Parameter	D	R	0	0	0	0	RGB	0	SS	GS	00h
	2nd Parameter	D	R	0	0	0	0	IDMON	0	SLPOUT	NORM	01h
	3rd Parameter	D	R	0	0	INV	0	0	DISPON	TEON	0	00h
	4th Parameter	D	R	0	0	TELOM	0	0	0	0	0	00h

	RGB: RGB/BGR order status		
	SS: Flip horizontal status		
	GS: Flip vertical status		
	IDMON: Idle mode status		
	SLPOUT: Sleep out status		
Description	NORM: Normal mode status		
	INV: Inversion mode status		
	DISPON: Display on status		
	TEON: TE status		
	TELOM: TE mode status		
Restriction			
	Status	Availability	
Register	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
Availability	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	

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14.1.5 Read Display Power Mode (0Ah)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D0	POR
R0Ah	RDDPM	0	W	0	0	0	0	1	0	1	0	-
	1st Parameter	1	R	0	IDMON	0	SLPOUT	NORON	DISON	0	0	08h

	-This con	nmand indicates	s the current status of the d	lisplay as described in the table below	<u> </u>							
	Bit	Bit Symbol	Description	Value								
	D7	Reserved	-	-								
	D6	IDMON	Idle Mode On/Off	'0' = Idle Mode Off, '1' = Idle Mode On,								
	D5	Reserved	-	-								
Description	D4	SLPOUT	Sleep In/Out	'0' = Sleep In '1' = Sleep Out,								
	D3	NORON	Display Normal mode On/Off	'0' = Normal Display Off, '1' = Normal Display On,								
	D2	DISON	Display On/Off	'0' = Display Off, '1' = Display On,								
	D1	Reserved	-	-								
	D0	Reserved	-	-								
Restriction			-									
		Sta	fus	Availability								
Register Availability	Norma		Mode Off, Sleep Out	Yes								
			e Mode On, Sleep Out	Yes								
		Slee		Yes								

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14.1.6 Read Display MADCTL (0Bh)

Hex Code	Command	D/C	W/R	D 7	D6	D5	D4	D3	D2	D1	D 0	POR
R0Bh	RDDMADCTL	0	W	0	0	0	0	1	0	1	1	-
	1st Parameter	1	R	0	0	0	0	BGR	0	SS	GS	00h

	-This co	mmand indicat	tes the current status o	f the display as described in t	the table below		
	Bit Bit Symbol		Description	Value			
	D7	Reserved	-	0			
	D6 Reserved		-	0			
	D5 Reserved		-	0			
Description	D4 Reserved		-	0			
Description	D3 BGR		RGB/BGR Order	'0'=RGB, '1'=BGR			
	D2	Reserved	-	0			
	D1	SS	Flip Horizontal	'0' = Normal '1' = Flipped horizontally			
Restriction	D0	GS	Flip Vertical	'0' = Normal '1' = Flipped vertically			
Register Availability		S	tatus	Availability			
	Norm		lle Mode Off, Sleep O		Yes		
			dle Mode On, Sleep O				
	1,0111		eep In	Yes			

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14.1.7 Read Color format (0Ch)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D 0	POR
R0Ch	RDPIX	0	W	0	0	0	0	1	1	0	0	-
	1st Parameter	1	R	0	0	0	0	0		DBI[2:0]		07h

Description	-This command read pixel color format.							
Restriction	-							
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Sleep In	Availability Yes Yes Yes						

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14.1.8 Read Display Image Mode (0Dh)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D0	POR
R0Dh	RDDIM	0	W	0	0	0	0	1	1	0	1	-
	1st Parameter	1	R	0	0	INVON	0	0	0	0	0	00h

Description	-This of Bit D7 D6 D5 D4 D3 D2 D1 D0	D7 D6 INVON D4 D3 D2 D1 D0	Description Revered Inversion On/Off Reserved	f the display as described in the Value '0' '0' = Inversion is Off. '1' = Inversion is On.	e table below:
Restriction	-				
Register Availability		mal Mode On,	Status Idle Mode Off, Sleep O Idle Mode On, Sleep O Sleep In		

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14.1.9 Read Signal Mode (0Eh)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D 0	POR
R0Eh	RDDIM	0	W	0	0	0	0	1	1	1	0	-
	1st Parameter	1	R	TEON	TELOM	0	0	0	0	0	0	00h

			licates the current status of the disp		ne table below:			
	Bit	Bit Symbol	Description	Value				
	D7	TEON	Tearing Effect Line	'0': Off '1': On				
Description	D6	TELOM	Tearing Effect Line Output Mode	'0': Mode 0 '1': Mode 1				
Description	D5	D5						
	D4	D4						
	D3	D3	D 1	°0°				
	D2	D2	Revered	U				
	D1	D1						
	D0	D0						
				3776				
Restriction	-							
			Status	Avoilability				
Register	Not	mal Mode Or	Status n, Idle Mode Off, Sleep Out	Availability Yes				
Availability			n, Idle Mode On, Sleep Out	Yes				
2 Ivanaonity	1101	illul Wode O	Sleep In	Yes				
	2.000							

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14.1.10Read Signal Mode (0Fh)

Hex Code	Command	D/C	W/R	D7	D6	D 5	D4	D3	D2	D1	D 0	POR
R0Fh	RDDSDR	0	W	0	0	0	0	1	1	1	0	-
	1st Parameter	1	R	NVLD	FUND	0	0	0	0	0	0	00h

	-This	command ind	licates the current status of the di	splay as described in th	ne table below:	
	Bit	Bit Symbol	Description	Value		
	D7	NVLD	NVM Loading Detection	'0': Not OK '1': OK		
Description	D6	FUND	Functionality Detection	'0' : Not OK '1' : OK		
Description	D5	D5				
	D4	D4				
	D3	D3	D 1	°0°		
	D2	D2	Revered	U		
	D1	D1				
	D0	D0				
Restriction	-					
			C4-4	A !1 -1. !1!4		
Danistas	NI	mal Mada O	Status - Idla Mada Off Slaar Out	Availability		
Register Availability			n, Idle Mode Off, Sleep Out n, Idle Mode On, Sleep Out	Yes Yes		
Availability	INOI	mai ivioue Oi	•	Yes		
			Sleep In	168		

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14.1.11Sleep In (10h)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D 0	POR
R10h	SLPIN	С	W	0	0	0	1	0	0	0	0	-

Description	 This command causes the LCD module to enter the low power consumption mode. In this mode the DC/DC converter is disabled, and panel scanning is stopped. 								
Restriction	only be exit by the Sleep Out Command (11H) It will be necessary to wait 5msec before sendir supply voltages and clock circuits to stabilize.	 It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent. 							
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Sleep In	Availability Yes Yes Yes Yes							

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14.1.12Sleep Out (11h)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D 0	POR
R11h	SLPOUT	C	W	0	0	0	1	0	0	0	1	-

Description	 This command turns off sleep mode. In this mode the DC/DC converter is enabled, and panel scanning is started. 								
Restriction	can only be exit by the Sleep In Command (10H) - It will be necessary to wait 5msec_before sending the supply voltages and clock circuits to stabilize								
	Status	Availability							
Register	Normal Mode On, Idle Mode Off, Sleep Out	Yes							
Availability	Normal Mode On, Idle Mode On, Sleep Out Yes								
	Sleep In	Yes							
	Sicep in	ies							

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14.1.13Normal Display Mode On (13h)

Hex Code	Command	D/C	W/R	D7	D6	D 5	D4	D3	D2	D1	D0	POR
R13h	NORON	С	W	0	0	0	1	0	0	1	1	-

Description	- This command causes the display module to enter	r the Normal Mode.						
Restriction	-This command has no effect when Normal mode is already active.							
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Sleep In	Availability Yes Yes Yes Yes						



14.1.14Display Invert Mode Off (20h)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D0	POR
R20h	INVOFF	С	W	0	0	1	0	0	0	0	0	-

Description	-This command is used to recover from display in this command does not change any other status. (Example) Data	Display
Restriction	-This command has no effect when module is already	eady inversion off mode.
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Sleep In	Availability Yes Yes Yes Yes

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14.1.15Display Invert Mode On (21h)

Hex Code	Command	D/C	W/R	D7	D 6	D5	D4	D3	D2	D1	D0	POR
R21h	INVON	С	W	0	0	1	0	0	0	0	1	-

	-This command is used to enter into display inversion-This command does not change any other status.-To exit from Display Inversion On, the Display Inverten.	
Description	Top-Left (0,0) Data Data	Display
Restriction	-This command has no effect when module is already	Inversion On mode.
	Status	Availability
Register	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Availability	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

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14.1.16Display Off (28h)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D 0	POR
R28h	DISPOFF	С	W	0	0	1	0	1	0	0	0	-

Description	-This command is used to enter into DISPLAY O - In this mode, the white or black image is display -This command does not change any other status -There will be no abnormal visible effect on the o -Exit from this command by Display On (29H)	yed, which depends on the panel type.
Restriction	-This command has no effect when module is alre	eady in display off mode.
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Sleep In	Availability Yes Yes Yes Yes

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14.1.17Display On (29h)

Hex Code	Command	D/C	RDX	D7	D6	D5	D4	D3	D2	D1	D0	POR
R29h	DISPON	С	1	0	0	1	0	1	0	0	1	-

Description	-This command is used to recover from DISPLAY -This command does not change any other status. (Example)	OFF mode.
Restriction	-This command has no effect when module is alrea	ady in display on mode.
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Sleep In	Availability Yes Yes Yes Yes

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14.1.18Set Column (2AH)

Hex Code	Command	D/C	W/R	D 7	D6	D5	D4	D3	D2	D1	D0	POR
R2Ah	SELCOL	С	W	0	0	1	0	1	0	1	0	-
	1st Parameter	D	W		SC[15;8]				00h			
	2nd Parameter	D	W		SC[7:0]				00h			
	3rd Parameter	D	W	EC[15:8]				01h				
	4th Parameter	D	W		EC[7:0]				8Fh			

Description	SC[15:0]: set start column EC[15:0]: set end column	
Restriction	- SC must be 4M, where M is integer - EC must be 4N-1, where N is integer	
	Status	Availability
Register	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Availability	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

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14.1.19Set Row (2BH)

Hex Code	Command	D/C	W/R	D7	D7 D6 D5 D4 D3 D2 D1 D0					D0	POR	
R2Bh	SELPAGE	С	W	0	0 0 1 0 1 0 1 1					-		
	1st Parameter	D	W		SP[15;8]					00h		
	2nd Parameter	D	W		SP[7:0]					00h		
	3rd Parameter	D	W		EP[15:8]					01h		
	4th Parameter	D	W		EP[7:0]							8Fh

Description	SP[15:0]: set start row EP[15:0]: set end row	
Restriction	-	
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Sleep In	Availability Yes Yes Yes

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14.1.20Write memory start (2CH)

Hex Code	Command	D/C	W/R	D7	D6	D 5	D4	D3	D2	D1	D 0	POR
R2Ch	WRMEMST	С	W	0	0	1	0	1	1	0	0	-

Description	Start to write memory data									
Restriction	Cannot write whole frame data using 0x2C.Separate whole frame into several segment. Use	Cannot write whole frame data using 0x2C. Separate whole frame into several segment. Use 0x2C and 0x3C to write whole frame data.								
	Status	Availability								
Register	Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Availability	Normal Mode On, Idle Mode On, Sleep Out	Yes								
	Sleep In Yes									

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14.1.21Set Tearing Off (34H)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D0	POR
R34h	TEOFF	С	W	0	0	1	1	0	1	0	0	-

Description	- This command turns off the Tearing effect output sig	gnal from the TE signal line						
Restriction	- This command has no effect when Tearing Effect ou	atput is already off.						
	Status	Availability						
Register	Normal Mode On, Idle Mode Off, Sleep Out	Yes						
Availability	Normal Mode On, Idle Mode On, Sleep Out Yes							
	Sleep In Yes							



14.1.22Set Tearing On(35H)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D0	POR
R35h	TEON	С	W	0	0	1	1	0	1	0	1	-
	1st Parameter	D	W	0	0	0	0	0	0	0	TELOM	00h

Description	- This command turns on the Tearing effect output	signal from the TE signal line.						
Restriction	- This command has no effect when Tearing Effect output is already off Changes in parameter TELOM is enabled form the next frame period.							
Register Availability	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes							

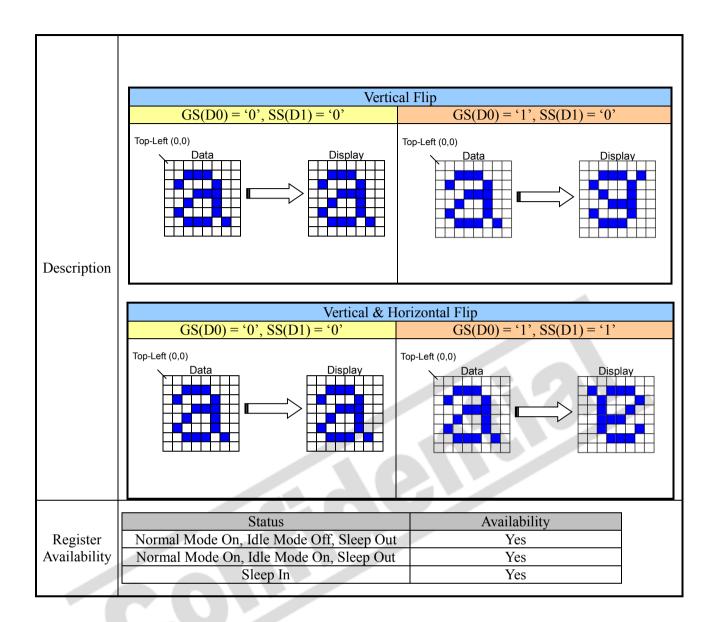
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14.1.23Data Access Control (36H)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D 0	POR
R36h	MADCTR	С	W	0	0	1	1	0	1	1	0	-
	1st Parameter	D	W	0	0	0	0	RGB	0	SS	GS	00h

	mi ·	1.1.0		· · · · · · · · · · · · · · · · · · ·						
	-This co	mmand define	s write scanning direc	tion from the host processor.						
	Bit	Bit Symbol	Description	Value						
	D7	Revered	- Description	O						
	D6	Revered	_	0						
	D5	Revered	-	0						
	D4	Revered	_	0						
	D3	BGR	RGB/BGR Order	'0'=RGB, '1'=BGR						
	D2	Revered	-	0						
	D1	SS	Flip Horizontal	'0' = Normal '1' = Flipped horizontally						
	D0	GS	Flip Vertical	'0' = Normal '1' = Flipped vertically						
			RGB-	BGR Order						
		D3 (R0	GB) = '0'	D3 (RGB) = '1'						
		,								
	,		ver IC	Driver IC RGB RGB RGB						
		KUB KUB - -	RGB	RGB RGB RGB						
Description		V	—							
Description		- R <mark>GB RGB</mark> -	RGB	BGR BGR BGR						
		RGB RGB -	RGB	BGR BGR BGR						
		LCD	Panel	LCD Panel						
			Hori	zontal Flip						
1		GS(D0) = '0	', SS(D1) = '0'	GS(D0) = '0', SS(D1) = '1'						
	Top-Left	(0.0)		Top-Left (0,0)						
		Data	Display	Data Display						

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14.1.24Idle Mode Off (38H)

Hex Code	Command	D/C	W/R	D7	D6	D 5	D4	D3	D2	D1	D0	POR
R38h	IDMOFF	C	W	0	0	1	1	1	0	0	0	-

Description	-This command is used to recover from Idle mode	e on.							
Restriction	- This command has no effect when module is alr	This command has no effect when module is already in idle off mode.							
Dagistar	Status Normal Mode On Idle Mode Off Sleep Out	Availability							
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes								
	Sleep In	Yes							

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14.1.26Idle Mode On (39H)

Hex Code	Command	D/C	W/R	D7	D 6	D 5	D4	D3	D2	D1	D0	POR
R39h	IDMON	С	W	0	0	1	1	1	0	0	1	-

ir	1			
		d is used to enter into Idle		
				d the secondary colours using
	MSB of each R	, G and B in the Frame M	emory, 8 colour depth da	ta is displayed.
		(Exa	imple)	
	Top-Left (0	Data	Display	
Description	Color	R ₇ R ₆ R ₅ R ₄ R ₃ R ₂ R ₁ R ₀	G ₇ G ₆ G ₅ G ₄ G ₃ G ₂ G ₁ G ₀	B ₇ B ₆ B ₅ B ₄ B ₃ B ₄ B ₁ B ₀
	Black	0xxxxxxx	0xxxxxxx	0xxxxxxx
	Blue	0xxxxxxx	0xxxxxxx	1xxxxxxx
	Red	1xxxxxxx	0xxxxxx 0xxxxxxx	0xxxxxxx
	Magenta	1xxxxxxx	0xxxxxxx	1xxxxxxx
	Green	0xxxxxxx	lxxxxxxx	0xxxxxxx
	Cyan	0xxxxxxx	1xxxxxxx	lxxxxxx
	Yellow	1xxxxxxx	1xxxxxxx	0xxxxxx
	White	1xxxxxxx	1xxxxxxx	1xxxxxxx
Restriction	- This command	d has no effect when mod	ule is already in idle off n	node
Restriction	- This command	a has no effect when mod	ure is already in fale on in	node.
		Ct. t		1 1 '1',
	27 1261	Status		lability
Register		e On, Idle Mode Off, Slee	1	Yes
Availability	Normal Mod	e On, Idle Mode On, Slee		Yes
\		Sleep In	Y	Yes

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14.1.27Set Color format (3Ah)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D0	POR
R3Ah	SETPIXEL	С	W	0	0	1	1	1	0	1	0	-
	1st Parameter	D	W	0	0	0	0	0		DBI[2:0]		07h

Description	-This command set pixel color format. DBI[2:-0]=7: 16.7M color DBI[2:-0]=6: 262k color DBI[2:-0]=5: 65k color	
Restriction	-	
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Sleep In	Availability Yes Yes Yes Yes

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14.1.28Write memory Continue (3CH)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D 0	POR
R3Ch	WRMEMCONT	С	W	0	0	1	1	1	1	0	0	-

Description	Continue to write memory data	
Restriction	-	
	Status	Availability
Register	Status Normal Mode On, Idle Mode Off, Sleep Out	Availability Yes
Register Availability		3

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14.1.29Set Tear Scanline (44h)

Hex Code	Command	D/C	W/R	D7	D6	D 5	D4	D3	D2	D1	D0	POR
R44h	TESS	C	W	0	1	0	0	0	1	0	0	-
	1st parameter	D	W				STS	[15:8]				00h
	2 nd parameter	D	W				STS	5[7:0]				00h

Description	This command turns on the Tearing effect output	signal from the TE signal line.								
Restriction	signal is already ON, TE signal is output accordi	This command takes effect on the frame following the current frame. Therefore, if the TE signal is already ON, TE signal is output according to the old set tear on and set tear scanline commands until the end of currently scanned frame.								
	Status	Availability								
Register	Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Availability	Normal Mode On, Idle Mode On, Sleep Out Yes									
	Sleep In Yes									

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14.1.30Get Scanline (45h)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D 0	POR
R45h	RSS	С	W	0	1	0	0	0	1	0	1	-
	1st parameter	D	R				GTS[[15:8]				00h
	2 nd parameter	D	R				GTS	[7:0]				00h

Description	The display module returns the current scan line. The first scan line of back porch period is defined	
Restriction	-	
	Status	Availability
Register	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Availability	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

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14.1.31Write Display Brightness (51h)

Hex Code	Command	D/C	W/R	D 7	D6	D5	D4	D3	D2	D1	D0	POR
R51h	SETBR	C	W	0	1	0	1	0	0	0	1	-
	1st parameter	D	W				DBV[13:6]				00h
	2 nd parameter	D	W	0	0			DBV	[5:0]			00h

Description	- This command is used to set the display brightn	ess value.
Restriction		
	Status	Availability
Register	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Availability	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

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14.1.32Set Display Brightness mode(53h)

Hex Code	Command	D/C	W/R	D7	D6	D 5	D4	D3	D2	D1	D0	POR
R53h	SETMODE	C	W	0	1	0	1	0	0	1	1	-
	1st parameter	D	W	0	0	BCTRL	0	DD	BL	0	0	00h

	This comm	and is used to s	set the value of display b	orightness control.				
	Bit	Bit Symbol	Description					
	D7	D7						
	D6	D6	Reserved					
	D5	BCTRL	switch brightness for displayed a constraint of the switch brightness for displayed and the switch bready and the switch brightness for displayed and the switch brigh	1 = On When this bit is set to off, the setting on DBV(51h) will be ignored. The PWM duty will be controlled only by CABC				
	D4	D4	Reserved					
Description	D3	DD	0 = Off 1 = On: This bit is used to enable When this bit is set to "1 existing value to the targ	1 = On: This bit is used to enable/disable PWM dimming function. When this bit is set to "1", the PWM duty will change from existing value to the target value (DBV) in a constant speed while the transition timing is control by the field "BCB" of				
	D2	BL						
	D1	D1	D					
	D0	D0	Reserved					
	5)							
Restriction								
	31 13	Statu	-~	Availability				
Register Availability			Mode Off, Sleep Out Mode On, Sleep Out	Yes Yes				
Availability	INUITIALI	Sleep	, 1					

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14.1.33Read Display Brightness mode(54h)

Hex Code	Command	D/C	W/R	D7	D6	D 5	D4	D3	D2	D1	D0	POR
R54h	RDMODE	С	W	0	1	0	1	0	1	0	0	-
	1st parameter	D	R	0	0	BCTRL	0	DD	BL	0	0	00h

	This comma	nd returns the va	ulue of display brightness control.
	Bit	Bit Symbol	Description
	D7	D7	
	D6	D6	Reserved
	Brightness Control Block On/Off, This bit is always used to switch brightness for display 0 = Off 1 = On When this bit is set to off, the setting on DBV(51h) will be ignored. The PWM duty will be controlled only by CABC function.		
	D4	D4	Reserved
Description	D3	DD	Display Dimming (DD): (Only for manual brightness setting) 0 = Off 1 = On: This bit is used to enable/disable PWM dimming function. When this bit is set to "1", the PWM duty will change from existing value to the target value (DBV) in a constant speed while the transition timing is control by the field "BCB" of command 0xC8.
	D2	BL	BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On
	D1	D1	D. I
	D0	D0	Reserved
	5		
Restriction			
Register Availability			Mode Off, Sleep Out Yes Mode On, Sleep Out Yes

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14.1.34Set CABC control (55h)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D 0	POR
R55h	SETPWR	C	W	0	1	0	1	0	1	0	1	-
	1st parameter	D	W	0	0	0	0	0	0	CABO	C[1:0]	00h

	This com	mand set the pov	ver saving level.						
	Bit	Bit Symbol	Description	on					
	D7	D7							
	D6	D6							
	D5	D5	Reserved						
	D4	D4	Reserved						
Description	D3	D3							
	D2	D2							
	D1	CABC[1:0]							
	D0	CABC[1.0]	'10' = middle '11' = high						
Restriction	-								
		Statı		Availability					
Register			Mode Off, Sleep Out	Yes					
Availability	Norma		Mode On, Sleep Out	Yes Yes					
		Sleep	Ш	168					

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14.1.35Read CABC control (56h)

Hex Code	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D0	POR
R56h	RDPWR	C	W	0	1	0	1	0	1	1	0	-
	1st parameter	D	R	0	0	0	0	0	0	CABO	C[1:0]	00h

	This com	mand returns the	power saving level.							
	Bit	Bit Symbol	Descript	ion						
	D7	D7								
	D6	D6								
	D5	D5	Reserved							
	D4	D4	Reserved							
Description	D3	D3								
	D2	D2								
	D1									
	D0	CABC[1:0]	'10' = middle '11' = high							
Restriction	-									
_	_	Statı		Availability						
Register			Mode Off, Sleep Out	Yes						
Availability	Norma		Mode On, Sleep Out	Yes						
		Sleep	In	Yes						

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14.1.36Set CABC Minimum Brightness (5Eh)

Hex Code	Command	D/C	R/W	D 7	D6	D5	D4	D3	D2	D1	D 0	POR
R5Eh	SETMINBR	С	W	0	1	0	1	1	1	1	0	-
	1 st parameter	D	W				CMB	[13:6]				
	1 nd parameter	D	W	0	0			CME	B[5:0]			00h

Description	This command set CABC minimum brightness.	
Restriction	-	
	Status	Availability
Register	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Availability	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

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14.1.37Read CABC Minimum Brightness (5Fh)

Hex Code	Command	D/C	R/W	D7	D6	D5	D4	D3	D2	D1	D0	POR
R5Fh	RDMINBR	С	W	0	1	0	1	1	1	1	1	-
	1st parameter	D	R				CMB	[13:6]				
	2 nd parameter	D	R	0	0			CME	B[5:0]			00h

Description	This command returns CABC minimum brightne	ess.						
Restriction	-							
	Status	Availability						
Register	Normal Mode On, Idle Mode Off, Sleep Out	Yes						
Availability	Normal Mode On, Idle Mode On, Sleep Out Yes							
	Sleep In	Yes						

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14.1.38Read DDB Start (A1h)

Hex Code	Command	D/C	R/W	D7	D6	D5	D4	D3	D2	D1	D0	POR		
RA1h	RDDDBS	С	W	1	0	1	0	0	0	0	1	-		
	1 st parameter	D	R		SID[7:0]									
	2 nd parameter	D	R		SID[15:8] MID[7:0]									
	3 rd parameter	D	R											
	4 th parameter	D	R		MID[15:8] RID[7:0]									
	5 th parameter	D	R											
	6 th parameter	D	R		RID[15:8]									

	Start to read manu	ıfacturer ID	
	Parameter	Code	Description
	1st Parameter	SID[7:0]	Upper Byte of SSL ID code
.	2 nd Parameter	SID[15:8]	Lower Byte of SSL ID code
Description	3 rd Parameter	MID[7:0]	Upper Byte of Manufacturer version
	4 th Parameter	MID[15:8]	Lower Byte of Manufacturer version
	5 th Parameter	RID [7:0]	SSL INTERNAL USED
	6 th Parameter	RID [15:8]	SSL INTERNAL USED
Restriction	-		
		Status	Availability
Register		On, Idle Mode Off, Sle	
Availability	Normal Mode (On, Idle Mode On, Slee	eep Out Yes
		Sleep In	Yes

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14.1.39Read DDB Continue (A8h)

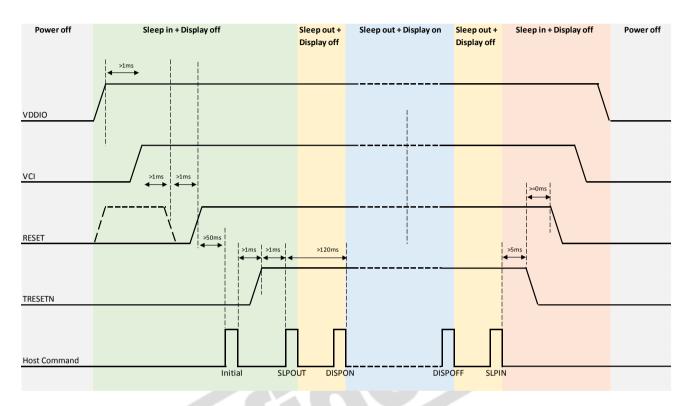
Hex Code	Command	D/C	R/W	D7	D6	D5	D4	D3	D2	D1	D0	POR		
RA8h	RDDDBCON	C	W	1	0	1	0	1	0	0	0	-		
	1st parameter	D	R		SID[7:0]									
	2 nd parameter	D	R		SID[15:8] MID[7:0] MID[15:8]									
	3 rd parameter	D	R											
	4 th parameter	D	R											
	5 th parameter	D	R	RID[7:0]										
	6 th parameter	D	R				RID[15:8]				00h		

									
	Continue to read 1	manufacturer ID							
	Parameter	Code	Descri	ption					
	1st Parameter	SID[7:0]	Upper	Byte of SSL ID code					
Description	2 nd Parameter	SID[15:8]	Lower	Lower Byte of SSL ID code					
r r	3 rd Parameter	MID[7:0]	Upper Byte of Manufacturer version						
	4 th Parameter	MID[15:8]	Lower	Lower Byte of Manufacturer version					
	5 th Parameter	RID [7:0]	SSL IN	SSL INTERNAL USED					
	6 th Parameter	RID [15:8]	SSL IN	SL INTERNAL USED					
					_				
Restriction		6.0							
		Status		Availability					
Register	Normal Mode (On, Idle Mode Off, Slee	p Out	Yes					
Availability	Normal Mode (On, Idle Mode On, Sleep	o Out	Yes					
		Sleep In		Yes					

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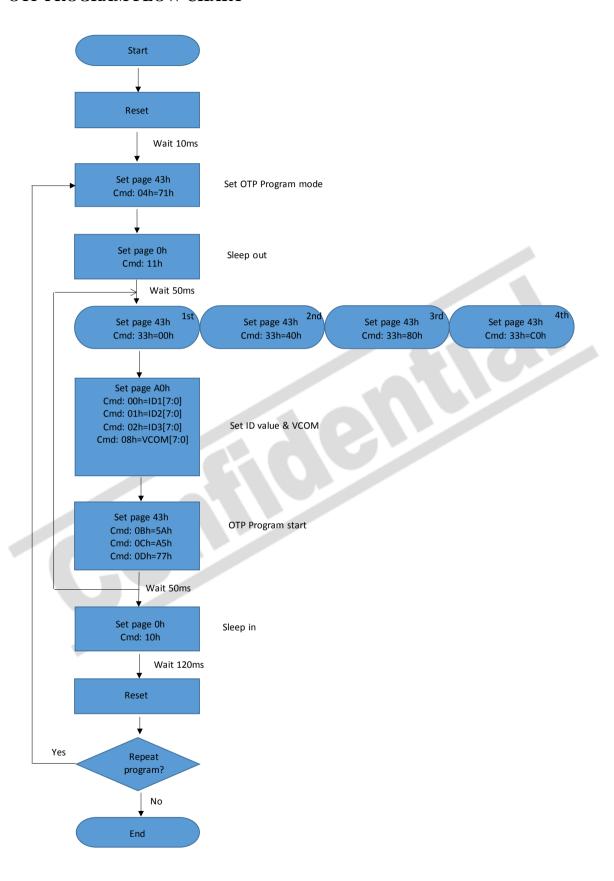
15 POWER ON/OFF SEQUENCES

Figure 15-1: Power On/Off Sequence



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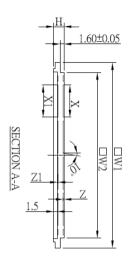
16 OTP PROGRAM FLOW CHART

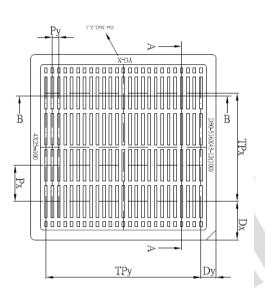


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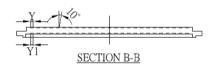
17 PACKAGE INFORMATION

17.1 Chip Tray Information

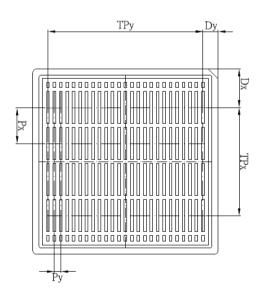




z	Z1	Y1	X1	Z	Y	Х	TPy	Dy	TPx	Dx	Py	Px	H	W3	W2	W1	
100(pocket number)	0.30±0.05 (12)	1.098±0.05 (43)	13.104±0.05 (516)	0.30±0.05 (12)	1.098±0.05 (43)	13.104±0.05 (516)	63.60±0.10 (2504)	6.20±0.05 (244)	44.40±0.10 (1748)	15.80±0.05 (622)	2.65±0.05 (104)	14.80±0.05 (583)	4.20±0.10 (165)	68.30±0.10 (2689)	68.00±0.10 (2677)	76.00±0.10 (2992)	Spec



2.Tray material : ABS
2.Tray color code: Black
3.Tray warpage: Max. ± 0.1mm
4.Surface resistance: 10 *\(^{2}\)\Color \(^{2}\)\Color \(^{2}\)\



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The product(s) listed in this datasheet comply with Directive (EU) 2015/863 of 31 March 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances and People's Republic of China Electronic Industry Standard GB/T 26572-2011 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子电器产品中限用物質的限用要求)". Hazardous Substances test report is available upon request.

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