Address Decoder mit Testbench

Code

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity addrDec is
  port (
    addr_i     : in  std_logic_vector(7 downto 0);
    cs_o       : out  std_logic_vector(2 downto 0);
    addr0_o    : out  std_logic_vector(5 downto 0);
    addr1_o    : out  std_logic_vector(5 downto 0);
    addr2_o    : out  std_logic_vector(6 downto 0)
    );
end entity;

architecture rtl of addrDec is
begin
  cs_o <= "001" when addr_i(7 downto 6) = "00" else
          "010" when addr_i(7 downto 6) = "01" else
          "100" when addr_i(7) = '1' else
          "000";
  addr0_o <= addr_i(5 downto 0);
  addr1_o <= addr_i(5 downto 0);
  addr2_o <= addr_i(6 downto 0);
end rtl;

configuration addrDec_conf of addrDec is
  for rtl
  end for;
end addrDec_conf;
```