VASAVI COLLEGE OF ENGINEERING

(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Embedded System Design

[2020 – 2021]

Faculty: **N Abid Ali Khan**	Program: ME	Branch: **ESVLSID**		SEE Marks: **60**	Course Code: **PI20PC110EC**
L: T: P (Hr/week): **3:0:0**	Year: **First**	Sem – **I**	Credits: **3**	CIE Marks: **40**	Duration of SEE: **3 Hours**

LESION PLAN

Sl. No	Unit	Date	Topic	Lect.	Cum Lect.
1.		21.12.20	Embedded System: Definition, Examples, Classifications	1	1.
2.		22.12.20	Selecting CPU & Memories; Quality of Service (QoS)	1	2.
3.	**1**	24.12.20	Design Challenges: Embedded Systems Product Life Cycle	1	3.
4.		28.12.20	MPU Vs MCU Vs DSP; Languages: ASM Vs Embedded C/C++	1	4.
5.		29.12.20	Compiler Vs Cross compilation: IDE; RISC Vs CISC	1	5.
6.		31.12.20	8051 Block Diagram; Architecture; System Design Approach	1	6.
7.		04.01.21	Addressing modes of 8051; Embedded–C/C++ [Quiz – 0]	1	7.
8.		05.01.21	TMOD, TCON, SCON, PCON, IE Reg. configuration options	1	8.
9.		07.01.21	Embedded C–Timer0, Timer1, UART for 8051 programming	1	9.
10.	**2**	11.01.21	Interfacing LED, Seven Segment Displays–program [Quiz – 1]	1	10.
11.		12.01.21	Sensor interface: ADC0804/08, Sampling options & DAC i/f.	1	11.
12.		14.01.21	Pongal Festival Holiday	-	-
13.		18.01.21	LCD interfacing: command & data (8-bit mode & 4-bit mode)	1	12.
14.		19.01.21	4x4 Keypad interfacing; algorithm & flowchart, program **[A1]**	1	13.
15.		21.01.21	Interface – RTC, DC motor, principle & PWM generations	1	14.
16.		25.01.21	Introduction to ARM Core: Functional advantages of ARM	1	15.
17.		26.01.21	Republic Day Celebrations & Holiday	-	-
18.		28.01.21	ARM CPU engine architecture: Use of barrel shift register	1	16.
19.		01.02.21	ARM Nomenclature and Design philosophy opted by MCU	1	17.
20.		02.02.21	CPU Core Registers–Modes, registers; CPSR; SPSR	1	18.
21.	**3**	04.02.21	AMBA Bus architecture: Functionality, Principles of APB, AHP	1	19.
22.		08.02.21	CIE – 1 (Mid-1) Theory Examinations.	1	20.
23.		09.02.21	CIE – 1 (Mid-1) Theory Examinations.	1	21.
24.		11.02.21	CIE – 1 (Mid-1) Theory Examinations.	1	22.
25.		15.02.21	ARM7, ARM9 Pipeline hierarchy and performance of RISC	1	23.
26.		16.02.21	Thumb support; ARM family version variants & comparisons	1	24.
27.		18.02.21	ARM IVT, Dhrystone; ARM7 Vs 9; Cortex Families features.	1	25.
28.		22.02.21	Introduction to Embedded Networking & Issues – [Quiz – 2]	1	26.
29.	**4**	23.02.21	UART networking: Functioning, Frame format and Signaling	1	27.
30.		25.02.21	MAX232 IC Protection circuit for UART; soft & NULL modem.	1	28.

31.		01.03.21	I^2C working principle; Frame formats, states; IIC advantages	1	29.
32.		02.03.21	SPI–topology; Comparison; JTAG support using SPI **[A2]**	1	30.
33.		04.03.21	CAN Protocol; Topology; Network Operation	1	31.
34.		08.03.21	Frame formats of CAN protocol; Versions, Pros and Cons.	1	32.
35.		09.03.21	USB: need, topology, principle, versions, Pros & Cons OTG	1	33.
36.		11.03.21	Sivaratri Festival Holiday	-	-
37.		15.03.21	Parallel protocols: PCI; PCIe & PCIx standards & ARM–AMBA	1	34.
38.	**5**	16.03.21	Embedded Debugging–Need, Definition; HW/SW Co-design	1	35.
39.		18.03.21	Co-design flowchart: ACC Case study of HW–SW partitioning	1	36.
40.		22.03.21	Cross IDE Simulators – Windows, Tools, Breakpoints, printf's	1	37.
41.		23.03.21	JTAG IAP facility for ARM MCUs; ETM, Tap Controller	1	38.
42.		25.03.21	Protocol Debugging–Null modem, loopback, IP Sniffing	1	39.
43.		29.03.21	Holi Festival Holiday	-	-
44.		30.03.21	Round Robin, RR with interrupts scheduler for RTS [Quiz-3]	1	40.
45.		01.04.21	Functional Queue Scheduler – Pros & Cons; RTOS need **[A3]**	1	41.
46.		05.04.21	Babu Jagjeevan Ram Birthday Holiday	-	-
47.		06.04.21	CIE – 2 (Mid-2) Theory Examinations.	1	42.
48.		08.04.21	CIE – 2 (Mid-2) Theory Examinations.	1	43.

Number of Contacting Lecture Hours: **38Hrs. +** Number Hours falling for CIE – 05**Hrs.**
= Total Number of Contact Hours in the Semester – **43Hrs.**

The break-up of CIE: Internal Tests + Assignments + Quizzes

1.	No. of Internal Tests	: 02	Max. Marks for each Internal Tests	:	30 .
2.	No. of Assignments	: 03	Max. Marks for each Assignment	:	05 .
3.	No. of Quiz Tests	: 03	Max. Marks for each Quiz	:	05 .

Duration for writing internal examination: 90 Mins.

Final Assessment: (100 Marks)

60 Marks of SEE (Sem End Exam) +
40 Marks Final CIE such that:
Final CIE = 30 Marks of CIE (Avg of Two CIEs) +
05 Marks of CIE – Assignments (Avg performance in 3 Assignments) +
05 Marks of CIE – Quizzes (Average performance in 3 Quizzes).

Learning Resources:

[1] Frank Vahid, Tony Givargis "Embedded System Design – A Unified Hardware/Software Introduction" John Wiley & Sons, Inc. 2002.
[2] Andrew N Sloss, Dominic Symes & Chris Wright, "ARM System Developer's Guide: Designing and Optimizing System Software", The Morgan Kaufmann Series 2004.
[3] Mazidi M.A and Mazidi J.G, "The 8051 Microcontroller and Embedded Systems", Pearson 2007.
[4] David E Simon, "An Embedded Software Primer", Pearson Education, 2005.

Signature of The Faculty	**Signature of The Head**	**Signature of The Principal**
Mr. N Abid Ali Khan	Dr. E Sreenivasa Rao	Dr. S V Ramana
Asst Prof – ECE; VCE(A)	Prof & Head – ECE; VCE(A)	Vasavi College of Engineering (A)