

**VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD – 500 031**  
**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**  
**M. E - ECE(ES&VLSID) 1st- Semester (2020-21)**

**Analog IC Design: CC:(PI19PC130EC)**

**Lesson Plan**

S.No.	Date	Topic	No. of Periods	Cumulative Periods	Remarks
1	22-12-2020	<b>UNIT-1 -Introduction:</b>	1	1	
2	24-12-2020	Analog vs Digital signal processing, Syllabus, Evaluation, Reading materials	1	2	
3	29-12-2020	Why Analog?, Why CMOS?, Levels of Abstraction	1	3	
4	31-12-2020	MOSFETS – I/V characteristics, MOS device models	1	4	
5	5-1-2021	MOS device layout, MOS device capacitance	1	5	
6	7-1-2021	MOS Small-signal models, MOS Spice models	1	6	
7	8-1-2021	Sub-threshold MOS model, Long-channel versus Short-channel devices	1	7	
8	12-1-2021	MOSFET $I_D$ , $g_m$ and $V_{th}$ relations, Mathematical treatment	1	8	

**UNIT-2: Analog CMOS Sub-circuits**

9	15-1-2021	MOS Switch, MOS Diode/ Active Resistor - Problems	1	9	
10	19-1-2021	Current Sinks and Sources, What is a Current Mirror?	1	10	
11	21-1-2021	Current Mirrors – Basic current mirror architecture – Specifications of current mirrors, Problems	1	11	
12	22-1-2021	Cascode current mirrors – Wide swing	1	12	

		current mirrors, Discussion			
13	28-1-2021	Wilson current mirror – Degenerate current sources , Interaction	1	13	
14	29-1-2021	Voltage references – VBE, VT and Zenner diode based references	1	14	
15	2-2-2021	Band gap reference <b>Revision</b>	1	15	
16	4-2-2021	<b>Assignment-1 and discussion</b>	1	16	
17	5-2-2021	<b>Quiz-1</b>	1	17	

### ***UNIT – III CMOS Single stage amplifiers:***

18	12-2-2021	Basic concepts, Common Source (CS) stage with Resistive load, CS stage with Diode-connected load - Analysis	1	18	
19	16-2-2021	CS stage with Current source load, CS stage with Triode load-Analysis	1	19	
20	18-2-2021	CS stage with Source Degeneration, Source Follower (CD stage)-Analysis	1	20	
21	19-2-2021	CG stage-Analysis, Cascode Amplifier - Basics	1	21	
22	23-2-2021	Cascode and Folded Cascode stages -Analysis	1	22	
23	25-2-2021	Choice of Device Models.	1	23	
24	26-2-2021	Output amplifiers-Analysis	1	24	
25	2-3-2021	High Gain amplifier architectures	1	25	
26	4-3-2021	<b>Assignmet-2 Discussion, Quiz-2</b>	1	26	

### ***UNIT – IV CMOS Operational amplifiers***

27	5-3-2021	Differential Amplifiers, Gilbert Cell	1	27	
28	9-3-2021	Specifications of a typical un-buffered Op-Amp, Design of CMOS Op-Amps, Compensation of Op Amps,	1	28	
29	12-3-2021	Small signal dynamics of a Two-stage Op Amp, Miller and Feed-forward compensation techniques,	1	29	
30	16-3-2021	Design of Two-Stage Op Amps,	1	30	

31	18-3-2021	Cacode Op Amps, Folded Cascode Op Amp,	1	31	
32	19-3-2021	Gain Boosting, Comparison of different schemes	1	32	
33	23-3-2021	Common-Mode Feedback with resistive sensing,	1	33	
34	25-3-2021	Input Range Limitations, Slew Rate, Power Supply Rejection,	1	34	
35	26-3-2021	Noise in Op Amps.	1	35	

***UNIT – V Oscillators:***

36	30-3-2021	General Considerations, Ring Oscillators, Tuning in Ring Oscillators	1	36	
37	1-4-2021	LC Oscillators - Crossed coupled oscillator, Tuning in LC oscillators,	1	37	
38	<i>Extra</i>	Colpitts oscillator, One-port oscillators,	1	38	
39	<i>Extra</i>	Voltage Controlled Oscillators (VCO) Mathematical model of VCOs .	1	39	
40	<i>Extra</i>	<b><i>Revision/ Assignment-3</i></b>	1	40	
41	<i>Extra</i>	<b><i>Discussion on Assignment-3</i></b>	1	41	
42	<i>Extra</i>	<b><i>Quiz-3</i></b>	1	42	

***Since we are getting only 37 periods for this course, at least another 4 or 5 periods are essential for covering the syllabus.***

  
Electronics and Communication

**20-12-2020**

**(Prof. N.S.Murthy)**

**(Head of ECE)**

**(Principal)**