$$\beta_n V_m - \left(\beta_N V_{tn} - \beta_n \frac{V_{DSatN}}{2}\right) V_{dsatN}$$

$$+ \beta_p V_m V_{DsatP} - \beta_p V_{DD} V_{DsatP} - (V_{tp})\beta_p \cdot V_{DSatP}.$$

$$- \beta_p \cdot \frac{V_{DsatP}}{2} \cdot V_{Dsatp}.$$

$$N\beta_n \left(V_{tn} - \frac{V_{DSatN}}{2}\right) + \beta_p \left(V_{DD} + V_{tp} + \frac{V_{DSatP}}{2}\right) \cdot V_{DSatP}.$$

$$= \left(V_{tn} - \frac{V_{DSatN}}{2}\right) + \frac{\beta_p V_{DSatP}}{\beta_n V_{DSatN}} \left(\frac{V_{DD} + V_{tp} + V_{Dsatp}}{2}\right).$$

$$\beta_n V_m V_{DSatN} + \beta_p V_m V_{DSatP} =$$

$$V_m \left[1 + \frac{\beta_p V_{DSatP}}{\beta_n V_{DSatN}}\right] = \left(V_{tn} - \frac{V_{DSatN}}{2}\right) + \frac{\beta_p V_{DSatP}}{\beta_n V_{DSatn}} \left[\frac{V_{DD} + V_{tp} + V_{Dsatp}}{2}\right]$$

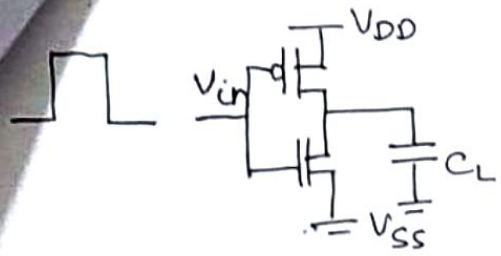
$$\therefore V_m = \frac{\left(V_{tn} - \frac{V_{DSat}}{N}\right) + \gamma \left[V_{DD} + V_{tp} + \frac{V_{DSatP}}{2}\right]}{1 + \gamma}$$

where $\gamma = \dfrac{\beta_p V_{DSatP}}{\beta_n V_{DSat N}}$.

For long channel devices, V_{Dsatp} & $V_{DSat N}$ are negligible when compared to V_{DD}.

$$\therefore V_M = \frac{\gamma V_{DD}}{1 + \gamma} \text{ for large } V_{DD}.$$

Design of Inverter :-



In short channel devices,

Let $V_{in} = V_M$

$$\beta_n = k_n'\left(\frac{W}{L}\right)_N \quad , \quad \beta_p = k_p'\left(\frac{W}{L}\right)_p$$

$$I_{DN} = \beta_N\left(V_m - V_{tn} - \frac{V_{DsatN}}{2}\right) V_{DsatN}.$$

$I_{DN} = |I_{DP}|$ as both are in Saturation.

$$I_{DP} = \beta_P\left(V_m - V_{DD} - |V_{TP}| - \frac{V_{DsatP}}{2}\right) V_{DsatP}.$$

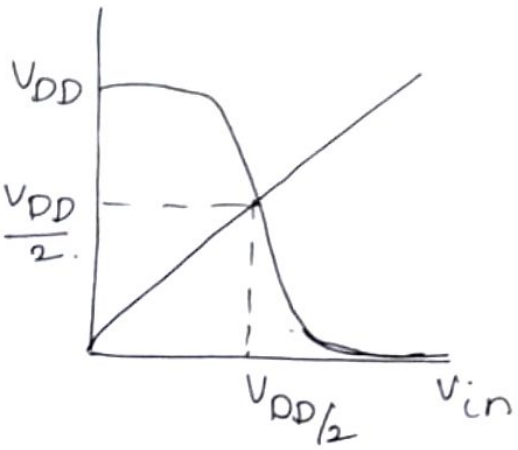
$$I_{DN} + I_{DP} = \beta_N\left(V_m - V_{tn} - \frac{V_{DsatN}}{2}\right) V_{DsatN} + \beta_P\left(V_m - V_{DD} - |V_{TP}| - \frac{V_{DsatP}}{2}\right) V_{DsatP} = 0$$

Similarly,

$$\frac{\left(\frac{W}{L}\right)_P}{\left(\frac{W}{L}\right)_N} = \frac{k_n' V_{DsatN}\left(V_m - V_{tn} - \frac{V_{DsatN}}{2}\right)}{k_p' V_{DsatP}\left(V_{DD} - V_m - |V_{tp}| - \frac{V_{DsatP}}{2}\right)}.$$

For short channel Devices ↑

More about CMOS inverter :-



* $\frac{W}{L}$ of NMOS & PMOS must be selected in such a way that the current through these transistors must be same.

∴ Resistances Same.

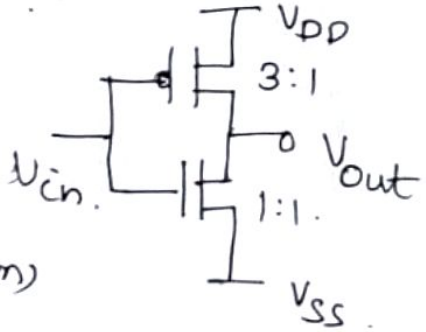
$$\left(\frac{W}{L}\right)_P = \left(\frac{\mu_n}{\mu_p}\right)\left(\frac{W}{L}\right)_N .$$

as L is same W_p must be 2 to 3 times that of W_N.

Resistance of the transistor, $R \propto L$.

$R \propto 1/W$.

This is known as balanced inverter.

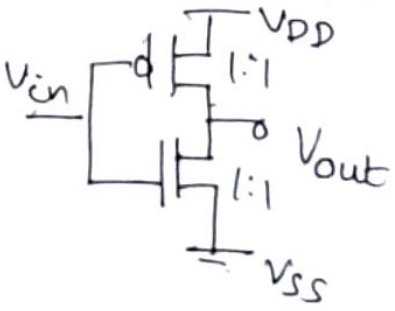


for balanced inverter,

$V_{SP} = V_{DD}/2$. (Both transistors are in Saturation)

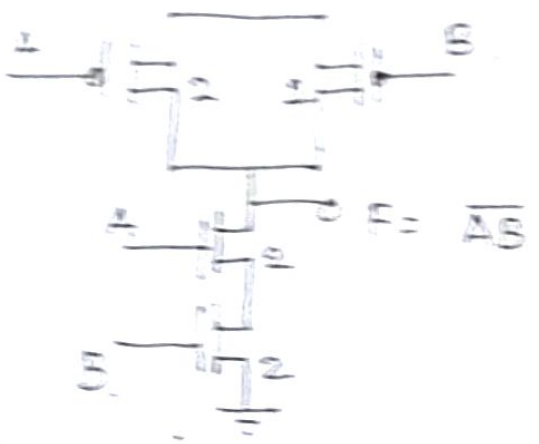
$\frac{\beta_p}{\beta_n} = 1$, $\mu_p \left(\frac{W}{L}\right)_p = \beta_p$, $\beta_n = \mu_n (W/L)_n$.

unbalanced CMOS inverter: (Currents are not Same).



Logical Effort :-

2 input NAND gate :-

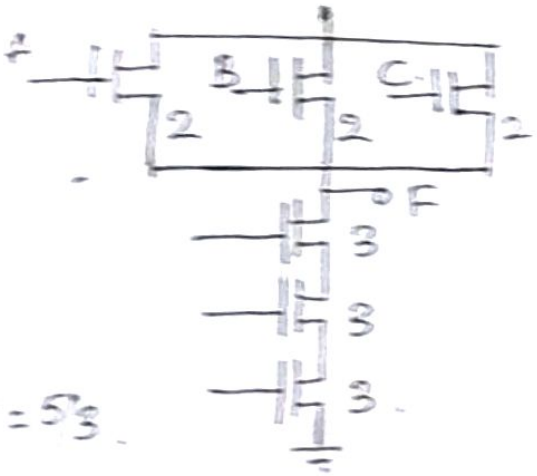


$$\text{LE} = \frac{\text{i/p Capacitance of gate}}{\text{i/p Capacitance of reference inverter}}$$

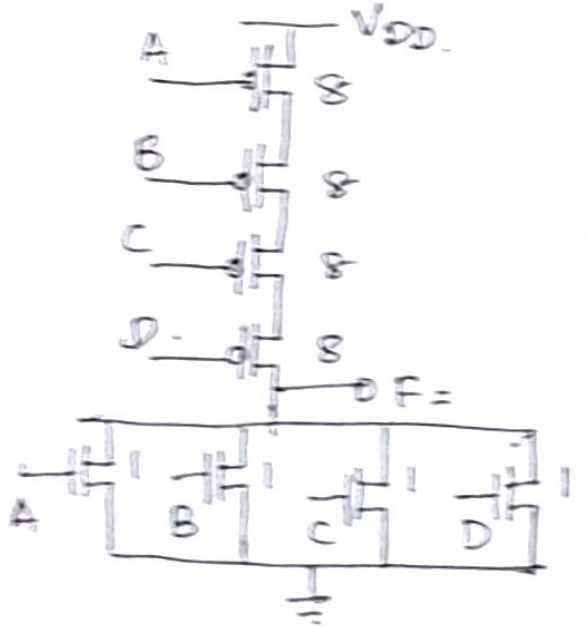
When transistors are in parallel their resistance is same.

When width = 2w, their resistance is R/2 when they are in series.

Find the LE of 3 input NAND gate & 4 input NOR gate.



LE = 5/3.



$$= \frac{8+1}{3} = \frac{9}{3}$$