DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD - 31

LESSON PLAN

M.E. (ES & VLSI Design), I-Semester Academic Year : 2020-21
Name of the Faculty : Prof. E. Sreenivasa Rao
Name of the Course : Advanced Computer Organization
Course Code : PI20PE110EC

S. No.	Topic(s) to be covered	No. of Hours	Cumulative Hours	Date
UNIT-I : Processor Design Techniques				
1.	Motivation class and Introduction to Computer Organization	1	1	22.12.2020
2.	Review of Data representation techniques in digital computers	1	2	23.12.2020
3.	Concept of Application Processing Unit , A note on the ARM processing model	1	3	24.12.2020
4.	Basic concepts of Linear pipeline and super pipeline processors	1	4	29.12.2020
5.	Advanced concepts of Superscalar and super pipeline processors	1	5	30.12.2020
6.	Performance metrics and comparison of different pipeline processors	1	6	31.12.2020
7.	**Flipped class:** Issues in pipeline design: Pipeline stalls and Pipeline hazards, Techniques for reducing pipeline penalties	1	7	05.01.2021
8.	**QUIZ-I test, Details of Tool Based Assignment-I**	1	8	06.01.2021
UNIT-II : Control Unit Design				
9.	Basic Concepts of control unit design and approaches used for control unit design, Hardwired Control Unit organization , its advantages and limitations	1	9	07.01.2021
10.	Block diagram of Micro programmed control unit organization and its principle of operation, Design concepts of Micro-programmed Control Unit : address sequencing logic	1	10	12.01.2021
11.	Design of Micro instruction sequencing for micro control unit	1	11	19.01.2021
12.	Case study of micro programmed control unit design	1	12	20.01.2021
13.	Comparison of hardwired and micro programmed control unit design approaches	1	13	21.01.2021
14.	**Design based class:** Processor Selection Criteria, Case studies on MicroBlaze Processor and Discrete FPGA-Processor	1	14	27.01.2021
15.	**QUIZ-II test, Details of Tool Based Assignment-II**	1	15	28.01.2021
UNIT-III : Memory Organization				
16.	Memory hierarchy in computer systems and performance parameters of memory, Organization of random access memory	1	16	02.02.2021
17.	Elements of cache memory design, Advanced concepts of cache memory organization	1	17	03.02.2021
18.	Analysis and comparison of Cache memory mapping techniques	1	18	04.02.2021
19.	**1st Internal Examination**	1	19	09.02.2021
20.	**1st Internal Examination**	1	20	10.02.2021
21.	**1st Internal Examination**	1	21	11.02.2021
22.	Concepts of virtual memory organization	1	22	16.02.2021

S. No.	Topic(s) to be covered	No. of Hours	Cumulative Hours	Date
23.	Protection and examples of virtual memory	1	23	17.02.2021
24.	**Tool based class:** Page replacement algorithms: Estimation of page faults	1	24	18.02.2021
25.	Analysis and performance comparison of Page replacement algorithms	1	25	23.02.2021
UNIT-IV : Input-Output Organization				
26.	Basic concepts of I/O interface, I/O Bus and accessing I/O devices, I/O mapped I/O Vs. Memory mapped I/O,	1	26	24.02.2021
27.	Modes of I/O Transfer : Programmed I/O technique, Interrupt driven I/O techniques, Daisy chaining and parallel priority interrupt technique	1	27	25.02.2021
28.	Modes of I/O Transfer : Direct memory Access, DMA controller and data transfer using DMA controller	1	28	02.03.2021
29.	**Case Studies class:** Serial bus communication protocols: USB bus protocol, Inter Integrated Circuit (I^2C) bus protocol, Controller Area Network (CAN) bus protocol	1	29	03.03.2021
30.	**Simulation based class:** Programmable Logic Interfaces, AXI Standard, AXI Interconnects and Interfaces	1	30	04.03.2021
31.	**Application based class:** Application of Processing system External Interfaces	1	31	09.03.2021
32.	**QUIZ-III test, Details of Assignment-III**	1	32	10.03.2021
UNIT-V : Parallel Computer Systems				
33.	Key concepts of Instruction Level Parallelism (ILP) organization, Concepts of thread level parallelism	1	33	16.03.2021
34.	Characteristic features of Multi-processors, Symmetric and Distributive Shared Memory Architectures	1	34	17.03.2021
35.	Basic concepts and key performance parameters of Vector Processors and super computer systems	1	35	18.03.2021
36.	Attached array processor organization and SIMD array processor organization	1	36	23.03.2021
37.	Characteristic features and performance parameters of SIMD and Super Computers	1	37	24.03.2021
38.	**Case Studies class:** High Performance Computing(HPC), Case study on advanced processing system, An Overview of HPC Applications.	1	38	25.03.2021
39.	**Seminars Presentation:** Advances in multi core processors : Dual, Quad and Octa and Deca core processors for general purpose applications	1	39	30.03.2021
40.	**Application Based:** Applications of multi core processors for embedded applications	1	40	31.03.2021
41.	**2nd Internal Examination**	1	41	06.04.2021
42.	**2nd Internal Examination**	1	42	07.04.2021
43.	**2nd Internal Examination**	1	43	08.04.2021

Signature of the Faculty **Signature of the HoD** **Signature of Principal**

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COURSE PLAN

M.E. (ES & VLSI Design), I-Semester Academic Year: 2020 - 21
Name of the Faculty : Prof. E. Sreenivasa Rao
Name of the Course : Advanced Computer Organization
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S. No.	Unit No.	Brief details of each Unit	No. of Hours required
1	I	Review of Computer Arithmetic, Application Processing Unit , A Note on the ARM processor Model, Standard Processor versus Processing system **Processor Design Techniques:** Instruction Pipelining, Super Scalar techniques, Super scalar and super pipeline design, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.	7
2	II	**Control Unit Design approaches:** Hardwired Control Unit Design approach, Micro-programmed Control Unit Design Approach, Processor Selection Criteria, Case studies on MicroBlaze Processor, Discrete FPGA-Processor.	6
3	III	**Memory Organization:** Memory Organization: the memory Hierarchy, Random access memories, Cache memory, Elements of cache design, Virtual memory- protection and examples of virtual memory, Replacement Policies.	7
4	IV	**I-O Organization**: I-O Organization: Accessing I/O Devices, Programmed I-O, Interrupts, DMA, Synchronous bus and asynchronous bus, IO Processor, General Purpose Input/Output ,Communications Interfaces,Programmable Logic Interfaces, AXI Standard, AXI Interconnects and Interfaces, Processing System External Interfaces.	6
5	V	**Parallel Computer Systems:** Instruction Level Parallelism (ILP) , Multi-processors – Characteristics, Symmetric and Distributive Shared Memory Architecture, Vector Processors, SIMD computers and Super computers, High Performance Computing(HPC), Case study on advanced processing system, An Overview of HPC Applications.	8
6	**QUIZZES, ASSIGNMENTS**		3
7	**INTERNAL EXAMINATIONS**		3+3
		Total	**43**

Signature of the Faculty **Signature of the HOD** **Signature of Principal**