DEPARTMENT OF ECE

VASAVI COLLEGE OF ENGINEERING (A)

Embedded System Design

[2020 – 2021]

Handout – Unit – 2 (Part – 1)

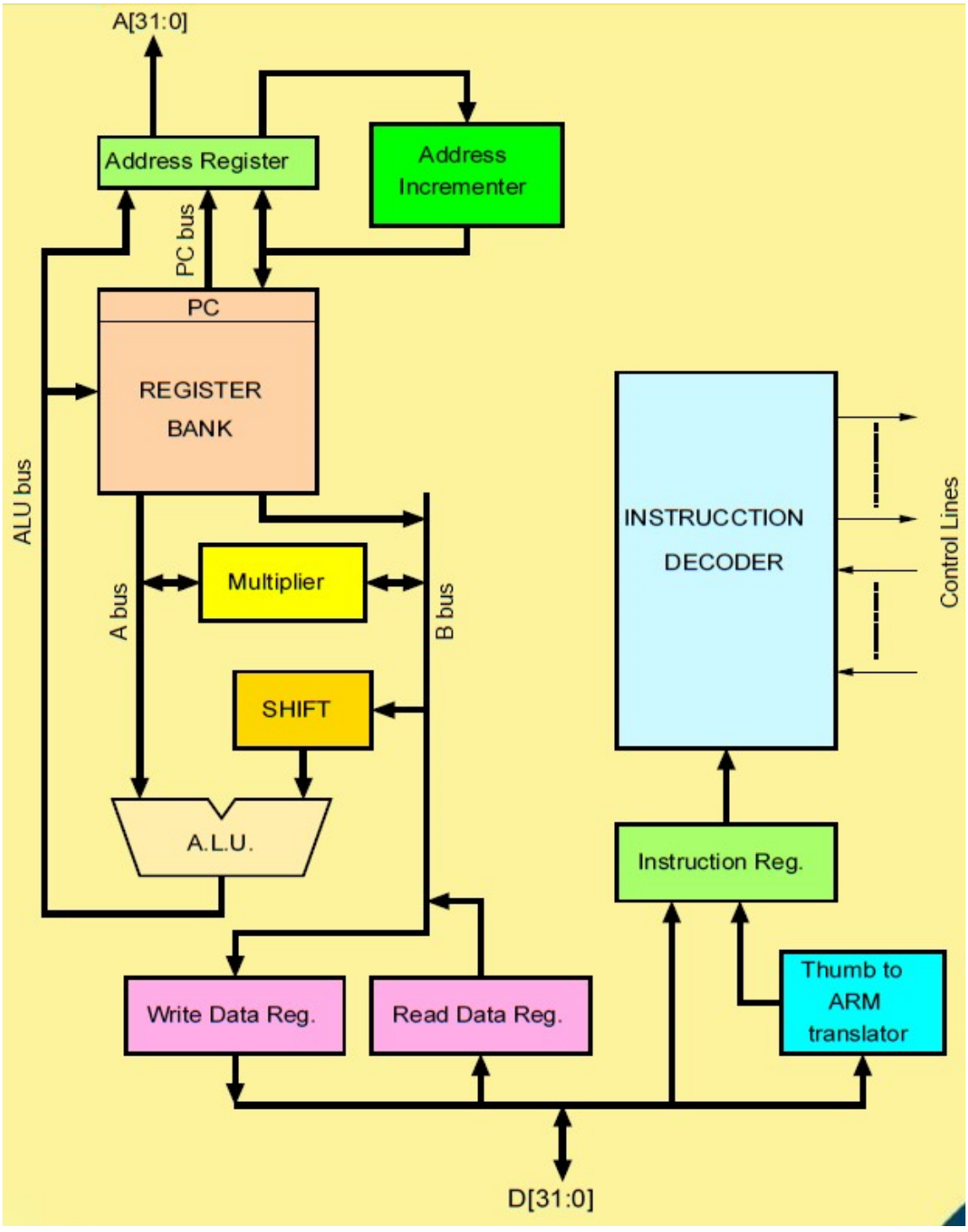
Faculty: N Abid Ali Khan	Program: ME	Branch: **ESVLSID**		SEE Marks: **60**	Classes: 3Hrs/Week
Course Code: PI20PC110EC	Year: **First**	Sem–**I**	Credits: **3**	CIE Marks: **40**	Duration of SEE: **3 Hours**

Background/Motivation:

- ARM acronym - Advanced RISC Machine (RISC - Reduced Instruction Set Computer)
- ARM is not a microprocessor or microcontroller, it is a Core.
- History (or) Background:
  - Initially this company was named as Acron, which was working for designing a RISC CPU for providing low-cost computer to school children to UK.
  - Apparently, Apple was interested in usage of its architecture for their upcoming PDA product. In 1990 November, this company was named as ARM with a different working philosophy in contrast to other IC fab firms.
- ARM design Philosophy: the design engineers of ARM will provide the ARM version CPU in the form of libraries so that if any IC manufacture firm is interested in their requirement they may use it in their designs and also extends the support for development environments (IDE) and other software tools with technical support. ARM company does not bother about manufacturing of ICs.
- Any IC fab firm if is interested to make use of ARM CPU, they have to join ARM Technology Access Program (ATAP) partnership model. Later, ARM will issues two types of licenses:
- Hard-view License:
  - RTL and Synthesis flows
  - Digital State Machine (DSM) models will be provided
  - Licenses to Original Equipment Manufactures (OEM)
  - Less cost
- Soft-view License:
  - GDSII layout
  - Gate-level netlists libraries are provided
  - Licenses to VLSI design and service companies
  - Expensive
- ARM Nomenclature of ARM{x}{y}{z}TDMIEJZFH–S
  - X - series of the CPU being used in RISC engine
  - Y - number of MMU units supports
  - Z - Number of Cache memory units
  - T - Thumb mode support (16 - bit CPU mode for low-power consumption)
  - D - On chip debugging (IAP - In Application Programming)
  - M - Hardware built in multiplier
  - I - Embedded In Circuit Emulator support
  - E - Enhanced instruction supports with DSP computations

- J - Java Byte Code (JBX) of 8-bits opcode with Java Virtual Machine (JVM)
- Z - Trust Zone support through boundary scanning
- F - support for floating point arithmetic ALU
- H - Handshake, clock-less MCU design.

ARM CPU Engine Architecture



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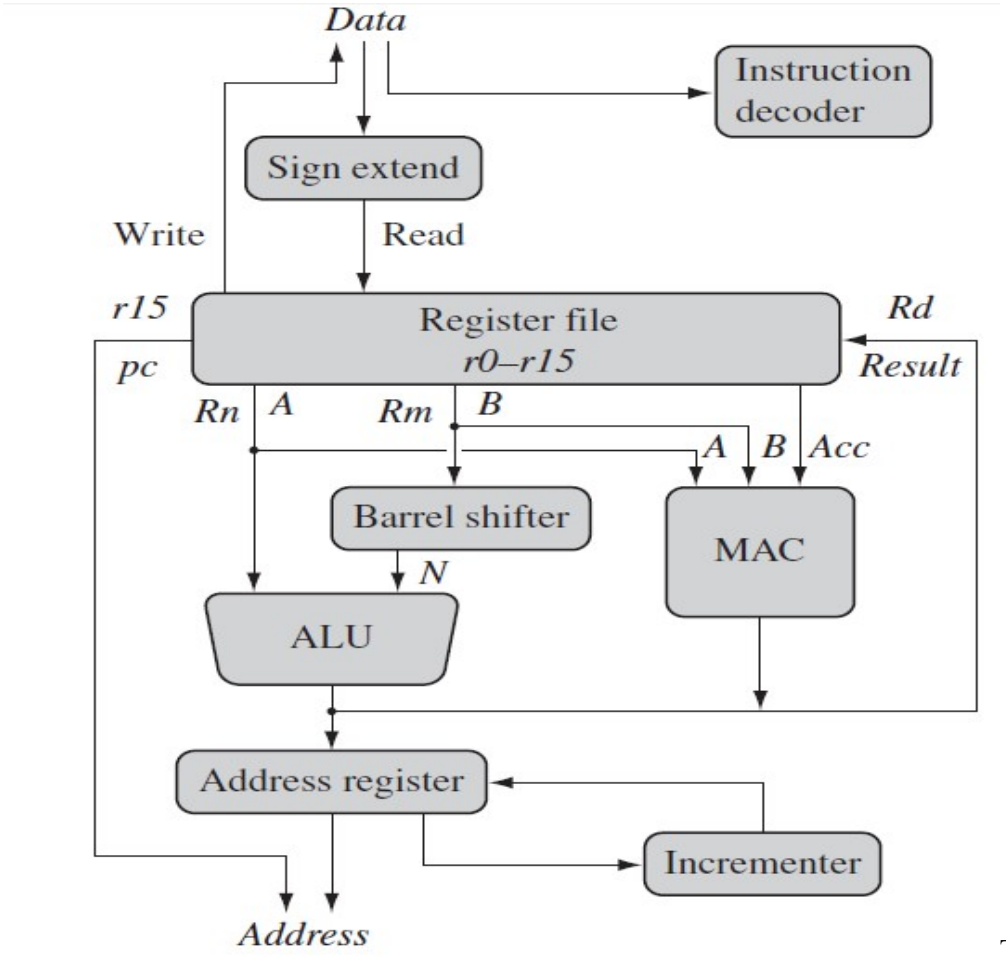
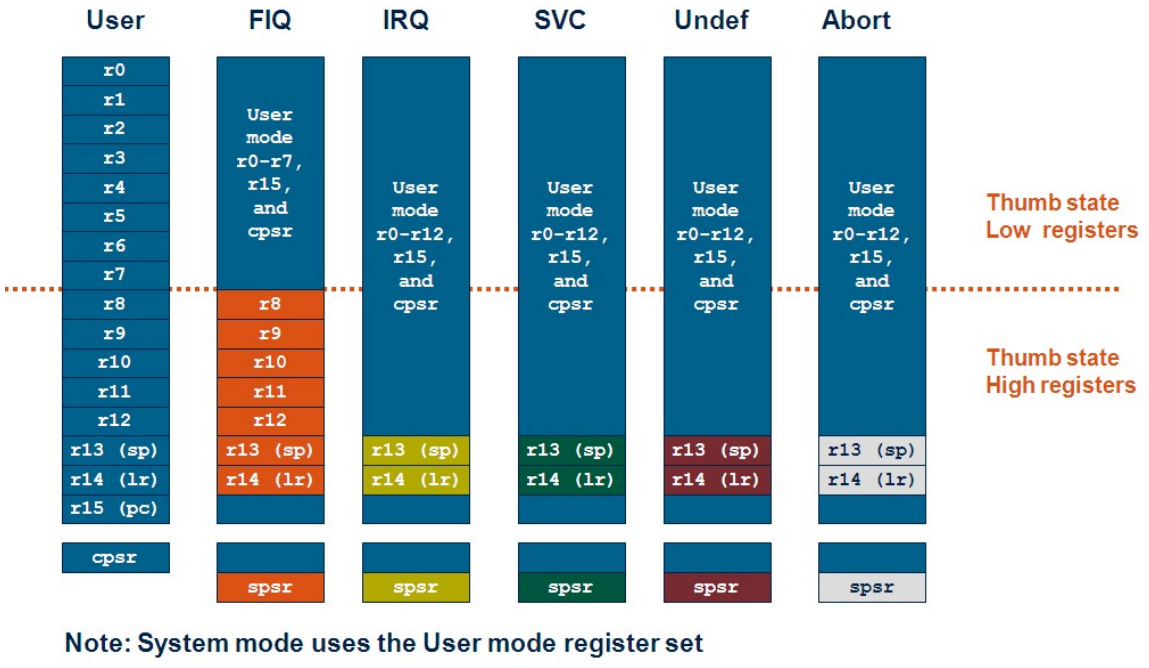
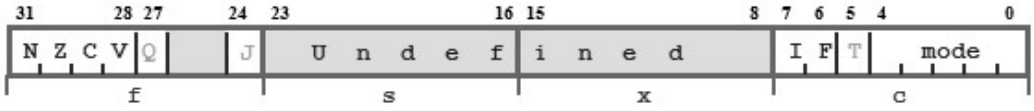


Thumb-2 (8-bit)

ARM programming model and ARM registers:,





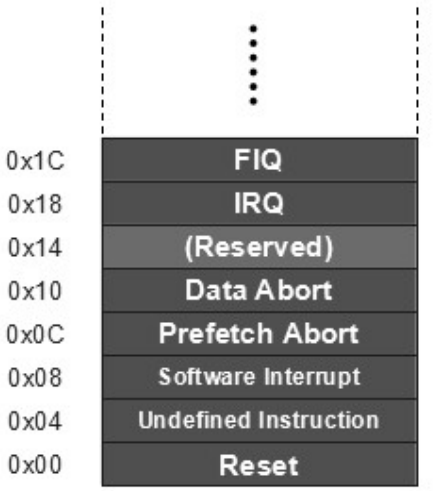
- **Condition code flags**
  - N = Negative result from ALU
  - Z = Zero result from ALU
  - C = ALU operation Carried out
  - V = ALU operation oVerflowed
- Sticky Overflow flag - Q flag
  - Architecture 5TE/J only
  - Indicates if saturation has occurred
- J bit
  - Architecture 5TEJ only
  - J = 1: Processor in Jazelle state
- **Interrupt Disable bits.**
  - I = 1: Disables the IRQ.
  - F = 1: Disables the FIQ.
- T Bit
  - Architecture xT only
  - T = 0: Processor in ARM state
  - T = 1: Processor in Thumb state
- **Mode bits**
  - Specify the processor mode

Mode	Abbreviation	Privileged	Mode[4:0]
Abort	abt	yes	10111
Fast interrupt request	fiq	yes	10001
Interrupt request	irq	yes	10010
Supervisor	svc	yes	10011
System	sys	yes	11111
Undefined	und	yes	11011
User	usr	no	10000

- The current processor mode governs which of several banks is accessible. Each mode can access
  - a particular set of r0-r12 registers
  - a particular r13 (the stack pointer, SP) and r14 (the link register, LR)
  - the program counter, r15 (PC)
  - the current program status register, CPSR
- Privileged modes (except System) can also access a particular SPSR (saved program status register)
- ARM CPU Family based Microprocessors Examples:
  - Microcontroller: LPC2148 (Powered by LPC2148)
  - Microprocessor: S3C26410 (Powered by ARM1176JZF-S) OR Raspberry Pi 2/3
  - MSP432 from TI powered by ARM Cortex M4
  - Kinetis NXP's MK66 ARM Cortex M4F Microprocessor
  - FPGA based Platform with ARM Cortex A9 as soft IP core in Zynq 7000/7100.

- **When an exception occurs, the ARM:**
  - Copies CPSR into SPSR_<mode>
  - Sets appropriate CPSR bits
    - Change to ARM state
    - Change to exception mode
    - Disable interrupts (if appropriate)
  - Stores the return address in LR_<mode>
  - Sets PC to vector address
- **To return, exception handler needs to:**
  - Restore CPSR from SPSR_<mode>
  - Restore PC from LR_<mode>

This can only be done in ARM state.



Vector Table

Vector table can be at
0xFFFF0000 on ARM720T
and on ARM9/10 family devices

Additional Learning Resources:

[1] ARM System Developer's Guide: Designing and Optimizing System Software (The Morgan Kaufmann Series in Computer Architecture and Design) 1st Edition by Andrew Sloss (Author), Dominic Symes (Author), Chris Wright (Author)

[2] Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C: Third Edition Paperback – July 1, 2017 by Yifeng Zhu (Author)

[3] Embedded Systems Fundamentals with ARM Cortex-M based Microcontrollers: A Practical Approach by Alexander G Dean (Author)

[4] The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors 3rd Edition by Joseph Yiu (Author)