

MN3005 4096-STAGE LONG DELAY BBD

Product Specification

Specification Revision History:

Version	Data	Description
2015-04-A1	2015-04	New-made





1. General Description

The MN3005 is world's first 4096-stage long delay BBD,8 times longer than 512-stage BBD manufactured by using a P-channel low noise silicon gate process.

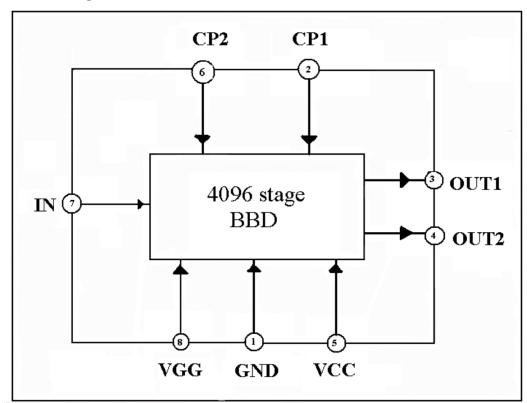
Long signal delay time 205ms can be obtained at clock frequency 10KHz.S/N is 75dB. S/N has been improved by more than 20dB in comparting with 8-connected 512-stage BBD's. The MN3005 is suitably used for reverberation and echo effects in electronic musical instruments such as electronic organ, guitar amplifier and music synthesizer which need long delay time.

Features:

- 1 chip 4096 stage and wide range of variable delay times: 20.48~204.8ms.
- High S/N in spite of multi-stage and wide dynamic range: S/N≈75dB typ.
- No insertion loss since the loss occurring in the signal transfer is corrected by the MOS capacity of input and output. Li = 0dB.
- High integration and high reliability by using P channel low noise silicon gate process.
- Special 8 lead dual-in-line plastic package.

2. Block Diagram And Pin Description

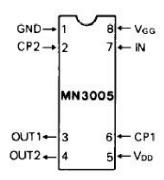
2.1 Block Diagram







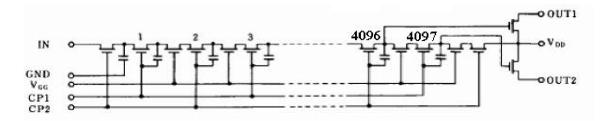
2.2. Pin Configurations



2.3 Pin Description

Pin No.	Pin Name	Description				
1	GND	Ground Pin				
2	CP2	Clock input Pin				
3	OUT1	Signal output Pin				
4	OUT2	Signal output Pin				
5	VDD	Power supply pin				
6	CP1	Clock input Pin				
7	IN	Signal input Pin				
8	VGG	Bar voltage				

2.4 Circuit Diagram



3. Electrical Parameter

3.1. Absolute Maximum Ratings

(Ta=25°C)

Characteristic	Symbol	Symbol Conditions		Unit
Terminal voltage	$V_{DD}, V_{GG}, V_{CP}, V_{I}$		-18~+0.3	V
Output voltage	Vo		-18~+0.3	V
Operating temperature	Topr		-20~+60	$^{\circ}$
Storage temperature	Tstg		-55~+125	$^{\circ}$





3.2. Operating Conditions

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Drain Supply Voltage	V_{DD}		-14	-15	-16	V
Gate Supply Voltage	V_{GG}			VDD+1		V
Clock Voltage "H" Level	V_{CPH}		0		-1	V
Clock Voltage "L" Level	V _{CPL}			VDD		V
Clock Input Capacitance	V _{CP}				2800	pF
Clock Frequency	Fcp		10		100	kHz
Clock Pulse Width *2	T_{CPW}	Test Circuit			0.5T*2	
Clock Rise Time *2	Tepr	Test Circuit			500	ns
Clock Fall Time *2	Tepf	Test Circuit			500	ns
Clock Cross Point	Vx		0		-3	V
Input DC Bias Voltage	V		-5		-10	V

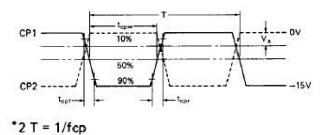
3.3, Electrical Characteristics

(Ta=25°C , VDD=V_{CPL}=-15V,V_{CPH}=0V,VGG=-14V, ~R_L=100k Ω)

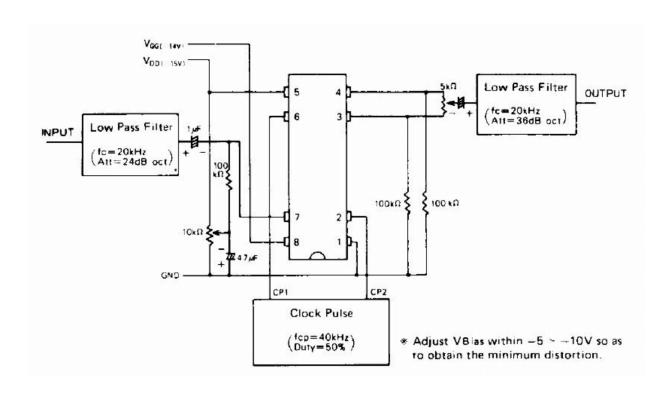
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Signal Delay Time	t_{D}		20.48		204.8	ms
Input Signal Frequency	fi	Fcp=40kHz,Vi=1Vrms,Output Attenuation ≤ 3dB	10			KHz
Input Signal Swing	Vi	Fcp=40kHz,fi=1kHz,THD=2.5%	0.9			Vrms
Insertion Loss	Li	Fcp=40kHz,fi=1kHz,Vi=1Vrms	-4	0	4	dB
Total Harmonic Distortion	THD	Fcp=40kHz,fi=1kHz,Vi=0.78Vrms		2.5	4	%
Noise Voltage	Vno	Fcp=100kHz weighted by "A" curve			0.8	mVrms
Signal to Noise Ratio	S/N			75		dB



3.4 Clock Pulse Waveforms



4. Testing Circuit

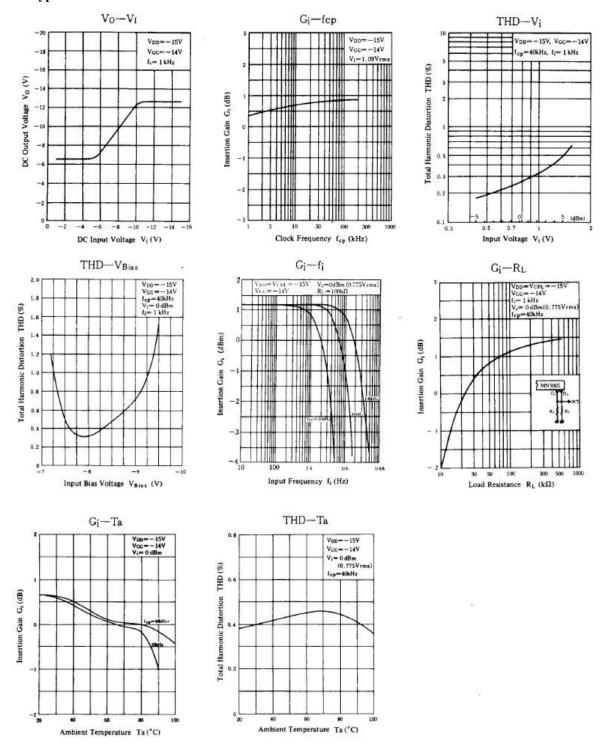






5. Characteristic Curve

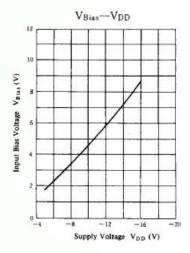
5.1. Typical Electrical Characteristic Curves

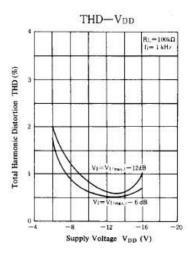


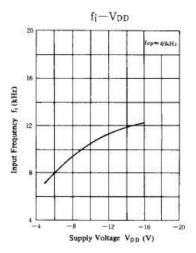


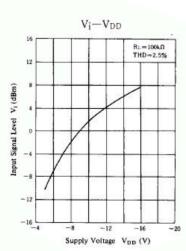


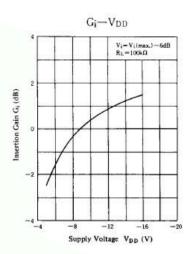
5.2. Supply Voltage Characteristics

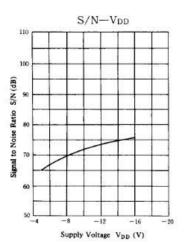








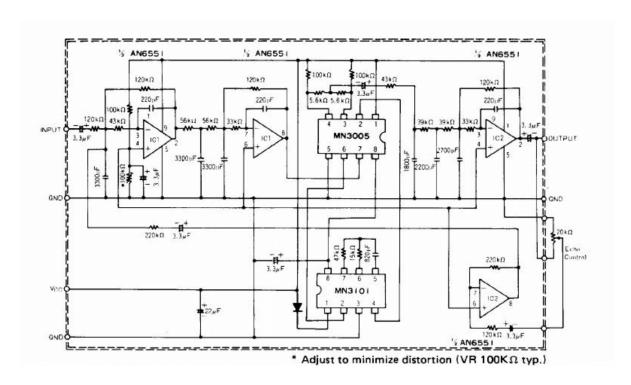








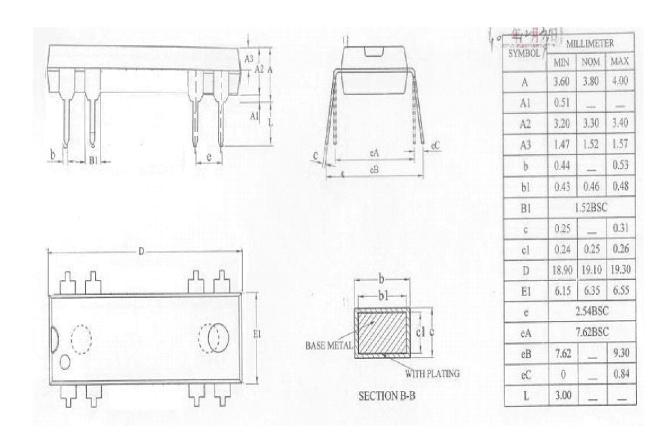
6. Typical Application Circuit





7. Package Information

7.1, PDIP14(C)







8. Statements And Notes:

8.1. The name and content of Hazardous substances or Elements in the product

	Hazardous substances or Elements							
Part name	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers		
Lead frame	0	0	0	0	0	0		
Plastic resin	0	0	0	0	0	0		
Chip	0	0	0	0	0	0		
The lead	0	0	0	0	0	0		
Plastic sheet installed	0 0 0 0 0							
	o: Indicates that the content of hazardous substances or elements in the detection limit							
explanation	of the following the SJ/T11363-2006 standard.							
	×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.							

8.2. Notion:

Recommended carefully reading this information before the use of this product;

The information in this document are subject to change without notice;

This information is using to the reference only, the company is not responsible for any loss;

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.