

LLVM Developers' Meeting 2025

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Mojo🔥 is a Pythonic **Systems Programming** Language Unified programming for CPU + GPU in one language

- Extensive generic programming, type system, and memory safety
- Blazing fast
- Best way to extend Python to CPUs and GPUs
- Bedrock for the MAX inference engine
- Full power of standard CUDA/ROCm, but “without CUDA”
  - Threads, warps, sync primitives, WMMA instructions
  - Generate executables without using vendor toolkits or libraries
- All GPU kernels for Nvidia, AMD, Apple in Mojo
- Library driven GPU compilation and kernel features
- MLIR unlocks seamless compiler integration
  - Mojo as MLIR sugar to extend language syntax but no parser change
- Leverage LLVM for different backends
- Simple compiler, no heroic magic

## CPU Host Code in Mojo

```

static_assert(
    GPU DeviceContext
GPU device buffers
GPU tensors
compile and launch GPU kernel
device buffer to host

```

```
def main():
    constrained[has_accelerator()], "This example requires a supported GPU")()

    # Get context for the attached GPU
    var ctx = DeviceContext()

    # Allocate data on the GPU address space
    var lhs_buffer = ctx.enqueue_create_buffer[float_dtype](VECTOR_WIDTH)
    var rhs_buffer = ctx.enqueue_create_buffer[float_dtype](VECTOR_WIDTH)
    var out_buffer = ctx.enqueue_create_buffer[float_dtype](VECTOR_WIDTH)

    # Fill in values across the entire width
    _ = lhs_buffer.enqueue_fill(1.25)
    _ = rhs_buffer.enqueue_fill(2.5)

    # Wrap the device buffers in tensors
    var lhs_tensor = LayoutTensor[float_dtype, layout](lhs_buffer)
    var rhs_tensor = LayoutTensor[float_dtype, layout](rhs_buffer)
    var out_tensor = LayoutTensor[float_dtype, layout](out_buffer)

    # Calculate the number of blocks needed to cover the vector
    var grid_dim = ceildiv(VECTOR_WIDTH, BLOCK_SIZE)

    # Launch the vector-addition function as a GPU kernel
    ctx.enqueue_function_checked[vector_addition, vector_addition]()
    lhs_tensor,
    rhs_tensor,
    out_tensor,
    VECTOR_WIDTH,
    grid_dim=grid_dim,
    block_dim=BLOCK_SIZE,
    )

    # Map to host so that values can be printed from the CPU
    with out_buffer.map.to_host() as host_buffer:
        var host_tensor = LayoutTensor[float_dtype, layout](host_buffer)
        print("Resulting vector: ", host_tensor)
```

## GPU Code in Mojo

```
from math import ceildiv
from sys import has_accelerator
from gpu import global_idx
from gpu.host import DeviceContext
from layout import Layout, LayoutTensor

alias float_dtype = DType.float32
alias VECTOR_WIDTH = 10
alias BLOCK_SIZE = 5
alias layout = Layout.row_major(VECTOR_WIDTH)

fn vector_addition(
  lhs_tensor: LayoutTensor[float_dtype, layout, MutableAnyOrigin],
  rhs_tensor: LayoutTensor[float_dtype, layout, MutableAnyOrigin],
  out_tensor: LayoutTensor[float_dtype, layout, MutableAnyOrigin],
  size: Int,
):
  """The calculation to perform across the vector on the GPU."""
  var global_tid = global_idx.x
  if global_tid < UInt(size):
    out_tensor[global_tid] = lhs_tensor[global_tid] + rhs_tensor[global_tid]
```

```
#
#
# thread_idx
#
#

@register_passable("trivial")
struct ThreadIdx(DefaultTable):
    """ThreadIdx provides static methods for getting the x/y/z coordinates
    a thread within a block."""

    @always_inline("nodebug")
    fn __init__(out Self):
        return

    @always_inline("nodebug")
    @staticmethod
    fn _get_intrinsic_name(dim: StringLiteral[]) -> StaticString:
        @parameter
        if is_nvidia_gpu():
            return "llvm.nvvm.read.ptx.sreg.tid." + dim
        elif is_amd_gpu():
            return "llvm.amdgcn.workitem.id." + dim
        elif is_apple_gpu():
            return "llvm.air.thread_position_in_threadgroup." + dim
        else:
            return ConstantTarget.UnsupportedTargetError[
                StaticString,
                operation="thread_idx field access",
            ]()

    1()

    @always_inline("nodebug")
    fn _getattr__dim: StringLiteral(self) -> UInt:
        """Gets the 'x', 'y', or 'z' coordinates of a thread within a block.

        Returns:
            The 'x', 'y', or 'z' coordinates of a thread within a block.

            """
        _verify_xyz[dim]()
        alias intrinsic_name = Self._get_intrinsic_name[dim]()
        return UInt(
            llvm_intrinsic(intrinsic_name, UInt32, has_side_effect=False)()
        )

alias thread_idx = _ThreadIdx()
```

[illegible]

## Compiling GPU offload in Mojo Compilation Pipeline

```
module attributes (M.target_info = MM.target<triple = "nvptx64-nvidia-cuda", arch = "sm_80", simd_bit_width = 128, index_bit_width = 64, tune_cpu = "sm_80">, kgen.env = <$kgen.env>{> {
  kgen.generator export @hello() : !kgen.module attributes (LLVMMetadataArray = ["kgen.offload.kernelId", 0 : index]) {
    !none = kgen.param.constant none = <$kgen.none>
    kgen.return !none : !kgen.none
  }
}
```

Input Mojo Program  
Host + GPU

[illegible]

## Slice out GPU Module

## PTX output

## Host code with compiled offload PTX

The diagram illustrates the Mojo compiler pipeline. It starts with the input `*.mojo (*.tm)` (red text). The main processing stage is a light blue box labeled **MojoParser** (green text). Inside this box, the flow is: `Parameter Domain IR` → `Optimized Parameter Domain IR` (accompanied by a Mojo logo icon) → `Materialized IR` → `LLVM Dialect`. To the right of this box, the stages are labeled: `Pre-elaboration opt` (green text) between the first two IR stages, `Elaboration (template instantiation)` (green text) between the second and third IR stages, and `Post-elaboration opt` (green text) between the third and fourth IR stages. Below the main box is a yellow box labeled **llvm pipeline** (blue text), which contains the `LLVM IR` stage (accompanied by an LLVM logo icon). A red arrow points from the `LLVM IR` stage to the output `*.o` (red text). To the right of the main box, a series of GPU compilation blocks are shown. Each block is a light blue box labeled **GPU compilation** (green text). The first block is labeled `kernel_0.mlr` (red text) and contains a Mojo logo icon, a `ptx/cubin 0` label (red text), and an LLVM logo icon. The second block is labeled `kernel_1.mlr` (red text) and contains a Mojo logo icon, a `ptx/cubin 1` label (red text), and an LLVM logo icon. An ellipsis (...) indicates more blocks, followed by a block labeled `kernel_n.mlr` (red text) containing a Mojo logo icon, a `ptx/cubin n` label (red text), and an LLVM logo icon. Dashed purple arrows show the flow of intermediate representations: from `Optimized Parameter Domain IR` to the first GPU compilation block, from `Materialized IR` to the second GPU compilation block, and from `LLVM Dialect` to the `n`-th GPU compilation block.

Multiple GPU kernels in one  
Mojo program or an MAX  
Model.

- Slice each kernel out to run full GPU pipeline.
- Ease to debug each kernel for lowering from input MLIR to LLVM. ✓
- Efficient to cache compiled kernels if they will be used in another program or model. ✓
- Logically easy to maintain.

Multiple GPU kernels in one Mojo program or an MAX Model.

- Slice out one GPU model with all the GPU kernels.
- Only run MLIR pipeline once instead of per kernel. ✓
- Split each kernel into separate LLVM modules to run backend pipeline in parallel. \* ✓
- Can cache LLVM compilation for kernels if they will be used in another program or model.
- Faster compilation time.

The diagram illustrates the Mojo compiler pipeline. It starts with **\*.mojo** (marked with a flame icon) as input. The main processing stage is a light blue box containing the following steps:

- Parameter Domain IR**: The initial intermediate representation.
- Optimized Parameter Domain IR**: The result of the **MojoParser** and **Pre-elaboration opt**.
- Materialized IR**: The result of **Elaboration (template instantiation)**.
- LLVM Dialect**: The result of **Post-elaboration opt**.

The output of the LLVM Dialect is **LLVM IR**, which is then processed by the **llvm pipeline** (indicated by a dragon icon).

A dashed purple arrow indicates the flow from the **Materialized IR** to the **GPU compilation** stage. This stage is shown in a separate box and involves:

- GPU compilation**: The LLVM IR is converted into **kernels.mir**.
- ptx/cubin 0**, **ptx/cubin 1**, and **ptx/cubin n**: The final output of the GPU compilation stage, which are then used by the **ptx/cubin** runtime.

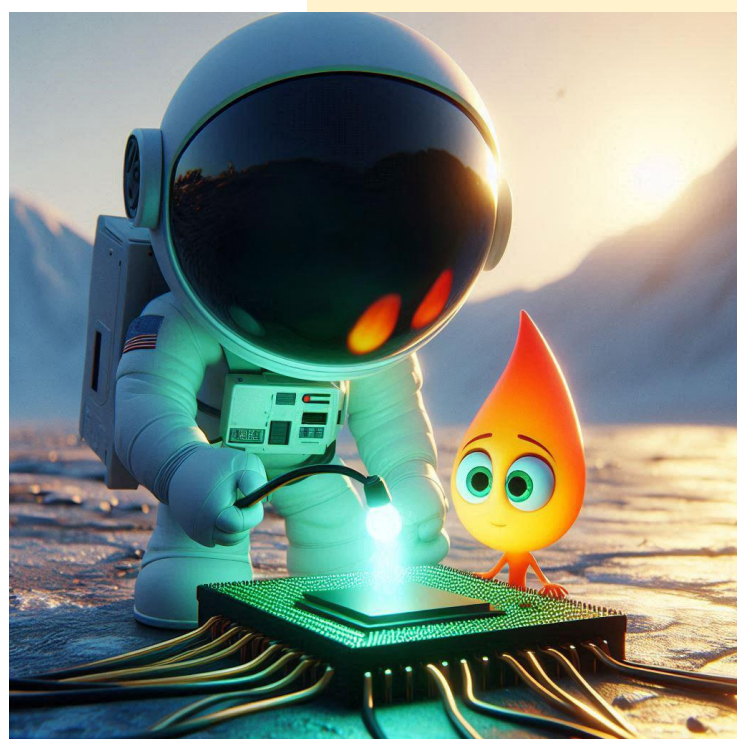
🔍 Inspecting Mojo GPU kernel in LLVM IR, assembly (PTX), or object file (cubin, hsaco, metal)

```
fn hello():
    pass

fn main():
    # compile kernel to asm.
    t1 = _compile_info(hello, emission_kind="asm"())
    print(t1.kernel)

    # compile kernel to llvm ir.
    t2 = _compile_info(hello, emission_kind="llvm"())
    print(t2.kernel)

    # compile kernel to optimized llvm ir.
    t3 = _compile_info(hello, emission_kind="llvm-opt"())
    print(t3.kernel)
```

[illegible][illegible]

```
//
// Generated by LLVM NVPTX Back-End
//
.version 8.1
.target sm_80
.address_size 64

// .globl compile_offload_hello6A6A0ApA
.compile_offload_hello6A6A0ApA

.visible .entry compile_offload_hello6A6A0ApA()
{
    ret;
}
```

[illegible]

- Mojo provides a unified way to write CPU+GPU code => **one MLIR module to LLVM**
- Library driven GPU feature implementation for different vendors => **simple compiler, leave performance magic to the programmer**
- MLIR unlocks seamless compiler integration:
  - Native compiler support to handle offloads
  - Extend language syntax through MLIR dialect and Mojo library API
  - Ease of writing library code that uses architecture specific dialects (NVVM, ROCm) and low-level intrinsics
- Compiling multiple kernels in one MLIR module and split for LLVM pipeline => **fast compilation**
- **Generally applicable** to compile other accelerator offloads built on top of LLVM/MLIR framework
- Mojo GPU kernels are open-sourced: <https://github.com/modular/modular/tree/main/max/kernels>
- pip install modular; pip install mojo

[What we've learned from building Mojo's optimization pipeline @ LLVM Dev 2024](#)  
[Parallelizing the LLVM pipeline with MCLink @ EuroLLVM 2025](#)

**Mojo 🔥** : A system programming language for heterogeneous computing @ LLVM Dev Meeting 2023