IADC - Integrating Analog to Digital Converter

Part-2
IC Design and Implementation

Digital Control Logic

Design and Verification Documentation

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1 Summary

The document is a summary of design and verification methods of digital control logic which includes the Finite state machine, Timing diagrams, and Verification plan for the Digital control block of IADC. The Digital design concept is developed considering the timing specification of analog block and different critical combinations of input voltages. The FSM (Finite state machine) describes the possible states of the digital control and also the conditions for transition from one state to other state. Finally the verification plan of the design concept is summarized.

2 Design Concept

The only input for the Digital control block from the analog block is the Vcomp signal so the state of Vcomp decides the control logic. As per the analog block specification, when the input is positive, the Vcomp is High logic.

The period of 2 clock cycles is choosen for non-overlapping of switch signals S1 and (S2a or S2b) and a reset time of 6 clock cycles is choosen for integrator reset phase (S3 switch).

When the small input signals are applied, due to the offset and noise the comparator might not switch. And for the maximum input even the comparator might not switch within the 1024 clock cycles. A logic is implemented to de-integrate for 16 more clock periods and then check the Vcomp. If the Vcomp doesnot switch even after 16 clock periods, the previous output is retained.

Also the control logic is designed in such a way that the overall conversion time is constant (2074 clock periods) and the time relation between Dout and Clkout is maintained for the measurement equipment specifications. The logic flow of which is shown in the FSM in following sections.

3 Finite State Machine

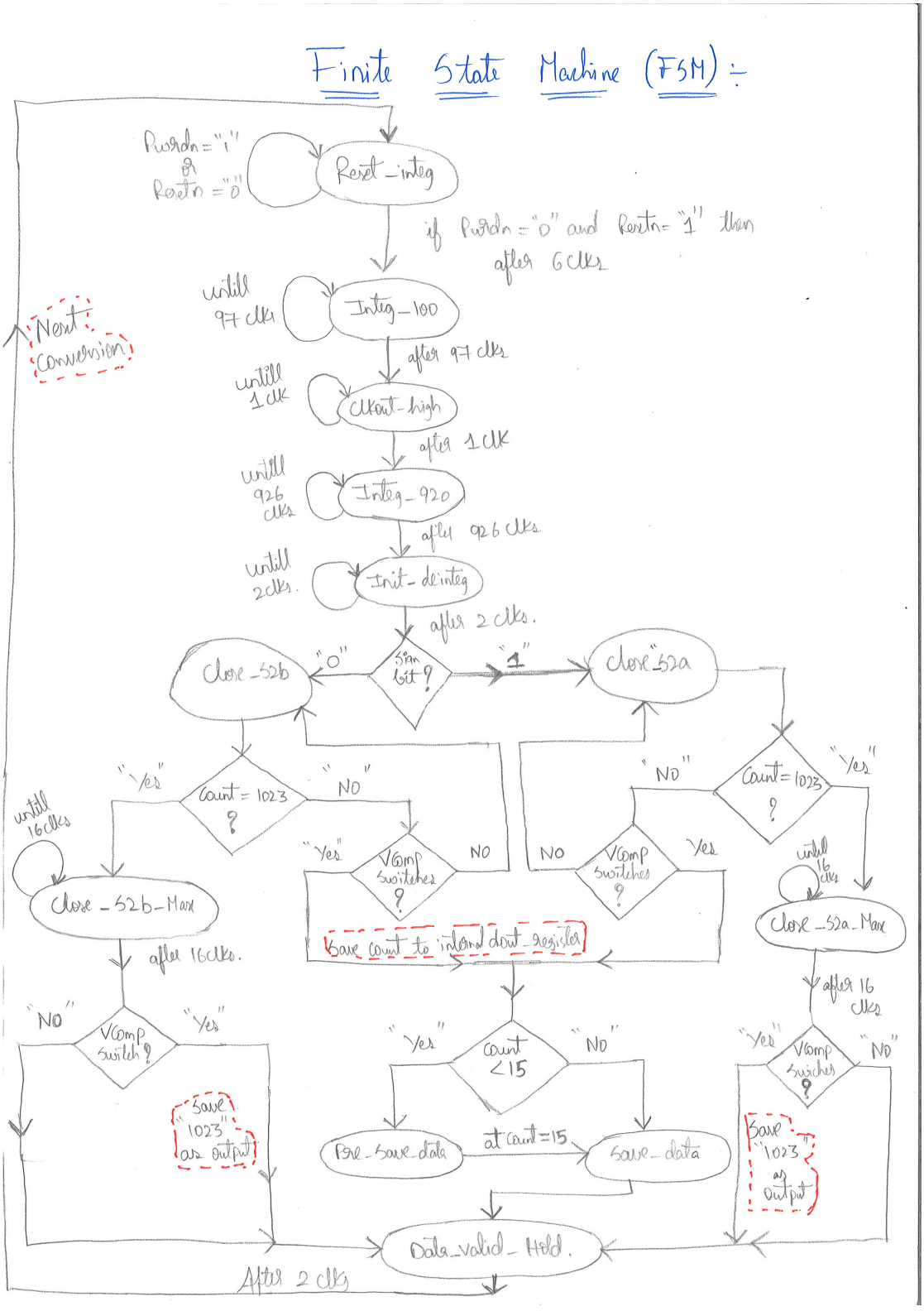

Figure 1: FSM of Digital Control BLock

4 Finite State Machine - States and Description

The FSM consists of 12 states as shown in the figure 1. An asynchronous reset is used, hence whenever the pwrdn is high or resetn is low the state transition is to reset_integ state.

The overall conversion time is 2074 clock periods. The sum of time period in the states from close_S2a or Close_S2b till data_valid_hold is 1040 clks. The states, description and time period for each state is given below:

State	**Description**	**Clock periods in this state**
reset_integ	Reset phase before the integration	6 clks after Pwrdn=0 and resetn = "1"
integ_100	Integration for 97 Clks to have Dout to Clkout time	97 Clks
clkout_high	Set Clkout to High	1 Clk
integ_920	Integration for remaining 926 Clks	926 Clks
init_deinteg	Non-Overlapping of S1 and (S2a or S2b) switches	2 Clks
close_S2b	De-integration with positive reference voltage	Maximum 1024 Clks
close_S2a	De-integration with negative reference voltage	Maximum 1024 Clks
close_S2b_max	De-integration with positive reference voltage for 16 more clks	16 Clks
close_S2a_max	De-integration with negative reference voltage for 16 more clks	16 Clks
pre_save_data	To ensure same conversion time for small inputs conflicting with S2amax or S2bmax	Untill count is 15
save_data	Assign the data to Dout register at the same time as from S2amax or S2bmax states	Remaining time period of conversion
data_valid_hold	Recover state before next conversion	2 Clks

5 Timing Diagrams

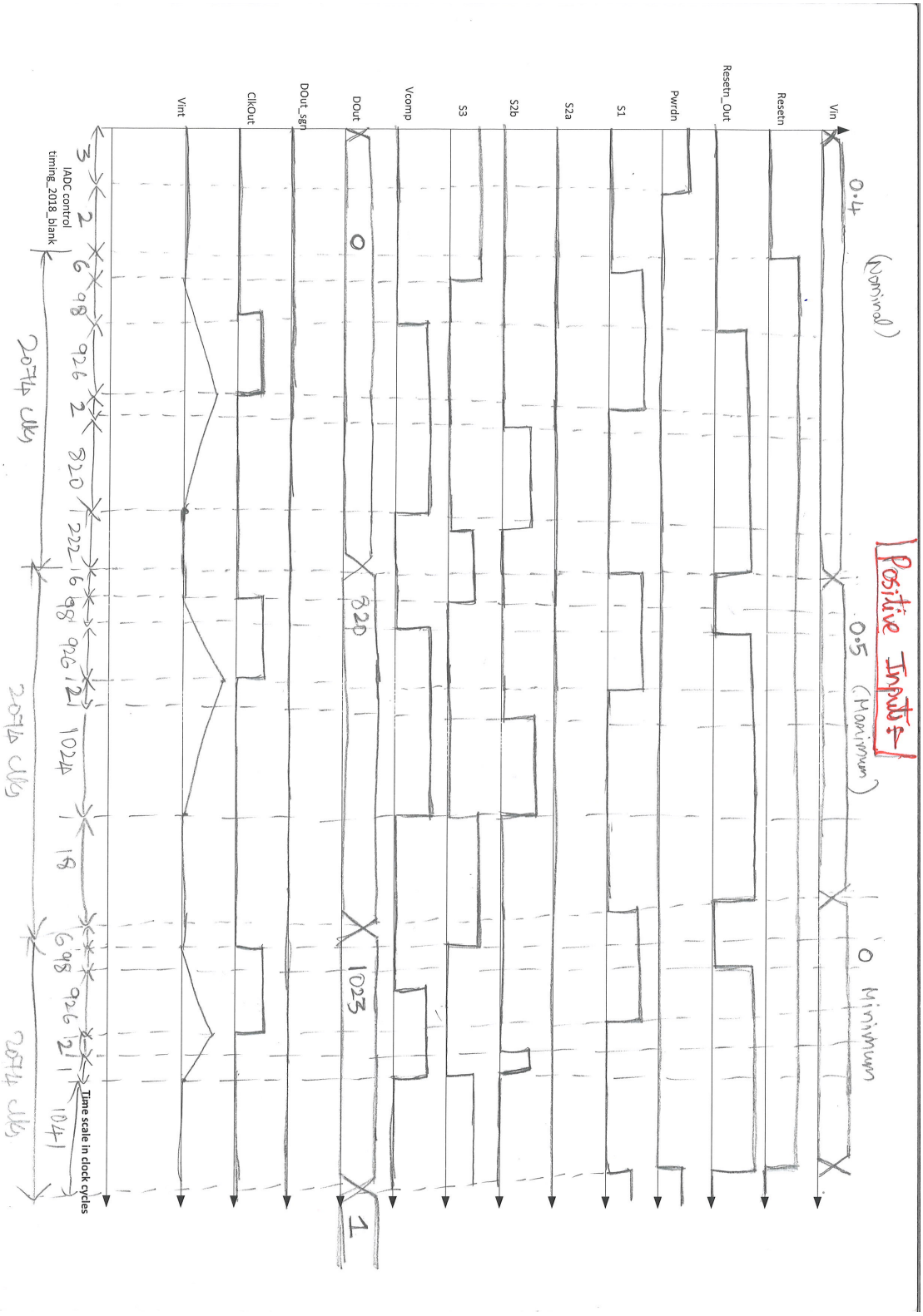

Figure 2: Timing Diagram for Positive Inputs

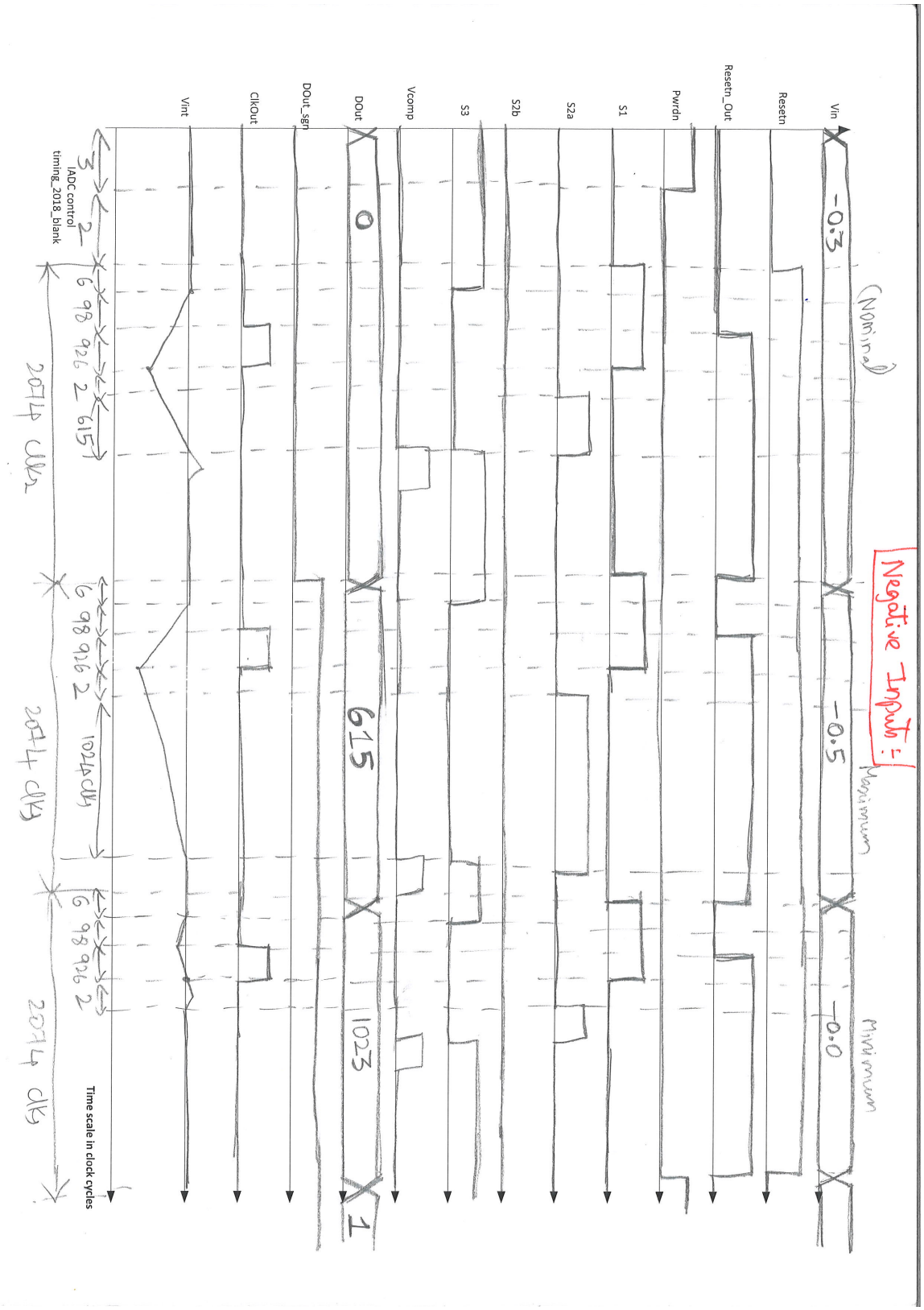

Figure 3: Timing Diagram for Negative Inputs

6 Verification Plan

Test Case	Setup Conditions	Expected Result	Observed Results Matched Yes/NO
Simulation of startup behaviour	resetn = "0" and pwrdwn = "1"	Dout=0 Dout_sgn=0 S1=0 S2a=0 S2b=0 S3=1 Clkout=0 and Resetn_Out=0	Yes
Simulation of nominal positive input	Input=0.4V	Dout=820 Dout_sgn=0	Yes
Simulation of small positive input	Input=0.006V	Dout=13 Dout_sgn=0	Yes
Simulation of maximum positive input	Input=0.5V	Dout=1023 Dout_sgn=0	Yes
Simulation of maximum positive input which Vcomp switches later than 1024 clks i.e goto S2bmax	Input=0.501V	Dout=1023 Dout_sgn=0	Yes
Simulation of case where Vcomp doesnot switch	Input=0.65V	Dout should have the previous output value	Yes
Checking the toggle of Passthrough signals	Set ts1 ts2 ts3 appropriately	Should have 100% toggle	Yes
Simulation of nominal negative input	Input=-0.35V	Dout=718 Dout_sgn=1	Yes
Simulation of small negative input	Input=-0.0055V	Dout=12 Dout_sgn=1	Yes
Simulation of maximum negative input	Input=-0.5V	Dout=1023 Dout_sgn=1	Yes
Simulation of maximum negative input which Vcomp switches later than 1024 clks i.e goto S2amax	Input=-0.501V	Dout=1023 Dout_sgn=1	Yes

Test Case	Setup Conditions	Expected Result	Observed Results Matched Yes/NO
Verification of Dout and Clkout timing specification	NA	Should have same timing relation for all inputs	Yes
Verification of total time conversion for all inputs is same	NA	Should have same conversion time for all inputs	Yes
Verification of reset and pwrdn during operation	reset should be activated during operation	Should go to reset_integ state	Yes
Checking toggle coverage for rtl synthesis and layout netlist	signals of interest are to be added to toggle	Should have 100% toggle	Yes
Checking the gate count and timing after synthesis	run synthesis	total of 42 registers should be generated and timing should be met	Yes
Checking the statement coverage branch coverage and fsm transitions	enable coverage	should be 100% covered	Yes
Perform the formality and coding rules check	run formality and code rule check	Warnings and errors should be explained	Yes
Complete the verification checklist provided	NA	NA	NA

List of Figures