Integrating Analog Digital Converter

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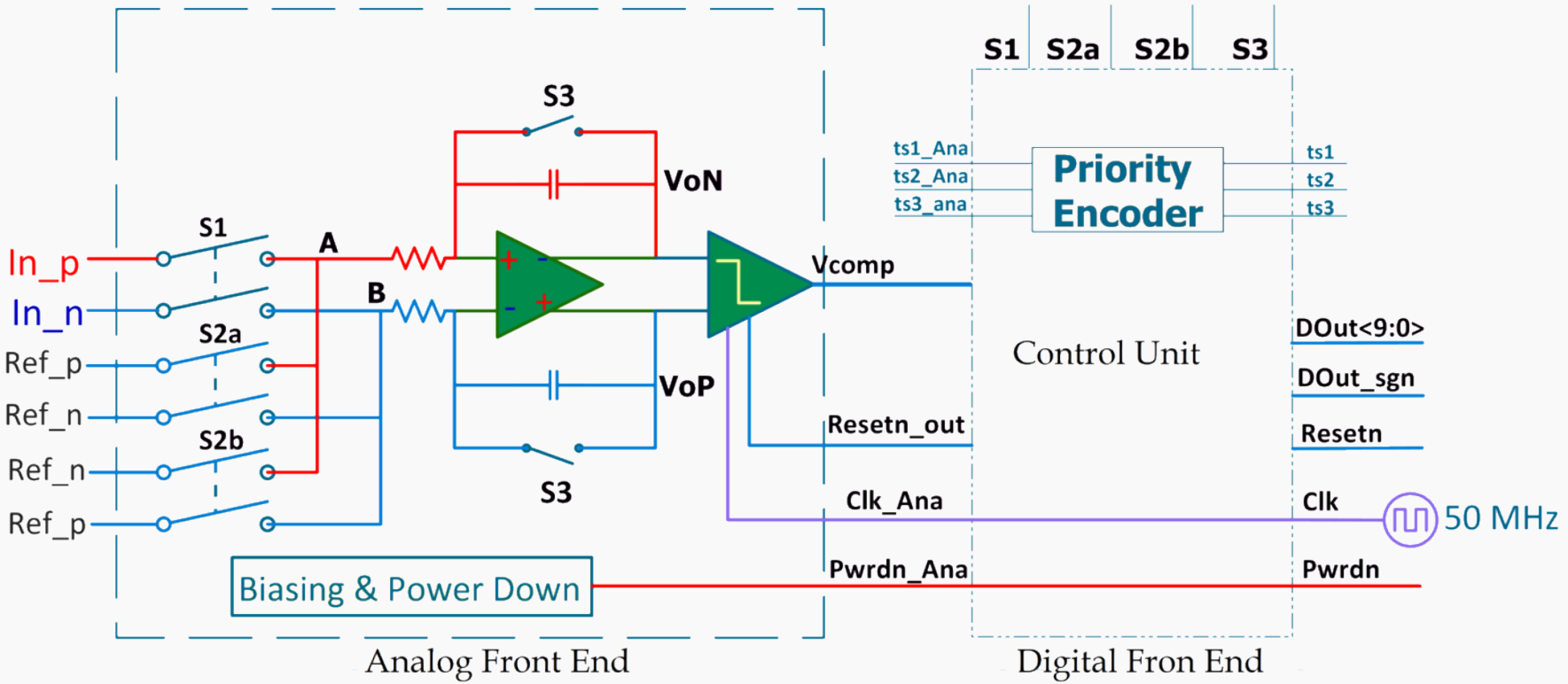
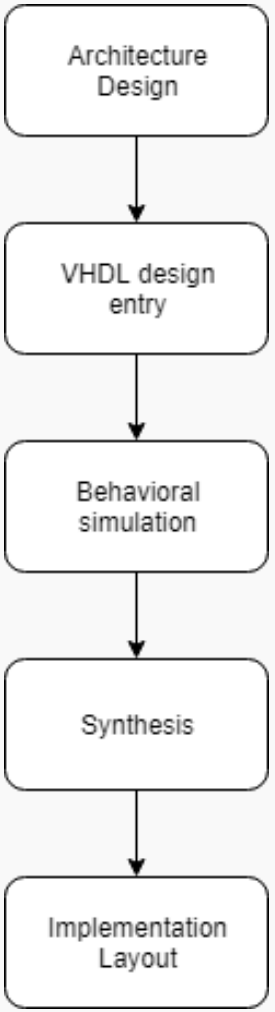
Agenda

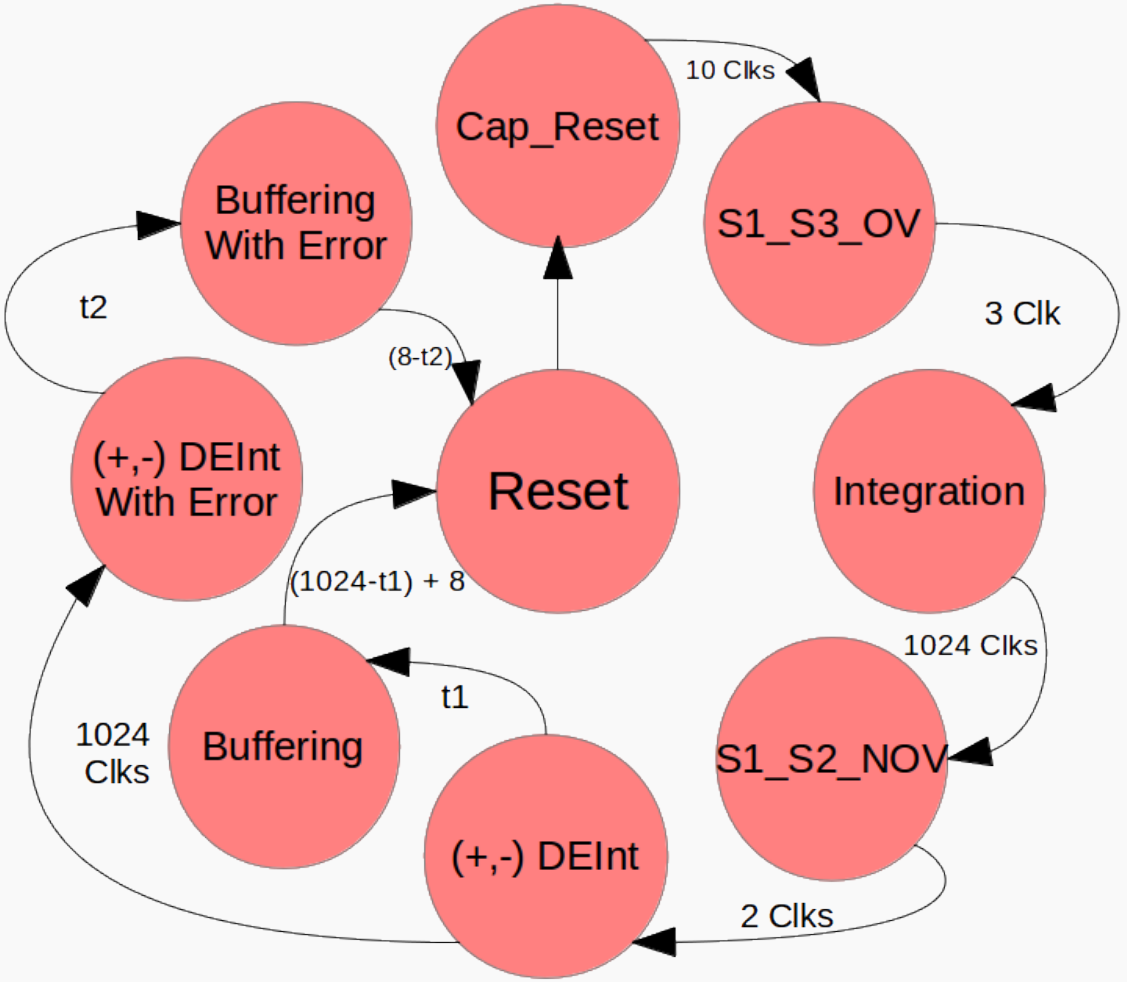
- Introduction
- Control Unit
  - Finite State Machine
  - Priority Encoder
  - Conversion Frequency
  - Timing Diagram
- Layout
  - Analog Front-end Layout
  - Digital Front-end Layout
- Simulation results


S1
S2a
S2b
S3
S3
VoN
VoP
In_p
In_n
Ref_p
Ref_n
Ref_n
Ref_p
S1
S2a
S2b
A
B
Vcomp
Resetn_out
Clk_Ana
Pwrdn_Ana
Biasing & Power Down
Analog Front End
ts1_Ana
ts2_Ana
ts3_ana
Priority Encoder
ts1
ts2
ts3
Control Unit
DOut<9:0>
DOut_sgn
Resetn
Clk
50 MHz
Pwrdn
Digital Fron End

Digital Design Flow



Finite State Machine



Cap Reset Phase

In this phase the switch S3 is close and all other switches are opened, until the capacitor is discharged.
To calculate the phase time, from the equation below 8*RC seconds are required to discharge the capacitor voltage to less than 0.5 LSB

$$\mathbf{V}_{out} = V_{cap} * \frac{-\tau}{RC}$$

Worst case switch resistance $R_{S3} = 750\Omega$.
Capacitor value, C = 10.7p F.
RC = 8.025 ns. Discharge time equals to 8*RC = 64ns.

S1 S3 Overlap Phase

- In this phase, some time spend to charge the internal resistor capacitance.
  By same calculations in the previous slide, 3 clock cycles are enough to charge the internal capacitance of the resistor.
- Duration 3 Clock cycle

Internal capacitance $C_{Int} = 32fF$.
$R = 1.8M\Omega$

Integration Phase

- In this phase the IADC integrate the input voltage for fixed time, 1024 clock cycle.
- The last clock cycle in this phase as the voltage reached maximum value for certain input, the polarity of the input signal is evaluated.
- Duration 1024 Clock cycle

S1 S2 Non-Overlap Phase

- To prevent short circuit between Vin and Vref, in-case of the two switches happened to be conducting at same time due to clock uncertainty.
  The control unit open S1 after integration and waits for two clock cycles then close S2 with respect to the polarity of the signal.
- Duration 2 Clock cycle

Positive/Negative De-integration Phase

- Integrate with reversed polarity until the comparator switches
- Duration not fixed "t1"

Stop De-int Phase

- In case of Vcomp switches, this phase start
- Stop de-integrating and discharge the capacitor S3
- Duration not fixed "1024 - t1"

Extra De-integration Phase

- Recall from the first semester the total analog front end offset is 8 LSB, therefore the phase De-integrate for 8 more clock cycles
- In case of no switching occurs the DOut value remain the same as the previous conversion cycle.
- Duration 8 Clock cycle

Buffering Phase

- Load DOut value to the output buffer and wait for some time to allow the measuring tool to detect.
- Duration 8 Clock cycle

Priority Encoder

- Control the test interface signal
- ts3 has the highest priority
- Prevent short circuit in the test interface

Table: Test Interface Encoder

ts1	ts2	ts3	ts1_Ana	ts2_Ana	ts3_Ana	T_IO_P	T_IO_N
1	0	0	1	0	0	Int_o_p	Int_o_n
X	1	0	0	1	0	Input_p	Input_n
X	X	1	0	0	1	Comp_o_p	Comp_o_n

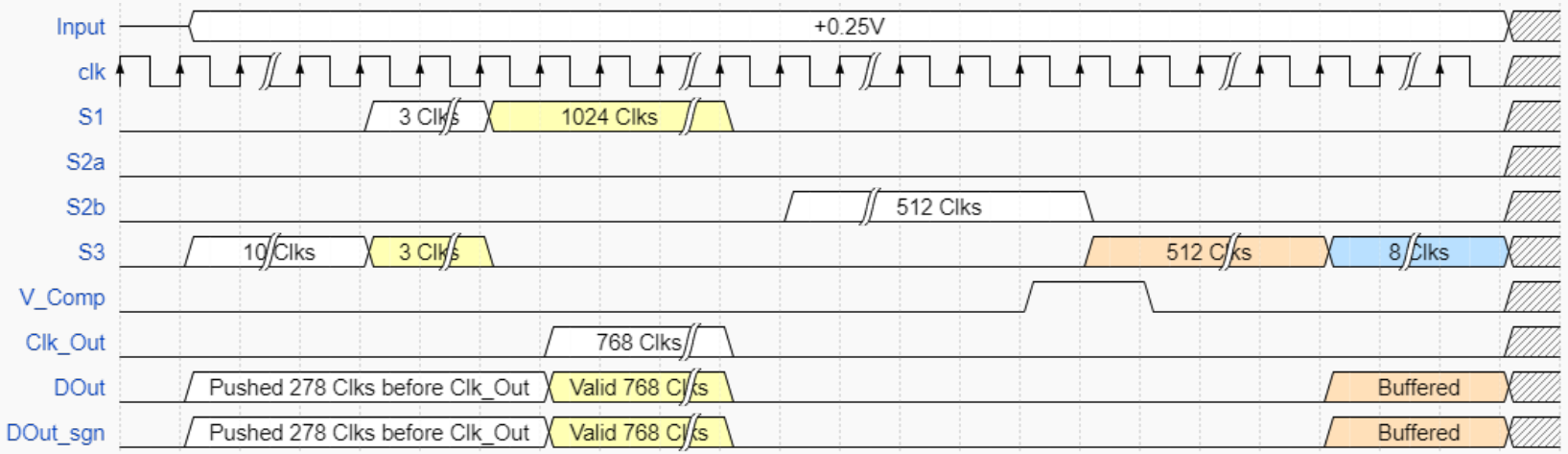
Conversion Cycle frequency

- The conversion frequency is fixed to 24.130 KHz.
- Conversion cycle is 2072 clock cycle

Clk_Out

- Clk_Out duration is 15.36 us, indicating that DOut is ready.
- DOut is pushed to output registers 5.56 us before Clk_Out raises.

Timing Diagram



Phase Cap Reset	10 Clk Cycle
Phase S1 S3 Overlap	3 Clk Cycle
Phase Integration	1024 Clk Cycle
Phase S1 S2 NOV	3 Clk Cycle
Phase De-Integ	t1 Clk Cycle
Stop De-Integ	1024-t1 Clk Cycle
Buffering	8 Clk Cycle

Control Unit offset

The Control unit has one LSB error, due to time required to evaluate the change in Vcomp.

- Subtract one from the final results

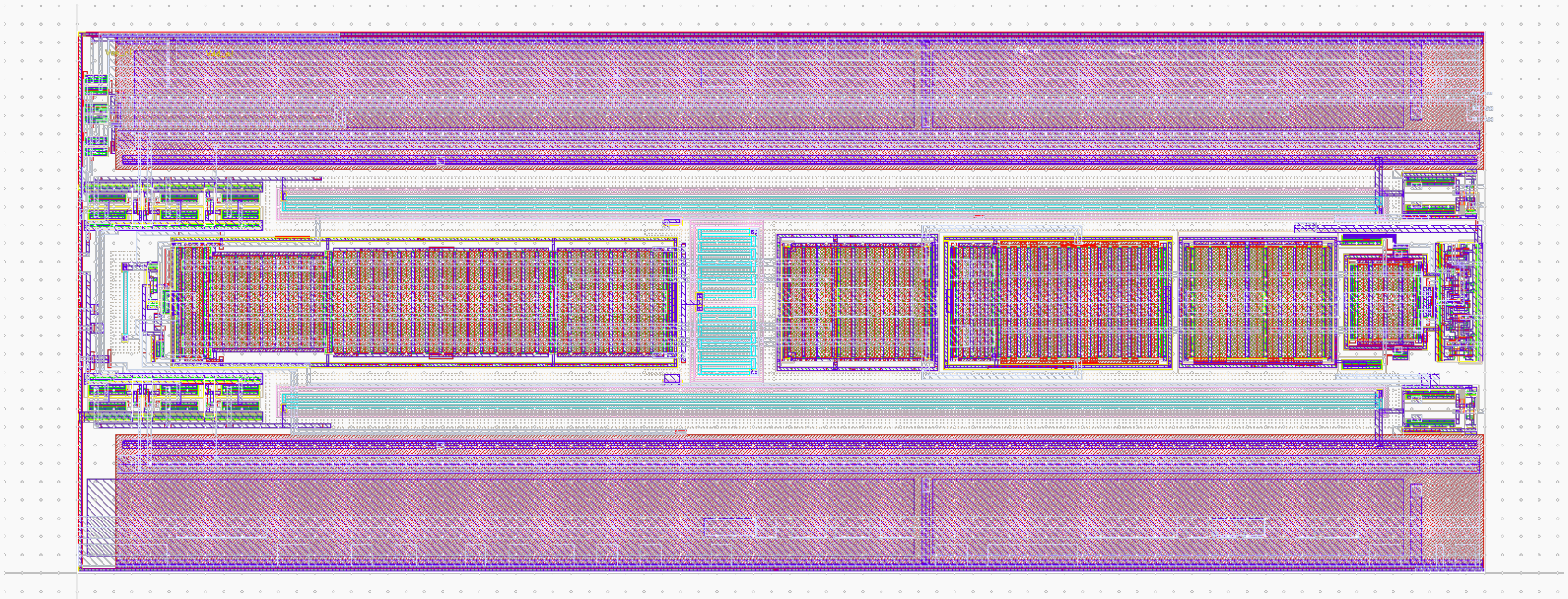
Maximum/Minimum input

- In case no switching accrues the output will the same as from the previous cycle.
- Control Unit De-integrate for extra 7 cycles, due to analog offset.

Table: Important test on iADC

Test	Input	RTL	Mixed Mode Simulation	Expected
Zero Input	0	0	6	0
Max Input	0.5	1023	1023	1023
Max + offset	0.502	1023	1023	1027
No switching	0.6	1023	1023	1227
Positive Input	0.2	410	416	410
Negative Input	-0.05	102	107	102

Analog Front End Layout



Layout

Analog frond end layout is consisted five main circuits.

- Current reference circuit for both comparator and integrator.
- Input switches stage
- Integrator, which is op-amp, feed back capacitor and resistors.
- Comparator
- Test interface.

Layout technique used

- All differential transistors or important to match are interleaved with each other to increase matching.
- Wires over the capacitors are shielded
- Empty space is filled with decoupling capacitor between Vdd and Gnd

Recall from first semester

Comparator

- Mean Offset 250 uV
- Sigma value 633 uV

Integrater

- Gain 188.9 V/V
- Offset 553.8 uV
- Vcm variations 99.06 mV