Fully Controlled Ring VCO 500Mhz-1Ghz Integrated 28 nm CMOS

Mixed Signals Project III

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***Abstract*—this document about multi-stage ring voltage controlled oscillator (VCO), operating at different process variation, compensate for variation by supply and temperature.**

I. INTRODUCTION

This project about Ring VCO, at range from 500 MHz to 1GHz. To achieve this range at variation of PVT there is control on VCR and the feedback line. Also, Vcon from (0.2v to 0.8v).

II. SCHIMATIC

A. Differential Inverter

First, the Differential inverter is the main block in the ring VCO. In the differential mode we can maintain the common mode gain in reasonable value around Vdd/2. Also, it's much efficient in controlling the gain of the inverter. The figure.1 below shows the Differential inverter. The two back to back transistors maintain the positive feedback to the circuit to assist in the oscillation.

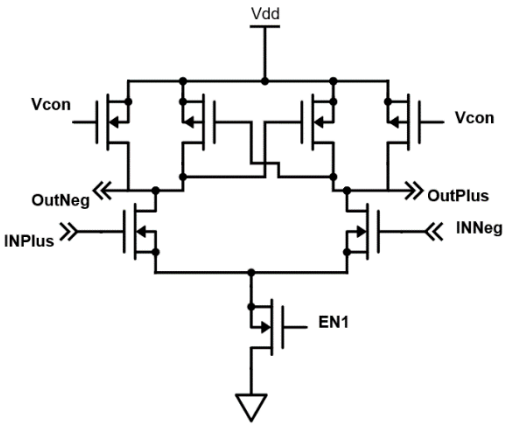

Figure 1

B. Voltage-controlled resistor (VCR)

VCR may be defined as a three-terminal variable resistor where the resistance value between two of the terminals is controlled by a voltage potential applied to the third.

The third terminal in our case is Vcon where we can control the amount of the current in the Differential inverter which reduce or increase the speed of the oscillation depending on the type of the transistor, for NMOS the positive coefficient between frequency and Vcon, but it's negative for PMOS. The equation below show the relation between current and time.

$$I = C * dv/dt \quad (1)$$

C. Swtiches and Multiplexers

The switches and the Multiplexers are used in this design to control the frequency over the variation PVT.
Switches are used in the same cell (Differential inverter) to control the number of the VCR connected to the circuit.
The CMOS Multiplexers are used to reduce the number of the inverters in the closed loop to increase the frequency at the low current corners. The figure 2 below show the mux gate level.
At Sel = 0, the number of inverters are 42 inverter, But at Sel =1 number of inverters drop to 6

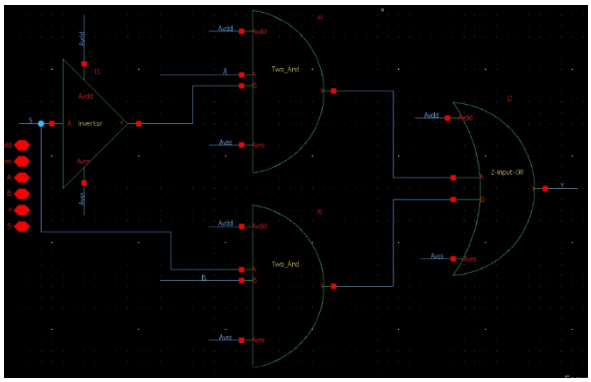

Figure 2

D. Comparator

The used comparator use basically an inverter that will drive the output from (0 to Vdd), that's since the swing of the delay cells level is high enough to drive the inverter.
To design the sizes of the transistor I had to measure the average of the output signal (Common mode). At most it's about Vdd/2

III. OUTPUT

The input of the VCO are S1,S2 and Sel, that S1 and S2 for the VCRs and Sel for the multiplexer.

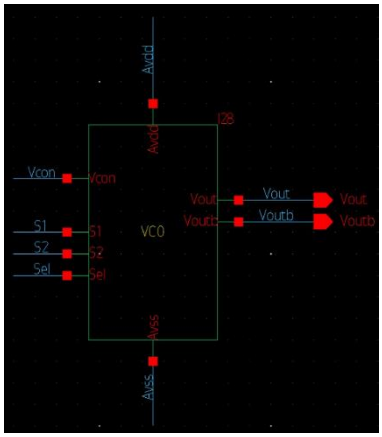

Figure 3

A. Table of Corners

#	Voltage supply	Temperature	Coroner	S1,S2,Sel
A	1.1	125	FF	0,0,0
B	1.1	-40	FF	1,0,0
C	1	50	TT	1,1,0
D	0.9	125	SS	0,0,1
E	0.9	-40	SS	1,0,1

B. Table of Output

Corner	Vcon @ 1G	Vcon @ 500Mhz	Max Freq.	Min Freq.
A	209 mV	800 mV	1.00G	501M
B	260 mV	652 mV	1.07G	302M
C	216 mV	503 mV	1.02G	100M
D	445 mV	620 mV	1.70G	220M
E	353 mV	491 mV	1.53G	123M

C. Simultion Graphs

Sweeping Vcon f
rom 0.2 volts to 0.8 volts and measuring the output frequency at different corners.

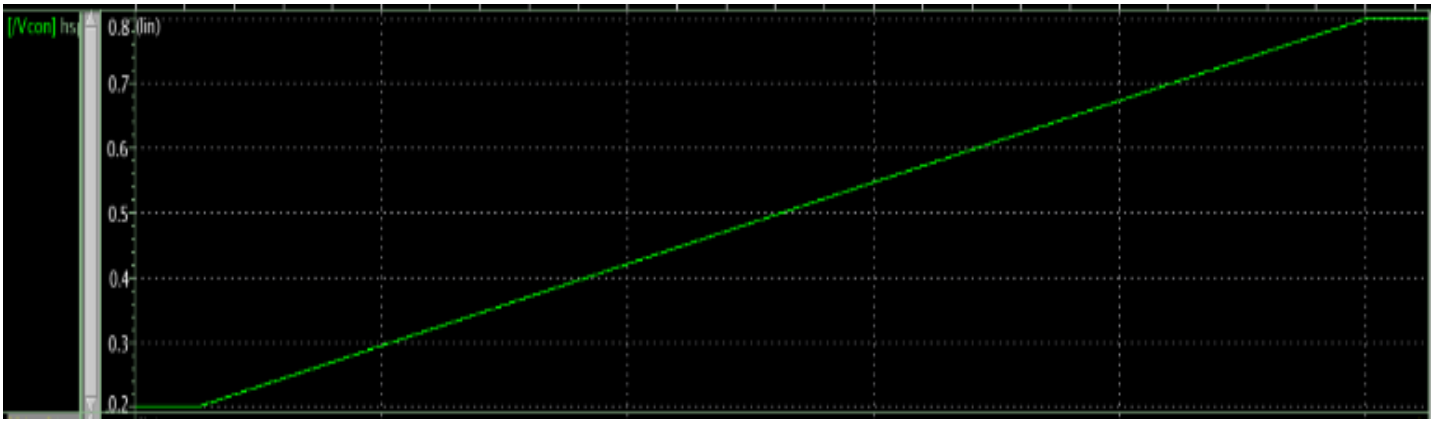

Figure 4

1) Corner A

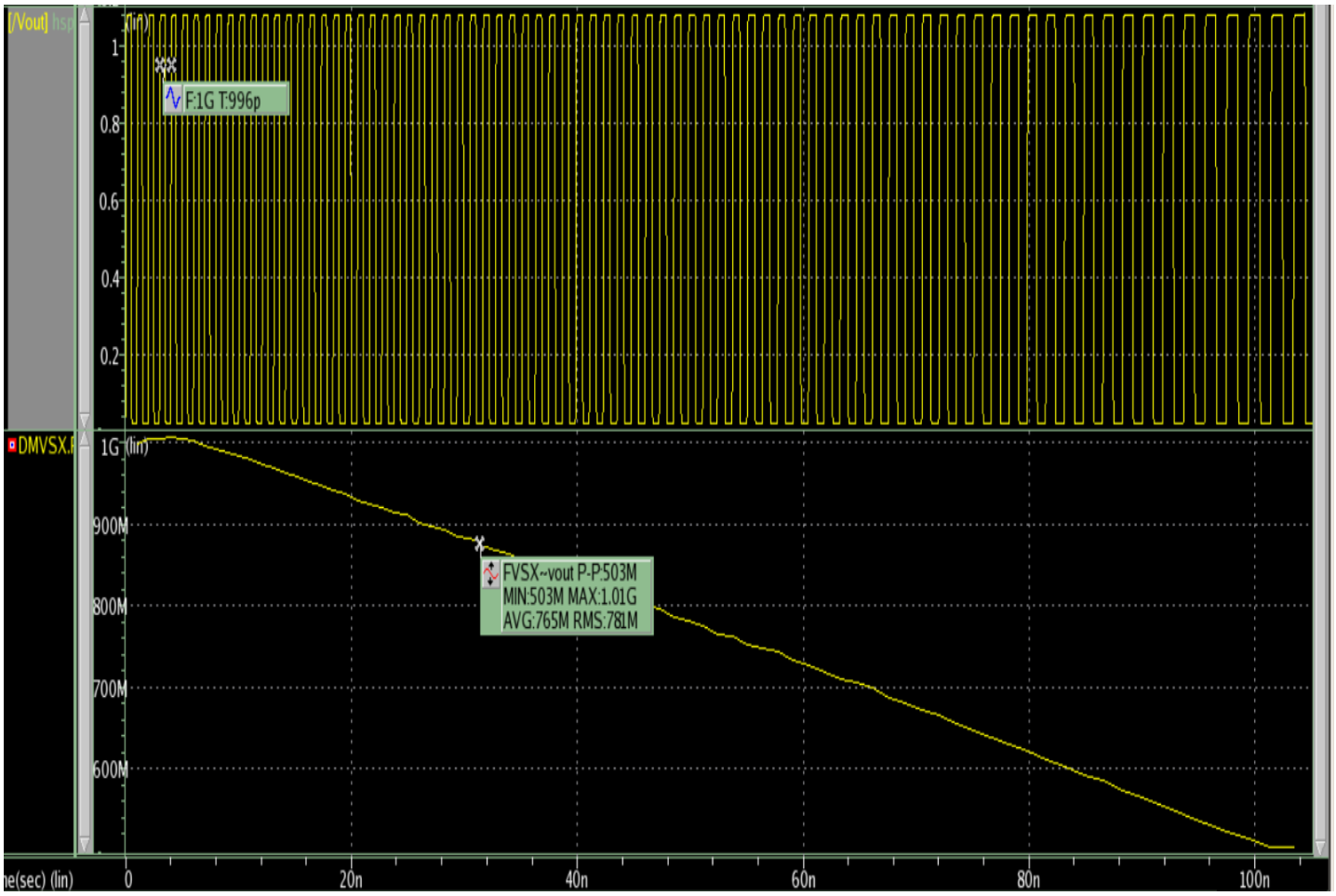

Figure 5

2) Corner B

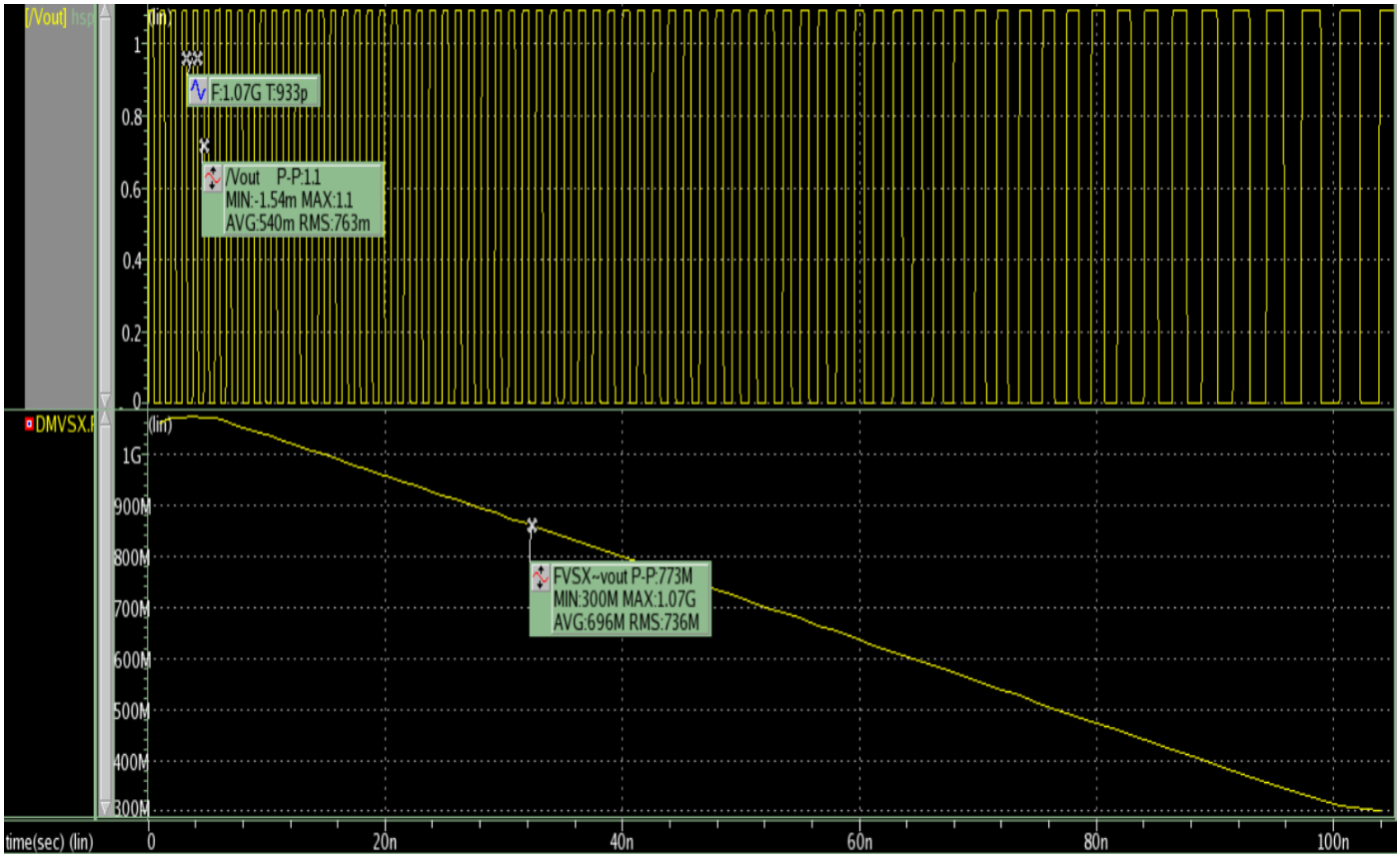

Figure 6

3) Corner C

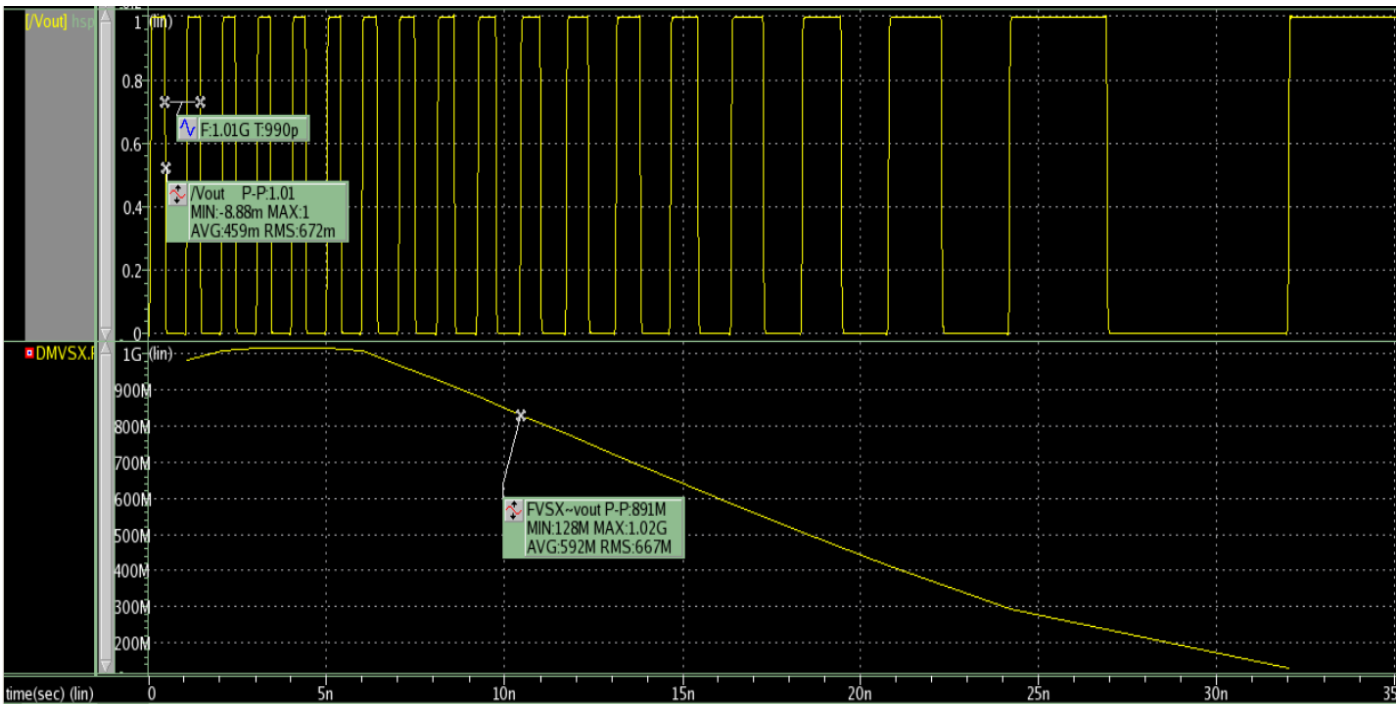

Figure 7

4) Corner E

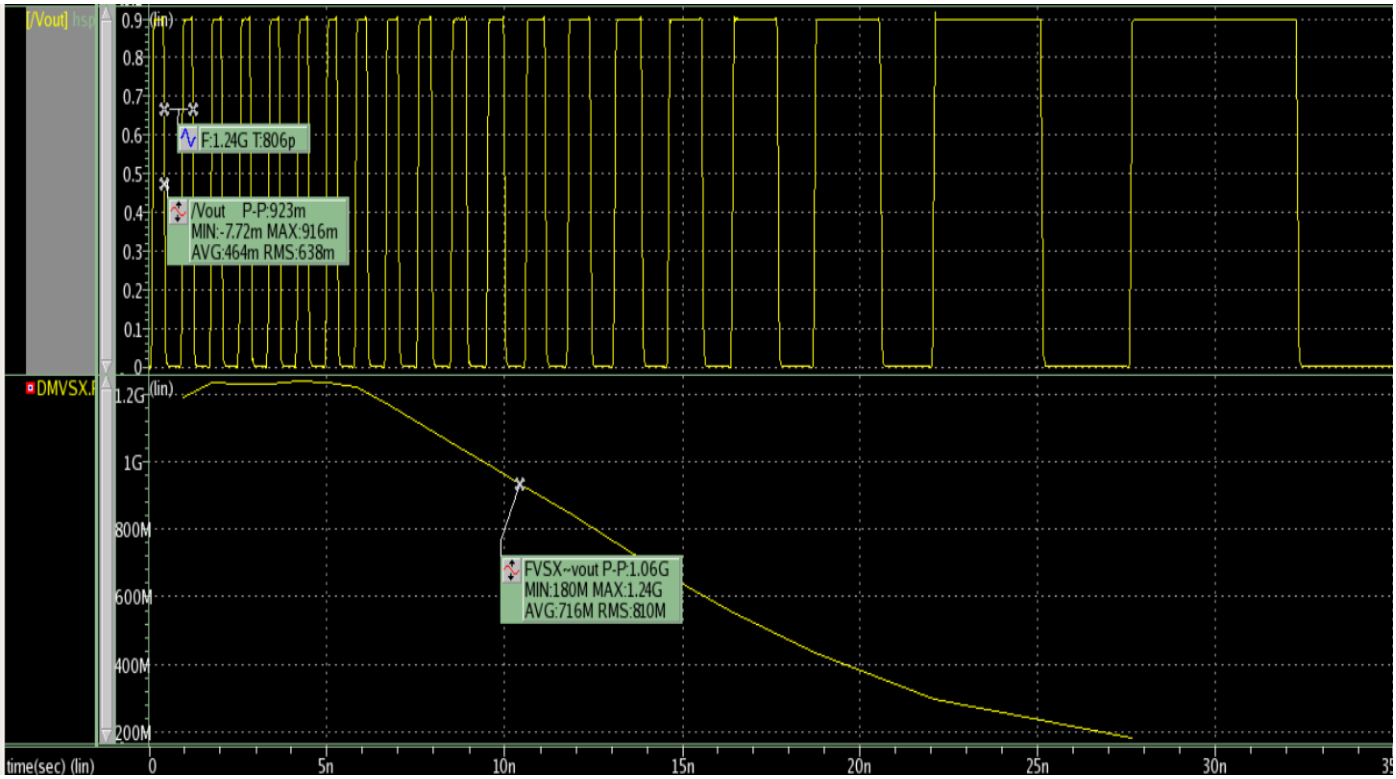

Figure 8

5) Corner E

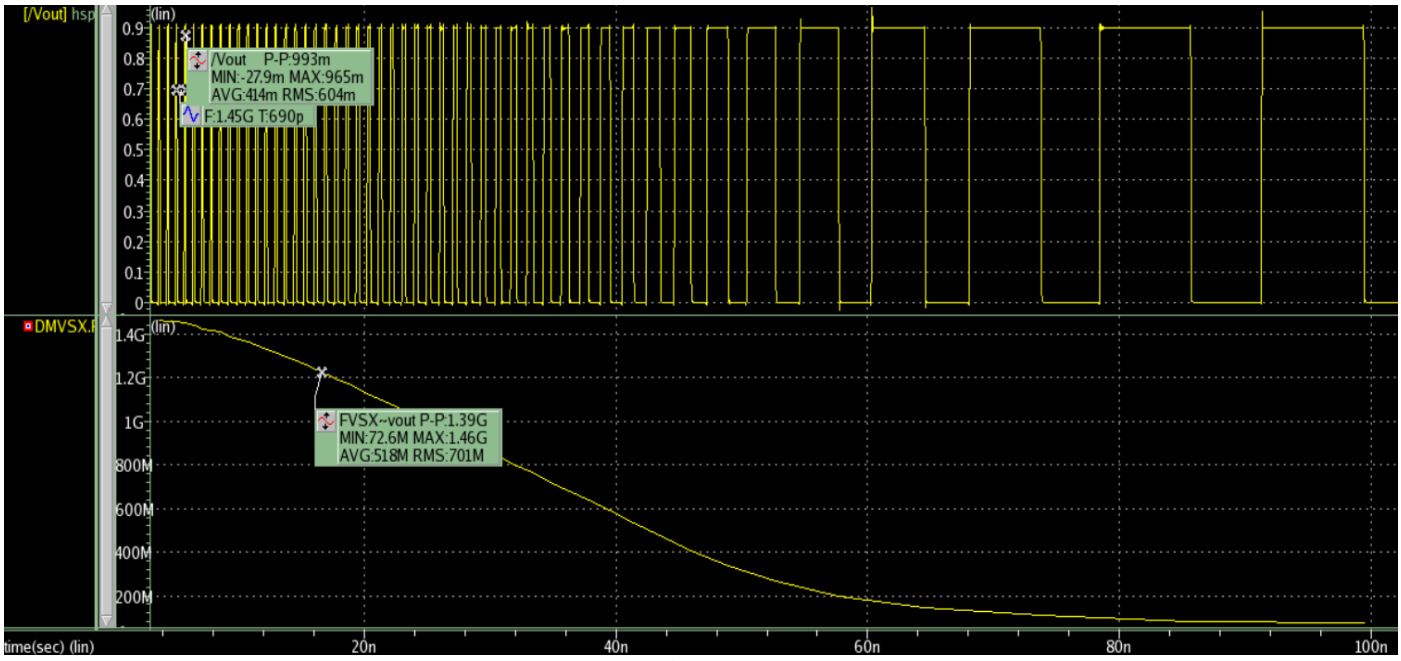

Figure 9