ISCD - Project

Integrating Analog to Digital Converter (IADC)

Johannes Sturm

December 18, 2017

Contents

1 Introduction **3**

2 Integrating Analog-to-Digital Converter **3**

3 IADC Specification **4**
3.1 Pin Description 4
3.2 IADC Architecture 6
3.3 Electrical Characteristics 6

4 Project Tasks **6**

5 Reporting **9**

6 Project Setup **9**
6.1 General Rules 9
6.2 CAD Setup and Naming Conventions 9

Bibliography **10**

A Project Structure **11**

1 Introduction

Integrating Analog-to-Digital converters (ADCs) are Nyquist-rate converters that are mainly used for high-accuracy applications with a high number of bits (high resolution) but with a very low conversion rate (low speed). The goal of this project is the development of an integrating ADC based on the dual-slope method. An introduction to Analog-to-Digital conversion and integrating ADCs can be found (for example) in the book of David Johns and Ken Martin [1] (Chapter 11 and Chapter 13.1) or more specific in (many) dedicated books on data converters (eg. [2]).

The students should get experience on all necessary design steps, including

- Specification and concept study
- Full-custom analog design and verification of building blocks (1. Semester)
- Full-custom layout of building blocks (2. Semester)
- Semi-custom digital design and layout of basic building blocks (2. Semester)
- Lab evaluation of IADC testchip (3. Semester)
- Documentation and presentation of all development steps

The design package and technology for development is the AMS HITKIT-4 $0.35\mu m$ CMOS technology.

2 Integrating Analog-to-Digital Converter

Figure 1 shows a block diagram of the dual-slope integrating ADC. It basically consists of an integrator circuit followed by a comparator. The comparator output is controlling a logic circuit defining the switch settings of the integrator. A digital counter is also part of the logic block, which defines the digital representation of the analog input voltage. The ADC function can be divided into two phases:

Phase1 The integrator is reset by switch S_3 for a short time. After reset, the ADC input signal V_{in} is applied to the integrator by switch S_1 and integration of the input signal is performed for a defined time period. The constant integration time T_1 corresponds to the time of a N-bit counter counting from 0 to full-scale ($T_1 = t_{clk} * 2^N$). The integrator output signal V_X is therefore increasing from 0V to a value depending on the input voltage level.

Phase2 A constant reference voltage V_{ref} with opposite polarity as the input voltage is applied to the integrator input (switch S_2 closed, S_1 open). Integration of a well-defined reference voltage is performed. Therefore the integrator output is decreasing, starting from the voltage level reached at the end of phase 1. The integration is done until the comparator is indicating 0V at the integrator output V_X. The comparator output must have CMOS logic levels ($1 = V_{dd}; 0 = 0V$). The reference voltage defines the maximum allowed (full-scale) value for the input voltage.

The integration time T_2 of phase 2 is a measure for the input voltage value and is represented by a counter value. The counter starts counting the clock cycles from the beginning of phase 2 until the end of phase 2. The number of counter bits N is defining the (theoretical) resolution of the ADC. In reality the integration time T_2 will vary due to technology variation which determines the real ADC accuracy.

The necessary control signals for switch S_1, S_2, S_3 are generated by the control logic.

For the real implementation a fully differential circuit will be used as shown in Figure 4 .

3 IADC Specification

This chapter summarizes the circuit architecture and performance requirements for the IADC. Furthermore the input/output pins of the module are specified.

3.1 Pin Description

The ADC pin-out is shown in Figure 3 while a pin description is collected in Table 1. The ADC module has two separate supply voltages for the analog part (V_{dd_a}, V_{ss_a}) and for the digital part (V_{dd_dc}, V_{dd_d}) with 3.3V each. A differential input voltage V_{in_d} will be applied to the input pins (*In_p, In_n*) and should be converted to a digital number of 10 bits provided at *DOut*. The sampling clock for the output data *DOut* is provided at the output pin *Clkout*. The input voltage range is specified between $\pm 0.5V_{pp}$, which means $1V_{pp,d}$. The maximum voltage range is defined by the reference inputs *Ref_p* and *Ref_n* which are provided by external voltage reference V_{ref}. A digtial output signal *DOut_sgn* indicates the differential input voltage polarity. The total ADC resolution is therefore 11bit. For a maximum input signal of $\pm 0.5V_{pp}$, a reference voltage $V_{ref} = (Ref\_p - Ref\_n) = +0.5V$ must be applied. The common mode voltage $(Ref\_p + Ref\_n)/2$ is provided to the

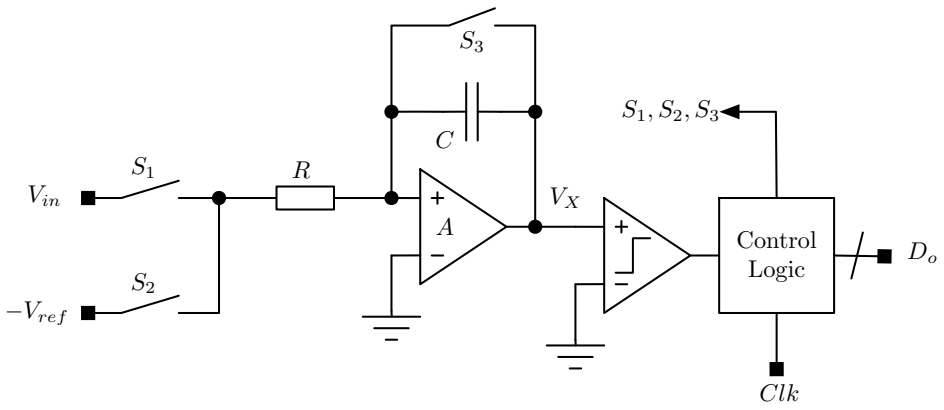

Figure 1: Basic block diagram of an integrating ADC

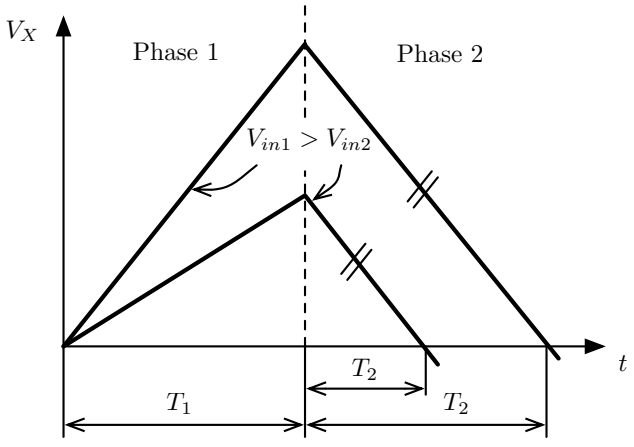

Figure 2: Dual-slope integrating-ADC operation phases.

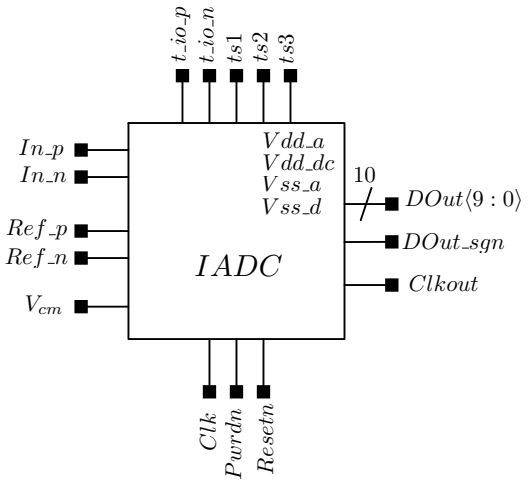

Figure 3: Integrating ADC pin out

input pin *Vcm* from external. A clock signal *Clk* of 50MHz is provided for digital control logic within the IADC. A power down signal *Pwrdn* is used to disable the IADC and setting the whole IADC block in a well-defined power-down mode with low power consumption. The *Reset* signal resets the digital IADC control logic. For test and debugging purposes a test interface is included. With the input signals *ts1, ts2* and *ts3*, different circuit nodes can be directly connected to the test pins *t_io_p* and *t_io_n*.

3.2 IADC Architecture

A more detailed differential architecture of the IADC circuit is shown in Figure 4 with basically the same functionality as discussed before.

3.3 Electrical Characteristics

The following specification in Table 2 covers the requested ADC performance from customer point of view. The final design must satisfy all specified parameters. This is no complete design specification for the different building blocks. A detailed design specification has to be derived from concept investigations.

4 Project Tasks

The project tasks for the IADC project cover more or less a complete mixed-signal IC development process from concept development, analog and digital

Table 1: Pin description of IDAC (I=input, O=output, P=power, A=analog, D=digital)

Name	Direction	Type	Description
In_p	I	A	Positive analog input
In_n	I	A	Negative analog input
Ref_p	I	A	Positive analog reference
Ref_n	I	A	Negative analog reference
Vcm	I	A	Common mode voltage
Clk	I	D	Clock for digital control logic (50MHz)
Pwrdn	I	D	Power down
Resetn	I	D	Logic reset (low active)
DOut<9:0>	O	D	10 bit digital data output representing the input voltage.
Dout_sgn	O	D	Output sign bit, indicate the differential input voltage polarity
Clkout	O	D	Output sampling clock to strobe the output data DOut.
ts1, ts2, ts3	I	D	Test interface select signals
t_io_p, t_io_n	IO	A	Differential, analog test interface pins
Vdd_a	n.a.	P	Analog power supply (3.3V ± 0.3V)
Vss_a	n.a.	P	Analog ground
Vdd_dc	n.a.	P	Digital power supply (3.3V ± 0.3V)
Vss_d	n.a.	P	Digital ground

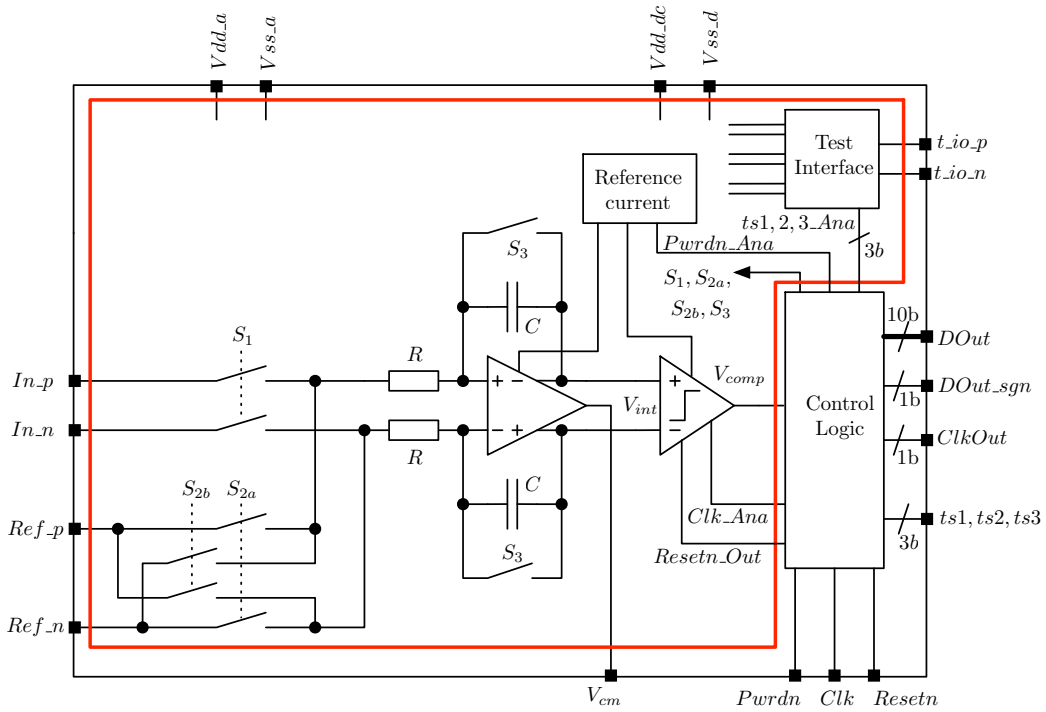

Figure 4: Integrating-ADC block diagram

Table 2: Electrical characteristics (nominal conditions: Vdd=3.3V; T=27°C)

Parameter	Symbol	Value min	Value nom	Value max	Unit	Remarks
Power Supply voltage	V_{dd}	3	3.3	3.6	V	
Power Dissipation	P_d		???		mW	With 0V at the input
Operating temperature	T	0	27	70	°C	nominal T=27°C
ADC input voltage range	$V_{in,pp,d}$	0		±0.5	V	$V_{in,pp,d} = In\_p - In\_n$ Peak to peak differential =1V!
Input common mode	V_{cm}	1.3	1.5	1.7	V	
Input clock rate	f_{Clk}		50		MHz	
Max. input signal frequency	$f_{in,max}$			???	V	According Nyquist theorem this is half the conversion rate! → From concept investigation!
ADC resolution	N		10		bits	For each input polarity → 11bit
ADC accuracy	ENOB		???		bits	Effective number of bits → Needs to be optimized!
Input impedance	R_{in}		???		$k\Omega$	Single ended impedance of $In\_p - In\_n$ up to maximum operating frequency.

circuit design and layout to chip production and lab characterization. The different development steps are distributed over 3 semesters.

Semester 1 The first semester starts with basic concept investigations to derive important circuit design specifications. Due to limited time, the concept development and modeling of the IADC is only briefly covered. Basically the architecture concept and all circuit building blocks are provided. The main part of semester 1 will be the analog circuit dimensioning and simulation of building blocks and also IADC analog frontend top-level simulations. At the end of semester 1, all analog building blocks schematics should be fully parameterized, optimized and verified by simulation.

Semester 2 The first task of semester 2 will be the full-custom layout of analog building blocks designed during semester 1. Furthermore the digital semi-custom design, verification and layout of the control logic including switch control, counter and IO handling will be performed. Finally the layout of digital control logic block will be (manually) included into the full-custom IADC layout and functional simulations of the complete IADC module will be done to verify the overall functionality. The complete and final IADC layout will be delivered to production fab at the end of semester 2 and wafer production will run during summer holidays.

Semester 3 The silicon of IADC testchips should be available at the beginning of the 3rd semester. To verify the IADC functionality and performance,

detailed lab characterization measurements will be done. If necessary, potential errors need to be identified and localized.

5 Reporting

A project report needs to be provided at the end of each semester. Each student has to present his own work, design steps, results and discussions in the report. Additionally a project workshop will be organized at the end of each semester, where each student should give a short presentation of his own work and results, followed by a discussion. The reports should be not longer than 10 to 15 pages → focus on the main important results and especially discussions.

6 Project Setup

6.1 General Rules

- The design work should be performed in small design groups, 2 students each
- Each design group has to develop the whole IADC block independently
- Finally each design group will receive their own IADC testchip for characterization

6.2 CAD Setup and Naming Conventions

- The whole project work should be done in following project directory: /opt/projects/iscd/iscd17/iadc/
- Do not work in your home directory or anywhere else!
- In the project drive .../iadc there a three folders available:

  .../home This folder can be used for documentation. Any student can create his own home folder within /home directory.

  .../docu This folder can be used for general documents and information

  .../design This is the working folder. It contains two sub-folders:

.../fullcustom This is the project folder for full-custom analog design (using Cadence tools). Each design group has a separate directory for their work (wk_grp1 to wk_grpx). These directories can only be entered by the corresponding group members. The group directory contains 3 sub-directories: one for each group member and a design directory for the final design. The group member has to start Cadence DFII in his sub-directory where he/she can generate working libraries which can also be accessed by the team mate. The final design has to be copied to the Cadence library TO which is located in $.../design/TO$. An overview of the project structure can be found in appendix A.

.../semicustom This is the project folder for semi-custom digital design (using eg. Synopsys tools). All digital design work should be done within this folder. The structure is similar to the structure described above.

- For the final tape-out data base in the library $.../design/TO$ you have to use a defined naming convention for any view. Each view name has to have the group as prefix eg. $.../design/TO/grp1\_\langle view\_name \rangle$
- The analog design work should be done on Cadence tools using AMS 0.35um CMOS technology (Cadence v6.1.5 and HitKit v4.10). Technology process option **C35B3C3**.
- Be careful with naming conventions for the different schematic views.
- Take care of references and access rights when copying views (schematic, symbol) from one library to another!

References

[1] David Johns, Ken Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, Inc. 1997

[2] Franco Maloberti, *Data Converters*, Springer, 2008

A Project Structure

```
/opt/projects/iscd/iscd17/iadc
  – design
    – fullcustom
      – wk_grp01
        – design
          – TO
        – student1
        – student2
      – wk_grp02
              .
              .
              .
    – semicustom
        .
        .
  – docu
  – home
```