10 Gb/s Voltage-Mode Logic Transmitter with 12dB gain

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Abstract:

This project about 20Gb/s Voltage mode logic transmitter using CMOS 28nm technology and design the transmitter to operate functionally on all of the process coroners, on different temperature and at different supply voltage, also to work on the noise due to high frequency or the lousy transition line.

Introduction:

The VML transmitter is differential output device that depend on inverters as drivers. We need to add the gain on the signal as a high frequency boost when $\mathrm{D[n]} \neq \mathrm{D[n-1]}$ and to take out the boost when $\mathrm{D[n]} = \mathrm{D[n-1]}$. This operation is done simply by adding an auxiliary differential driver as shown in figure (1.1).

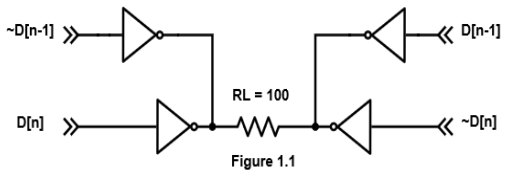

Figure 1.1

Calculation:

To calculate the suspected size of the main and auxiliary driver we have to match the total resistance of the main and auxiliary drivers to the transition line impendence which is equal to 50 Ω. Then the first equation

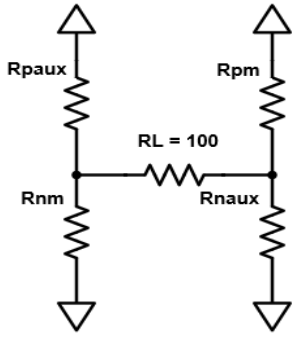

Figure 1.2

$$Rm//\mathrm{Raux} = 50$$

Note that Raux is larger than Rm which force the current to flow in the wanted direction. To find the second equation, as shown in figure (1.3) the voltage on the transition line during the boost $\frac{Vdd}{8}$.

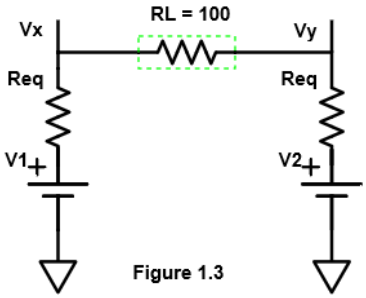

Figure 1.3

$$\frac{10}{16} = \frac{Rm}{(Rm + Raux)}$$

These two equation gives us an indication of the real resistance, then we can find the expected size of the transistors from the following relations at $Vds \ll 2v$

$$Rds = \frac{1}{Kn\frac{W}{L}(Vgs - Vt)}$$

I. Circuit design:

1. Serializer:

The serializer concept is parallel data in serial data out (PISO). The PISO in this project is 10 bits at 10Gb/s.

The input data should be at 1Gb/s, ten phases at 10Ghz is required to the design used in this work, the phase shift between the phases is 50ps. Ten parallel pass-gates function as tri state buffer when the data is selected it pass to the buffer stage, else the output of the pass-gate is high impedance.

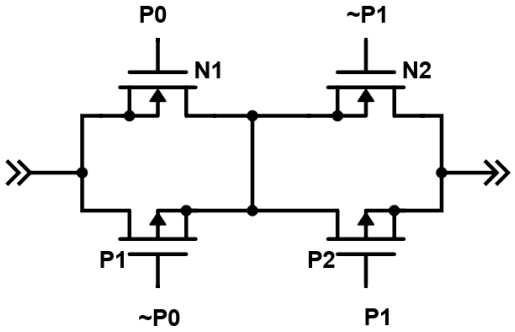

Figure 1.4

The table for ten pass-gates and 5 phases with their complement.

D0	P0 AND P1
D1	P1 AND !P2
D2	P2 AND !P3
D3	P3 AND !P4
D4	P4 AND P0
D5	!P0 AND P1
D6	!P1 AND P2
D7	!P2 AND P3
D8	!P3 AND P4
D9	!P4 AND !P0

Table 1.1 truth table for the data using pass gate.

After stage one, there is the buffer stage to boost the current that drive the transmitter, it also to prevent loading effect from the next stage. Figure 1.5 shows the buffer stage where the input for this stage is the parallel pass-gates.

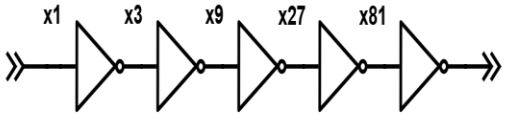

Figure 1.5

The data will be delayed due to the inverter (delay time, both rise and full time).

The graphs below (1.6 -1.7) shows the output of the serializer at 10Gb/s in the top corners of operation. For input bin (0001 1101 01) connected to the driver.

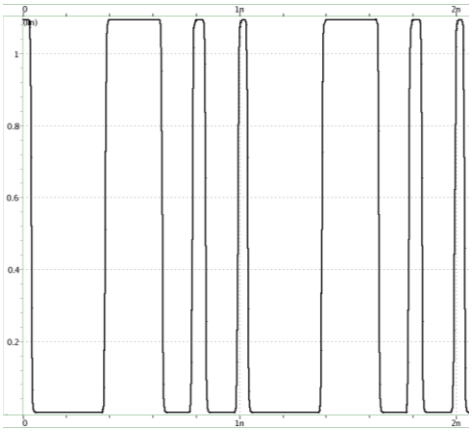

Fig 1.6 Vdd (1.1V) Temp (-40C) (FF)

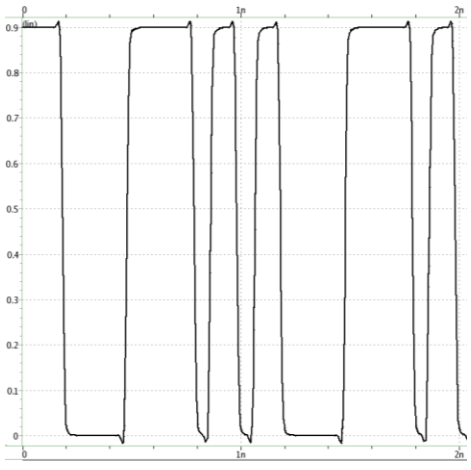

Fig 1.7 Vdd (0.9V) Temp (125C) (SS)

The main problem in the Serializer was that pass-gate represented as high resistance since its two series transistor then the first inverter of the buffer should be very small in size to help reduce the RC effect.

To partially solve this problem I had to raise the pass transistors sizes, and reduce the first invertor size.

2. Driver (Transmitter)

A large percentage of the signal is consumed in the transition line specially at high frequency and long channel, the voltage mode logic transmitter with 12 dB gain, is used in this case to boost the signal over this loses.

As shown in the figure 1.1 we have to add an auxiliary legs to boost the signal when needed, also to make it possible to work in all of the operation corners another set of legs should be added to the design as shown in figure (1.8). The figure 1.8 show the full transmitter circuit, with all legs connected. There are 4 switches to each transmitter pair-leg. The switches earthier connect the drive input to high impedance or pass the data. The switch could be very problematic at high speed since the drivers have high capacitance (Due to large size).

The boost is needed when $\mathrm{D[n]} \neq \mathrm{D[n-1]}$ such as the data pattern is (10101010) then the transmitter have to drive more current to swing fully (Logic one or zero).
The graph below 1.9 shows how the single ended output voltage should be for bin (1100).

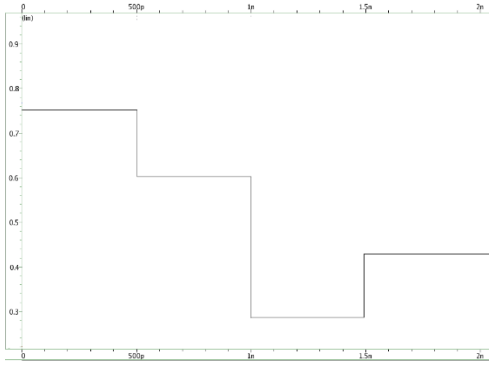

Fig 1.9 output wave form

II. Output wave forms

To get the best output form the driver the serializer should work in the Process voltage temperature (PVT), the graphs (1.6 & 1.7) shows that the serializer preform perfectly with full load capacitance.

For the driver output, any designer is interested in the following matters.

- Differential outputs $V\ vs\ Vbar$
- Common mode output $\frac{\mathrm{V+Vbar}}{2}$
- Differential mode $V - Vbar$

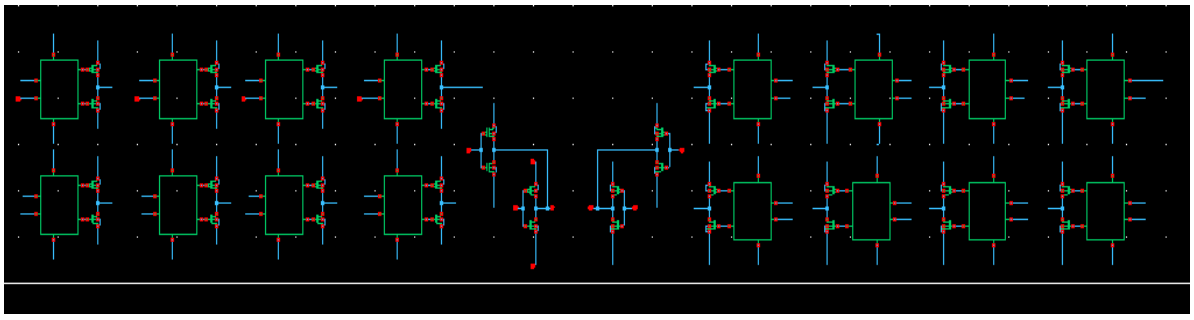

Fig 1.8 (Transmitter circuit)

- **Wave forms**

1) Corner I (FF_1.1_-40)

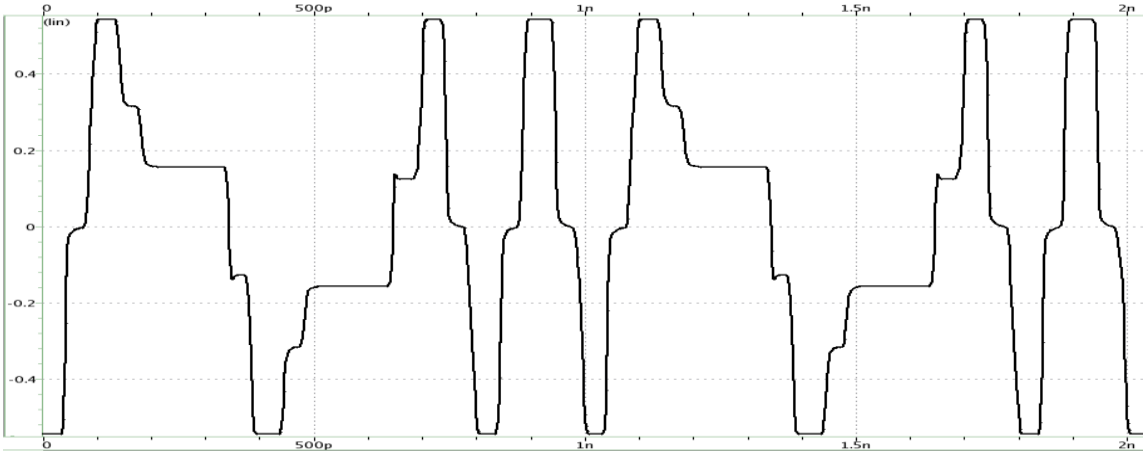

Fig 1.10 Differential swing from -0.5 to 0.5

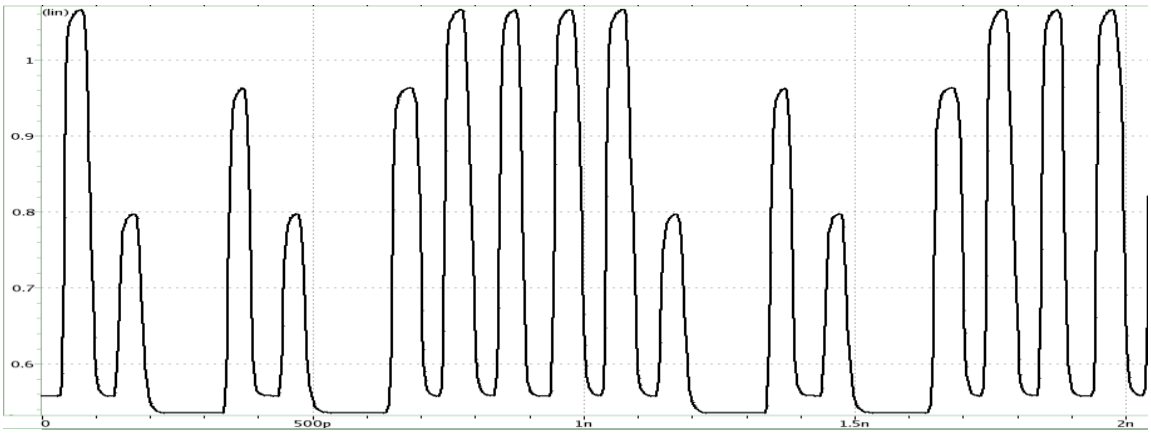

Fig 1.11 Common mode around $\frac{Vdd}{2}$

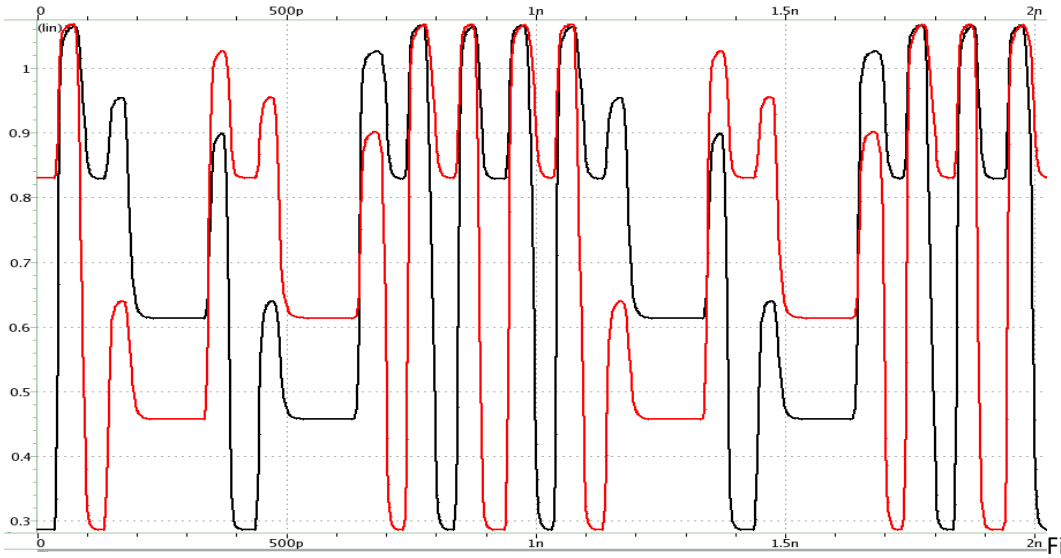

Fig 1.11

Fig 1.12 Differential output

2) Corner II (FF_0.9_-40)

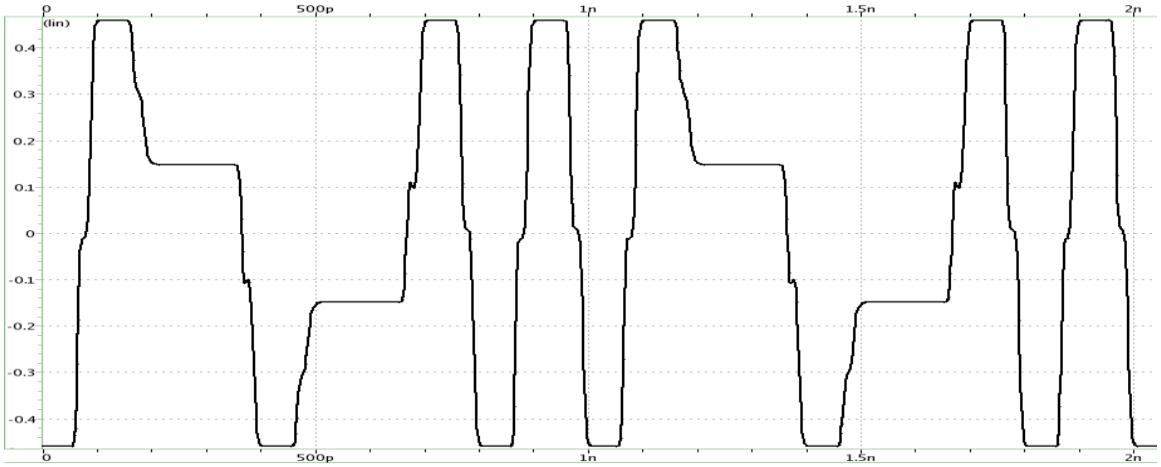

Fig 1.13 Differential swing

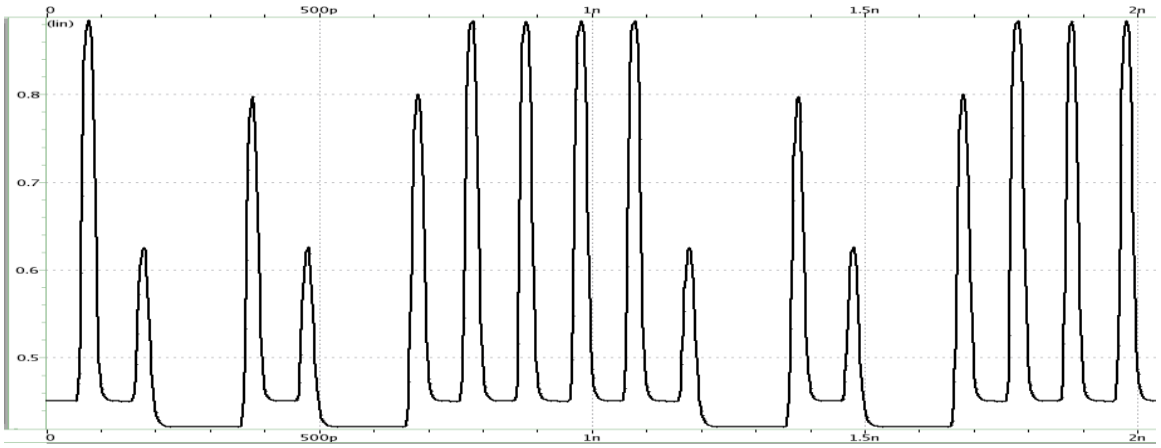

Fig 1.14 Common mode

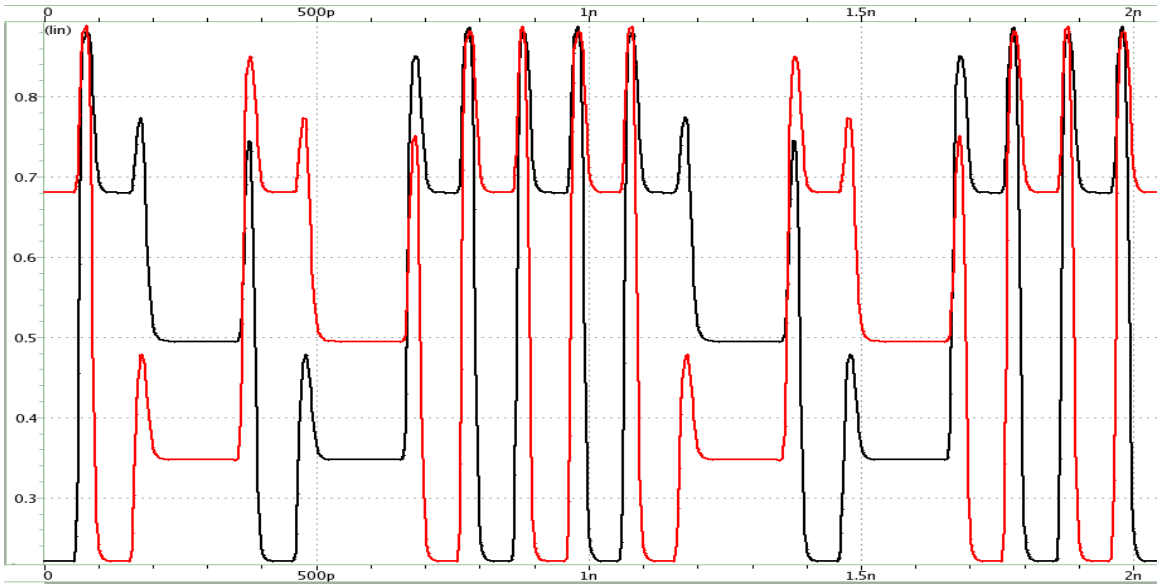

Fig 1.15 Differential output

3) Corner III (SS_1.1_125)

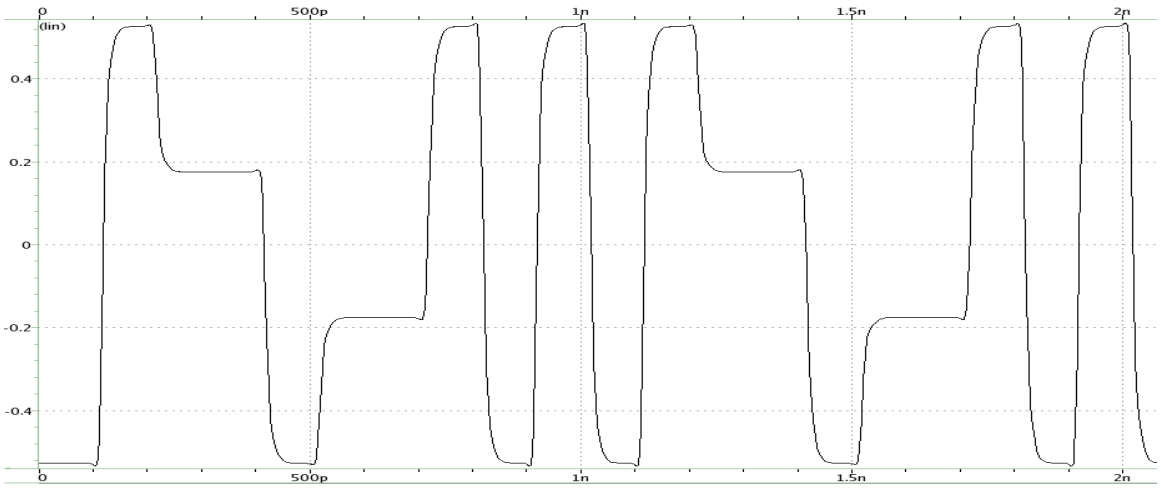

Fig 1.16 Differential swing

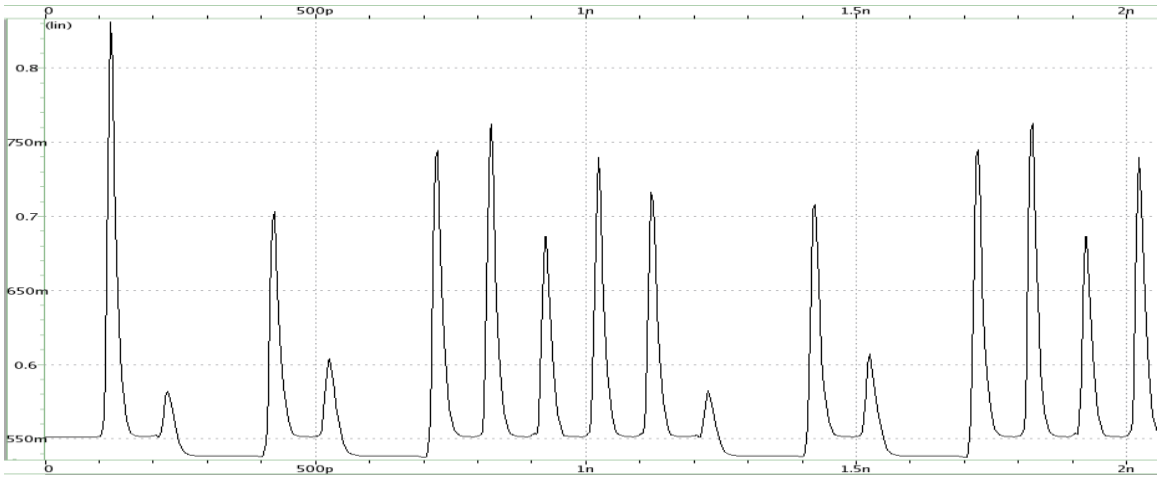

Fig 1.17 Common mode

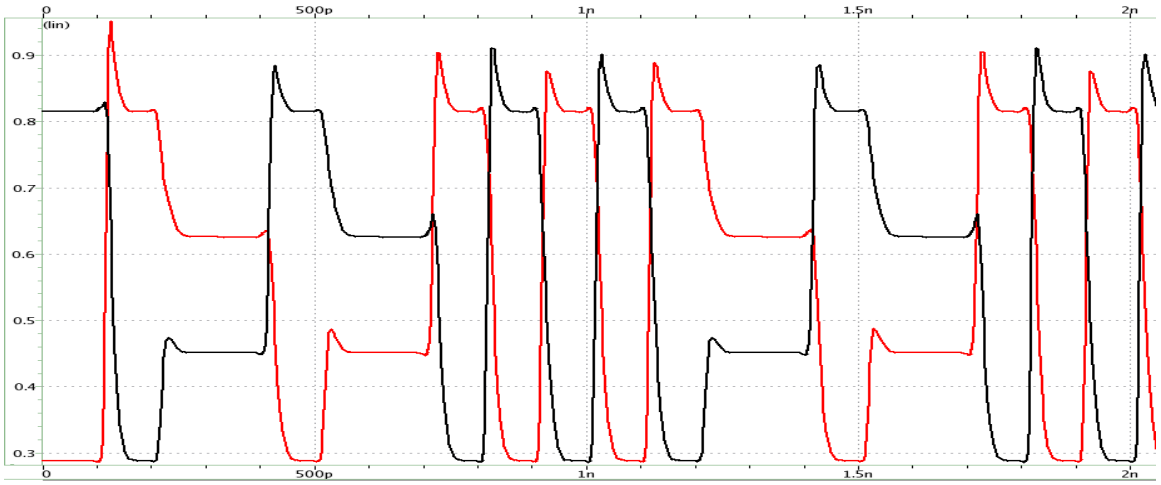

Fig 1.18 Differential output

4) Corner IV (TT_1.0_50)

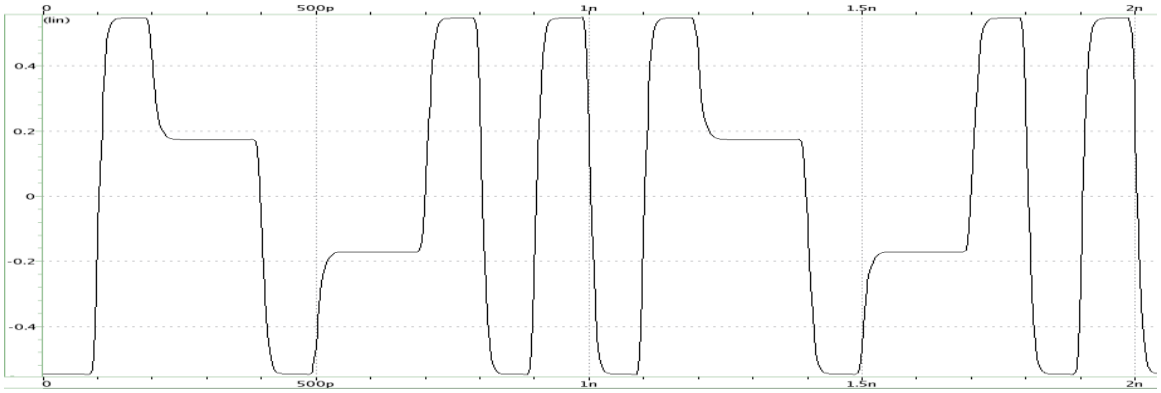

Fig 1.19 Differential swing

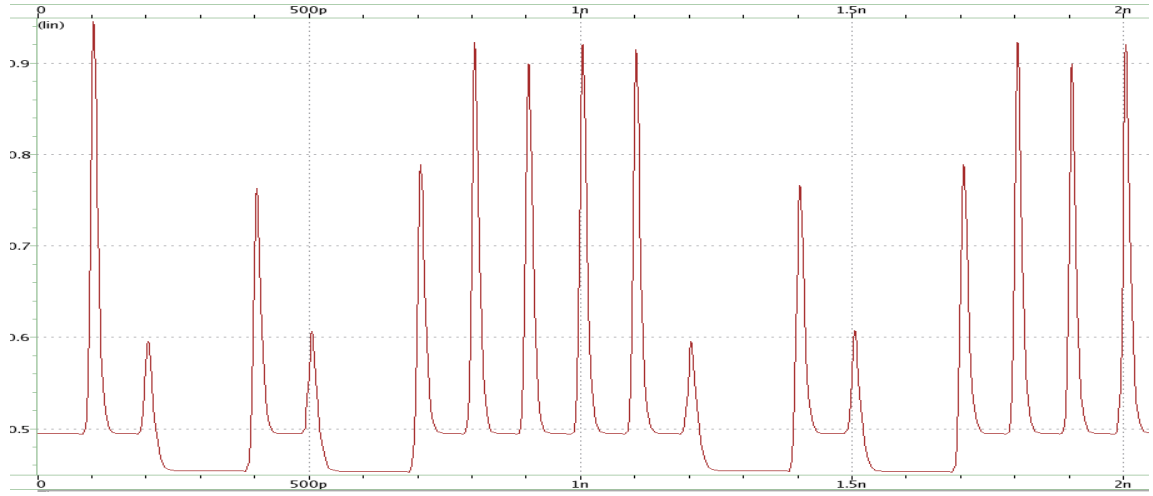

Fig 1.20 Common mode

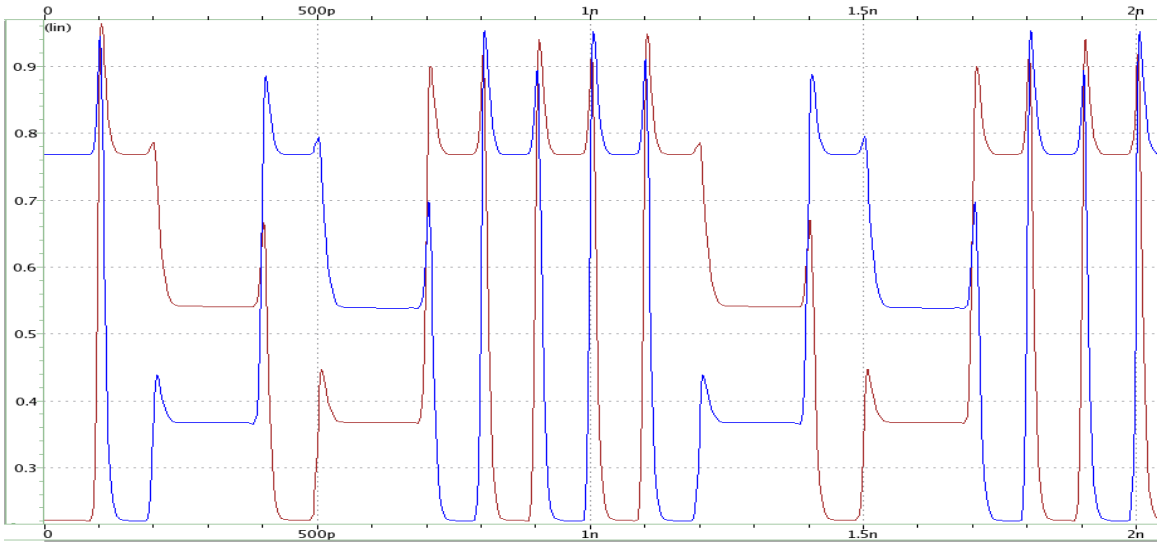

Fig 1.21 Differential output

5) Corner V (SS_0.9_125)

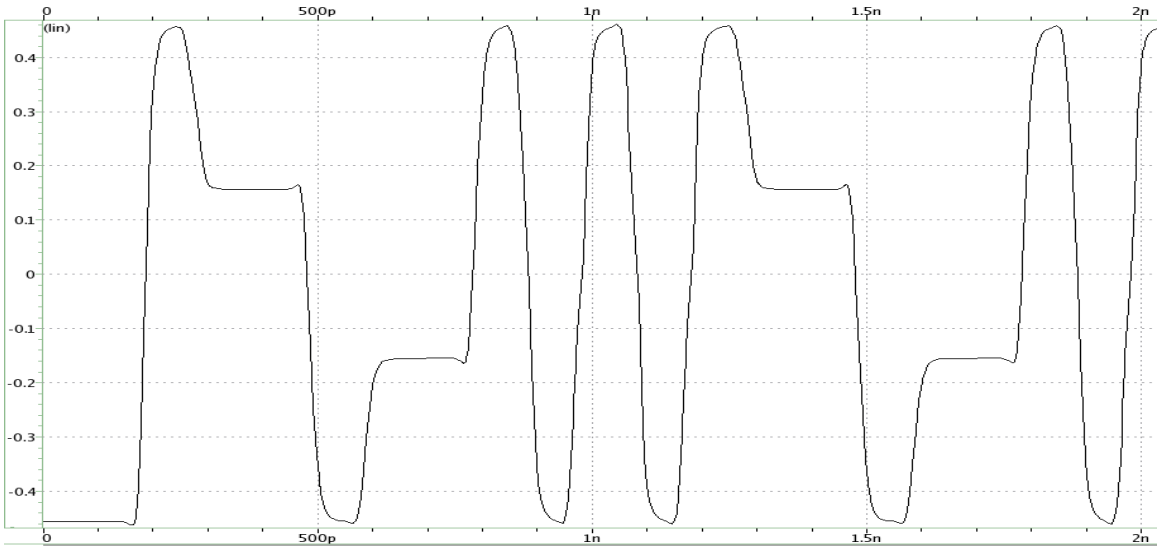

Fig 1.22 Differential swing

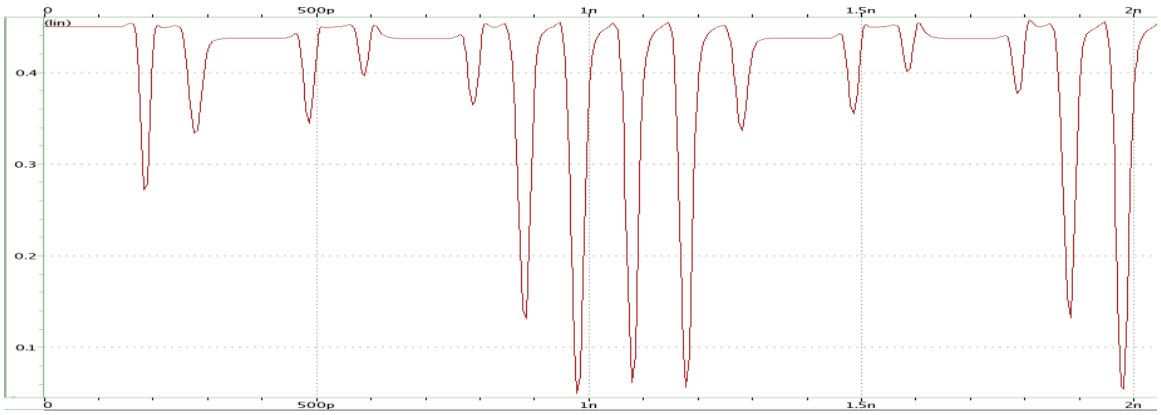

Fig 1.23 Common mode

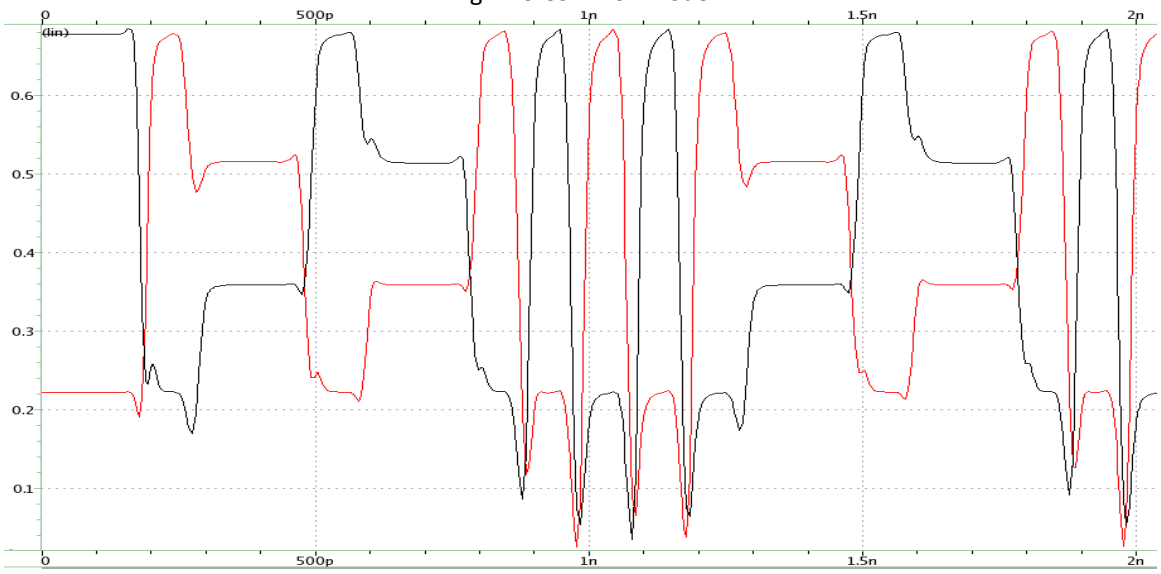

Fig 1.24 Differential output

III. Table

Voltage supply (V)	Temperature	Coroner	Boost Level (mV)	Low level (mV)
1.1	-40	FF	825-275	618 - 418
1.1	125	SS		
1	50	TT	750-250	562 - 437
0.9	-40	FF	675-225	506 - 393
0.9	125	SS		

Table 1.2 swing levels

Stage\Device	Main Nmos µm	Main Pmos µm	Axu Nmos µm	Axu Pmos µm
S0	14	18	7	12
S1	5	6	1	4
S2	6	8	3	4
S3	2.6	3	1.9	2.1
S4	7	20	4	7
Total size	34.6	55	16.9	29.1

Table 1.3 Devices size

IV. Summary

The output have some issues especially the common mode, it should maintains at $\frac{Vdd}{2}$, but in this work the CM ripples as a noise due to mismatch in raise time and fall time in the driver and the serializer. There was no enough time to get a full study on this mismatch and to solve it.