



! Caution !
 Current design lacks advanced self-protection features
 User is responsible for limiting unblanking duty cycle and bias voltage/current
 Current design is tested under following conditions:
 Supply voltage VB: 48V
 Bias current: 3.1A (in each FET)
 Max duty cycle: 3.5% (500us, 70Hz rep rate, passive convection)
 Max pulse width: 1ms

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