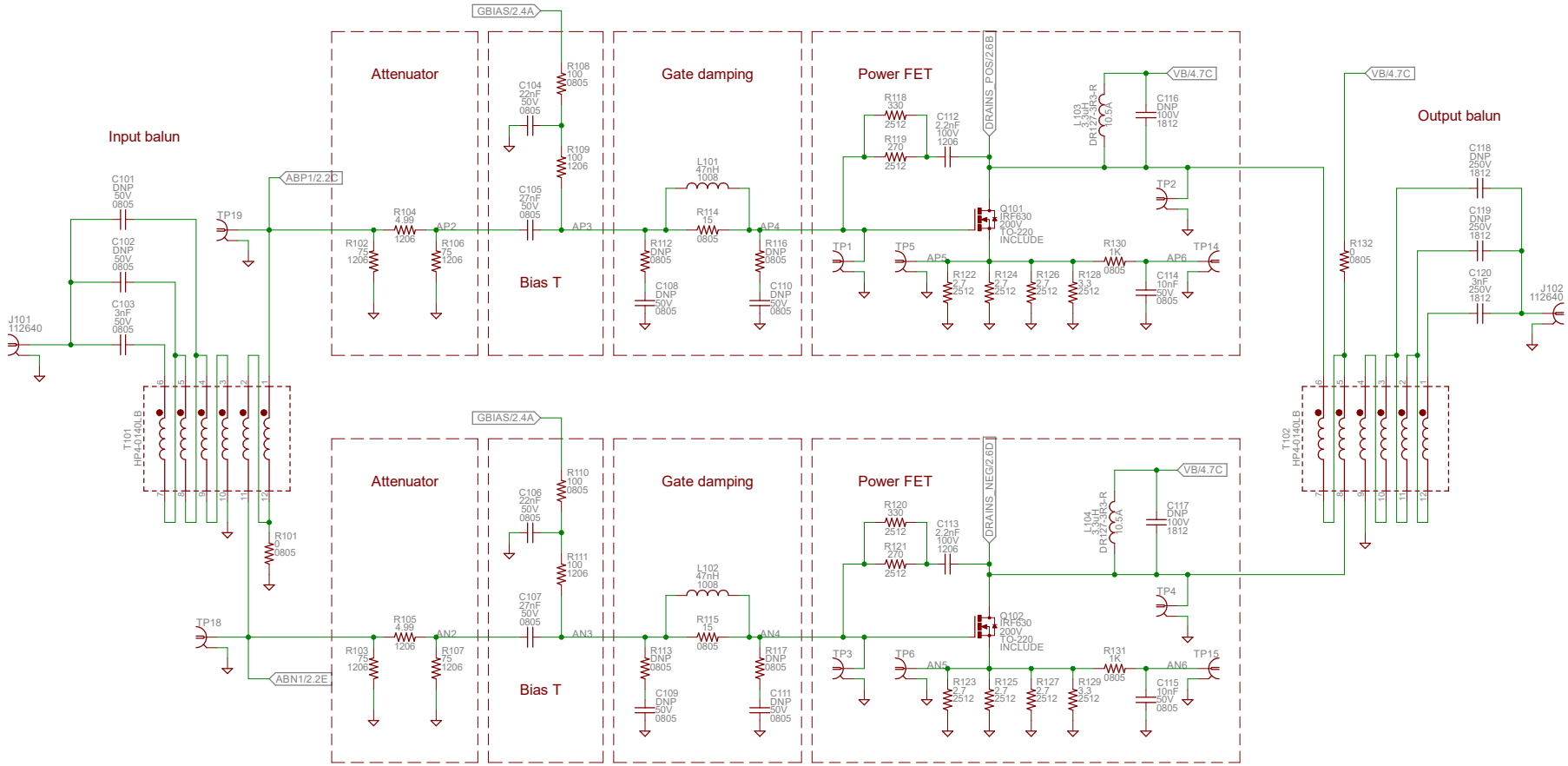

! Caution !
Current design lacks advanced self-protection features
User is responsible for limiting unblanking duty cycle and bias voltage/current
Current design is tested under following conditions:
Supply voltage VB: 48V
Bias current: 3.1A (in each FET)
Max duty cycle: 3.5% (500us, 70Hz rep rate, passive convection)
Max pulse width: 1ms

TITLE: Easy_RFPA_RevA_S2	
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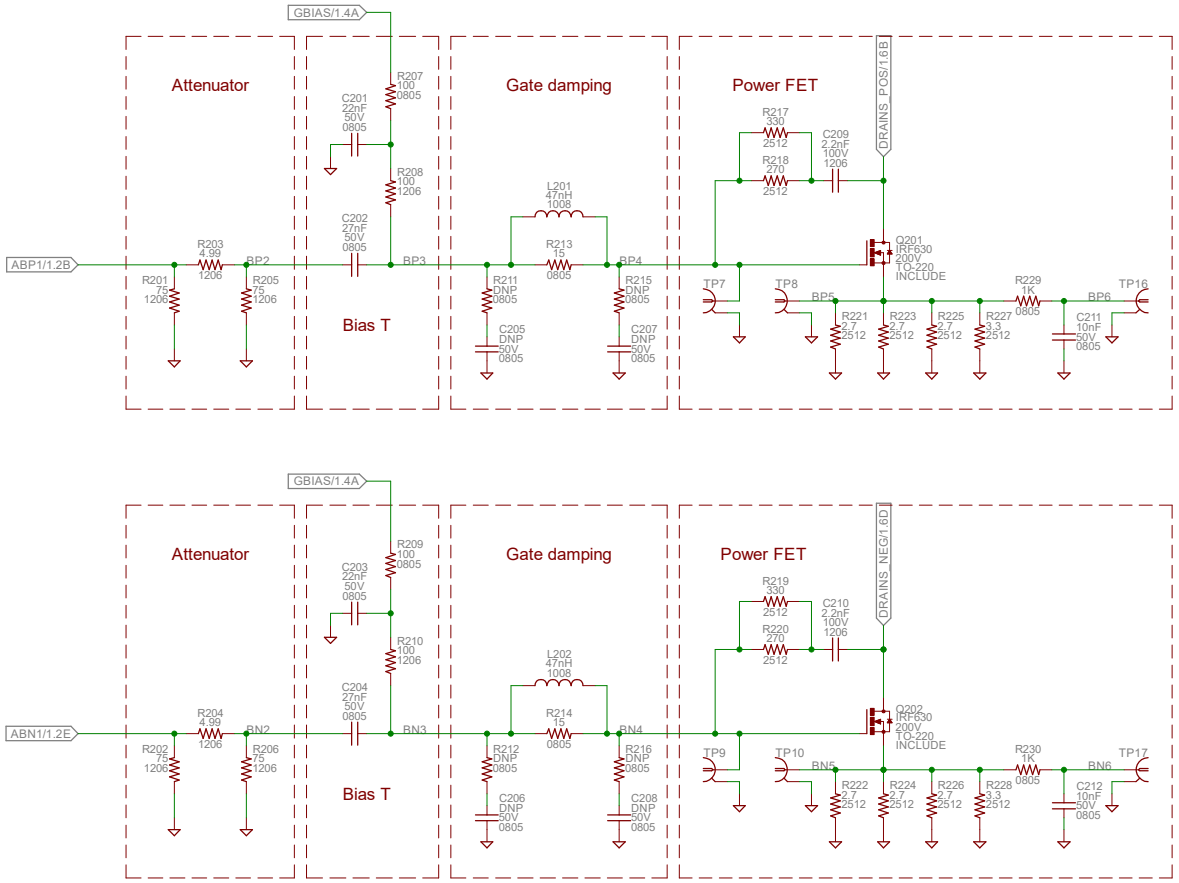

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TITLE: Easy_RFPA_RevA_S2	
Document Number:	REV:
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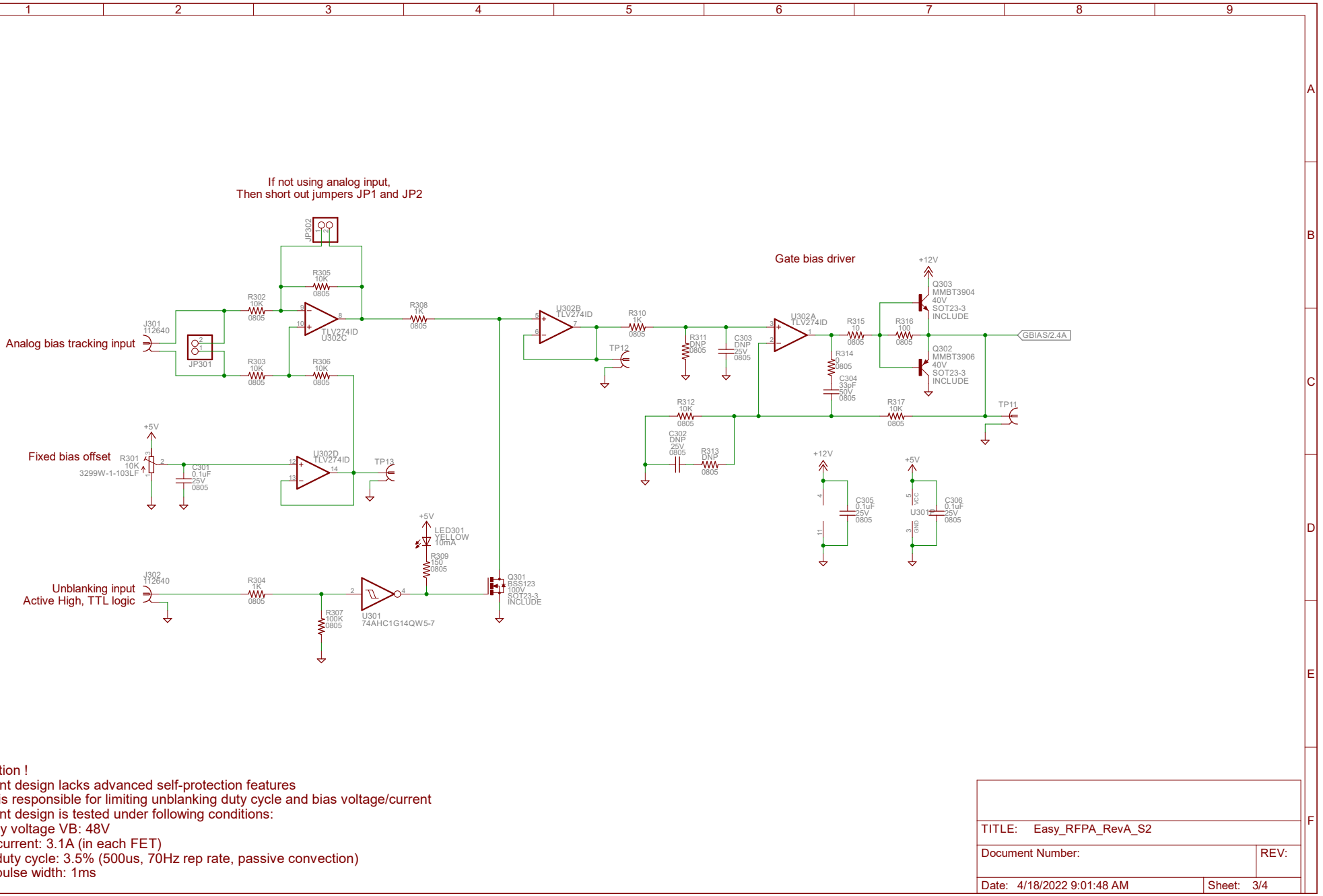
If not using analog input,
Then short out jumpers JP1 and JP2
Analog bias tracking input
Fixed bias offset
Unblanking input
Active High, TTL logic
Gate bias driver
GBIAS/2.4A
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TITLE: Easy_RFPA_RevA_S2
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REV:
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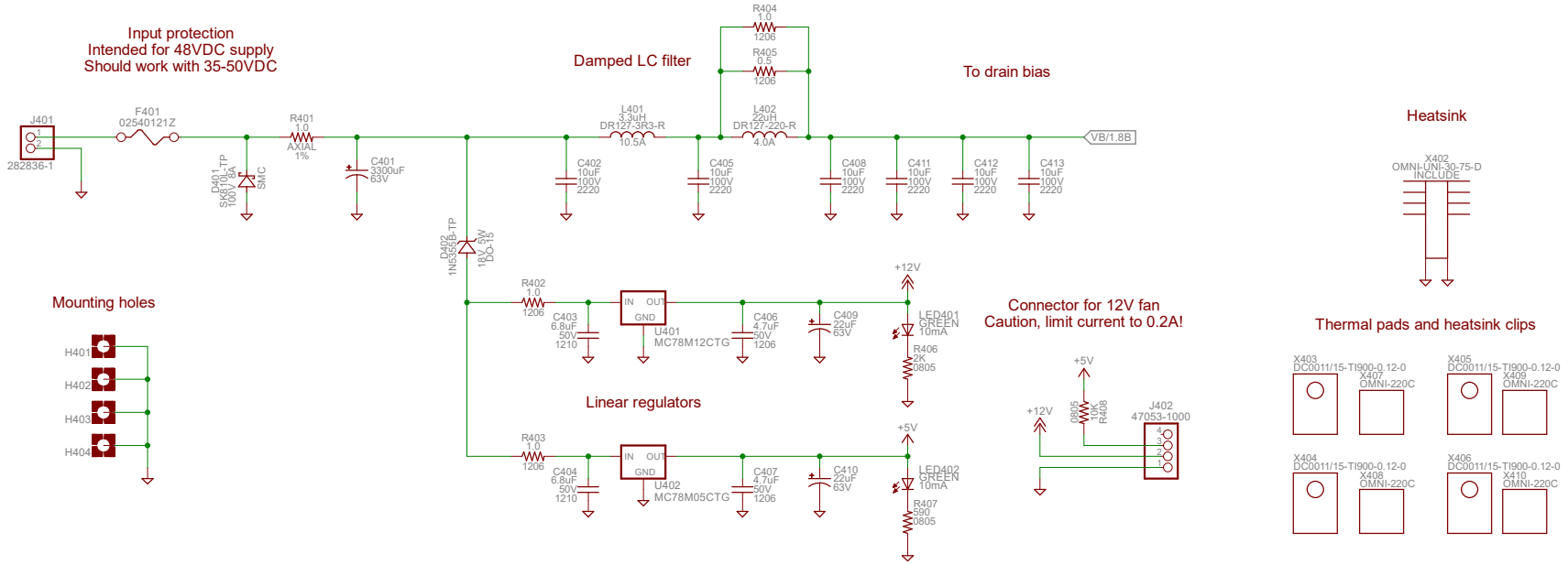

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