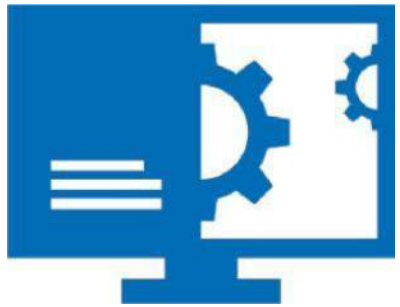


iADC - COMPONENT VERIFICATION

ISCD - LAB EVALUATION -WS2024

AMITH NANJESH

Integrated Systems and Circuit Design

Introduction to ADC measurement

Objective:
In this presentation, we will see the overview of the verification process for the ADC component.

Scope:
•Evaluate static and dynamic performance parameters.
•Utilize lab equipment and automated Python scripts for measurements.

Significance:
•Comparison of actual results with expected outcomes from simulations.

Overview of All Test Cases

Static Measurements:

- Full Scale Range, LSB Size, Resolution
- Gain and Offset
- Differential Nonlinearity (DNL)
- Integral Nonlinearity (INL)

Dynamic Measurements:

- Signal to Noise Ratio (SNR)
- Effective Number of Bits (ENOB)
- Spurious Free Dynamic Range (SFDR)
- Total Harmonic Distortion (THD)

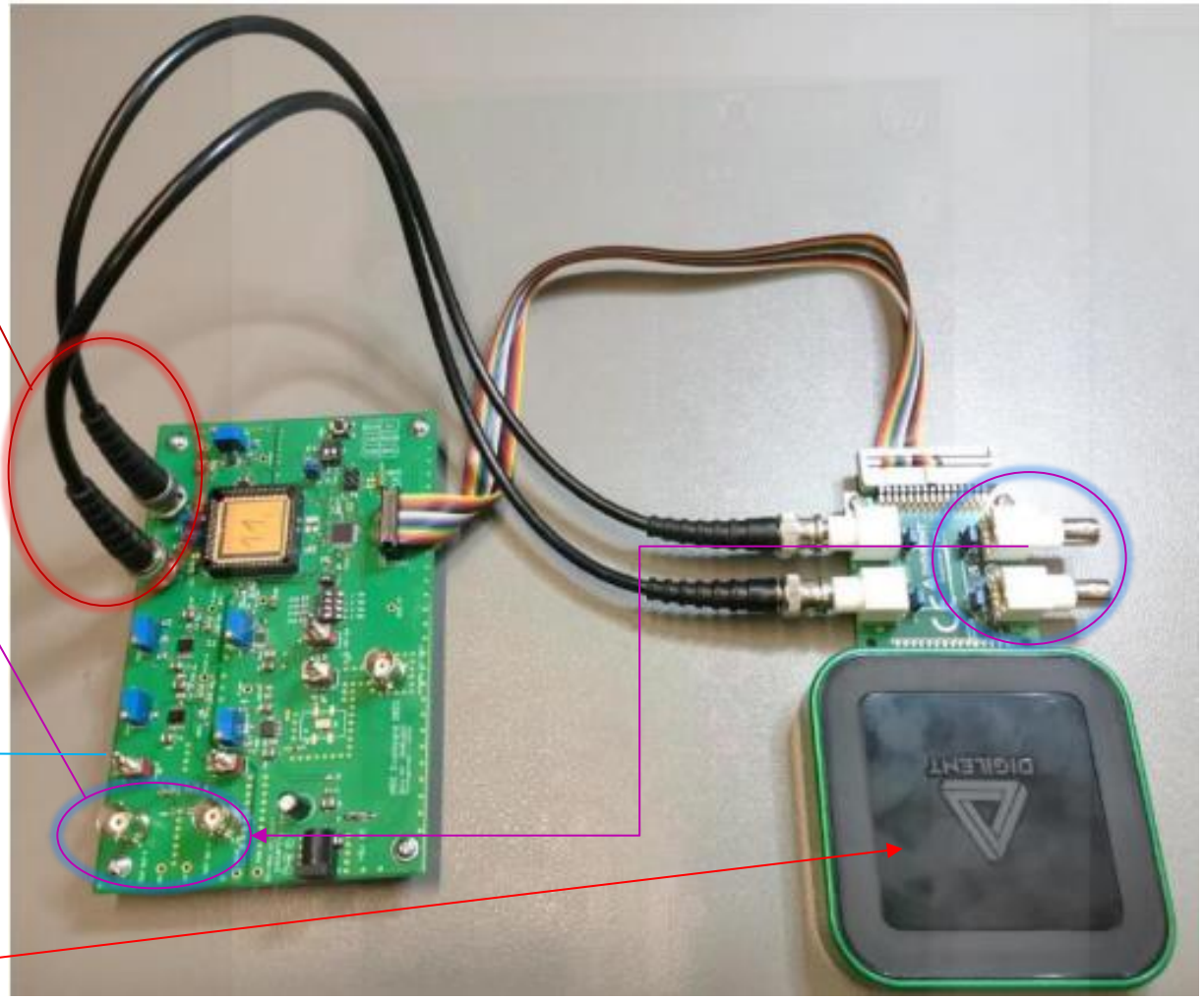
Investigation on internal nodes for debugging

- Comparator output
- Integrator output
- Digital Switches

Different Board Settings

This is the standard connection setup for conducting both static and dynamic tests, utilizing a 5V power supply with a compliance limit set to 200mA and an actual consumption of 18mA.
To use the test pins, we need to configure the DIL switches for TST by setting both switches to the left position ('00' setting) and utilize channels CH0 and CH1.

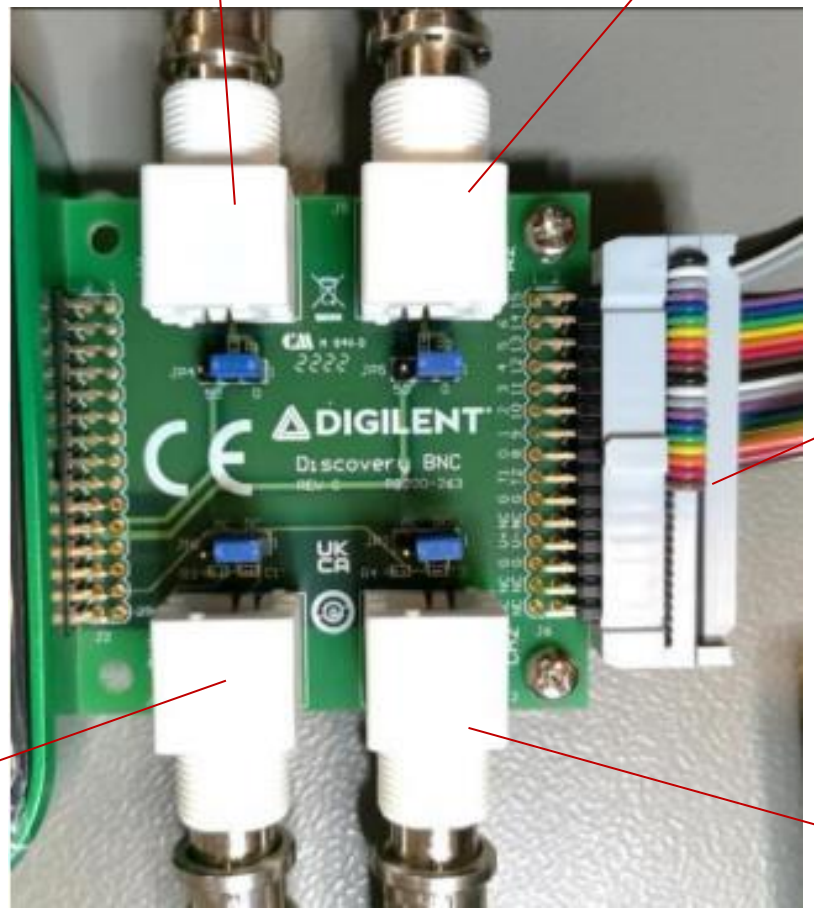
The ADC selection was based on the provided datasheet, where the DIL switch configuration for SEL1 to SEL4 is set to '0001', with a switch in the UP position representing '1'.
You can toggle the switches to select:
•Down: REF (to ADC)
•Up: TST (from ADC)
•The Analog Discovery 3 from Digilent consolidates several modern lab instruments, including multiple channels for digital and analog signal acquisition, an arbitrary waveform generator, and various trigger options.



Analog Discovery Connector PCB

The waveform output on channel 1 is utilized for the positive analog input.

The waveform output on channel 2 is utilized for the negative analog input.



Please ensure that all the jumpers are set correctly by positioning them all to the right, which is away from the AD3 device.

The logic analyzer inputs are used to read signals such as CLKOUT, SIGN, and DATA9...0. Please note that the connector is slightly oversized; when it is mounted symmetrically, one row of pins on each side will remain unconnected.

The input 1 of the V-Meter or oscilloscope is used for REFp/TSTp signals.

The input 2 of the V-Meter or oscilloscope is used for REFn/TSTn signals.

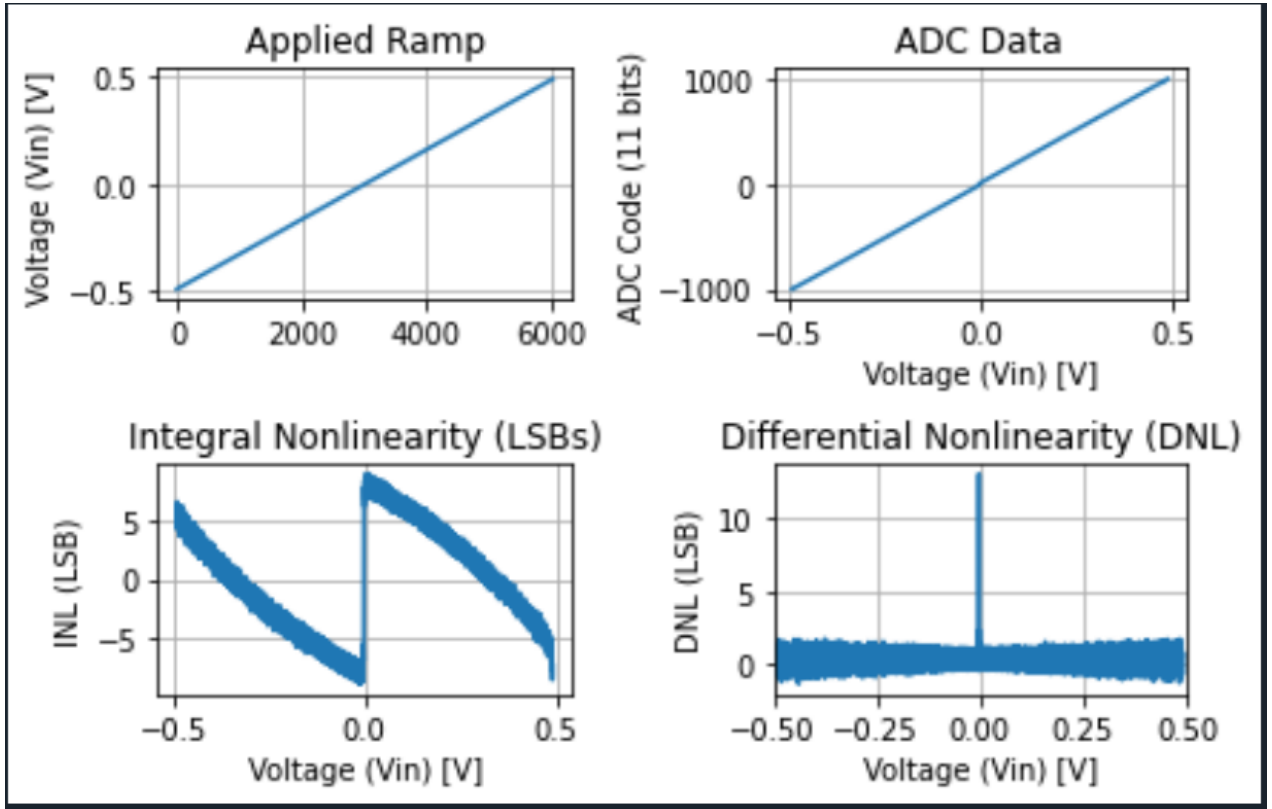
Example 1,2,3

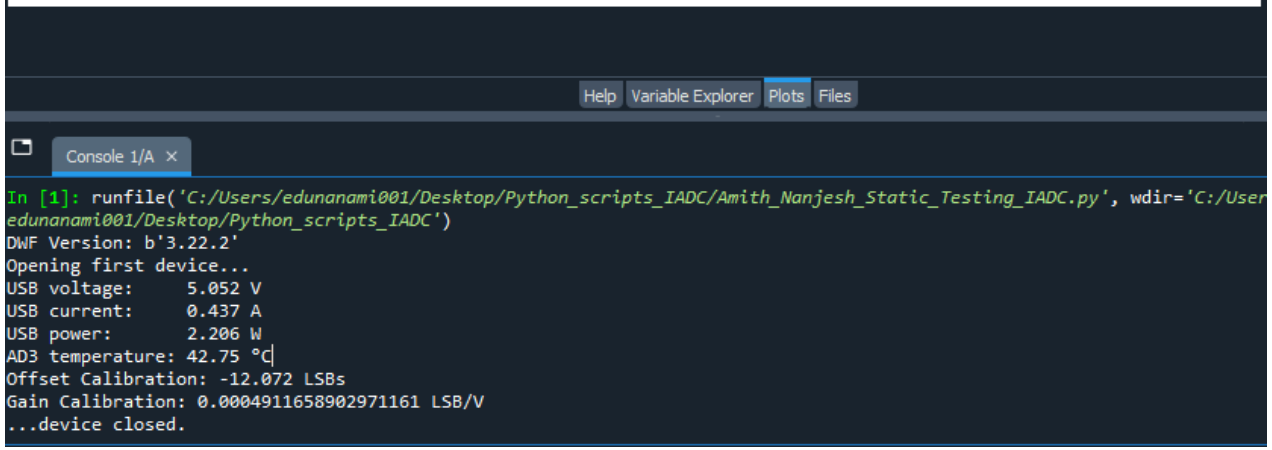
Before starting to test with the device, it was essential to ensure the basic setup was functioning properly. To achieve this, the following steps were taken:

1.Connect Loopback Cables: This ensures that the signals are properly routed and can be checked for integrity.
2.Measure the Created Stimulus: Verify that the stimulus generated by the setup is as expected and can be accurately measured.

Additionally, in the scripts, the term "True" indicates that a virtual device is being used for "mocking". This means the tests are being conducted in a simulated environment to validate the setup before working with the actual hardware.

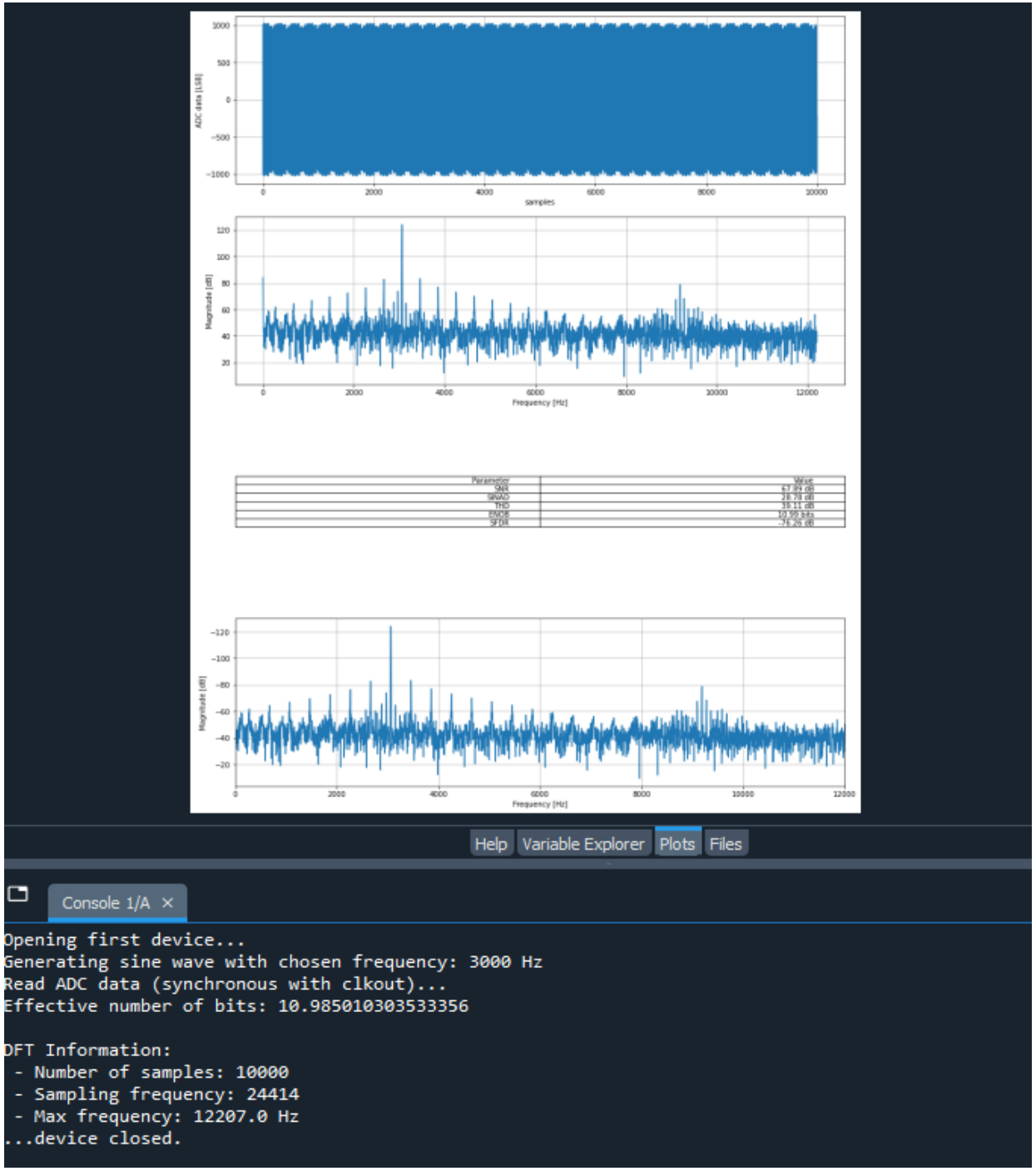
Static Testing





Using Python scripts, we performed static testing to calculate various ADC performance parameters, including offset calibration, gain calibration, Integral Nonlinearity (INL), and Differential Nonlinearity (DNL).

- **Offset Calibration:**
  - Applied a zero-voltage signal to determine the ADC's baseline offset.
  - Calculated the average offset from the ADC data and adjusted accordingly.
- **Gain Calibration:**
  - Applied a known reference voltage to determine the ADC's gain.
  - Computed the gain by comparing the ADC output to the known reference voltage.
- **INL and DNL Calculation:**
  - Generated a voltage ramp to evaluate the ADC's linearity.
  - Recorded ADC responses to the ramp and compared them to ideal values



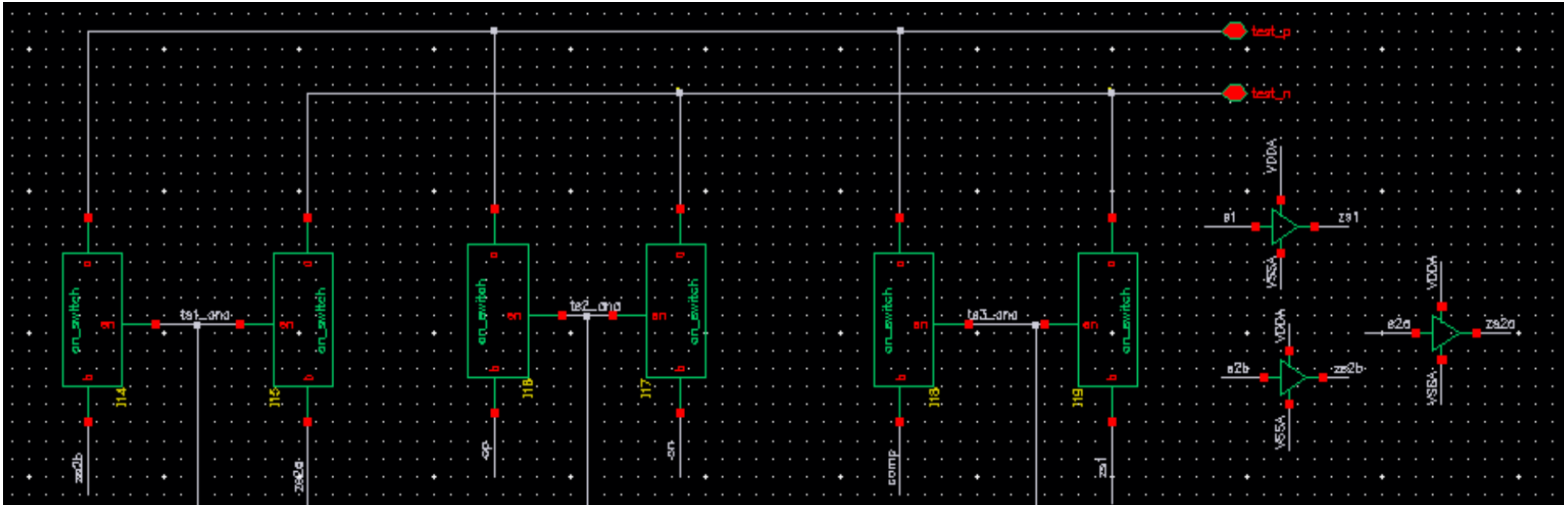
Dynamic Testing

Python scripts are utilized to perform dynamic testing, calculating various ADC performance parameters such as Signal-to-Noise Ratio (SNR), Signal-to-Noise and Distortion Ratio (SINAD), Total Harmonic Distortion (THD), Effective Number of Bits (ENOB), and Spurious-Free Dynamic Range (SFDR).

- **Signal Generation:**
  - A sine wave with a specified frequency is generated using the Analog Discovery 3 (AD3) tool.
- **Data Acquisition:**
  - ADC data is acquired synchronously with the clock output.
- **Dynamic Parameter Calculation:**
  - A window function is applied to the data followed by a Discrete Fourier Transform (DFT).
  - SNR, SINAD, THD, ENOB, and SFDR are calculated from the DFT results.

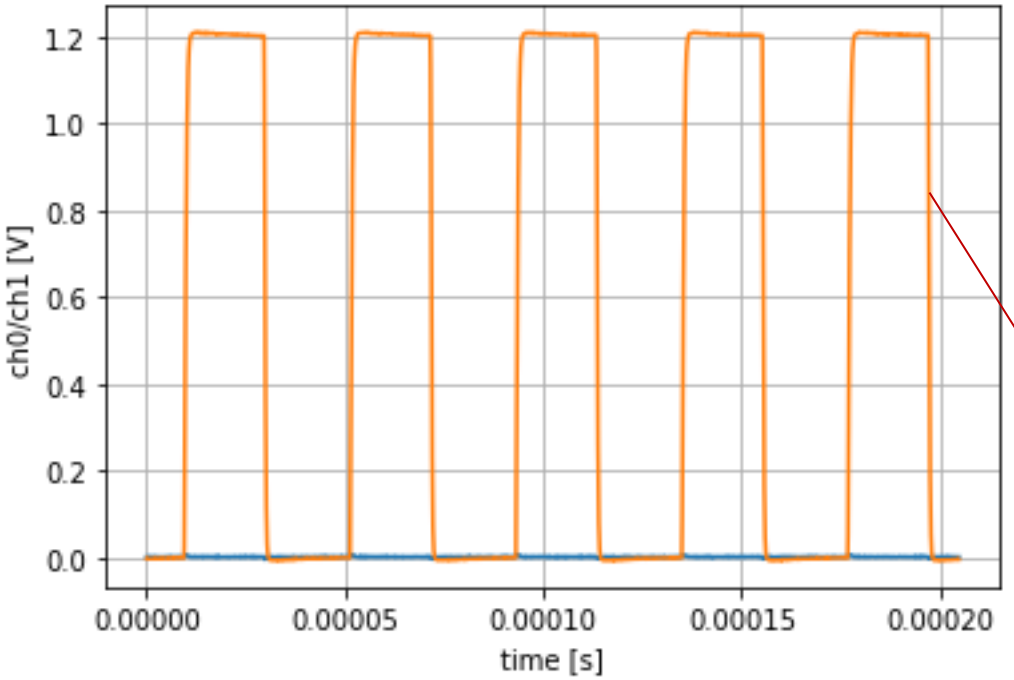
Test Pin switches

Internal nodes of the ADC, such as the comparator's output, integrator's output, and digital pins like S1, S2a, and S2b, were investigated using the test pin switches to observe their behavior. In the ADC, S2b is high for a positive input while the comparator is low in the same scenario. This behavior, along with the integrator displaying a full range of output, was clearly observed during testing

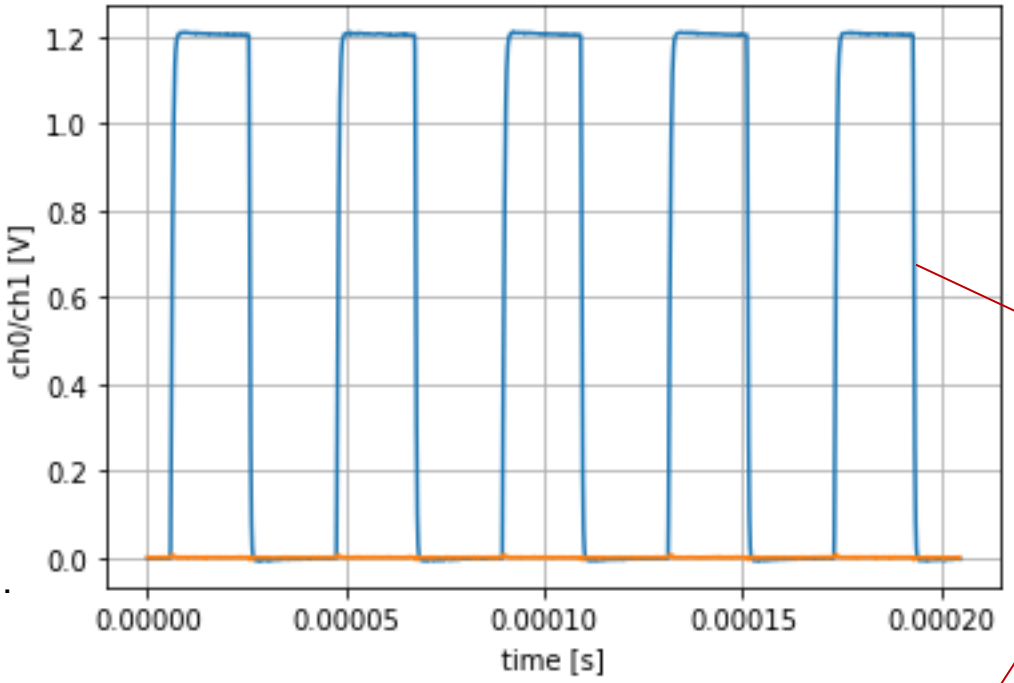


The above picture is for the reference for the test pins that have been considered during the design

Test Pin switche1



S2b remains high during positive deintegration.

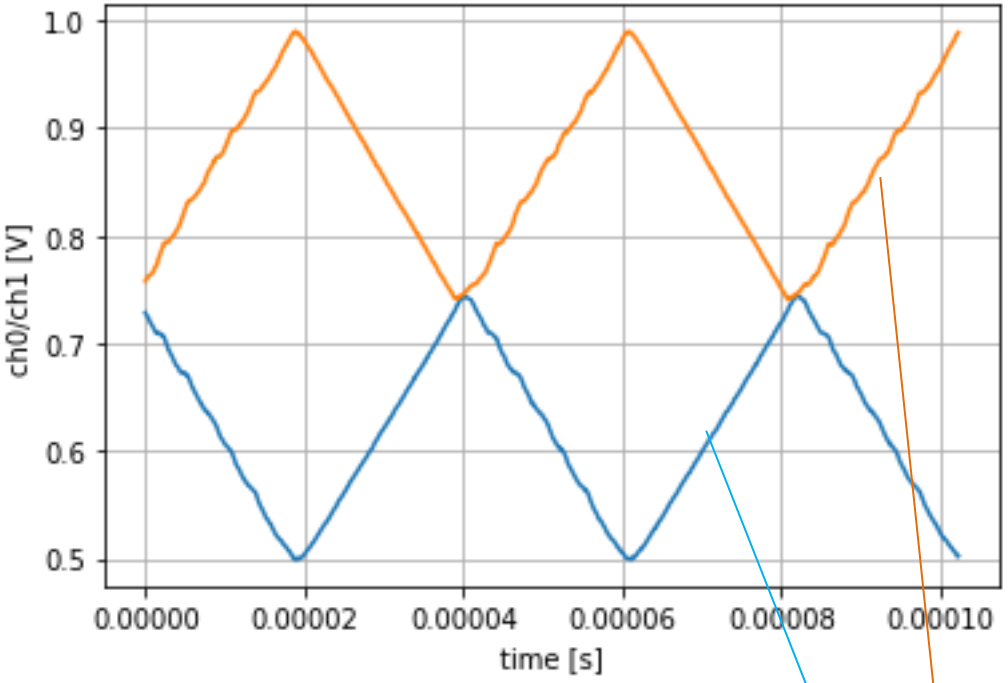


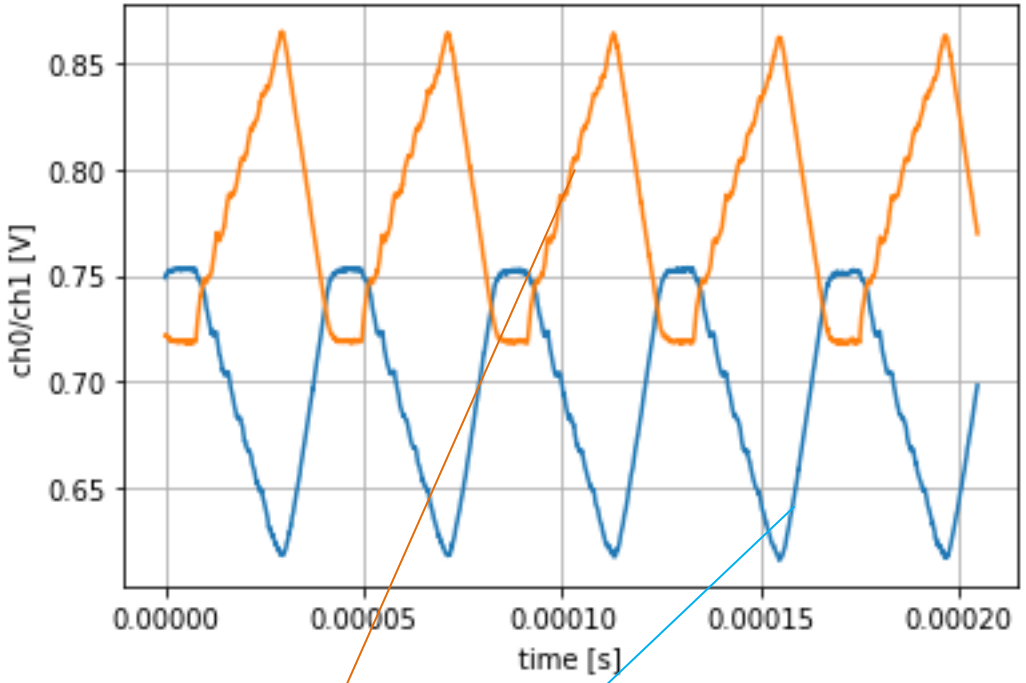
S2a remains high during negative deintegration.

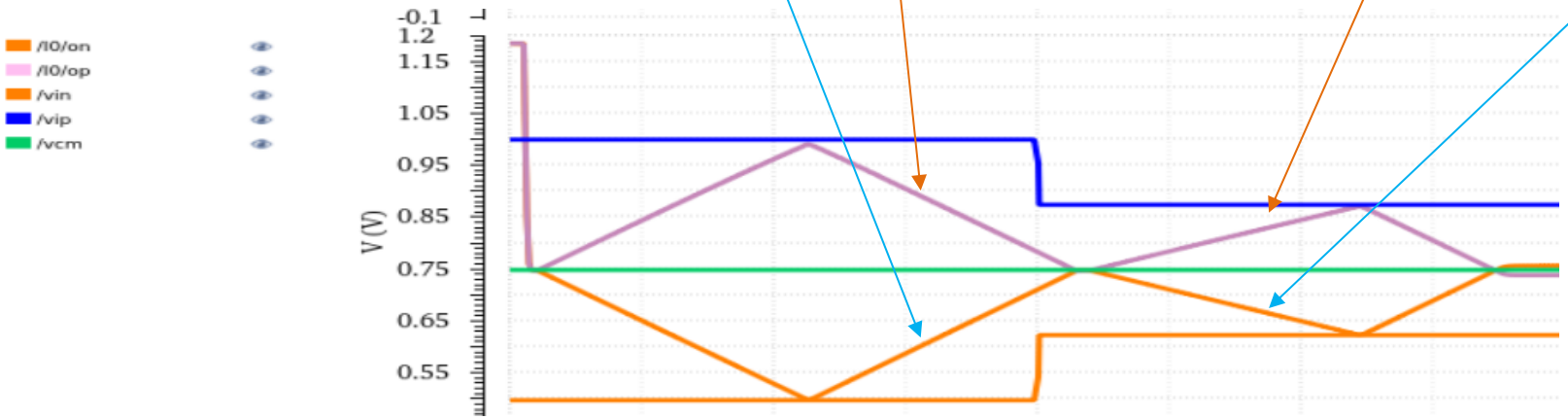
The purple-colored signal represents s2b, and it remains high for both the full scale and half scale of the positive input.

The blue-colored signal represents S2a, which remains high when negative half scale deintegration is completed.

Test Pin switche2

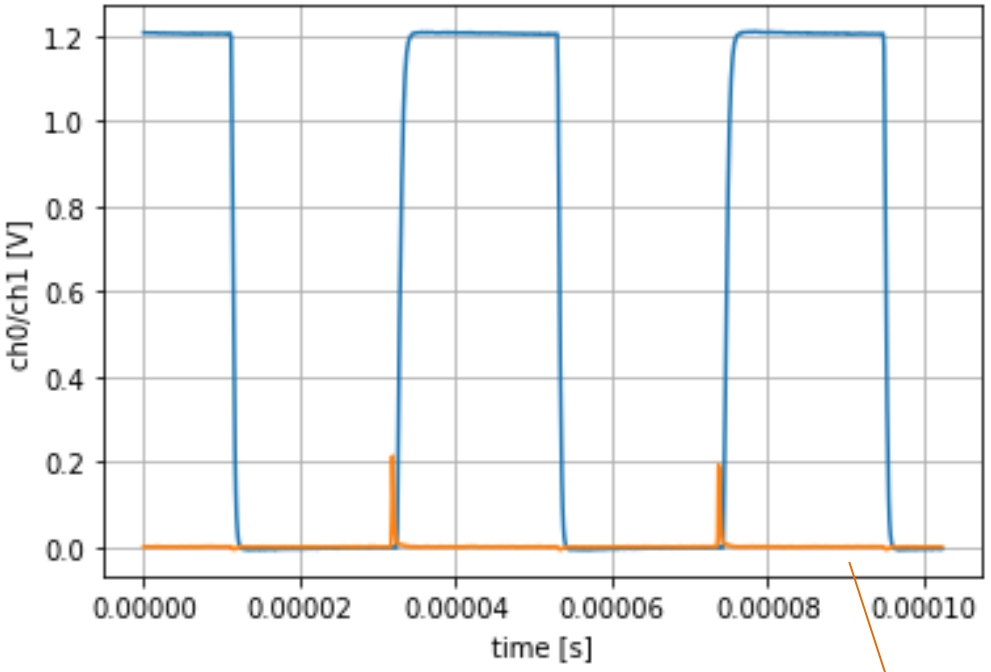


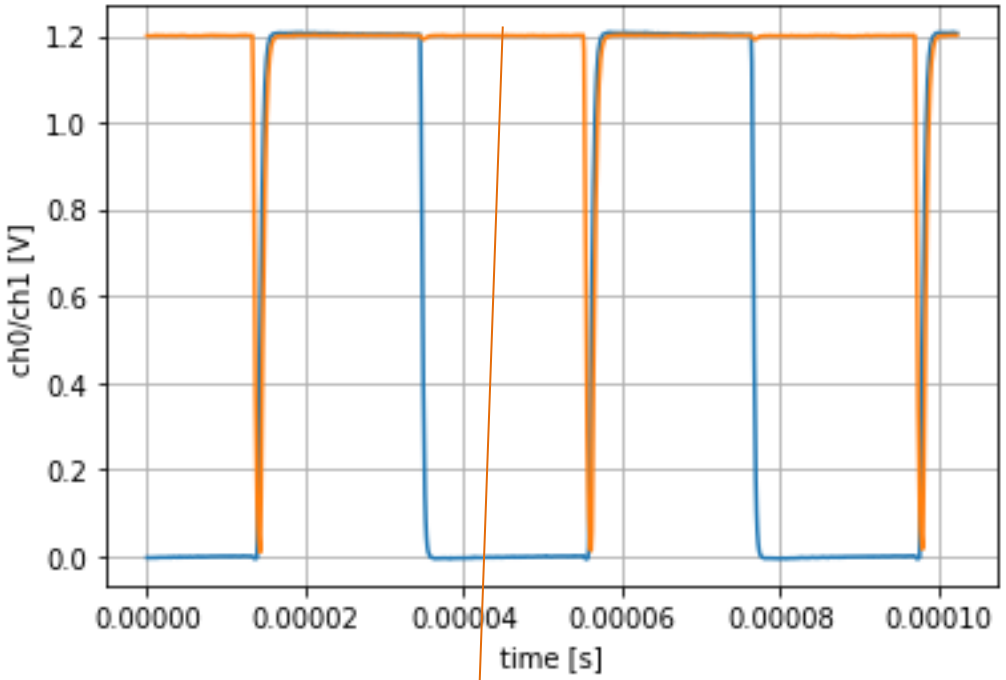




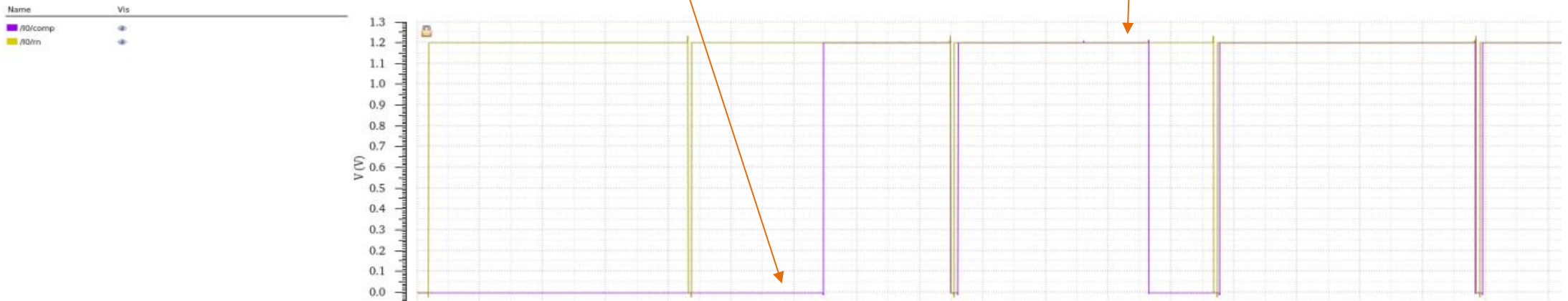
For test pin 2, which is connected to the output of the integrator, we can clearly observe the integration and deintegration processes occurring for both full scale and half scale ratios. While there are no glitches present during the full-scale operation, some disturbances are observed at half scale. These disturbances are somewhat expected, as they were noted during simulation.

Test Pin switche3



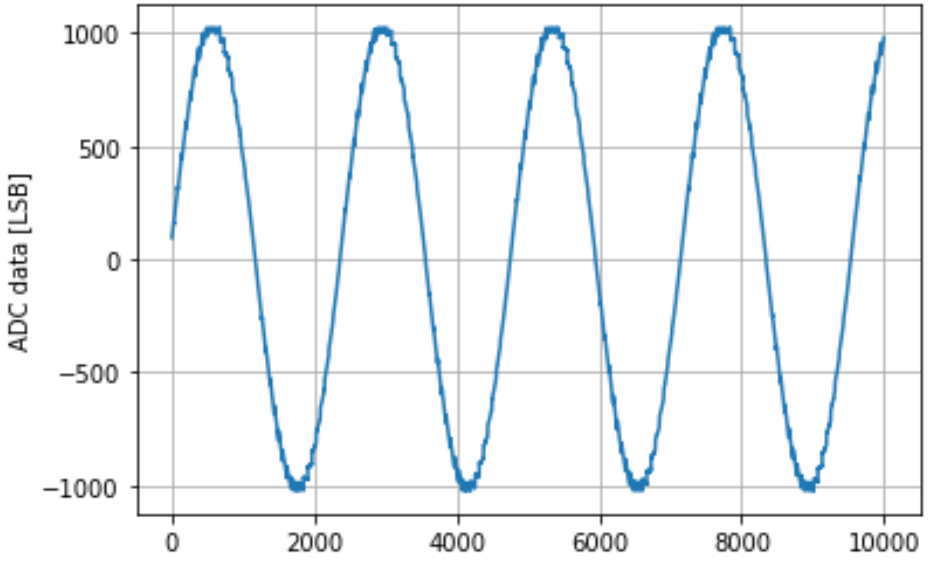


Here, we can clearly observe that for a positive input, the comparator remains low and toggles to high once deintegration is completed. Conversely, for a negative input, the comparator behaves in the opposite manner, remaining high and toggling to low once deintegration is done.

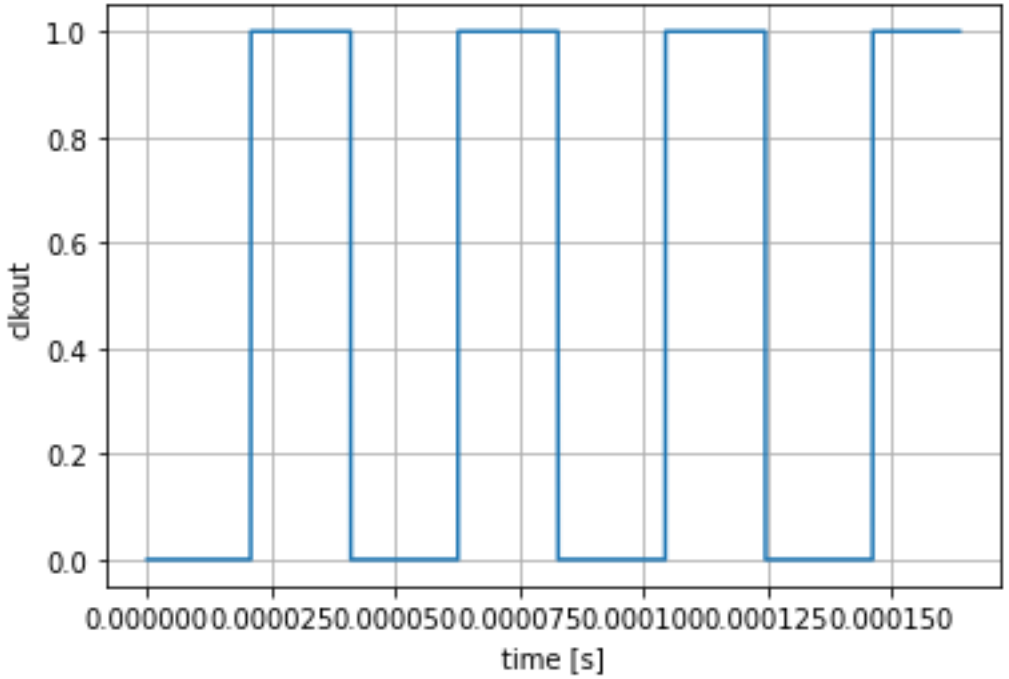


Note: Please ignore the yellow-colored signal as it does not represent S1.

Example Script for ADC Data Acquisition

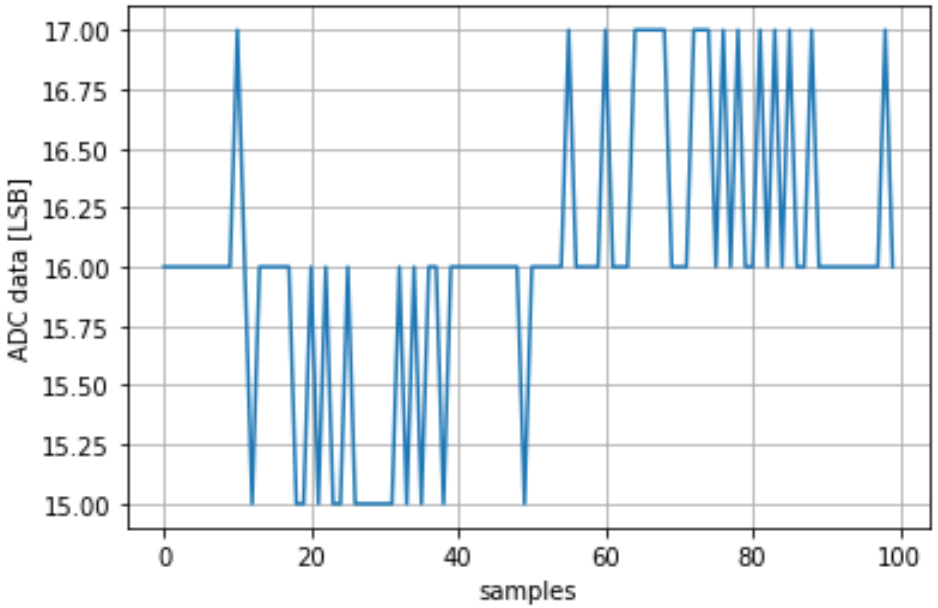


Using the provided script, the process of generating a sine wave, reading ADC data, and plotting the results using the Analog Discovery 3 (AD3) device was demonstrated.



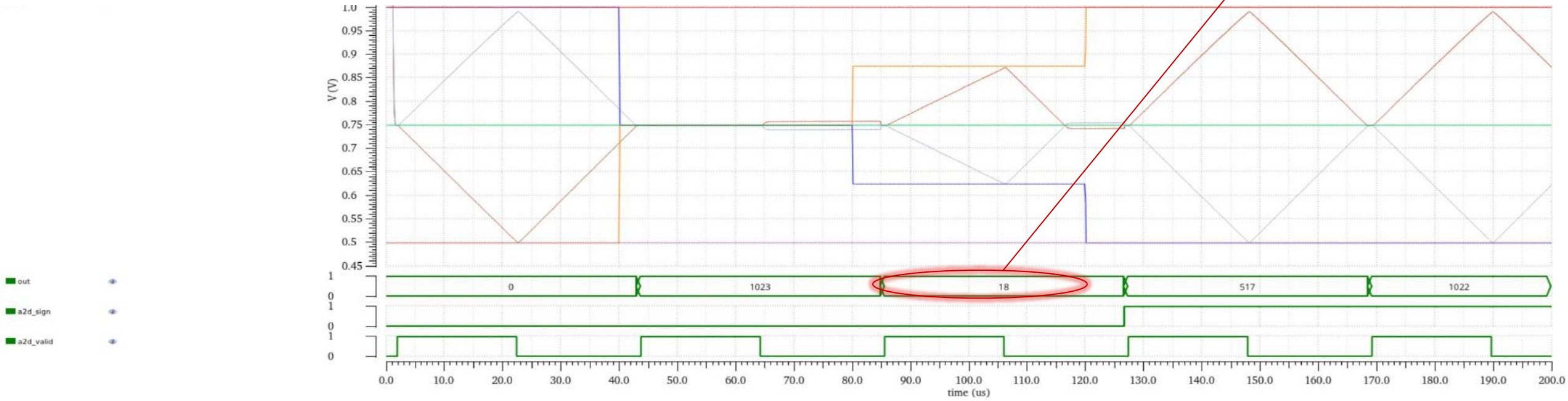
Using the ADC data acquisition script, the process of reading the clockout signal from the logic analyzer at 100MS/s using the Analog Discovery 3 (AD3) device was demonstrated

Results and Discussion.



The simulation result for the zero input case, after RC extraction, closely matches the ADC data output for the same condition, and the behavior aligns with expectations

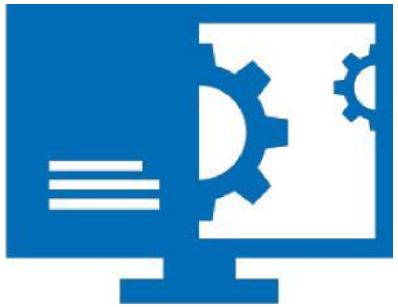
For the zero input case, the simulation shows an offset of 18 LSBs (Least Significant Bits).



Results and Discussion Cont…

Parameter	Value
SNR	56.42 dB
SINAD	42.26 dB
THD	14.15 dB
ENOB	9.08 bits
SFDR	-63.01 dB

If we consider the Signal-to-Noise and Distortion ratio (SINAD) for the Effective Number of Bits (ENOB) calculation, we roughly obtain an ENOB of around 7 bits.



THANK YOU FOR YOUR ATTENTION