Introduction to Integrated Circuits Design Project

Initial Design/Floorplanning Tasks and Layout Estimates

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1 ADC Function Description

The Analog-to-Digital Converter (ADC) function described below performs the continuous conversion of a differential input voltage ($V_{\text{in}_p} - V_{\text{in}_n}$) with respect to a differential reference voltage ($V_{\text{ref}_p} - V_{\text{ref}_n}$) into a digital sign/magnitude bus. The conversion is executed at a constant sample rate using a dual-slope integrating function to achieve the best possible conversion time.

Parameters

- Supply voltage: $V_{\text{dd}} = 1.2\,\text{V}$
- Common mode voltage: $V_{\text{cm}} = 0.75\,\text{V}$
- Reference voltages: $V_{\text{ref}_p} = 1\,\text{V}$, $V_{\text{ref}_n} = 0.5\,\text{V}$
- Digital input clock: 50 MHz
- Full-Scale Range (FSR):
  - $V_{\text{in}_{\text{max}p}} = V_{\text{in}_{\text{max}n}} = 1\,\text{V}$
  - $V_{\text{in}_{\text{min}p}} = V_{\text{in}_{\text{min}n}} = 0.5\,\text{V}$ (absolute)
  - $V_{\text{in}_p} = V_{\text{in}_n} = \pm 0.25\,\text{V}$ (relative to V_{cm})
  - $V_{\text{in}_{\text{pp, single\_ended}}} = 0.5\,\text{V}$, $V_{\text{in}_{\text{pp, differential}}} = 1.0\,\text{V}$ (dynamic range, with respect to V_{cm})
- Output code: 11 bits (using sign/magnitude format)
- Output clock: Signaling a new sample available with a constant period expected
- Conversion time: Better than 2500 input clock cycles ($< 50\,\mu\text{s}$) leading to at least 20 kS/s sample rate
- Total Unadjusted Error (TUE): ± 1 LSB typical is possible, aiming for less than ± 3 LSB

2 Dual-slope integrating ADC basics:

General Remarks

The literature has been reviewed to comprehend the principles of ADCs, gaining familiarity with differential signaling in comparison to single-ended methods. The fundamental components, encompassing switches, opamps, comparators, and the ADC state machine, have been understood. The concept of utilizing a fully differential integrator with an opamp has also been grasped. This collective knowledge has facilitated the understanding and addressing of pertinent questions regarding top-level ADC specifications and critical operational states.

2.1 What are the relevant phases of a dual-slope integrating ADC?

During its functioning, a dual-slope integrating ADC goes through numerous significant phases.
The following are the main stages of a dual-slope ADC:
1. Integration (Charge Phase):
-In this phase, the analog input signal integration is started by the ADC. It achieves this by charging a capacitor for a predetermined amount of time using a voltage source. The voltage across the capacitor determines the input voltage proportionately.

2. Phase of De-integration:
- The ADC goes through a phase where the input signal's polarity is reversed after the initial integration phase. The integrator is given a known reference voltage with the opposite polarity to accomplish this. And the increase in voltage is permitted to continue until the integrator output goes back to zero. During this phase, the capacitor is drained at a predetermined pace, which is substantially slower than the charge rate.

3. Comparator Phase:
-Following the integrate phase, a comparator is used to compare the voltage across the integrating capacitor to a reference value. This comparison causes the comparator to generate a logic signal.

4. Counter Phase:
-In this phase, a counter typically a binary counter is activated and starts counting clock pulses. The counter continues to count until the comparator signals that the voltage across the integrating capacitor has reached the reference value. At this point, the counter stops counting.

5. Digital conversion:
-After the counter phase, the count value acquired from the counter represents the analog input voltage. In digital representation, the count is correlated with the input voltage.

2.2 What is the difference between single-ended and differential signals?

-Single-Ended Input ($V_{\mathbf{se}}$)
The ADC measures the voltage in a single-ended input concerning ground (*gnd*). The voltage measured by the ADC, V_{se}, is the voltage at the input terminal (V_{in}) referenced to ground:

$$V_{\text{se}} = V_{\text{in}}$$

- It is more prone to noise and mistakes.

-Differential Input ($V_{\mathbf{diff}}$)
In a differential input, the ADC measures the voltage difference between two input terminals, typically labeled "V_{in_p}" and "V_{in_n}". The voltage measured by the ADC, V_{diff}, is the difference between the voltage at the positive terminal (V_{in_p}) and the

voltage at the negative terminal (V_{in_n}):

$$V_{\text{diff}} = V_{in_p} - V_{in_n}$$

- Because it considers the difference between the two measurements, it is more efficient at managing mistakes and noise.

These equations reflect the fundamental difference between single-ended and differential inputs in a dual-slope integrating ADC. Single-ended measurements are taken concerning a common ground, while differential measurements are made by calculating the voltage difference between two input terminals. A differential input can yield higher accuracy in a dual-slope ADC, particularly in the presence of noise or interference.

2.3 What is a common-mode voltage/level (of such a differential signal)?

Common Mode Voltage

The Common Mode Voltage (V_{cm}) is the average of the two differential signals and can be visualized as the DC level of the signals:

$$V_{\text{cm}} = \frac{V_{\text{in}_p} + V_{\text{in}_n}}{2}$$

Differential Signals

Differential signals have a few advantages:

-Greater Immunity to Environmental Noise: When the differential signal $V_{\text{in}_p} - V_{\text{in}_n}$ is taken into account, the noise that is present in both V_{in_p} and V_{in_n} will be eliminated.
-Greater Swing in Voltage for V_{in_p}: Based on the requirements provided in ADC, the differential signal $V_{\text{in}_p} - V_{\text{in}_n}$ achieves a greater voltage swing.

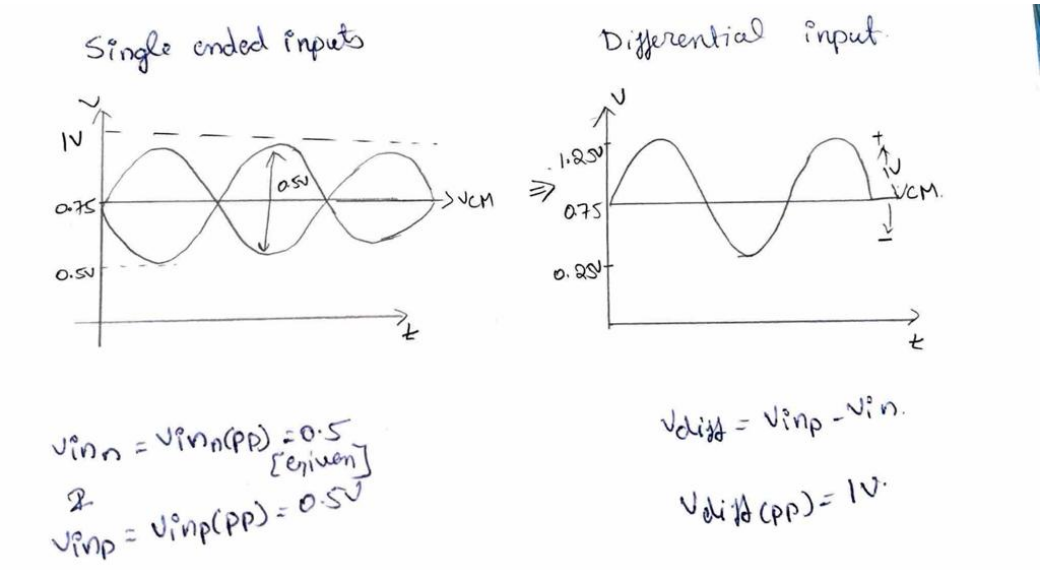

Figure 1: Differential input Signal

2.4 What are the components used in the dual-slope integrating ADC and how does the ADC circuit look like?

In this project, fully differential Dual slope ADC has been used. ADC circuit can be seen in Figure 2.
The components used in this dual slope ADC are:-

- Switches:- To be used in a future implementation, switches must have their values stated and their open and closed switch resistance mentioned.

- The differential input (In_p, In_p) voltage will be connected to the differential integrator via S1.
- The $Ref_p = 1$V reference voltage will be connected to In_p of the differential integrator by S2a, and the $Ref_n = 0.5$V reference voltage will be connected to In_n.
- The differential integrator's In_p will be connected to the $\mathrm{Rref}_n = 0.5\,\mathrm{V}$ reference voltage through S2b, and $\mathrm{Ref}_p = 1\,\mathrm{V}$ reference voltage to In_n.
- S3 will discharge the capacitors by resetting the differential integrator which are connected both the sides.

- Opamp configured as a differential integrator:-

In this phase, Opamp will perform the Integration and Measurement Phase(De-integration phase) when Vin is connected for a fixed time T1.A capacitance is charged by current during a predetermined period, producing an output voltage $V_{out,int}$. The input voltage value will determine the slope of the capacitor's charge.The time duration of this phase is given as:
$T1 = T_{\mathrm{clk}} \times 2N = \frac{1}{f_{\mathrm{clk}}} \times 2^n = \frac{1}{50\,\mathrm{MHz}} \times 2^{10} = 20.48\,\mu\mathrm{s}$
A constant current discharges the capacitor when the input voltage V_{in} is disconnected and a constant voltage (V_{ref}which must be lower than $V_{in}$is connected). Calculation of the output voltage of this phase can be seen in the figure 3.

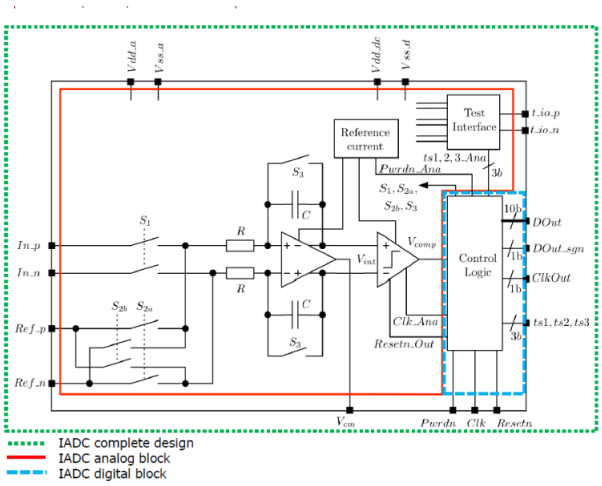

Figure 2: Fully differential Dual slope ADC circuit

- Opamp configured as a differential Comparator:-

The point at which the capacitors discharge is determined by comparing the integrator's output, $V_{out,\text{int,diff}}$. And control logic can then be enabled or disabled depending on the input received.Output behavior graph can be observed in figure 4.

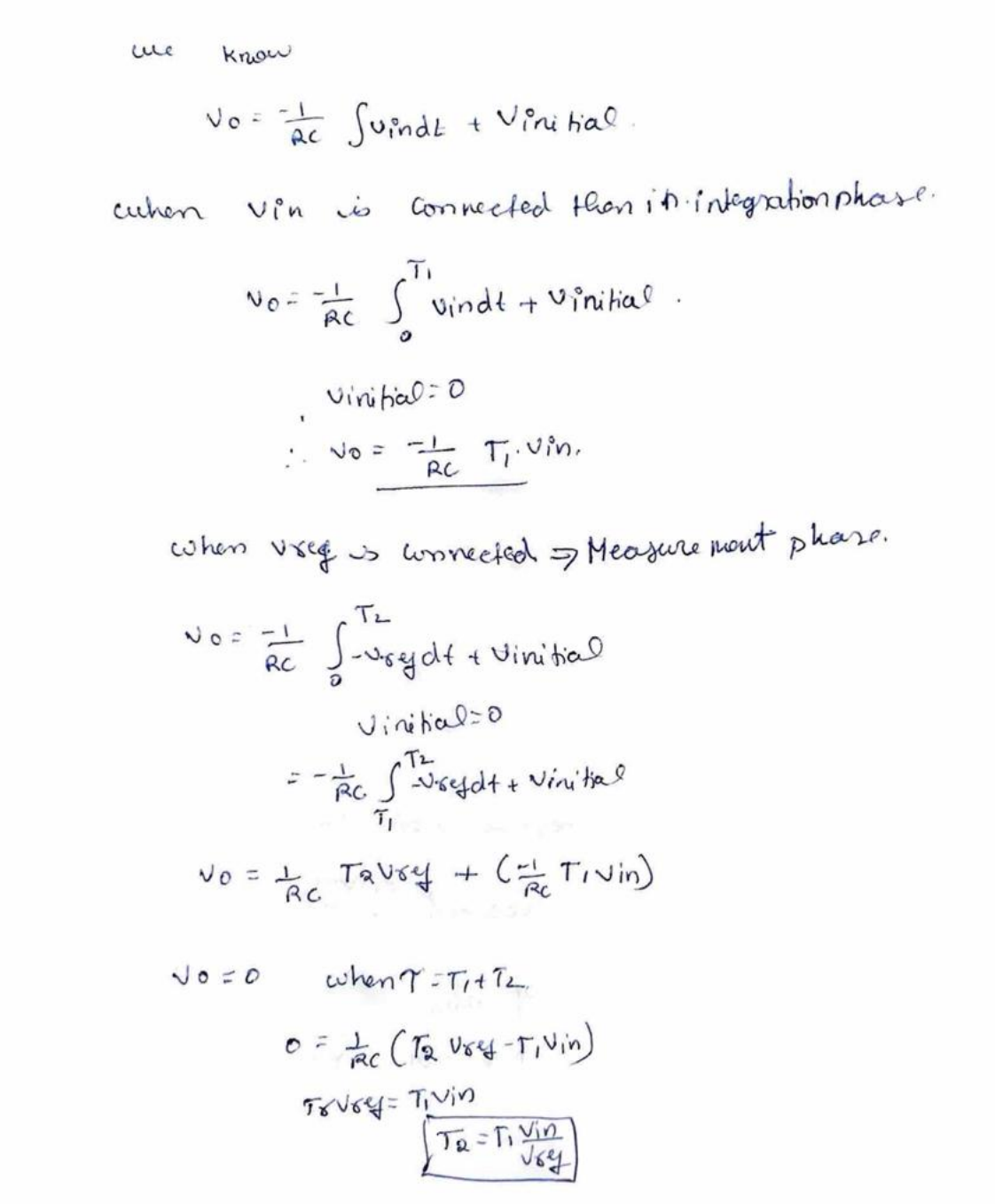

Figure 3: Vout of Integrator

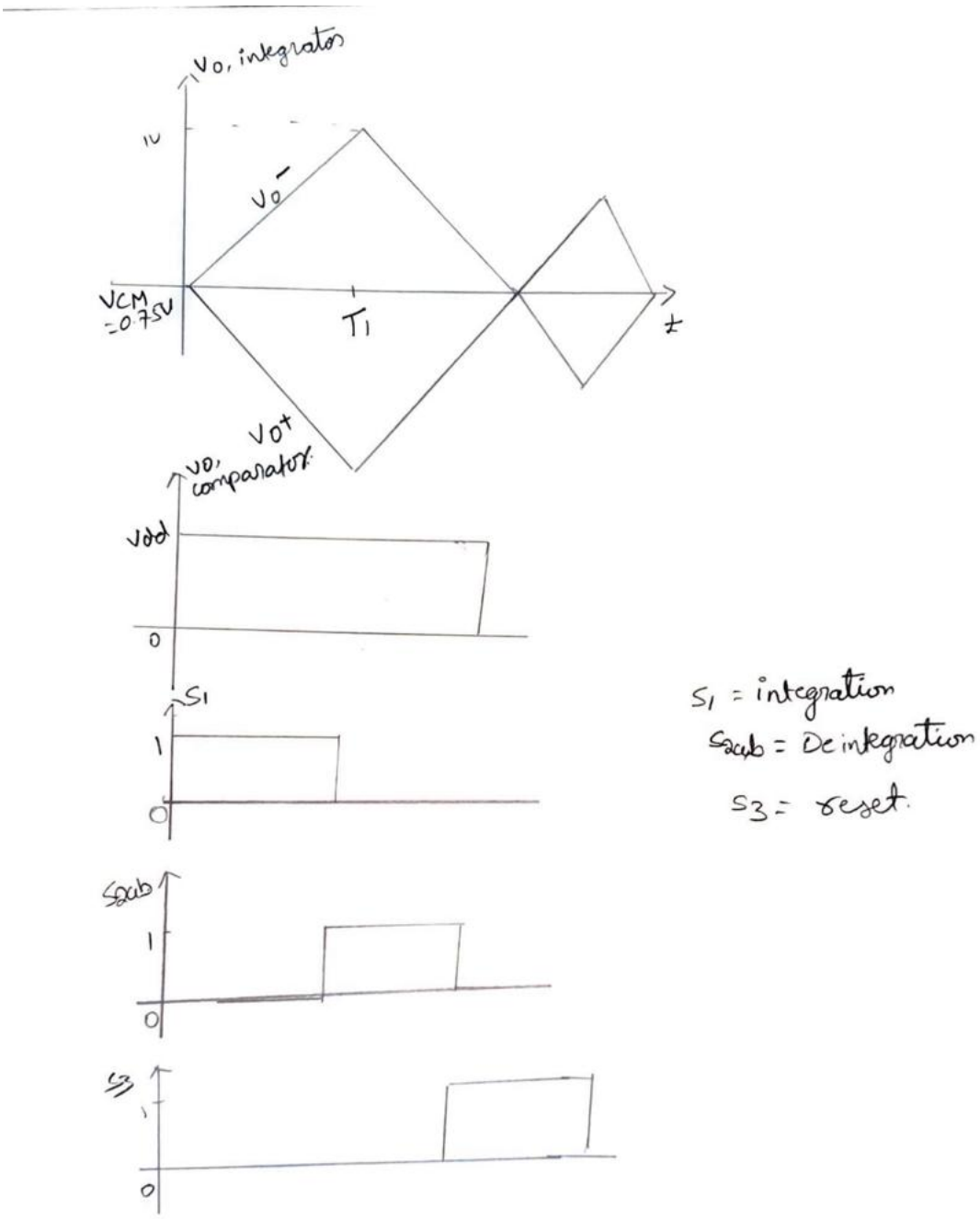

Figure 4: Integrator and comparator output for different switches

- Control Logic:- The value of $T2$ will be changed to D_{out} by the control logic. An AND gate with the inputs of the system clock clk and $V_{out,\text{comparator}}$ makes up the control logic. A counter of N bits will be enabled by the AND gate's output, providing a distinct digital output for each different vin voltage.The switch that connects V_{in} to the integrator will be controlled by the Most Significant Bit (MSB).

2.5 What are the most important characteristics of an amplifier/opamp for this ADC (the three most important ones)?

1. Gain(A)

$$A = \frac{V_{\text{out}}}{V_{\text{in}}}$$

- Open-Loop Gain:-

Must be high (value to be defined for this ADC); load, temperature, and output voltage levels may have an impact.

- Closed-loop Gain:

Configured by Opam; for this project, it will use the Integrator setup.

2. Bandwidth(BW):- The bandwidth of an op-amp refers to the range of frequencies over which the op-amp can operate without a significant attenuation of the input signal. In other words, it is the frequency range where the op-amp can effectively amplify signals. -The product of open-loop gain (A_{OL}) and bandwidth (BW) is a constant, indicating that as one increases, the other decreases to maintain the constant product.

3. Input Offset Voltage ((V_{os})): Input offset voltage is the voltage difference that must be applied between the inverting and non-inverting input terminals of an op-amp to nullify the output voltage. In other words, it represents the voltage that needs to be added or subtracted at the input to make the output voltage zero.

2.6 How is an differential integrator built with a differential opamp for this ADC?

A differential integrator using a differential op-amp for a dual-slope ADC is a circuit that measures the difference between two input voltages and integrates this difference over time. The calculation for it can be seen in below figure 5.

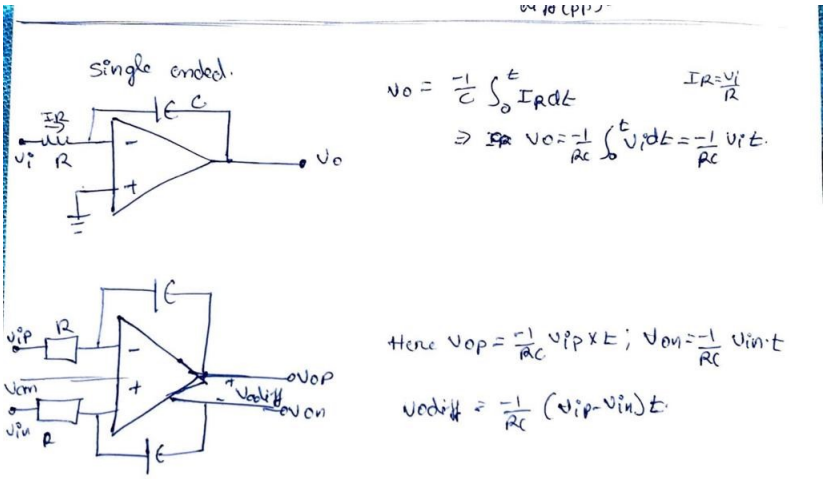

Figure 5: Vout of Integrator

2.7 How does a differential comparator work, important characteristics for this ADC (two most important ones)?

A differential comparator compares two voltages, IN^+ and IN^-, and generates a digital output based on the comparison:

- If $IN^+ > IN^-$, the output is High (1).
- If $IN^+ < IN^-$, the output is Low (0).

Important Characteristics for this ADC:

Low Propagation Delay (t_{delay}): In order to react rapidly to changes in the input voltages, the comparator should have a low propagation delay. The ADC's measurements are accurate and timely because of the brief delay:

t_{delay} = Time taken for the comparator to switch its output state after a change in input.

Input Offset V_{os}: Inappropriate voltage differential between the input terminals that are inverting and those that are not. This discrepancy may have an impact on the conversion's accuracy and lead to mistakes in the resultant value.

2.8 What must be done to keep a constant sampling rate for this type of ADC?

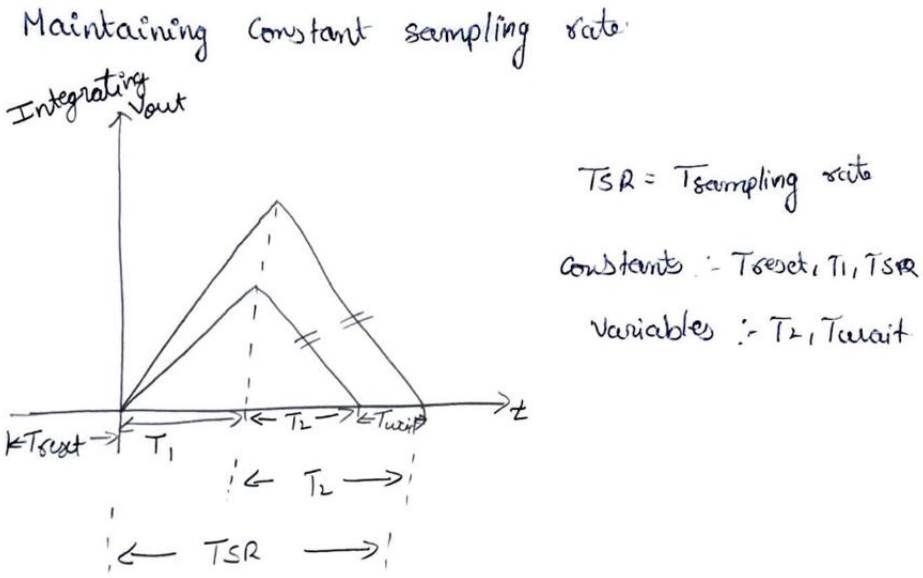

Figure 6: How to keep constant sampling rate

Observing from Figure 6 we can say that T1 and Treset are the same for both the signals. Here $T_{reset}, T1$ and $T3$ are constant but not T2. It must wait for a time T_{wait} before beginning the new conversion to maintain a constant sample rate. The time is typically reset first in the digital control logic. T1= 20.48us is the number that counts up to T1 during the integration phase. T2 changes based on the supplied input signal during

the de-integration phase. The control mechanism then resets itself again (or) waits for Twait before initiating the next conversion if the TSR is released.

$T_{\text{wait}} = T_{\text{SR}} - T_{total}$
$T_{\text{wait}} = T_{\text{SR}} - T_1 - T_2 - T_3$

We know that $T_{\text{sampling}} < 50us$

2.9 How is the conversion of the input voltage to a digital value done for this ADC?

2.10 How do you map the input via the integrator function/specification to the ADC resolution?

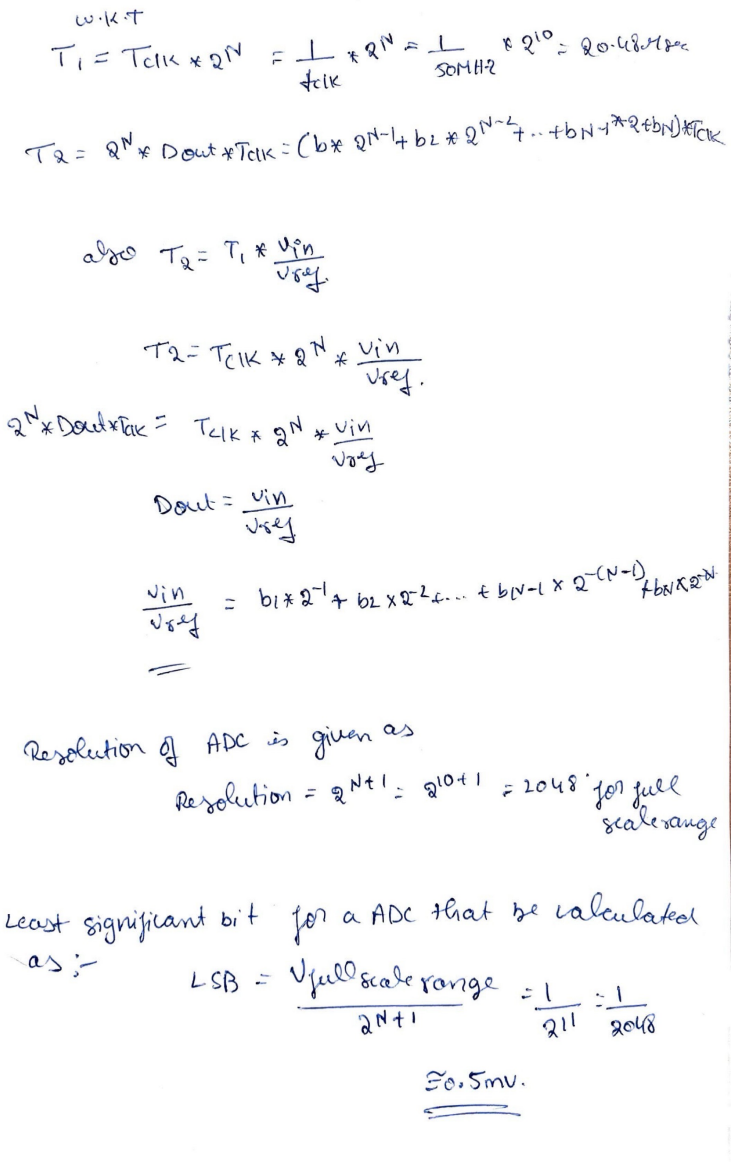

Figure 7: Conversion of input voltage to digital value

3 Modelling and Testbench Creation:

In the design of the Dual Slope ADC project, we have incorporated four primary building blocks: Switches, Opamp, Comparator, and Control Logic. The macro model implementation involves specifying key parameters such as gain, offset, and bandwidth, along with defining the block pinout. Verification of the functionality of each macro model has been carried out using a comprehensive test bench.

The integration of these distinct blocks forms the foundation for the creation of the top-level model. The operational validity of this top-level model has been confirmed through rigorous testing against an ADC-specific test bench.

3.1 Transfer Switche Model:-

The fundamental building block in this design is a switch, playing a crucial role in circuit control by supplying necessary voltage to other building blocks. The switch considered here has an open resistance of $1\,\mathrm{G}\Omega$ and a closed resistance of $1K\,\Omega$. It operates by opening for voltages at 0V and closing for voltages at 1.2V. Comprehensive testing of this switch has been carried out, and the circuit setup details can be found below.

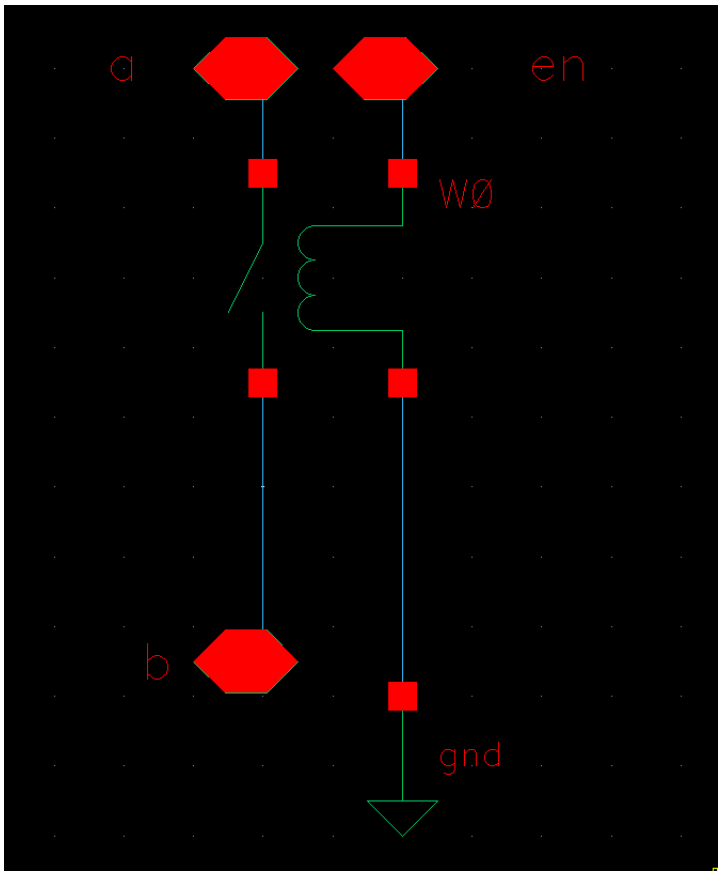

Figure 8: An Ideal Switch with Pin Configuration

In this configuration, three pins, all serving as input/output interfaces, are utilized. Positioned between pins "a" and "b" is an additional enable pin denoted as "en," responsible for activating the circuit.

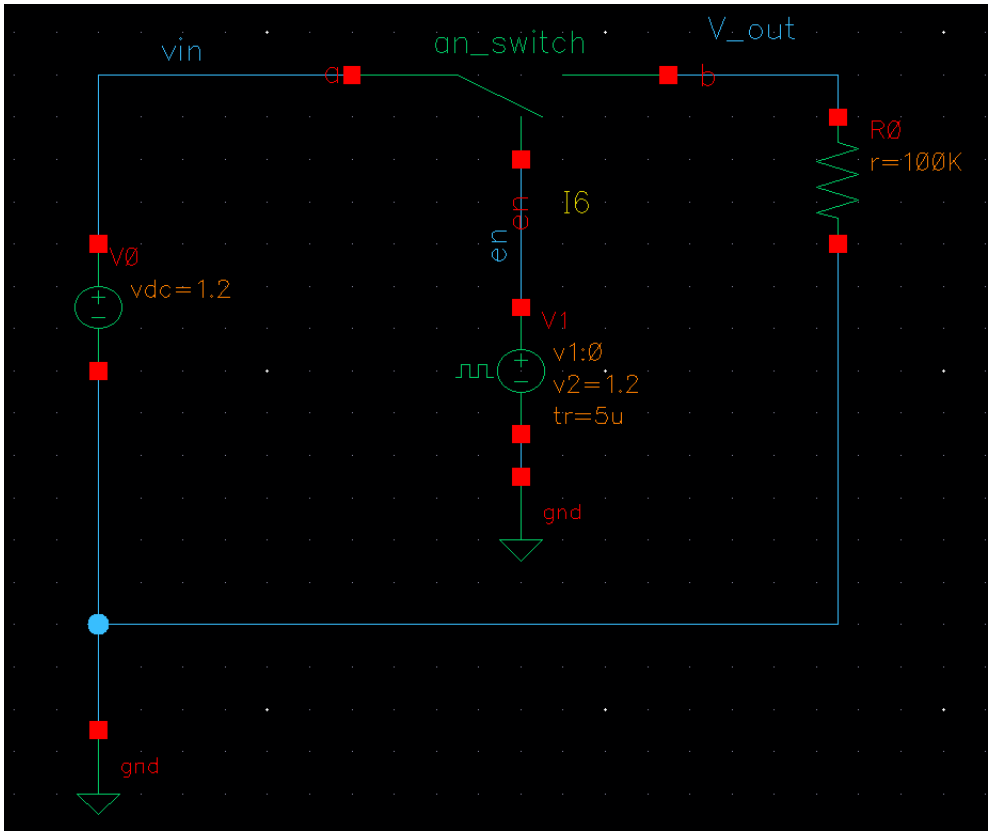

Figure 9: Test bench setup for Ideal Switch

In this test bench, a DC voltage of 1.2V is applied, and a pulse input is supplied to the enable pin. The resulting output voltage V_{out} is observed under a load resistance of 100kΩ.

- During transient analysis, with an input voltage of 1.2V and the switch enabled, the observed output voltage at V_{out} remains at 1.2V. Conversely, when the switch is in the off state under the same input voltage, a voltage of approximately $120\mu V$, nearly approaching zero, is observed. This operation signifies that the switch performs effectively for an input voltage of 1.2V.
- During the DC analysis, with the input voltage ranging from 0 to 1.2V while the switch is in the on state (DC voltage is 1), the output voltage V_{out} varies proportionally with the input voltage, reaching a maximum of 1.2V. Conversely, when the switch is in the off state (DC voltage is 0), the observed output at its maximum is 120 μV, affirming the switch's effective operation. The output waveform for both operations can be seen below.

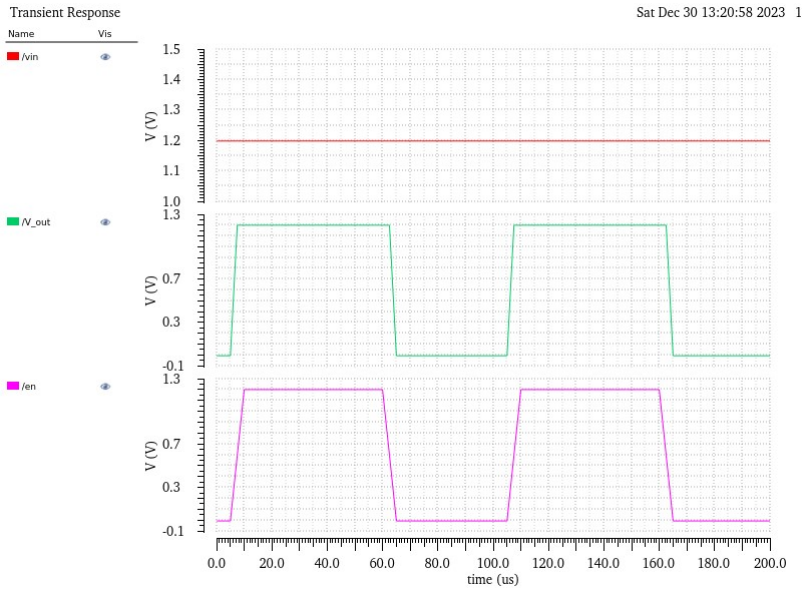

Figure 10: Switch Output in Transient analysis

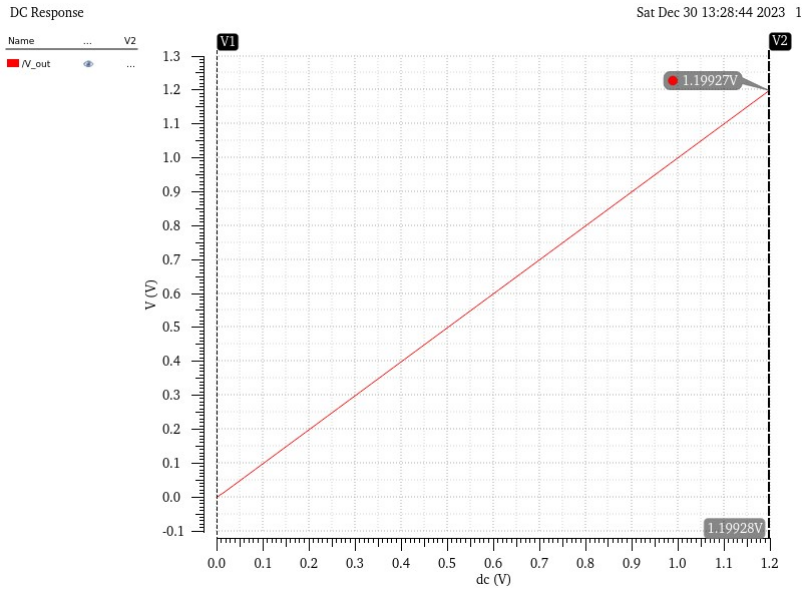

Figure 11: Switch Output in DC analysis

- In the corner simulation of switch resistance, an enable signal of 1.2 V was applied, indicating the switch is in the ON state. The observed resistance was 1kΩ, representing the closed resistance value. Conversely, when the enable signal was set to 0 V, signifying the switch is OFF, the resistance observed was 1GΩ, representing the open resistance. The simulation encompassed various corners with different voltages and temperatures. As anticipated, no discernible change in the minimum and maximum values occurred, affirming the ideal characteristics of the simulated elements.

-In the Monte Carlo simulation, the mean value obtained for the switch resistance is 1 GΩ when the enable signal is set to 0V, with a deviation of 0Ω. When the enable signal is high (1.2V), the switch resistance observed is 1 kΩ with a mean value of 1 kΩ.

The expression used to find this value is :-

$((\text{VDC}(\text{"/V}_i n\text{"}) - VDC(\text{"/}V_o ut\text{"}))/IDC(\text{"/}R0/PLUS\text{"}))$

3.2 Opamp Model:-

-The differential operational amplifier, functioning as a differential integrator, is pivotal in the integration phase of a dual-slope integrating ADC, converting analog signals into digital values. It integrates the input voltage over a specific duration, quantifying the charge on the capacitor, essential for subsequent conversion. Its functions include processing the input signal, integrating it by accumulating charge, managing the conversion process, and controlling switches during de-integration. The precise analog-to-digital conversion relies on the accurate operation of the differential integrator, regulated by the ADC's timing, switches, and reference voltages.

-In our model, the Op-Amp serves as a fully differential integrator responsible for both the integration and measurement phases. The previously calculated RC time constant is found to be 20.48 μs. The initial specifications include a given gain of 10,000, an offset of 0V, and a specified bandwidth of 10MHz.

-Initially, to set up the model, an amplitude of $\frac{1m}{2}$ and a frequency of 100kHz were considered. Through calculations, the resulting output voltage gain for this specification is determined to be 5V.

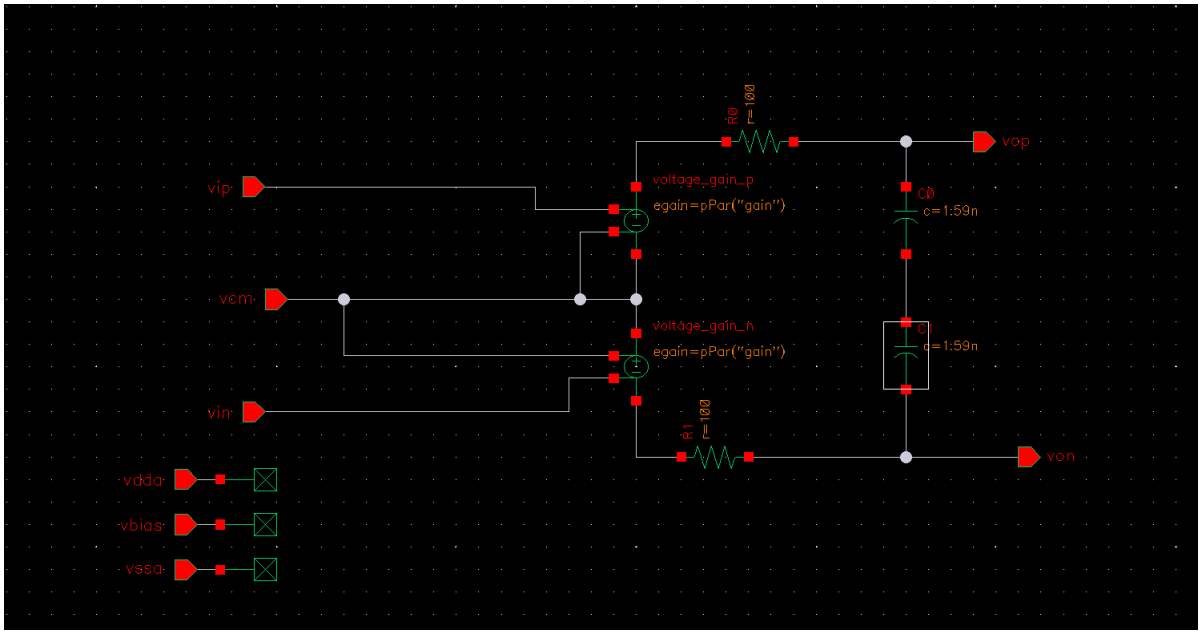

Figure 12: Schematic setup for Ideal Opamp Model

- In the circuit's ideal configuration, two Voltage-Controlled Voltage Source Piecewise (VCVSP) elements have been employed. The gain of the circuit is defined through the use of the CDF parameter. The circuit utilizes a total of 8 pins, where vip, vin, and vcm serve as input pins, while vop and von act as output pins. Additionally, the circuit incorporates the vdda pin set to 1.2V, the vassa pin set to 0V, and an external voltage is applied to the biasing pin Vbias for proper operation.
Vin p: Input pin for the Voltage-Controlled Voltage Source (VCVS).

Vin n: Input pin for the Voltage-Controlled Voltage Source (VCVS).
Vcm: Input pin providing the common-mode voltage to the circuit.
Vop p: Output pin of the operational amplifier.
Vop n: Output pin of the operational amplifier.
Vbias: Input pin responsible for setting up the DC operating point of the differential op-amp.
Vdda: Pin for supplying power voltage.
Vssa: Pin for grounding reference.

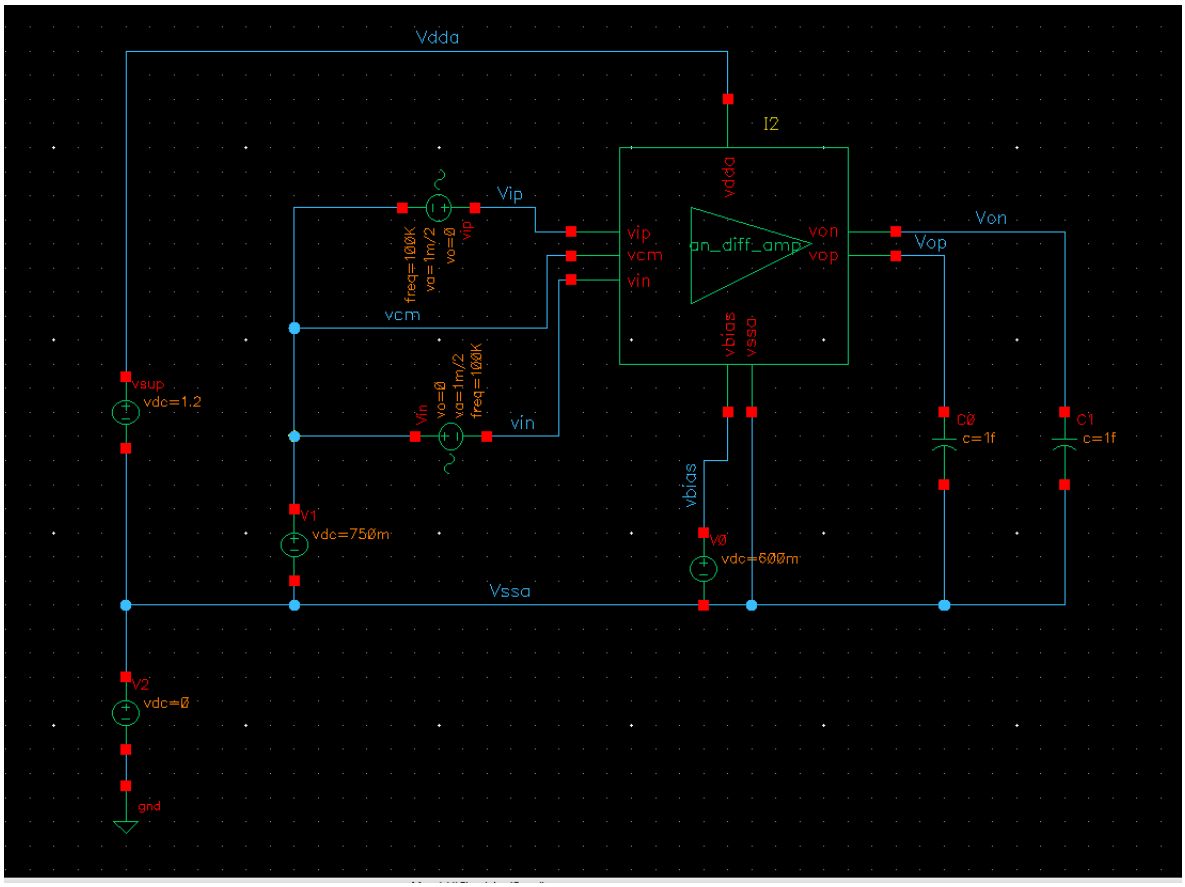

Figure 13: Test bench setup for Ideal Opamp Model

-In the test bench, a sinusoidal wave is applied to the input pins, with a common-mode voltage set at 750mV. The output pins are connected to a capacitor with a capacitance of 1fF, and the resulting output waveform can be observed in this configuration.

Transient analysis of the Differential Opamp.:-

-In the transient analysis waveform, it is evident that the output waveform has been amplified by a voltage of 5V, a value that aligns with the results obtained through manual calculations. Notably, there is no observable offset voltage in the output waveform, indicating precise synchronization in timing between the input and output voltages.In the positive cycles, output measured is (5v+0.75v) =5.75v and in the negative cycle (-5v+0.75v) = -4.25v.

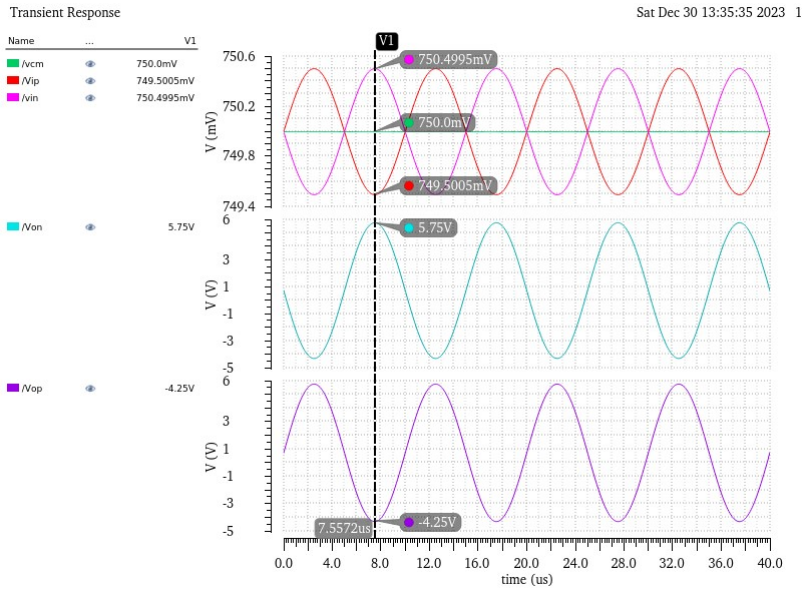

Figure 14: Output waveform of the Opamp in transient analysis

-The amplitude value must be adjusted to attain a maximum output voltage of 1.2V while maintaining the same gain. Through manual calculations, it is determined that for an output voltage of 1.2V and a gain of 10000, the corresponding amplitude should be reduced to 0.12mv. Alternatively, the same outcome can be achieved by decreasing the gain while maintaining the initially considered input amplitude.

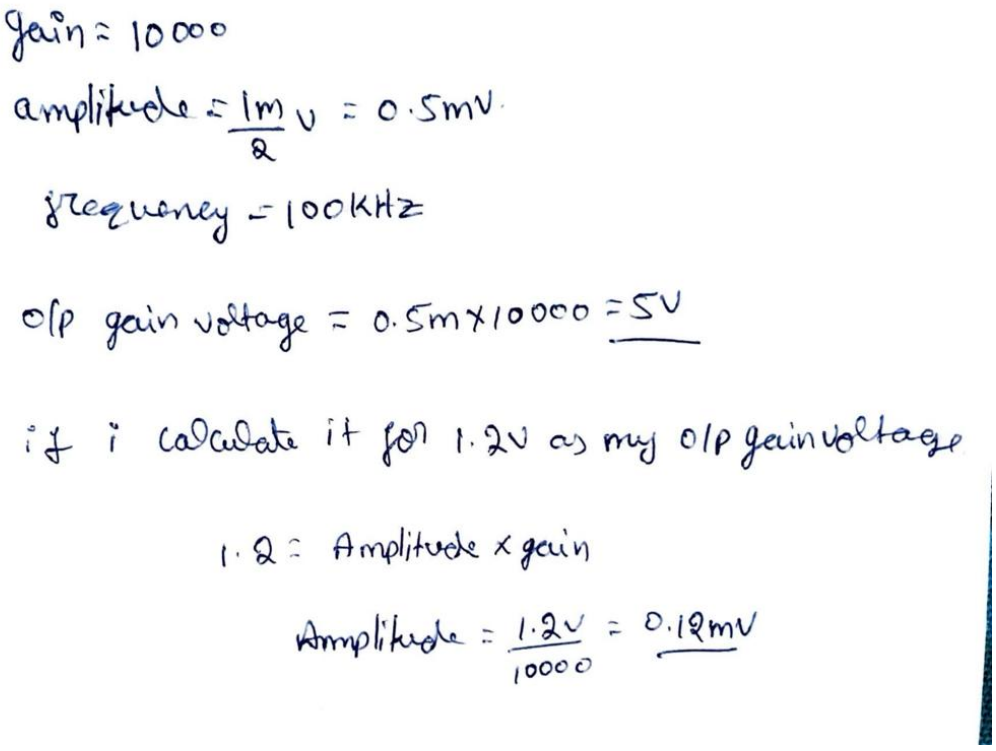

Figure 15: Amplitude and o/p voltage gain hand calculation

DC analysis of the Differential Opamp:-

-In the DC simulation, a voltage range of 0.1mV to -0.1mV has been applied. In the ideal schematic, specific maximum and minimum voltages are assigned for the input pins. The maximum voltage for V_{ip} is calculated as $V_{\text{dd}} - V_{\text{cm}} = 450\,\text{mV}$, and the minimum voltage is $V_{\text{ss}} - V_{\text{cm}} = -750\,\text{mV}$. Similarly, for V_{in}, the maximum voltage is $V_{\text{ss}} - V_{\text{cm}} = 750\,\text{mV}$, and the minimum voltage is $V_{\text{dd}} - V_{\text{cm}} = -450\,\text{mV}$.

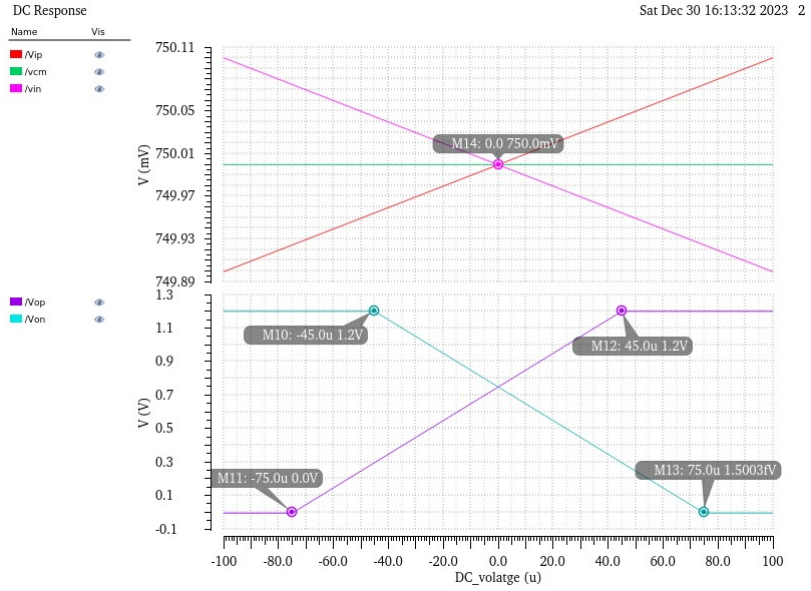

Figure 16: Opamp DC analysis

- The output waveform exhibits saturation whenever the output voltage surpasses the maximum or minimum specified values. This behavior is noticeable as the output becomes saturated when exceeding the defined maximum voltage, and similarly, saturation occurs when the output falls below the minimum specified voltage. This characteristic is consistently observed in the output waveform during the DC analysis.

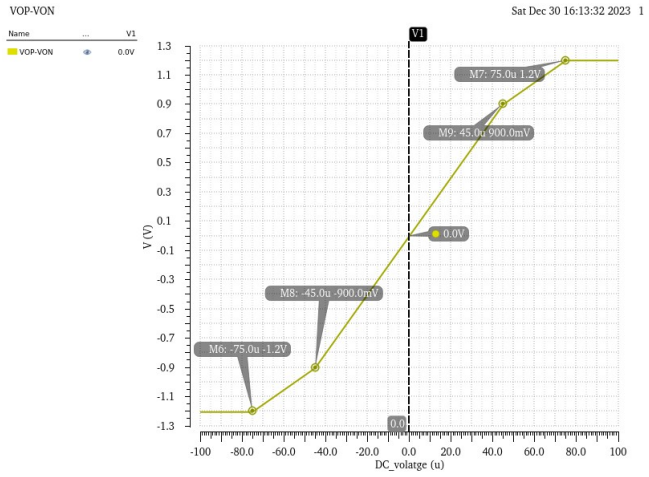

Figure 17: Opamp DC analysis for Voltage difference

- In the analysis of the difference between the output waveforms, specifically $V_{\text{op}} - V_{\text{on}}$, the behavior of the output swing range becomes evident. By sweeping different DC ranges, it is observed that the waveform tends to become more saturated. Notably, there is no observable offset, as indicated by the output being zero at time 0.

• **Offset in an opamp.** -Introducing an offset of 0.150 mV to the model, which is smaller than the amplitude, involves externally applying it to the ideal model while maintaining constant values for all other parameters. Subsequently, a DC simulation spanning from -0.4 mV to 0.4 mV is conducted to observe the resulting output.

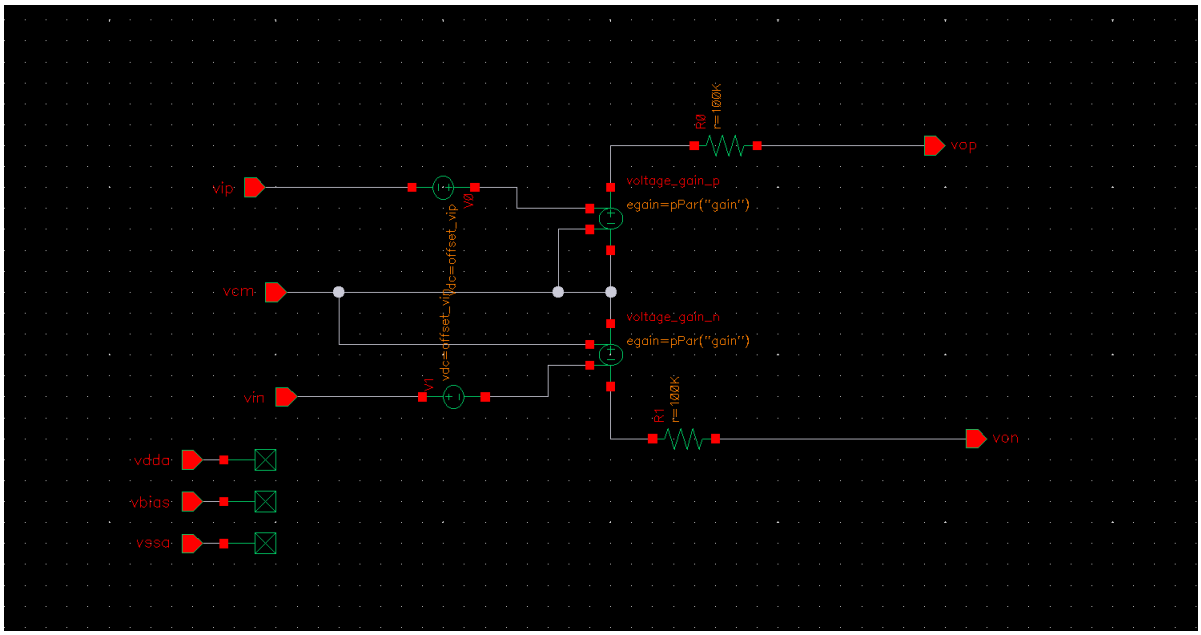

Figure 18: Schematic for Opamp DC offset analysis

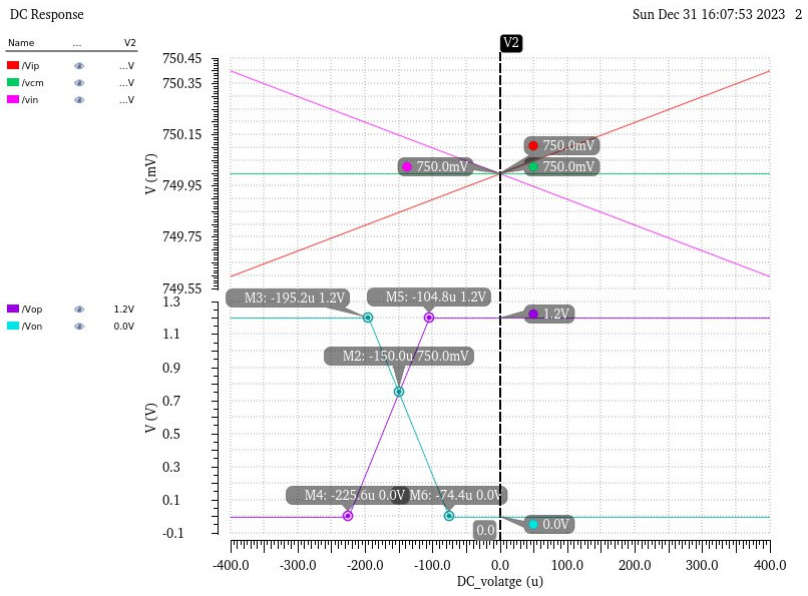

Figure 19: Opamp DC offset analysis

- In the observation, it is evident that upon introducing the offset, the output signal V_{on}

saturates at -195μV and subsequently returns to 0 at -75μV. This behavior signifies that the introduced offset voltage is contributing to both the maximum and minimum input voltages. Similarly, V_{op} exhibits a variation between -225μV and -105μV.

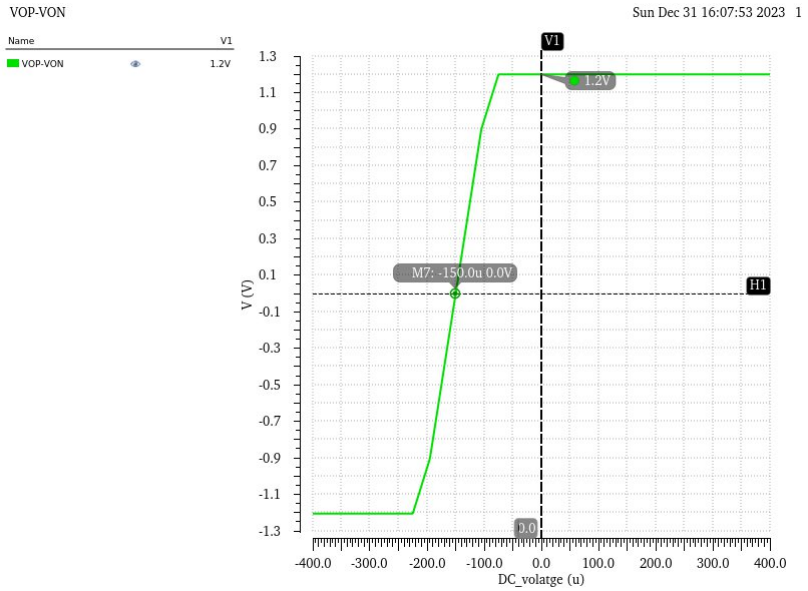

Figure 20: Opamp DC offset analysis for Voltage difference

-In the output voltage difference graph, a distinct change is observed upon introducing the offset value. Instead of remaining at 0V, it saturates to 1.2V. Examining the x-axis curve, it is evident that at 0, the voltage is -150μV, indicating the presence of the offset. Notably, the offset was independently applied to both inputs, each with a magnitude of 75μV.

AC analysis of the Differential Opamp.:-

- To determine the cutoff frequency the ac simulation has been performed by plotting the difference of Vop - Von in db. The resistor value was set to $100\,\Omega$ for simplicity. The desired bandwidth is specified as 1 MHz, and using the formula

$$BW = \frac{1}{2\pi RC}$$

with $R = 100$ ohm and $BW = 1$ MHz, the resulting capacitance (C) is approximately 1.59×10^{-9} farads, equivalent to 1.59 nanofarads (nF).

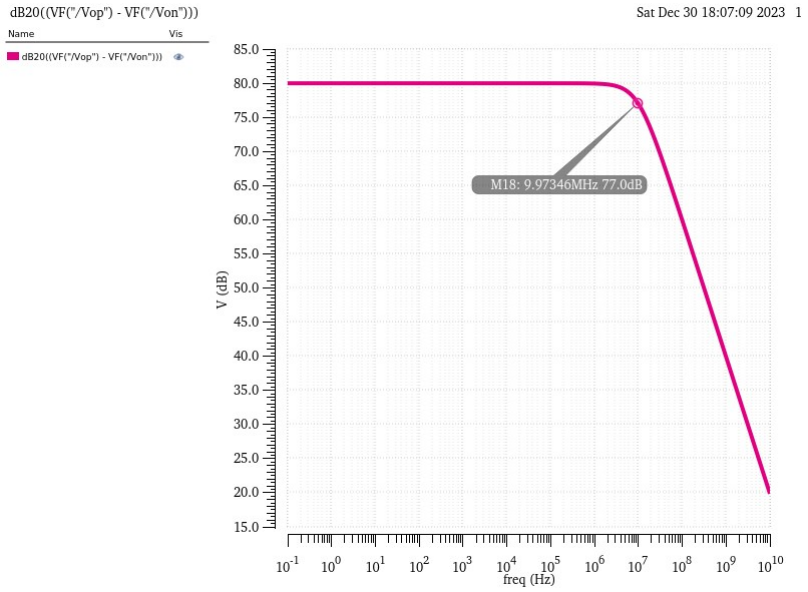

Figure 21: Cutoff frequency calculation for opamp

The cutoff frequency obtained by simulation is 9.973MHz.

Corner and Monte Carlo Simulations:-

-During the corner simulation encompassing Bandwidth, Offset, and Gain of the opamp across various corners at different temperatures (−30°C, 27°C, 80°C) and voltages (1.02V, 1.2V, 1.32V), as anticipated, no discernible alterations in the minimum and maximum values were observed. This consistent behavior aligns with the characteristics of an ideal element, indicating an absence of temperature and voltage effects.

-The expressions used to perform the corner and Monte Carlo simulations are:
Output Gain in dB = value(dB20((VF("/Vop") - VF("/Von"))) ymax(dB20((VF("/Vop") - VF("/Von")))) ?period nil ?xName "time")

Output Offset = cross((v("/Vop" ?result "dc") - v("/Von" ?result "dc")) (ymax((v("/Vop" ?result "dc") - v("/Von" ?result "dc"))) - 1.2) 1 "either" nil nil nil)

$\text{Cutoff}_{frequency} = cross(dB20((VF("/Vop") - VF("/Von")))(ymax(dB20((VF("/Vop") - VF("/Von")))) - 3)1"either"nilnilnil)$

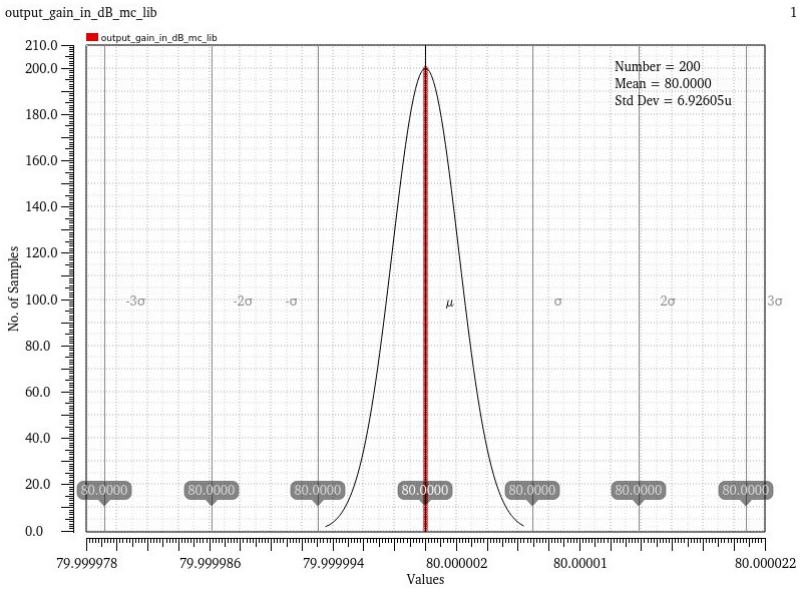

Figure 22: Histogram representation Output Gain

-Monte Carlo simulation was done for nominal voltage and the Histogram representation of it can be seen. The mean and standard deviation of it can be seen on the output waveform.

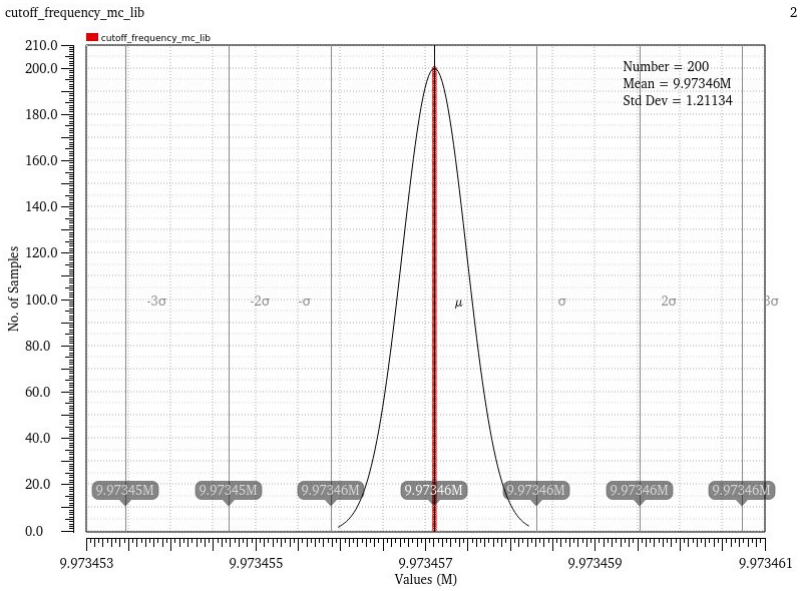

Figure 23: Histogram representation Cutoff frequency

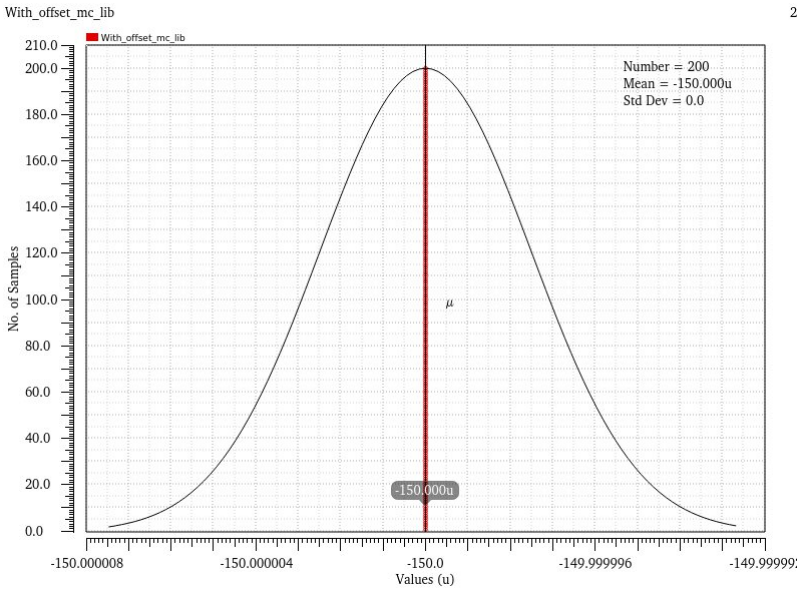

Figure 24: Histogram representation Offset

-Monte Carlo simulation by introducing offset, here the offset is 150uV which can be seen in the simulation.

3.3 Comparator Model:-

In a dual-slope ADC, the comparator plays a key role in detecting when the output voltage of the integrator reaches a predefined reference level, marking the end of the integration phase. It's essential to note that the comparator may need to handle signals near the zero-volt reference level. Hence, it's crucial for a differential comparator to effectively compare small voltage differences with reliability.

-In the comparator model, a Voltage-Controlled Voltage Source Piecewise (VCVSP) is utilized, and its output is fed into a digital block, generating a digital waveform. In this configuration, the input is linearly varied, and the Piecewise Linear (PWL) input voltage starts from -0.01 mV and increases to 0.01 mV. Initially, there is no offset in the system.

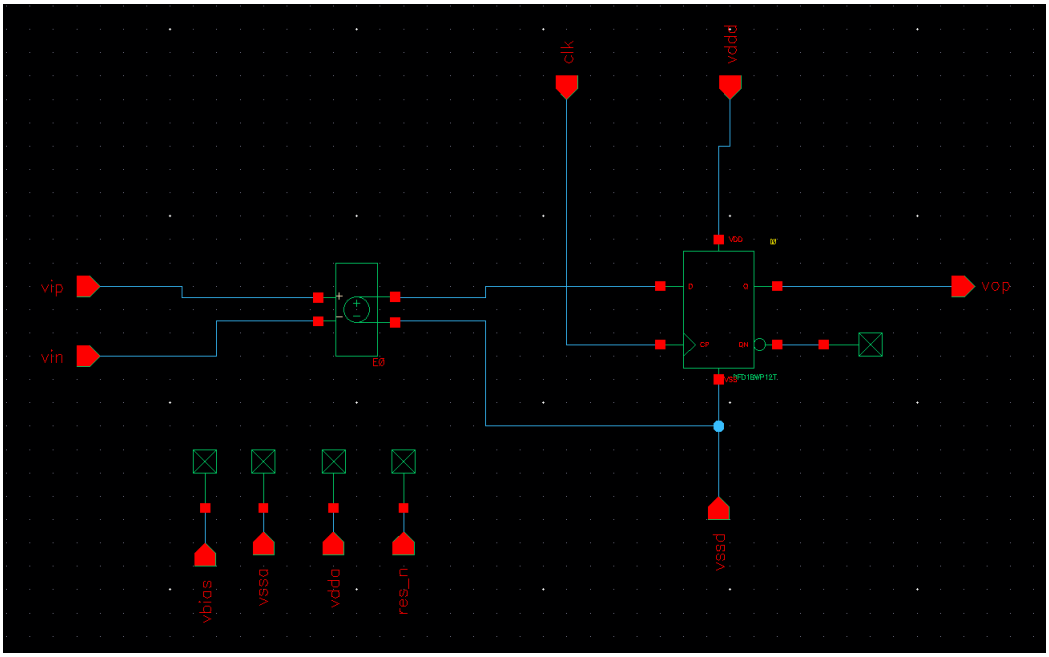

Figure 25: Schematic setup of ideal Comparator

-In this setup, a total of 10 pins are employed, including input pins such as Vin and Vip, and the output is observed at the pin Vop. The digital waveform, along with a clock signal (provided to the digital block via the clk pin), is generated. Additionally, there is a res_n pin that resets all initial conditions.

-

- **Vin p:** Input pin for the Voltage-Controlled Voltage Source Plus (VCVSP).
- **Vin n:** Input pin for the Voltage-Controlled Voltage Source Plus (VCVSP).
- **Clk:** Input pin for the clock signal supplied to the digital unit.
- **Vop p:** Output pin of the digital unit.
- **Vdda:** Power supply reference pin.
- **Vssa:** Ground reference pin.
- **Vbias:** Power pin responsible for establishing the DC operating point of the comparator.
- **resn:** Control pin for resetting the comparator's output to its initial conditions.

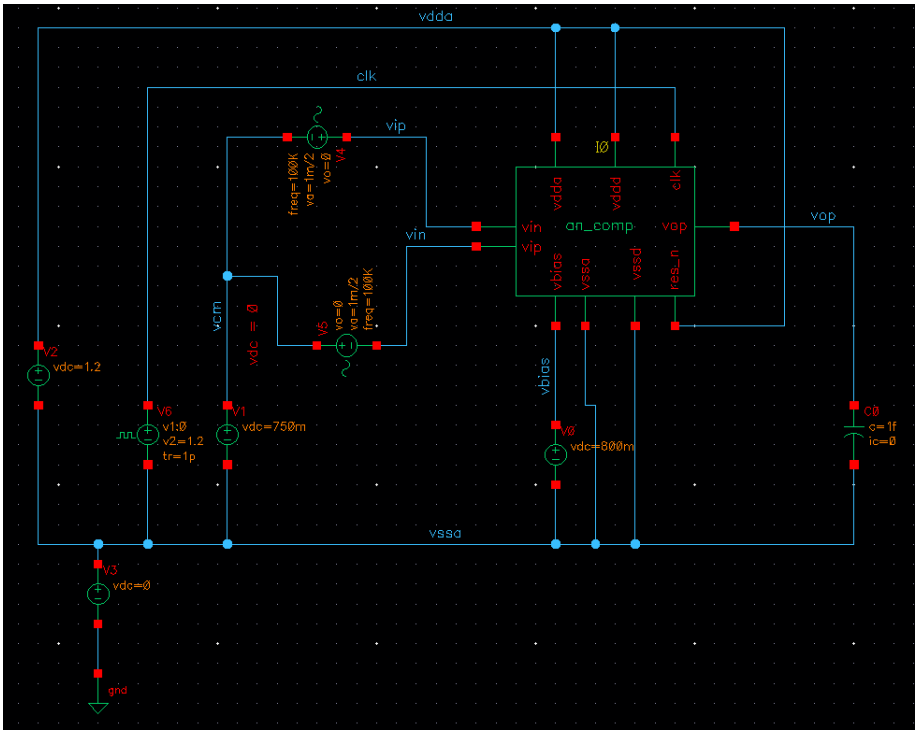

Figure 26: Test bench setup of ideal Comparator

-In the comparator test bench, two sinusoidal waves are applied as input voltages with an amplitude of 1 mV and a frequency of 100 kHz. The resulting digital output waveform is observed at V_{op}, which is connected to a capacitor with a capacitance of 1 fF.

-Additionally, a clock signal with an input pulse voltage featuring rise and fall times of 1 ps, a period of 100 ns, and a pulse width of 50 ns is utilized in the test bench. This clock signal is likely employed to synchronize and trigger the comparator's operation.

Transient analysis of the comparator:-

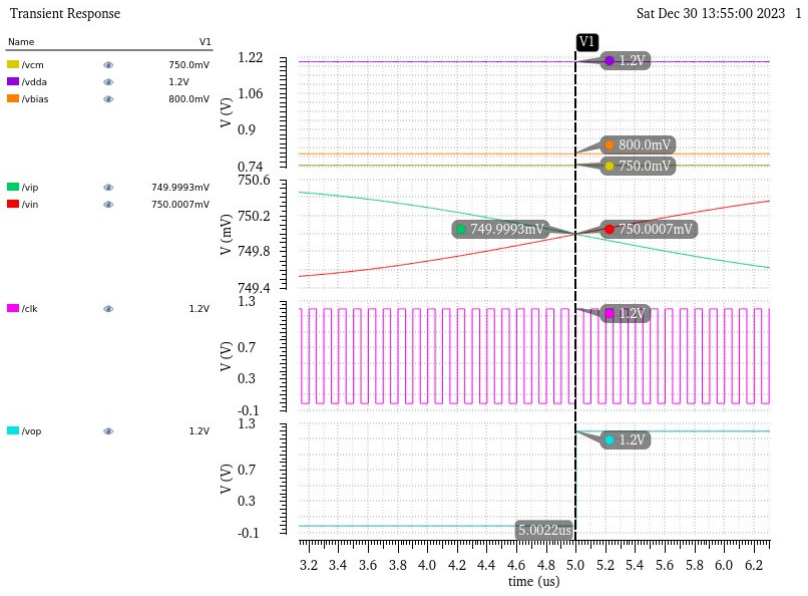

Figure 27: Transient analysis for ideal Comparator

-In the output waveform, it is noticeable that at a time of 5μs, the output achieves a voltage of 1.2V, synchronizing with the input waveform at 750mV. Since no offset has been introduced, there is no delay in the output voltage.

DC analysis of the comparator:-

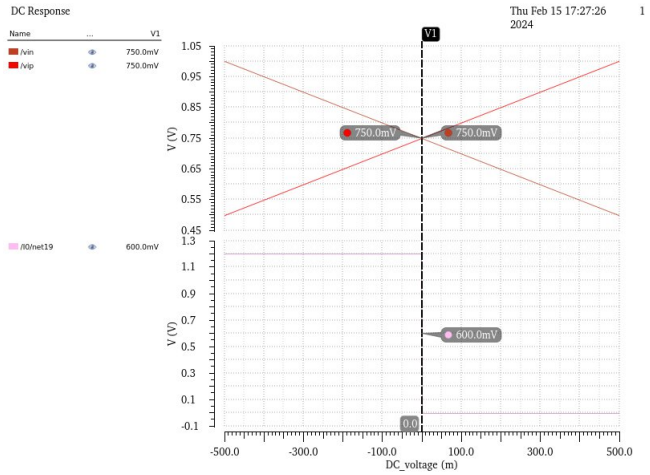

Figure 28: DC analysis for ideal Comparator

-In the DC simulation, a voltage range of ±0.5mV is applied. The output is evaluated at the ideal VCVSP's output before being directed to the flip-flop. The simulation reveals that the output changes states solely based on differences in the input, without exhibiting any noticeable offset. This underscores the comparator's ability to promptly react to input fluctuations, demonstrating its efficacy in precisely comparing voltage levels.

Comparator Offset:-

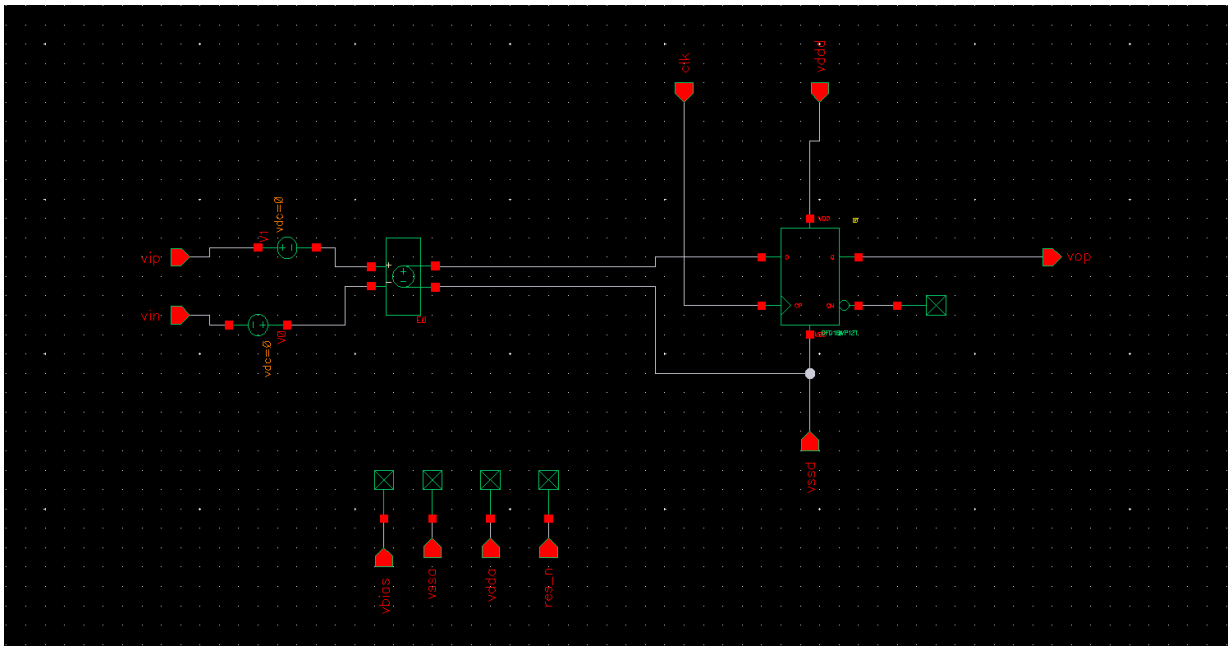

Figure 29: Schematic configuration for introducing DC offset in an ideal comparator.

-To introduce an offset to the comparator, two separate voltage sources are utilized for Vin and Vip. Consequently, the offset introduced to the positive and negative terminals is aggregated, resulting in the overall offset value applied to the comparator.

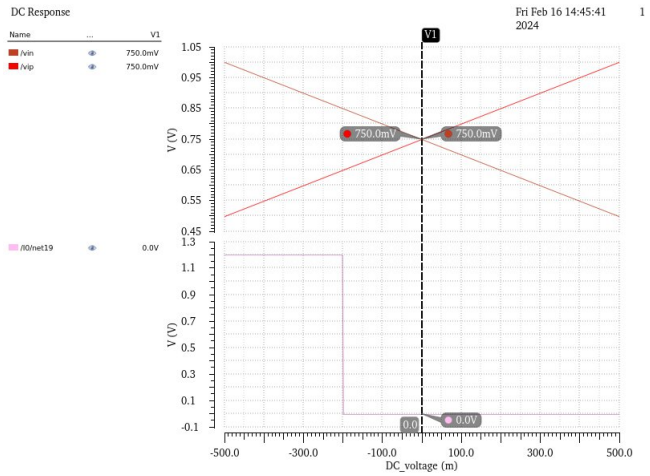

Figure 30: Result of DC offset in an ideal comparator.

-Following the introduction of an offset to the comparator, it becomes evident that the comparator transitions states approximately 200mV earlier than expected due to the offset. This occurrence stems from the application of a 100mV offset to both positive and negative terminals of the input. In cases of a positive offset, a negative output offset occurs, attributed to the input pins of the comparator being interconnected in a mirrored configuration on the test bench.

Corner and Monte Carlo Simulations:-

-During the corner simulation encompassing the offset of the comparator across various corners at different temperatures ($-30°C$, $27°C$, $80°C$) and voltages (1.02V, 1.2V, 1.32V), as anticipated, no discernible alterations in the minimum and maximum values were observed. This consistent behavior aligns with the characteristics of an ideal element, indicating an absence of temperature and voltage effects.

-The expressions used to perform the corner and Monte Carlo simulation is below:-

$$cross(v("/I0/net19"?result"dc")(ymax(v("/I0/net19"?result"dc"))-0.6)1"either"nilnilnil)$$

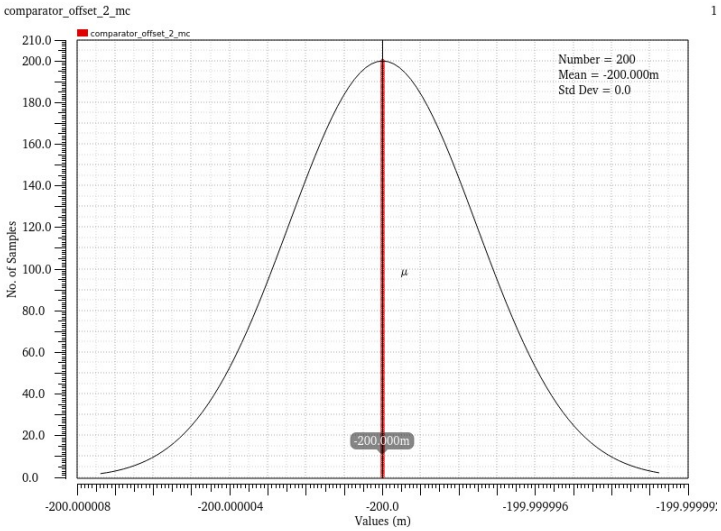

Figure 31: Histogram representation Offset in ideal comparator.

3.4 Top level ADC model :-

-At the top level, the model integrates all previously mentioned components alongside a digital control unit. This comprehensive structure encompasses multiple input and output pins. Initially, the differential integrator is established using a differential op-amp, a resistor, and a capacitor in a negative feedback arrangement, alongside input switches such as V_{ip}, V_{in}, V_{cm}, V_{rn}, and V_{rp}.

-The outputs of the differential integrator, V_{op} and V_{on}, feed into the inputs of the differential comparator, V_{ip} and V_{in}. Equipped with a clock input and a reset function, the comparator ensures the initialization of its output to predefined conditions, guaranteeing error-free operation.

-The comparator's output, V_{op}, along with the clock and reset signals, is directed to the digital control unit, typically consisting of a binary counter. Upon activation, the counter initiates pulse counting. Once the comparator detects that the voltage across the integrating capacitor matches the reference voltage, the counter halts operation. At this juncture, the count value obtained from the counter digitally represents the analog input voltage, thereby completing the conversion process.

-To set up this block diagram, it is necessary to specify the values of R and C at the integrator. Given an RC time constant of 20.48μs and assuming a capacitor value of 10pF, the calculated resistance value is 2.048 MΩ.

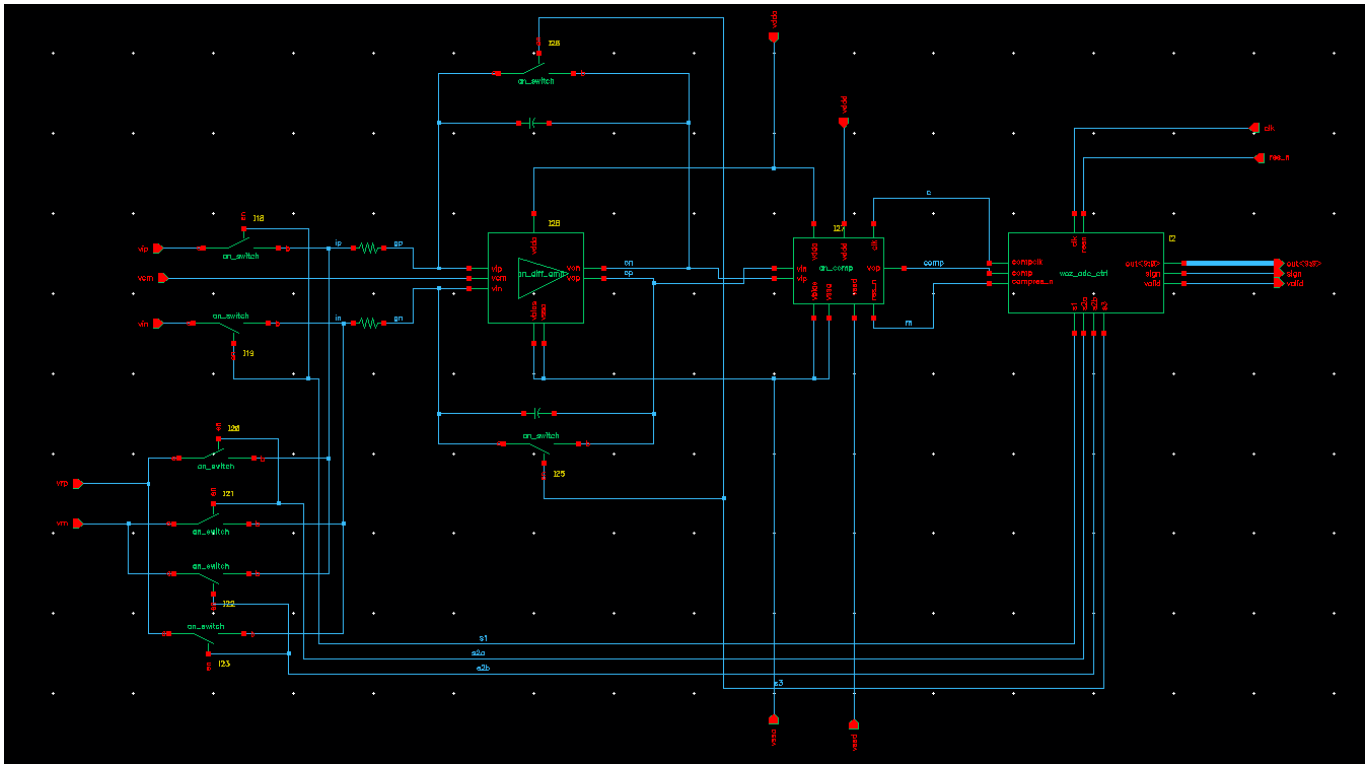

Figure 32: Schematic of Top Model Ideal ADC

The testbench of the top-level ADC has been setup and shown as below.

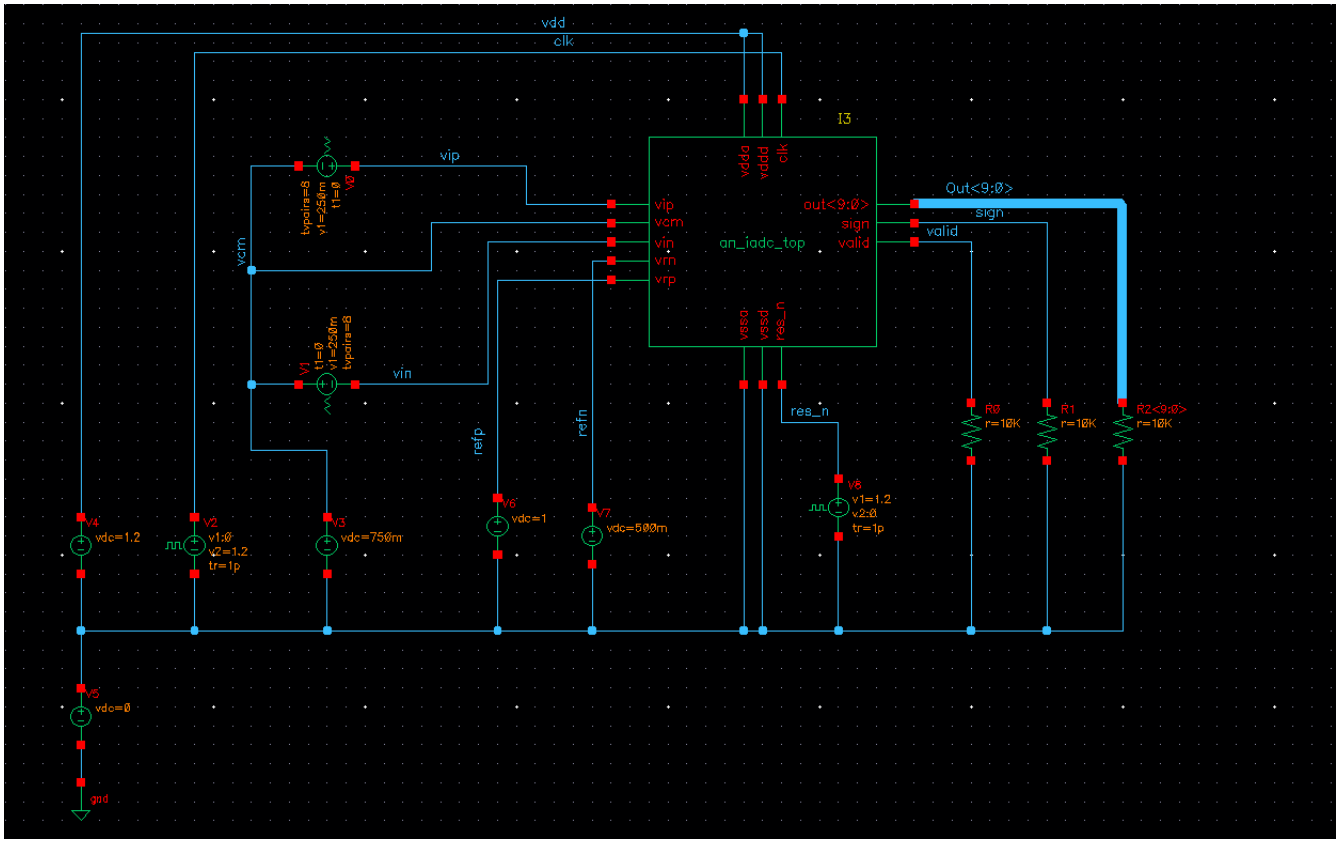

Figure 33: Test bench setup for top model ADC

- In the test bench for the top model, a piece-wise linear voltage source (vpwl) is employed as the input cell. This source facilitates the specification of a voltage source using a piece-wise linear curve, where voltages are entered as discrete values for different time instants. In this scenario, the time difference provided for the input is 40μs, encompassing both positive and negative voltages.

- In the test bench, the clock pulse voltage is set at 1.2 V, with a period of 20 ns and a pulse width of 10 ns, featuring rise and fall times of 1 ps. Meanwhile, for the reset pin pulse input, V_1 is specified as 1.2 V, V_2 as 0 V, with a period lasting 1 s and a pulse width of 1 μs, along with rise and fall times of 1 ps.

In the top-level ADC block diagram, a table detailing the block pinouts is provided. This table includes information about the pins, their direction type, and their functions within the system.

Table 1: Block Pinouts of the top-level ADC.

Pin	**Direction Type**	**Function of the Pin**
V_{in_p}	Input	Input to the Opamp.
V_{in_n}	Input	Input to the Opamp.
V_{cm}	Input	Vcm of the Opamp.
V_{rp}	Input	Reference input voltage to the Opamp.
V_{rn}	Input	Reference input voltage to the Opamp.
V_{rn}	Input	Reference input voltage to the Opamp.
V_{out_p}	Output	Output of the Opamp.
V_{out_n}	Output	Output of the Opamp.
V_{op}	Output	Output of differential comparator.
Clk	Input	Clock input provided to the digital unit
res_n	Control	Resets the comparator's output to initial conditions.
V_{dda}	Power	Supply reference pin.
V_{ssa}	Power	Ground reference pin.
V_{bias}	Power	Sets up DC operating point of the comparator.
$comp_{clk}$	Input	Input of the digital control unit from the clock of the comparator.
$comp_{res\_n}$	Control	Reset of the digital control unit from the comparator's reset.
$S1$	Input	Switch to turn on during the integration.
$S2a$	Input	Switch to turn on during the de-integration when V_r is positive.
$S2b$	Input	Switch to turn on during the de-integration when V_r is negative.
$S3$	Input	Reset.
$Sign$	Input	Indicates whether the output is positive or negative.
$out < 9:0 >$	Output	Gives the digital 10-bit output data bus.

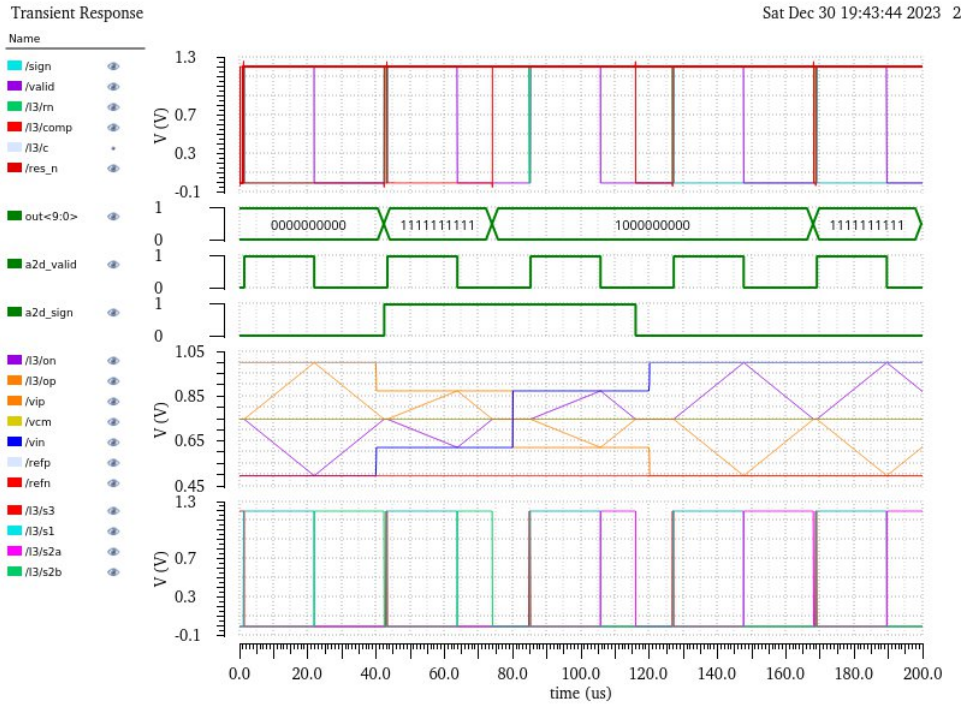

Figure 34: Transient top model ADC

-In the transient analysis waveform mentioned above, the signal *a2d_valid* remains high during the charging phase and low during the discharge phase of the integrator output. On the other hand, the signal *a2d_sign* is set high only when the integrator output falls within half of the full-scale range ($\pm FSR/2$); otherwise, it remains low for the entire full-scale range.

-The digital bus `out<9:0>` depicts analog signals as digital values. Initially, the data bus is initialized to zero, after which it begins counting for the first full-scale range (FSR), covering both integration and de-integration phases. Subsequently, the process transitions to the half-scale range of ±FSR/2 as the phase shifts, and finally to the range of ±FSR. During this transition, the first half bits are replaced by the second half bits.

-The provided data illustrates a dual-phase process unfolding: During Phase 01, the analog input undergoes integration on both positive and negative sides with a known voltage.

-Phase 02 consists of de-integration using a reference voltage of opposite polarity to the input, ensuring a consistent de-integration slope. The time taken from initiation to the crossover point is directly proportional to the applied input voltage. This timing is monitored by a 50MHz clock, initiating counting from the integration start to the crossover.

-Upon detecting the transition from integration to de-integration, the digital block initiates counting until the comparator signals the crossover. The comparator ensures precise polarity switching, resulting in numerical output.

-Integration lasts 20.48 microseconds, with the counter spanning 10 bits, representing the full-scale range (FSR) of the ADC from 0 to 1024. Following this, the transition from Phase 1 to Phase 2 prompts a counter reset, continuing until the crossover.

-Counter progress directly reflects the applied input voltage, with the FSR maintaining constant integration and de-integration slopes. Analysis reveals the FSR crossover occurring at 20.48 microseconds(ideally), while half-scale input crossing occurs at 10.24 microseconds(ideally).

-In brief, this process involves integrating and de-integrating analog input with known voltages, monitored by a clock. The digital block counts until the comparator signals crossover, with integration lasting 20.48 microseconds and the counter spanning 10 bits. Counter progress correlates with the applied input voltage, with FSR maintaining constant slopes.

Behavior of the ADC Top Model with Ideal Op-Amp Gain, Offset, and Comparator Offset:-

-Op-Amp Gain:-

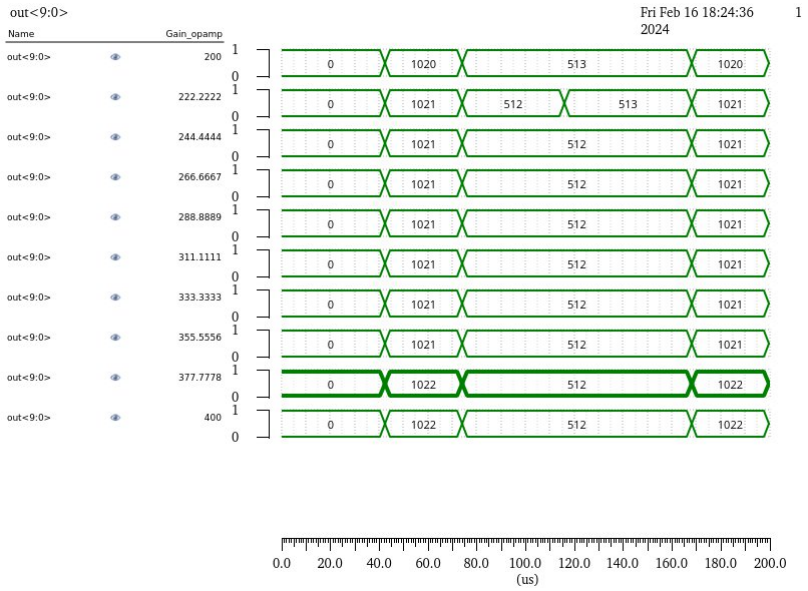

Figure 35: Op-Amp Gain variation in the Top Model ADC

-By adjusting the op-amp gain, it's noticeable that up to a gain of 1300, the digital data bus output exhibits no errors ideally, with values of 1023 and 512 for ±FSR and ±FSR/2, respectively. However, from a gain of 1300 down to 380, there is a single LSB error in the output data. Given that a single LSB error is negligible in an ideal ADC output, the ADC model is configured with a gain of 380.

-Op-Amp Offset:- -Adjusting the Opamp offset within the range of $-0.1\,\text{mV}$ to $+0.09\,\text{mV}$ introduces an error of up to 1 LSB in the output data bus. Beyond this range, the error increases to around ±20. However, below this threshold, there is no observable error in the output data bus.

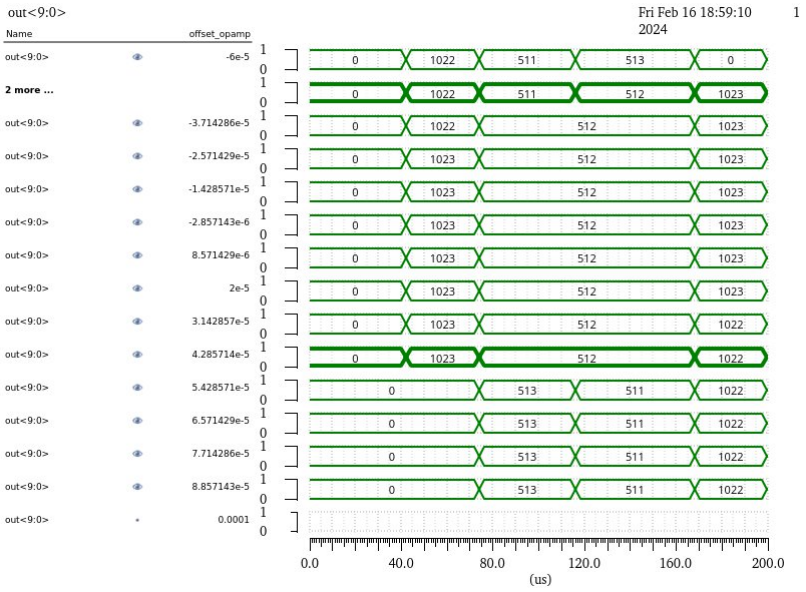

Figure 36: Op-Amp Offset variation in the Top Model ADC

Comparator Offset:-

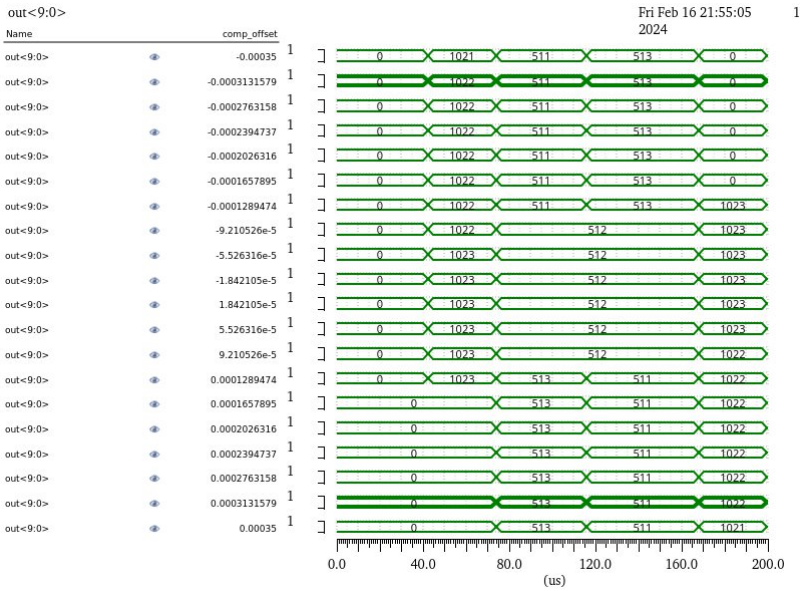

Figure 37: Comparator Offset variation in the Top Model ADC

-When adjusting the comparator offset within the range of $\pm 0.64\,\text{mV}$, an error of up to 1 LSB is observed in the output digital bus. If the offset exceeds this range, the error increases to 2 LSB. Thus, it can be inferred that the offset error tolerance for the output is within $\pm 0.64\,\text{mV}$.

4 Initial Design/Floorplanning Tasks and Layout Estimates:

-The initial steps in designing and planning the iADC project involved tasks such as estimating component areas, becoming familiar with Virtuoso tools, and examining differences in ADC behavior. Additionally, a floorplan was created, focusing on signal routing considerations, and biasing blocks were set up to enhance the design further. These activities were aimed at laying a strong foundation for the development and execution of the iADC project, and they are all documented within this section dedicated to floorplanning efforts.

4.1 Area estimates of Resistor and Capaciotr:-

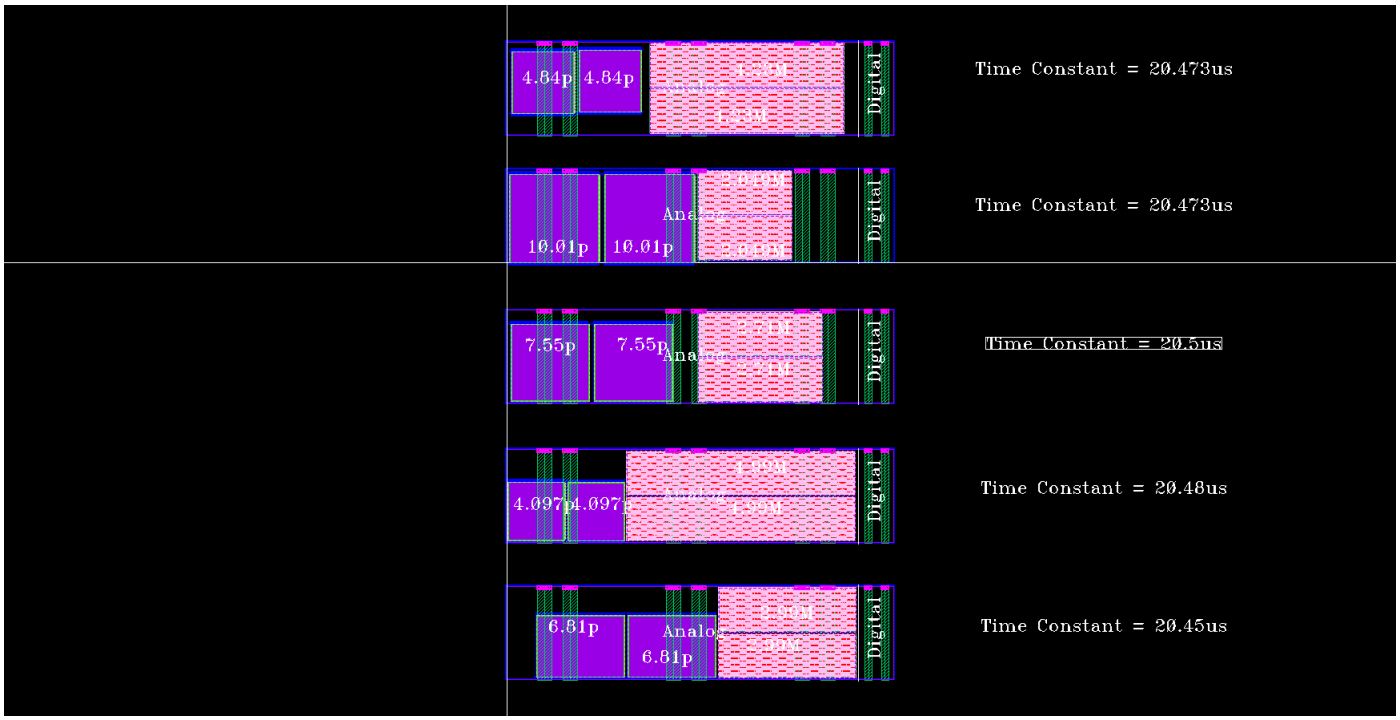

Figure 38: Area Estimation of R,C for different Values.

-Area estimation for different values of R and C has been conducted in the layout, while maintaining a Time Constant of $20.48\mu s$ as specified. It is observed that the minimum and maximum area required by the capacitor and resistor from the technology library are determined to fit into the analog layout. The resistor utilized is sourced from the technology library as rnpolywo_m, while the capacitor used is crtmom.

-When replacing the resistors and capacitors in the top model with estimated values in the digital bus, it became apparent from the simulation that there was an error exceeding 1 LSB. This underscored the significant sensitivity of both the resistor and capacitor components in the circuit.

4.2 Area estimates of Transfer Switches:-

-In the CMOS transfer switch configuration, NMOS and PMOS transistors are connected in parallel. The gate terminal of the NMOS is linked to the input of the enable pin, while the gate of the PMOS is connected to the output of an inverter. The MOS transistors are sourced from the technology library as `nch_mac` and `pch_mac`, and the inverter utilized is from the digital library (`tcbn65lpbwp12t`) with the designation `INVD0BWP12T`.

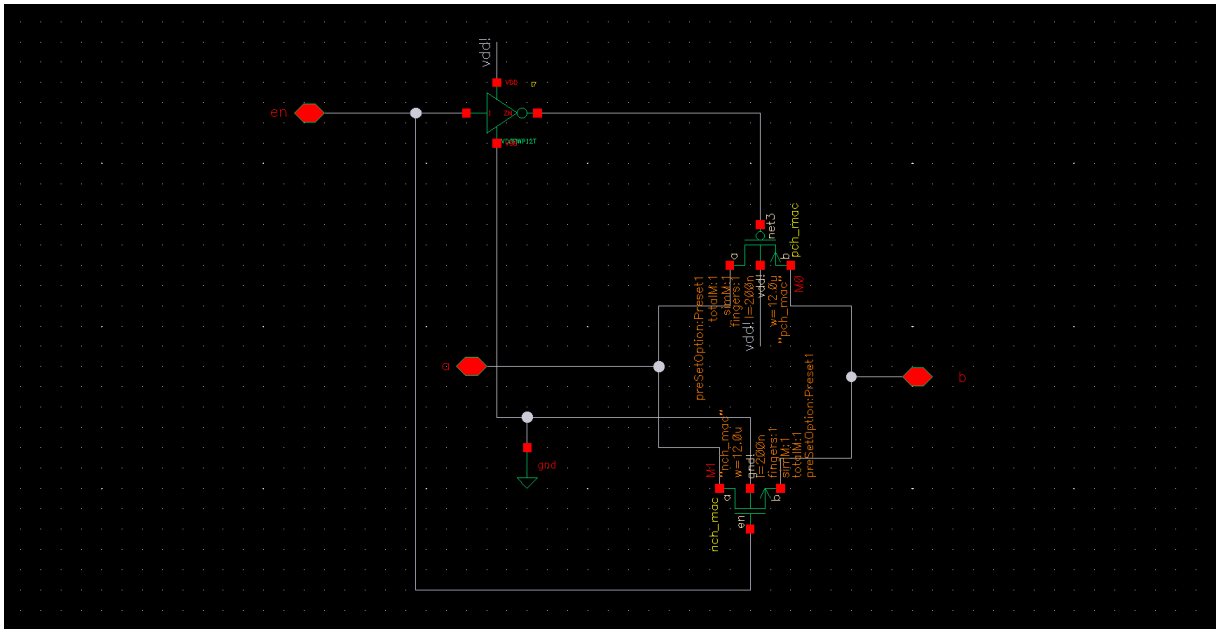

Figure 39: Schematic of CMOS Transfer Switch

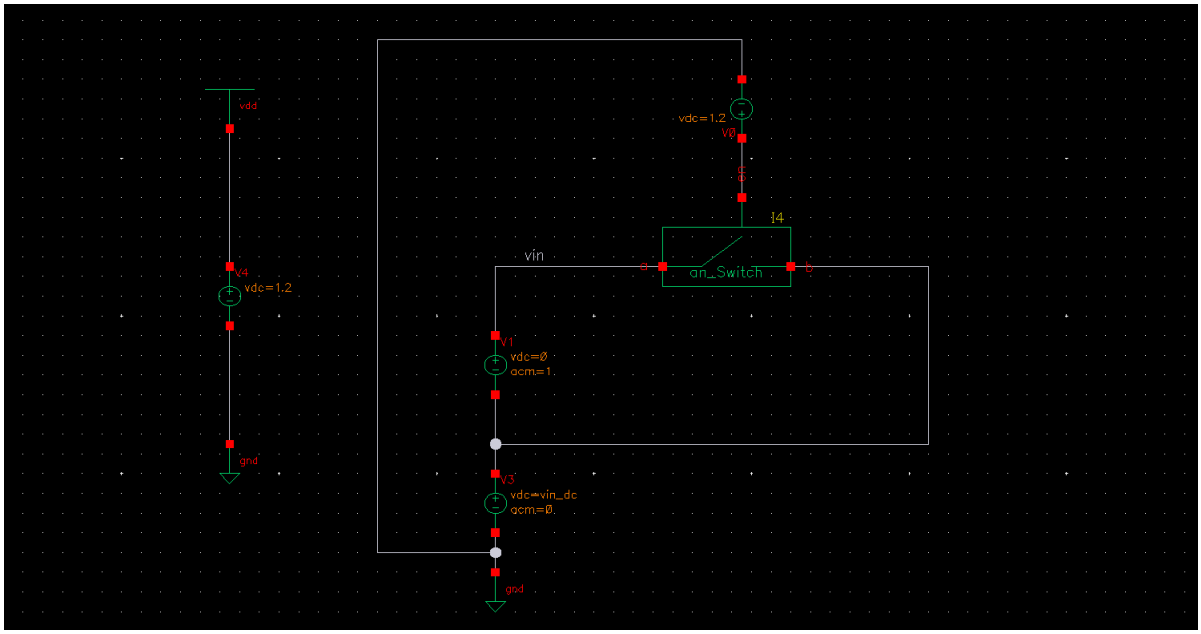

Figure 40: Test Bench Setup of CMOS Transfer Switch

-In the test bench schematic of the CMOS transfer switch, the enable pin is supplied with a DC voltage of 1.2V to turn it on and 0V to turn it off. The input pin is provided with

an AC magnitude of 1V, which is then combined with a DC voltage sweep variable. In the AC analysis, the DC voltage is swept from 0 to 1.2V with a frequency of 1kHz.

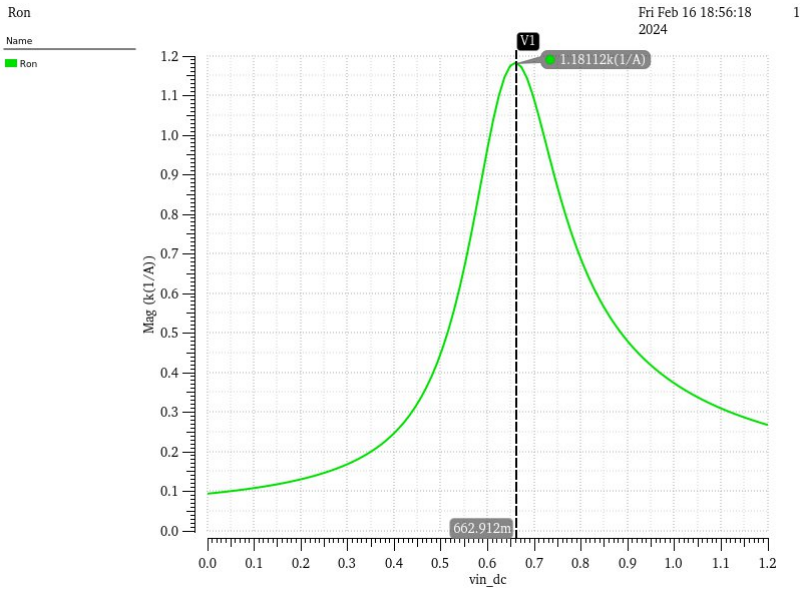

Figure 41: Waveform of a Resistance when the switch is On

-The resistance when the switch is on and off at the input side was measured by observing the current at node a and dividing it by the AC magnitude of 1V. With a W/L ratio of 60, the observed resistance when the switch is on was 1.18 kΩ, and when it's off, it was 11.12 GΩ.

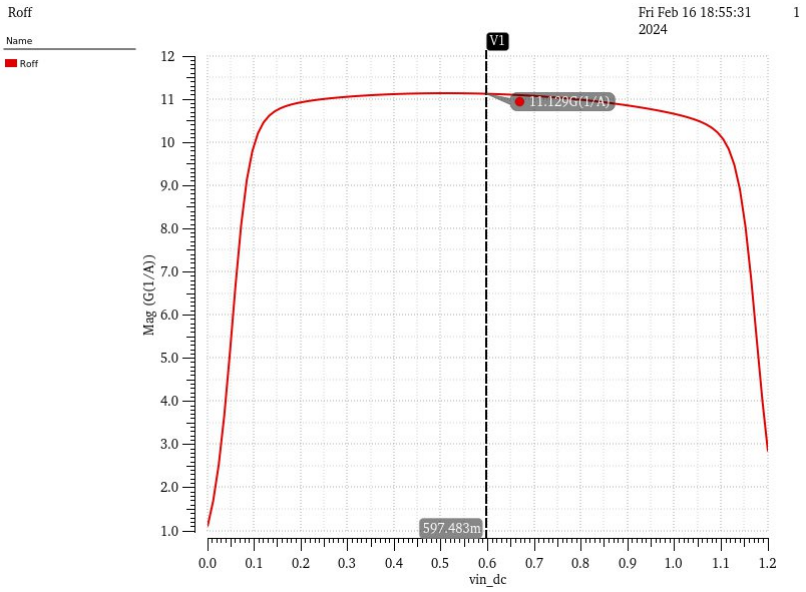

Figure 42: Waveform of a Resistance when the switch is Off

-Started the layout design of the transfer switch by utilizing a pre-built layout of the inverter. However, encountered challenges in resolving all the errors.

5 References

1. T. Chan Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd ed.
2. B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed.
3. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed.
4. Sergio Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, 4th ed.