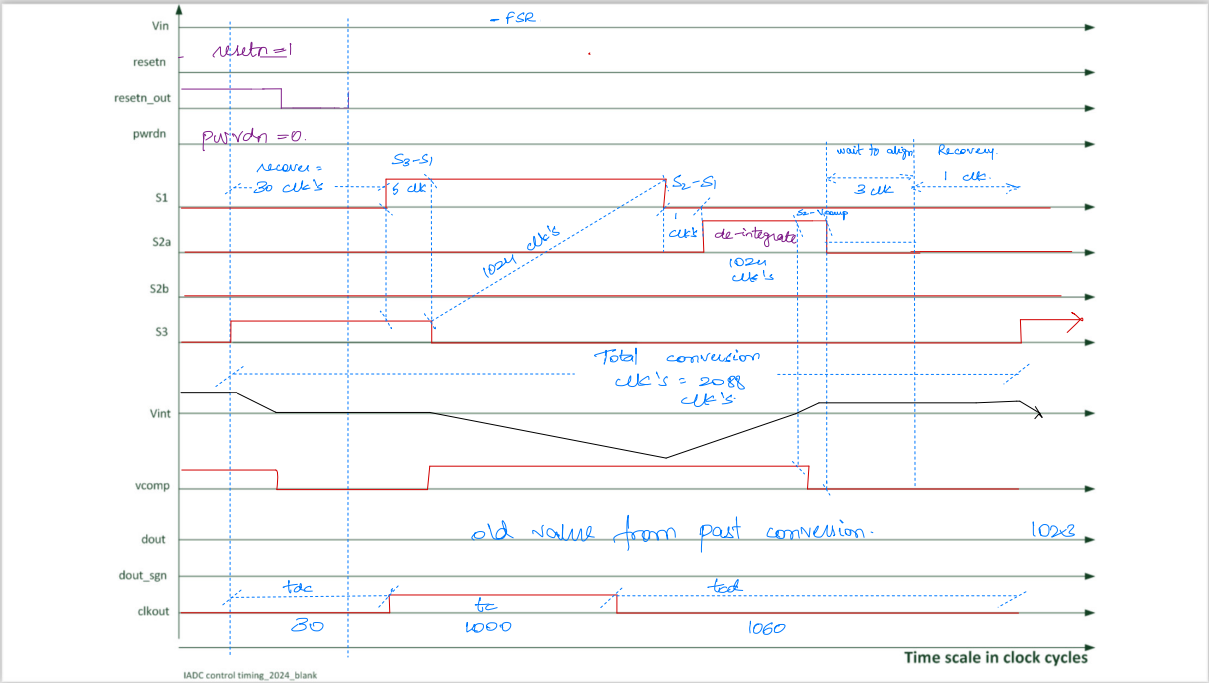
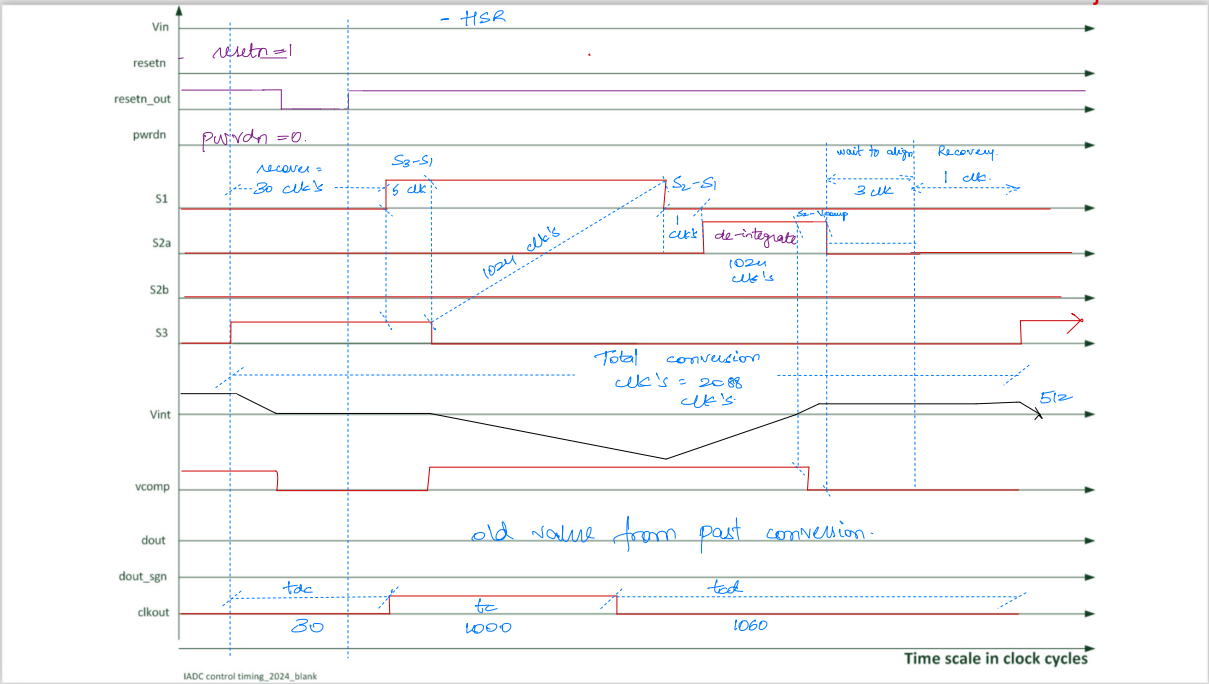
Amith Nanjesh



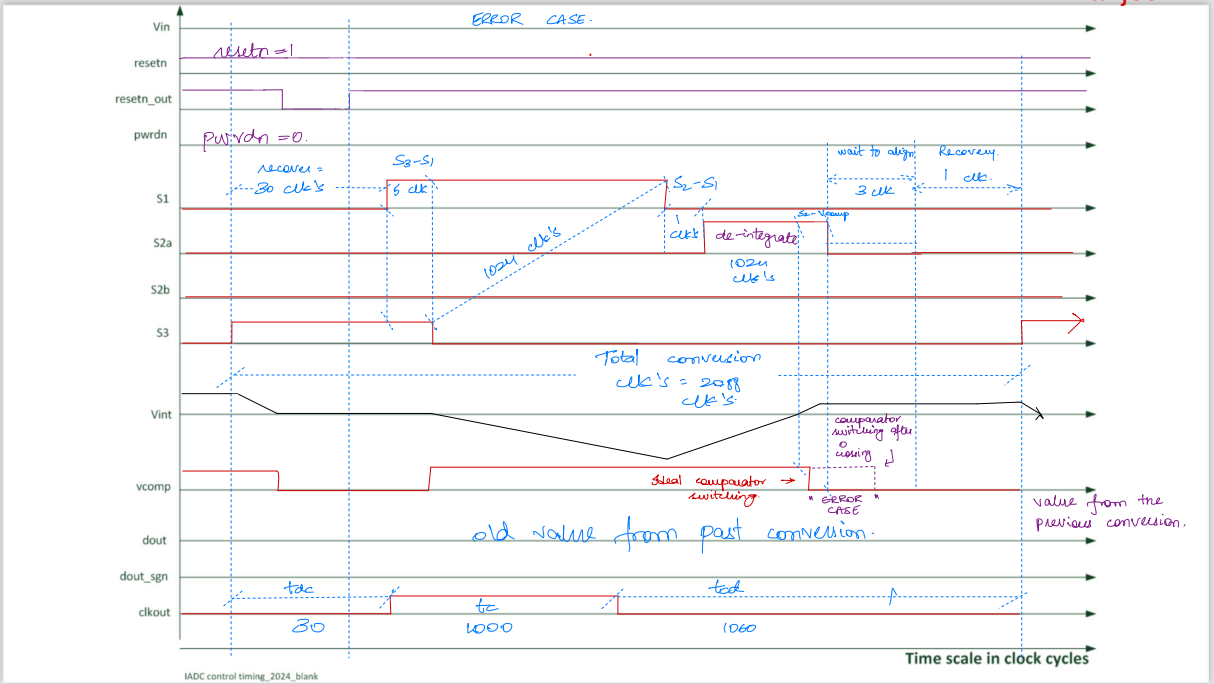
IADC control timing_2024_blank

Amith Nanjesh



IADC control timing_2024_blank

Amith Nanjesh



IADC control timing_2024_blank

⊙ FSM State Diagrams.

① Initial: Pwrdn = 1 ; Resetn = 0

$S_1 = 0$; $S_{2A} = 0$; $S_{2B} = 0$; $S_3 = 0$; clkout = 0 ; Rsm_out = 0

② Resetpwd: Pwrdn = 0 ; Resetn = 1

$S_1 = 0$; $S_{2A} = 0$; $S_{2B} = 0$; $S_3 = 0$; clkout = 0 ; Rsm_out = 1

③ Startup phase:

$S_1 = 0$; $S_{2A} = 0$; $S_{2B} = 0$; $S_3 = 1$; clkout = 0 ; Rsm_out = 1

④ Nonovp S_1 - S_2:

$S_1 = 1$; $S_{2A} = 0$; $S_{2B} = 0$; $S_3 = 1$; clkout = 0 ; Rsm_out = 1

⑤ Initial integration:

$S_1 = 1$; $S_{2A} = 0$; $S_{2B} = 0$; $S_3 = 0$; clkout = 1 ; Rsm_out = 1

⑥ Nonovp $S_1 - S_2$:

$S_1 = 1$; $S_{2A} = 0$; $S_{2B} = 0$; $S_2 = 0$; clkout = 0 ; Rsm_out = 1

⑦ (+ve) / (−ve) Deint:

$S_1 = 0$; $S_{2A} = 1$; $S_{2B} = 1$; $S_2 = 0$; clkout = 0 ; Rsm_out = 1

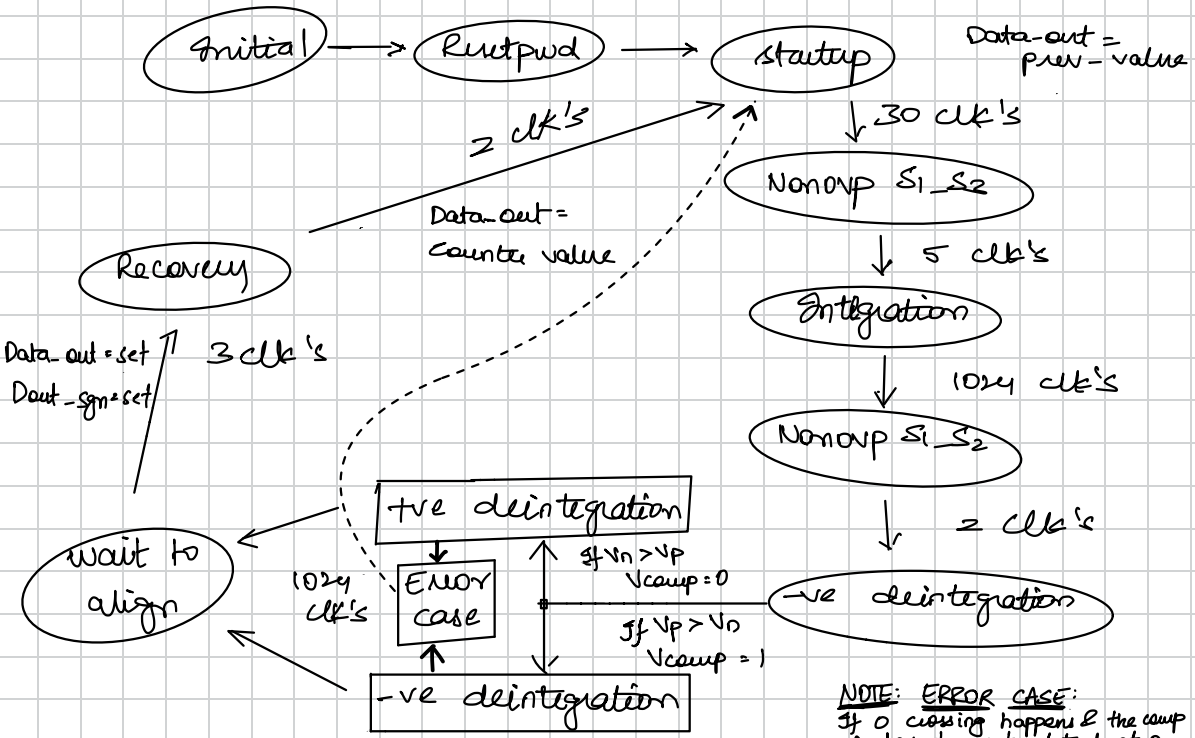
(+ve deint) ↵ ↳ (−ve) deint.

⑧ wait to align

$S_1 = 0$; $S_{2A} = 0$; $S_{2B} = 0$; $S_2 = 0$; clkout = 0 ; Rsm_out = 1

⑨ Recovery:

$S_1 = 0$; $S_{2A} = 0$; $S_{2b} = 0$; $S_2 = 0$; clkout = 0 ; Rsm_out = 1


Initial
Rstpwd
Startup
Data_out = prev_value
2 clk's
30 clk's
Nonovp S1_S2
Data_out = Counter value
Recovery
5 clk's
Integration
1024 clk's
Nonovp S1_S2
2 clk's
Data_out = set
Dout_sgn = set
3 clk's
+ve deintegration
Wait to align
1024 clk's
ERROR case
If Vn > Vp
Vcomp = 0
If Vp > Vn
Vcomp = 1
-ve deintegration
-ve deintegration
NOTE: ERROR CASE:
If 0 crossing happens & the comparator does not detect at 0 crossing but detects later.

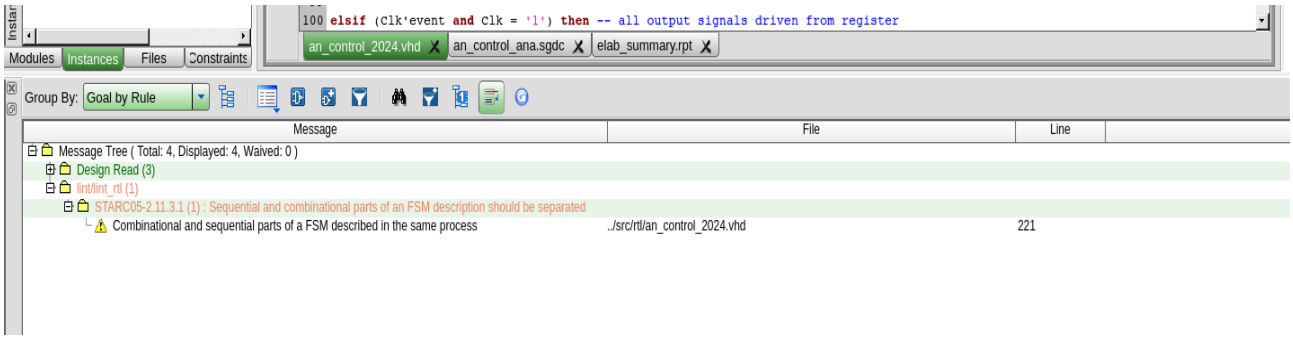
IADC Verification Plan
Amith Nanjesh
FH Kaernten

Abstract: This document consists of Verification plan timing diagram for typical voltages, description of VHDL blocks and testbench.

1. VHDL CODE:

Entity and file names are set as per the prefix (an)

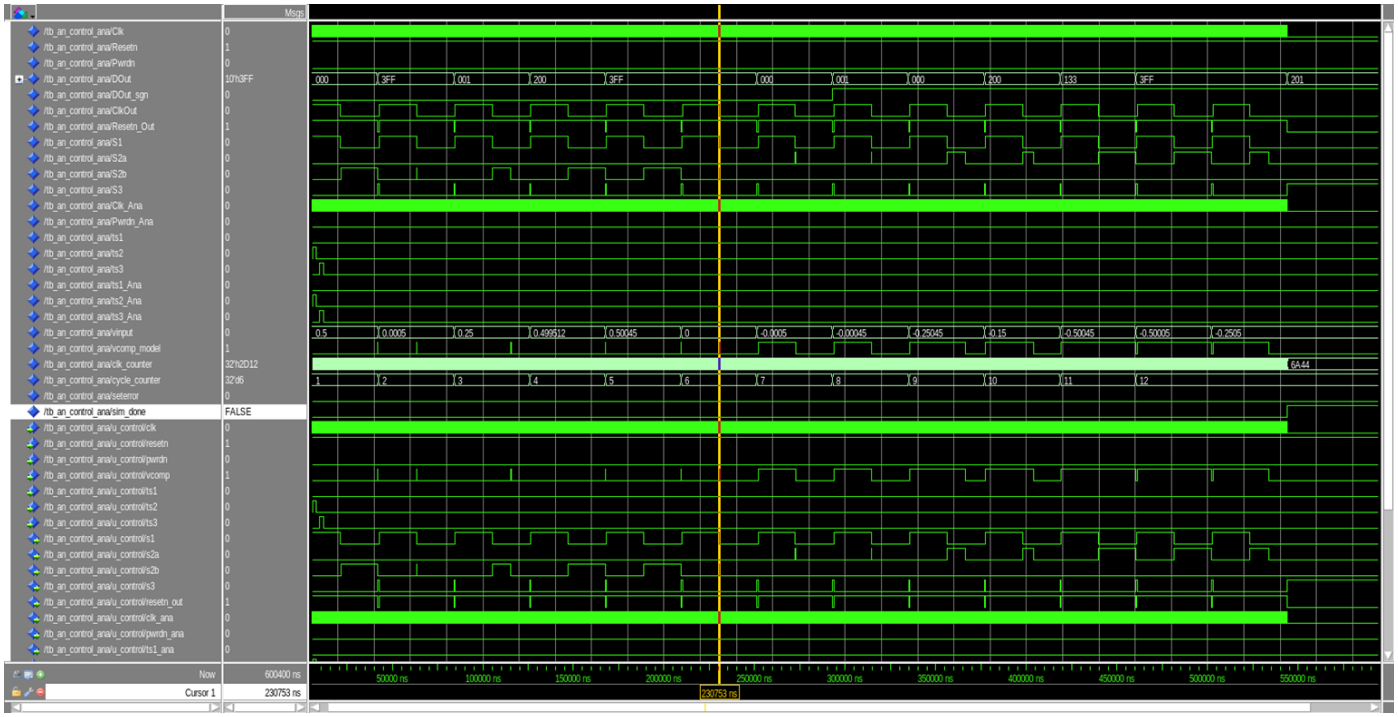
For the spyglass verification of the rtl, below is the screenshot attached.



The image contains a warning related to an FSM design process.

Warning A: A sequential process and a combinational process have been declared within the same FSM process.

2. SIMULATION:



For all valid input cases (excluding error cases), the Dout values are correctly reflecting the expected outputs.Additionally, the clkout period remains constant across each cycle.

Verification plan basically describes how each input is validated w.r.t generate output on output pins. To do any operation the clk is most important input signal because whole VHDL code is synchronized w.r.t input clock edge triggered. In this rising edge of the clk is used.

Resetn : When Resetn is 0, all the outputs are reset to 0 as well as all the internal registers should be reset to 0.

Pwrdn : When Pwrdn is 0, all the outputs should be reset to 0 as well as all the registers should be reset to0 and Pwrdn signal should be input to Pwrdn_Ana output pin.

The input Pwrdn to digital is connect directly through buffers to avoid the feedback through.
If Pwrdn=0 and Resetn=1, then go to Phase 1 reset and transit to the next corresponding states.

If Pwrdn=1 or Resetn=0, then go to Phase 0 Start-up phase all the values should be zero.

S3=1 for 35 clock cycles during the startup phase.

Analog Input	Expected output	Output Shown
|LSB|	1	1
0.5	1023	1023
0.25	512	512
-0.5	1023	1023
-0.25	512	512
| 0.5 or 0.25| +/- LSB	1024/512	1024/512

Case 1:
Verify if Resetn and Pwrdn are responding according to the initial timings specified in thetestbench. Ensure S3 switches on for 35 clock cycles before the integration phase begins.

Case 2:
Confirm that the integration phase lasts for 1024 cycles with S1 on. During this period, no other switches should toggle. Once the Comparator is on then Comparator output should be stored to refer as sign value
before going to DeIntegration Phase. Depending on the comparator's sign, either S2a or S2b should activate to handle positive or negative de-integration, respectively.

Case 3:
Ensure there is a delay after de-integration as specified to prevent any overlap between two switches.

Case 4:
In DeIntegration Phase check when the VCOMP switches and stop the DeIntegration as well as hold the count
value. In this phase the case when vcomp toggles more than once should be checked.It should remain in the
same phase till vcomp is stable.Maximum count value can be 1023. Validate the Dout based on diff analog

input. Dout should be validated w.r.t Analog Input. Compare the count value from the expected.

Case 5:
Vary input values from -0.5V to 0.5V and validate for error cases.
(Note: Error cases are not yet implemented but will be addressed soon.)

Case 6:
Ensure the Clkout period remains constant.

Case 7: Validate Resetn during the integration, de-integration, and recovery phases.

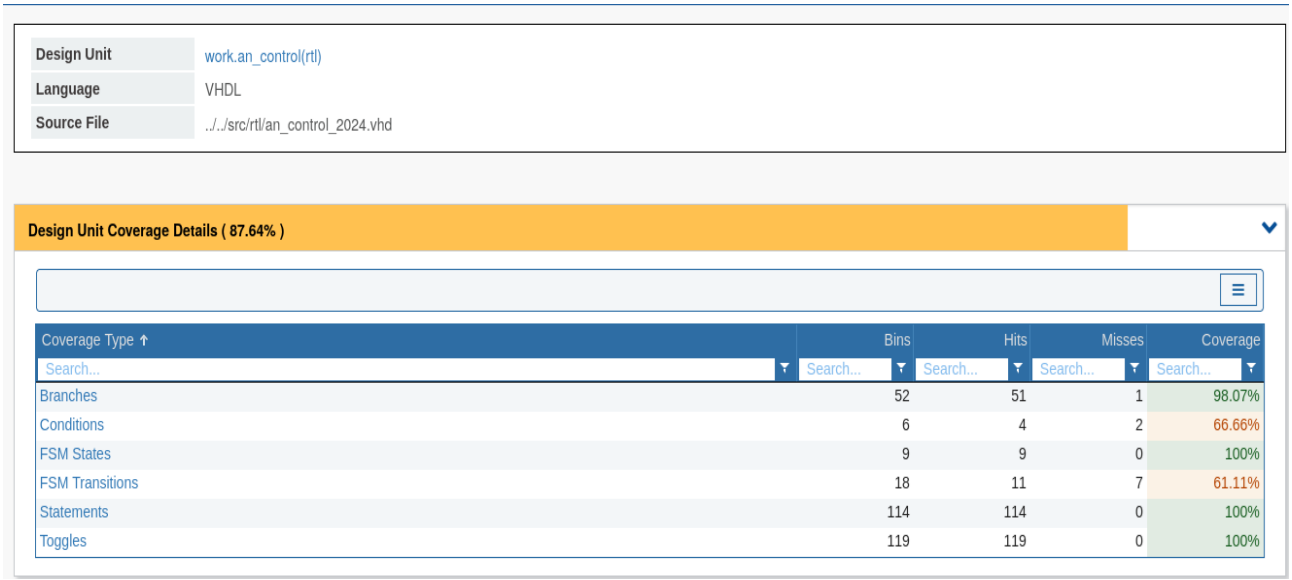
Case 8: Validate Pwrdn during the integration, de-integration, and recovery phases.

Case 9: Validate Dout values.

Case 10: Validate Output if VCOMP does not switch. This happens when the input is out of the range from -0.5 to 0.5. The value should be 1023.

Case 11: Validate Output if input is less than one LSB.

3. COVERAGE REPORTS:



Design Unit	work.an_control(rtl)
Language	VHDL
Source File	../../src/rtl/an_control_2024.vhd

Design Unit Coverage Details (87.64%)

Coverage Type	Bins	Hits	Misses	Coverage
Branches	52	51	1	98.07%
Conditions	6	4	2	66.66%
FSM States	9	9	0	100%
FSM Transitions	18	11	7	61.11%
Statements	114	114	0	100%
Toggles	119	119	0	100%

-State transitions are at 66.66% since not all states transition back to the resetpwd state. Forcing all states to transition back to resetpwd would violate the implemented FSM.
- There are few conditions related to switch which also can't be toggled at a single time.

SYNTHESIS:-

Analog Input	Expected output	Output Shown	Functionality
0	0	0	For zero input 0 output is verified.

<|LSB|	0	0	Minimum 1LSB is should be given else 0 value is output
|LSB|	1	1	Detect 1 LSB magnitude input signal output is 1 verified
|0.25|	512	512	Half of maximum input is verified
|0.5|	1023	1023	Maximum input is verified
|0.5	+ |LSB|	1023	1023	Maximum input signal is 0.5 should be given else 1023 value is output
	0.5 - LSB|	1023	1023	Value is 1023 verified

The output is same as the expected output for all the input values after synthesis simulation.

Timing Diagram for Analog Inputs after Synthesis

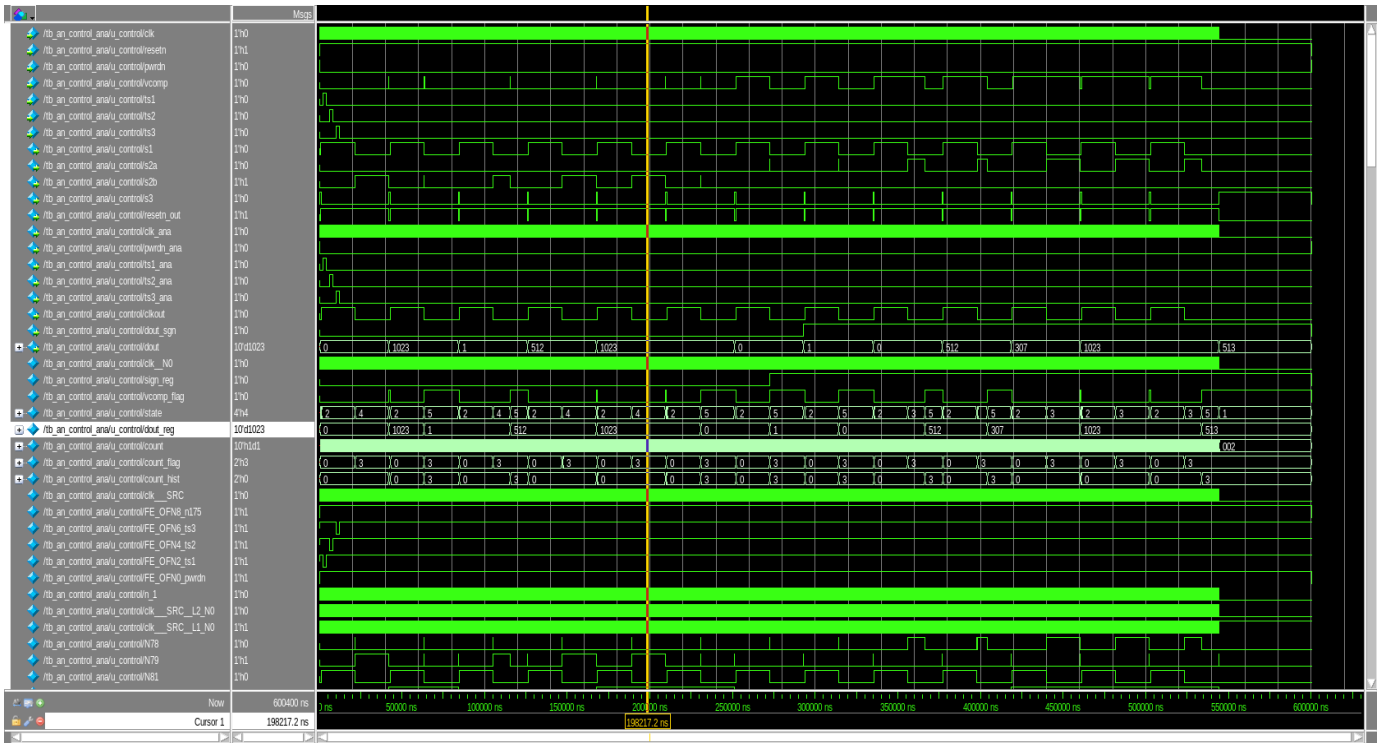
LAYOUT:-

Analog Input	**Expected output**	**Output Shown**	**Functionality**
0	0	0	For zero input 0 output is verified.
<|LSB|	0	0	Minimum 1LSB is should be given else 0 value is output
|LSB|	1	1	Detect 1 LSB magnitude input signal output is 1 verified
|0.25|	512	512	Half of maximum input is verified

|0.5|	1023	1023	Maximum input is verified
|0.5 | + |LSB|	1023	1023	Maximum input signal is 0.5 should be given else 1023 value is output
| 0.5 - LSB|	1023	1023	Value is 1023 verified

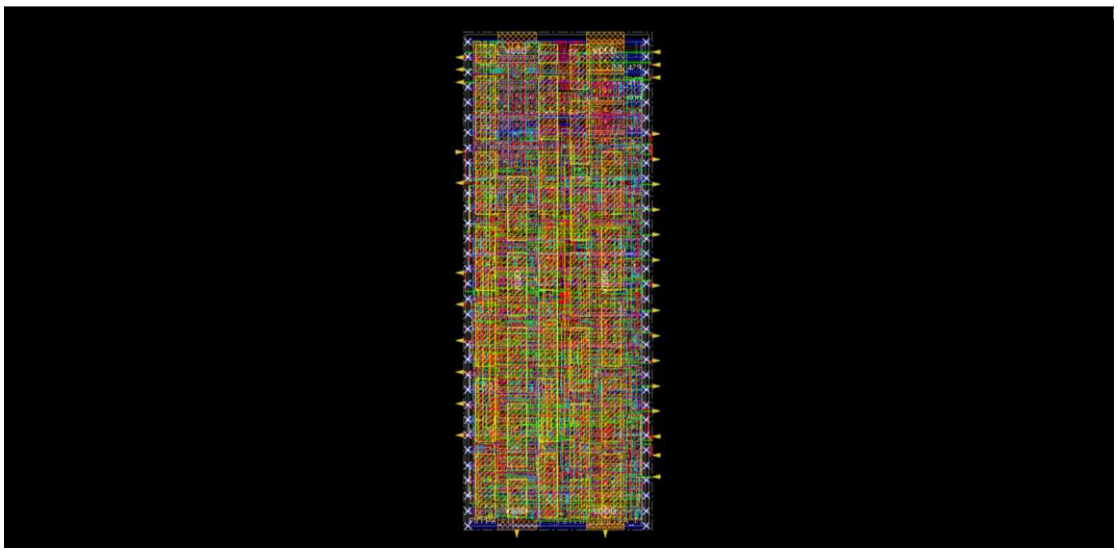
The output is same as the expected output for all the input values after layout simulation.

The expected output for rtl , synthesis, layout is same as the output. They do not change after each stage like synthesis and layout.



Timing Diagram for Analog Inputs after Layout

Layout DRC and LVS Check:

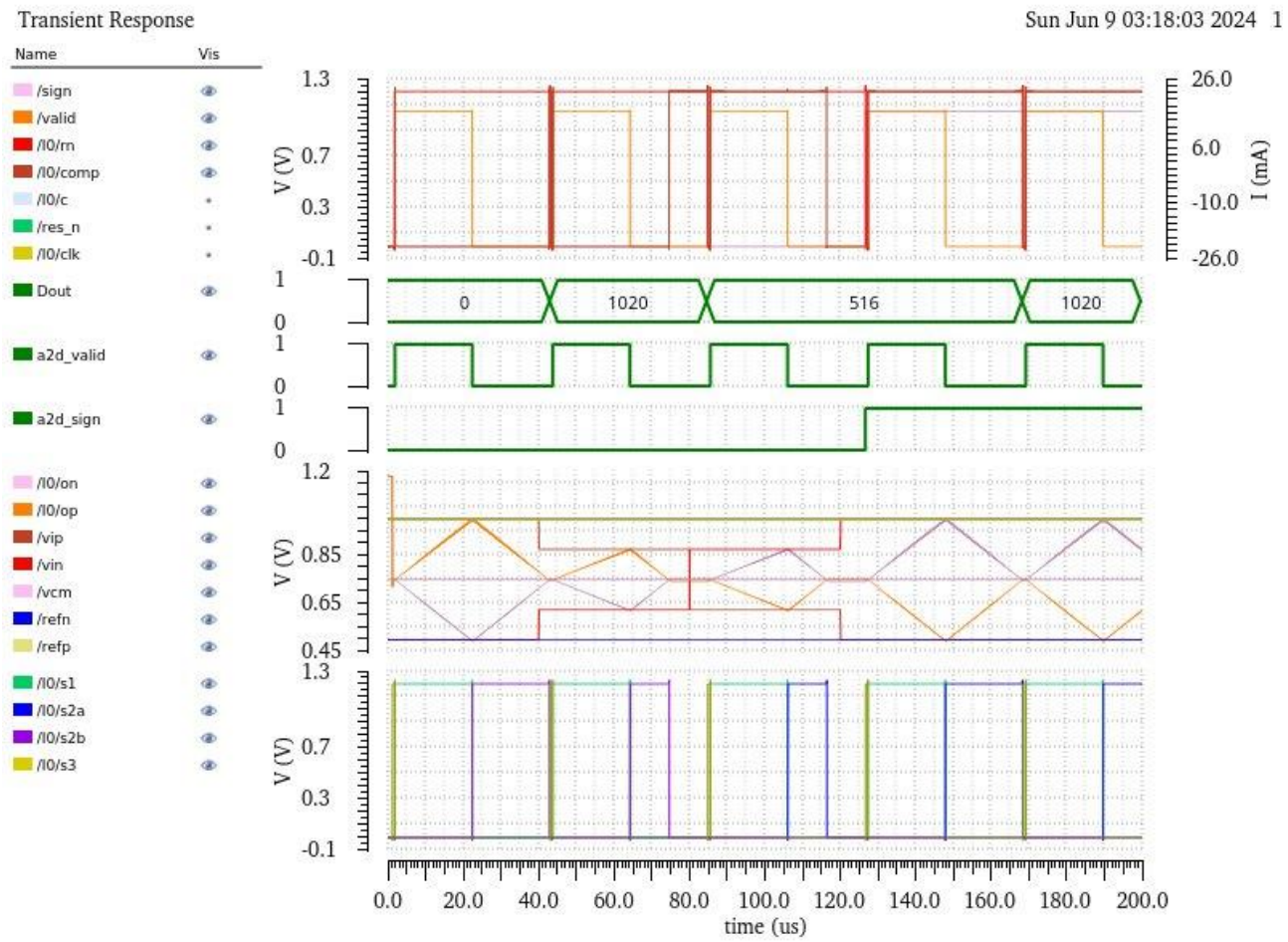


Final Layout

The Layout is done with DRC and LVS clean.

Mix Mode simulation:

Analog simulation was held with digital symbol all the control signals are working, output waveform can be seen below. Output data is seen below is the expected data with analog schematic top.



Top waveform in the analog setup with digital symbol.